SmartFusion2 and IGLOO2 SmartDebug Hardware Design Debug Tools - Libero SoC v11.7



Power Matters."

TU0530 Tutorial



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1 Preface

1.1 About this Document

This tutorial describes the following topics:

- Launching SmartDebug from Libero: Accessing SmartDebug from Libero[®] System-on-Chip (SoC)
- View Device Status: Checking the device status
- View Flash Memory (eNVM) Content: Checking the flash memory (eNVM) content
- Debug FPGA Array: Debugging FPGA array (setting Live Probes, Active Probes, and reading and modifying fabric SRAM content)
- Probe Insertion: Post-Layout Probe Insertion
- SERDES Debug: Debugging SERDES blocks

1.2 Intended Audience

This tutorial is intended for:

- FPGA designers
- System-level designers

1.3 References

1.3.1 Microsemi Publications

Refer to the following web page for a complete and up-to-date listing of the SmartFusion2 device documentation: http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2

Refer to the following web page for a complete and up-to-date listing of the IGLOO2 device documentation: http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga

- SmartDebug for Software v11.7 User's Guide
- FPGA On-Chip Debug Tools
- IGLOO2 FPGA Evaluation Kit
- SmartFusion2 Security Evaluation Kit Board
- http://soc.microsemi.com/kb/article.aspx?id=SL5636
- UG0451: SmartFusion2 and IGLOO2 Programming User Guide
- UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide

1.3.2 Others

Pasternack[®] PE39429-12 technical datasheet:

Pasternack Industries part number PE39429-12



1 SmartFusion2 and IGLOO2 SmartDebug Hardware Design Debug Tools

1.1 Introduction

Design debug is a critical phase of the field programmable gate array (FPGA) design flow. Microsemi multiple design debug tools and features complement design simulations by allowing verification and troubleshooting at the hardware level. Microsemi SmartDebug tools help the designer to analyze the key elements of a flash design, such as the embedded non-volatile memory (eNVM) data, SRAM data, and probes capabilities. Microsemi SmartFusion[®]2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO[®]2 FPGA devices have built-in probe points that greatly enhance the ability to debug logic elements within the device. The enhanced debug features implemented in the SmartFusion2 and IGLOO2 devices give access to any logic element through Live Probe and Active Probe features, which enable designers to check the state of inputs and outputs in real-time, without any re-layout of the design.

1.2 Design Requirements

Table 1 • Design Requirements

Design Requirements	Description
Hardware Requirements	
SMA Male-to-SMA Male Precision Cables, such as Pasternack Industries part number PE39429-12 (or equivalent)	Optionally recommended for evaluation board SERDES testing.
IGLOO2 Evaluation Kit or SmartFusion2 Security Evaluation Kit (M2 <mark>S090TS-FGG</mark> 484)	Rev D or later
Software Requirements	•
Libero SoC software	v11.7
FlashPro4	v11.7

1.2.1 Reference Documents

For more information on using SmartDebug, see the SmartDebug for Software v11.7 User's Guide.

1.2.2 Project Files

Extract the http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_tu0530_liberov11p7_df

Libero SoC project along with the Readme.txt file and programming (.stp) file to a folder on the PC (for example: C:*Microsemiprj*). Confirm that the following design files are extracted from the downloaded folder:

- m2gl_SmartDebug_Tutorial For IGLOO2 Evaluation Kit (M2GL010T)
- m2s_SmartDebug_Tutorial For SmartFusion2 Security Evaluation Kit (M2S090TS)

1.3 Design Overview

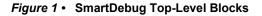
The design consists of two main blocks: the SERDES debug block (SERDES_Debug) and the fabric debug block (Fabric_Debug), as shown in Figure 1.

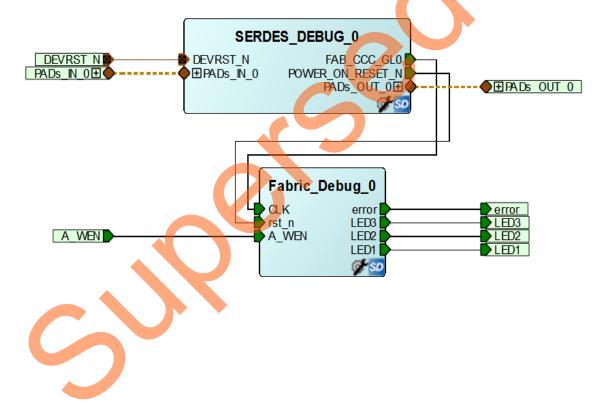


The SERDES_Debug block is used to demonstrate the SmartDebug capabilities that can be used to perform SERDES real-time signal integrity testing and debugging. The design consists of a System Builder block (SD_DEMO) and an instance of SERDES Interface block (SERDES_IF), as shown in Figure 2. Within the System Builder, a Data Storage client is stored in the flash memory (eNVM). SmartDebug provides the capabilities to view the eNVM content by reading the content in real-time from the device.

The Fabric_Debug block demonstrates the way to use SmartDebug to perform FPGA array debugging. To demonstrate this, the Fabric_Debug uses a counter to load a counting pattern into the LSRAM instance (DPSRAM). The data stored is the same as the address. On the read side of the LSRAM, there is a count checker (count_chk) to ensure that the count progresses as expected. If there is an error, the output (error) is latched high, as shown in Figure 3. This Fabric_Debug block design is used to demonstrate the different silicon built-in capabilities, such as setting Live Probes to monitor an internal user-selected point on the device in real-time.

In addition, you can set Active Probes, which provide the capabilities for dynamic asynchronous read and write to a flip-flop or probe point. This enables you to quickly observe the output of the logic internally or to quickly experiment on how the logic is affected by writing to a probe point. Finally, the Fabric_Debug design block is used to demonstrate the SmartDebug capabilities, where you can read and modify the fabric SRAM content in real-time.









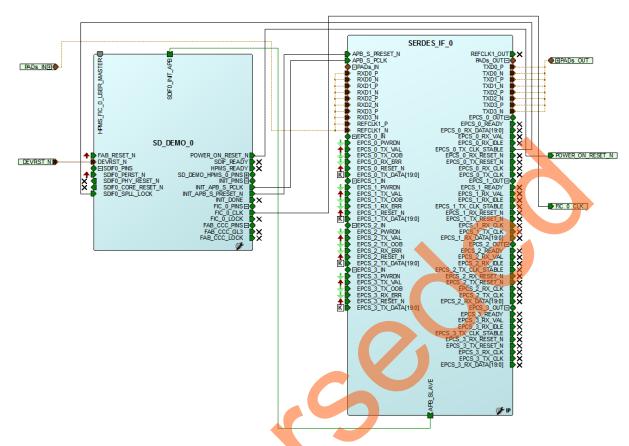
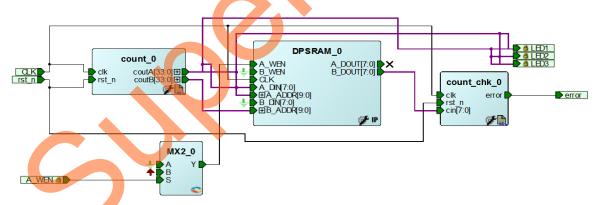


Figure 3 • Fabric_Debug Overall Design Blocks (IGLOO2 Design Block)



A WEN is used to pause the write operation to the SRAM while demonstrating the SmartDebug write to the SRAM capability. It is assigned to SW2 on the board. When SW2 is pressed, the write operation from the counter pauses and does not overwrite the SmartDebug write into the SRAM.

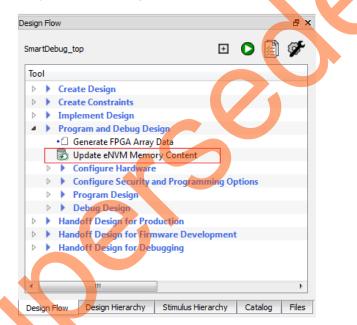


1.4 Programming the Device

The following steps describe how to program the IGLOO2 or SmartFusion2 Security Evaluation Kit board:

- 1. Connect the **FlashPro4/5 programmer** to the **J5** connector on the IGLOO2 or SmartFusion2 Security Evaluation Kit.
- 2. Connect the **power** supply to the **J6** connector.
- 3. Switch **ON** the power supply (**SW7**). For more information, refer to the *IGLOO2 FPGA Evaluation Kit* Board or *SmartFusion2 Security Evaluation Kit Board*.
- 4. Launch Libero SoC v11.7.
- 5. From the Project menu, select Open Project.
- 6. Browse to the folder where the design files are extracted and open the appropriate design file (IGLOO2 or SmartFusion2). For more information, refer to the "Project Files" section on page 7.
- 7. Based on the location where the project files are extracted, update the paths in the eNVM data clients as follows:
 - a. On the **Design Flow** window, double-click **Update eNVM Memory Content** as shown in Figure 4.

Figure 4 • Update eNVM Memory Content in Design Flow Window



The **eNVM Update Tool** window is displayed, as shown in Figure 5. b. Double-click the **sram_envm** client.



Figure 5 • eNVM Update Tool Window

💵 eNVM Update Tool			_		?	
Available Client types		Us	er Clients in eN	VM		
Data Storage Serialization	Client Type	Client Name	DepthxWidth	Start Address(Hex)	Page Start	
	1 Data Storage	sram_envm	64 x 8	2000	64	
Add to System	2 Data Storage	Start_prog	500 x 32	0	0	
Available Pages: 4032 Used Pages: 17 Free Pages: 4015	You can disable programming for The content will be preserved a Optimize	or a client by editing and programming of	III the client and selecting this client can be re-en ndo Redo	the 'No Content' option. abled by selecting the preserved Edit	Delete	

c. In the **Modify Data Storage Client** window, browse to the location of the sram_envm.mem file located in the eNVM_files folder included in the project as shown in Figure 6.

Figure 6 • Modify Data Storage Client Window

Modify Data Storage Client Key Memory file: Start Debug_Tutorial/eNVM_files/sram_envm.mem Format: Microsemi-Binary Use absolute addressing Content filled with 0s No Content (Client is a placeholder and will not be programmed) Start address: 0x 2000 Size of word: 8 Bits Number of Words: 64 Use as ROM Use Content for Simulation
Help Ok Cancel

d. If the SmartFusion2 Security Evaluation Kit is used, double-click the **Start_prog** client (see Figure 5). In the **Modify Data Storage Client** window, browse to the location of the <code>start_prog.hex</code> file located in the eNVM_files folder included in the project as shown in Figure 7.

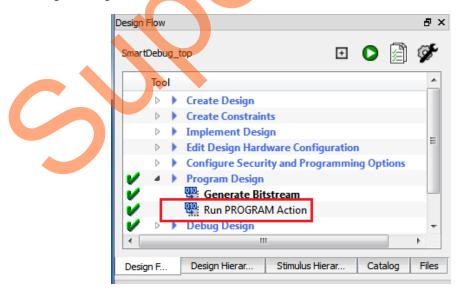


Figure 7 • Modify Data Storage Client Window - Specifying Start_prog.hex File

Modify Data Storage Client	
Client name: Start_prog	
Content:	
Memory file: m2s_SmartDebug_Tutorial/eNVM_files/Start_prog.hex Format: Intel-Hex	
Use absolute addressing	
Content filled with 0s	
\bigcirc No Content (Client is a placeholder and will not be programmed)	
Start address: 0x 0 🐳	
Size of word: 32 V Bits	
Number of Words: 500 (Decimal)	
Use as ROM 🕤	
Use Content for Simulation	
Help Ok Cancel	

- **Note:** The .hex file is a simple user boot code loop program that is programmed into address zero (eNVM address 0x60000000). This is to ensure that there is a valid user boot code for the ARM[®] Cortex[®]-M3 to execute on power-up or at power-on reset. For more information, refer to *http://soc.microsemi.com/kb/ article.aspx?id=SL5636*
 - 8. In the **Design Flow** window, select **Run PROGRAM Action**, as shown in Figure 8. This programs the design into the device.

Figure 8 • Programming the Device





1.5 Launching SmartDebug from Libero

On the Design Flow window, double-click SmartDebug Design, as shown in Figure 9.

Figure 9 • Launching SmartDebug Design Tools

)esign	Flo	W				Β×
Smari	tDe	bug_top	+	0		¢۶۰
Тоо	I					•
\triangleright	۲	Create Design				
\triangleright	۲	Create Constraints				
\triangleright	۲	Implement Design				
\triangleright	۲	Edit Design Hardware Configura	tion			
\triangleright	۲	Configure Security and Program	ming O	otions		=
⊿	۲	Program Design				
		🎬 Generate Bitstream				
		Run PROGRAM Action				
⊿	۲	Debug Design				
		🕺 Identify Debug Design				
		🐵 SmartDebug Design				
⊳	₽	Handoff Design for Production				-
•		III				•
Desi	gn I	F Design Hierar Stimulus H	lierar	Cat	alog	Files

The SmartDebug window is displayed, as shown in Figure 10.

Figure 10 • SmartDebug Window Debug Options

SmartDebug Eile View Help	
Device: M2GL010T (M2GL010T) ID code read from device: F8031CE	Programmer: (93455 (usb93455) -
Vièw Device Status View Flash Mémory Content	Debug FPGA Array Debug SERDES
Log	
Errors A Warnings 1 Info	

SmartDebug tools provide the following features and capabilities:

• Live Probes: Two dedicated probes can be configured to observe a probe point, which is any output of a register. After selecting the probe points, the probe data can be sent to two dedicated pins (PROBE_A and PROBE_B). PROBE_A and PROBE_B are two dedicated pins on the device. You can connect an oscilloscope to the probe pins and monitor the signals status.



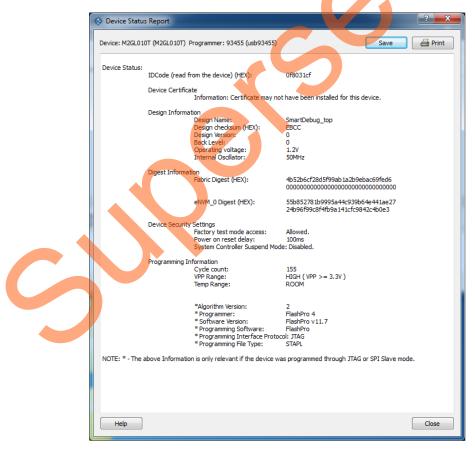
- Active Probes: Active probes allow dynamic asynchronous read and write to a flip-flop or probe point. This enables you to quickly observe the output of the logic internally, or to quickly experiment on how the logic is affected by writing to a probe point.
- SRAM and eNVM Debug Capabilities: SmartDebug includes test capabilities that can access SRAM and eNVM to assist with checking the flash memory (eNVM) content and reading and modifying the fabric SRAM content.
- **Probe Insertion**: Probe insertion is a post-layout process that enables you to insert probes into the design and brings signals out to the FPGA package pins to evaluate and debug the design.
- SERDES Debug Capabilities: SERDES debug capabilities makes debugging high-speed serial designs simple. The SmartDebug JTAG interface extends access to configure, control, and observe SERDES operations and is accessible in every SERDES design. The designs are implemented using the Libero System Builder to incorporate the SERDESIF block enabling SERDES access from the SmartDebug toolset. The SERDES Debug window displays real-time system and lane status information. SERDES configurations are supported with Tcl scripting, allowing access to the entire SERDES register map for real-time customized tuning.

1.6 Debugging the Design

1.6.1 View Device Status

The View Device Status option provides the device status report. It summarizes the device information, programmer information, user information, factory serial number, and security information, if any are set. Figure 11 shows a sample of the device status information.

Figure 11 • Device Status Report Sample





1.6.2 View Flash Memory (eNVM) Content

The View Flash Memory Content can be accessed from the **SmartDebug** window, as shown in Figure 10. This option provides the capabilities to retrieve the eNVM content from the device using the Memories pages of the System Builder under the SERDES_Debug block. To demonstrate how to retrieve the content of the eNVM, the data to be programmed into the eNVM is defined first. One way to perform this is by defining an eNVM data storage client using the eNVM configurator. The client can be stored into any page of the eNVM. eNVM Page 64 is used here for demonstration purposes. Figure 12 shows an excerpt of the data storage client content that was defined in the eNVM.

Figure 12 • Memory File Content Saved into the eNVM



The content of eNVM is retrieved from the device, displayed, and is equivalent to what is shown in Figure 12.



The following steps describe how the eNVM content can be read in real-time from the device:

- 1. On the **SmartDebug** window, click **View Flash Memory Content** (see Figure 10). The **Flash Memory** window is displayed, as shown in Figure 13.
- 2. Enter the Start Page and End Page as 64. Page 64 is used here for demonstration purpose.
- 3. Click **Read from Device**. The content related to page 64 is displayed.

Figure 13 • Flash Memory (eNVM) Content Read from the Device

Flash Memory										? ×
Retrieve Flash Memory Content from Device:										
Select <page range=""> •</page>	Read from	Device						•		
Start Page: 64	(address 0x2000)									
End Page: 64	(1 page, 128 bytes	s)								
Latest Content Retrieved from Device:									Thu Mar 10 13:46:34	1 2016
									The Mar 10 13:46:34	12010
Retrieved Content: at Page 64, 128 bytes starting fro	m address 0x2000									
View All Page Status	io to Address (hex):		Go	1						
	o to Address (nex):		GO							
Status for Page #64:	Page Number Address	s 0 1	2 3	4	5 6	Cont 7	ent 9	ABC	DE	E
	64 02000		55 E2		F0 53		53 FF 55	EZ AA	F0 53	FF A
Recoverable ECC1 error detected: False Non recoverable data error detected: False	64 02010	53 FF	55 E2	AA	F0 53	FF	53 FF 55	E2 AA	F0 53	FF
Write counter over threshold: False Write count: 5 *** This v	64 02020	53 FF	55 E2	AA	F0 53	FF	53 FF 55	E2 AA	F0 53	FF
Use as ROM: Off Overwrite Protect: Not set	64 02030	53 FF	55 E2	AA	F0 53	FF	53 FF 55	E2 AA	F0 53	00 =
FlashFreeze state: False	64 02040	00 00	00 00	00	00 00	00	00 00 00	00 00	00 00	00
	64 02050	00 00	00 00	00	00 00	00	00 00 00	00 00	00 00	00
< III +	64 02060	00 00	00 00	00	00 00	00	00 00 00	00 00	00 00	00
	64 02070	00 00	00 00	00	00 00	00	00 00 00	00 00	00 00	00 🛫
		•			· · ·					P I
Help										Close
- ich										Close

eNVM UI shows the status of the page selected eNVM page. When you click the **View All Page Status** button, a dialog appears, and displays details such as:

- Number of images that have ECC errors.
- Number of overwrite threshold warnings.

After these details, eNVM UI shows the status of each page that you select to view in the eNVM debug page.

1.6.3 Debug FPGA Array

The SmartFusion2 and IGLOO2 devices have built-in probe points that enhance the ability to debug the logic within the device using the Live Probes and Active Probes features. The enhanced debug features implemented in the devices give access to any logic element and enable you to check the state of inputs and outputs in real-time, without re-layout of the design.

In addition to the ability to specify probe points, SmartDebug also provides the capability to read, modify, and write into the fabric SRAM block. The **Debug** UI includes both a **Hierarchical** and **Netlist** view to easily find test points. The **Hierarchical View** lets you view the instance-level hierarchy of the design programmed on the device. This view also lets you select the signals that are required to add to the Live Probes, Active Probes, and Probe Insertion tabs in the **Debug FPGA Array** dialog box.

You can expand the hierarchy tree to see the lower level logic. Signals with the same name are grouped automatically into a bus that is presented at instance level in the instance tree. The probe points are added by selecting any instance or the leaf level instance in the Hierarchical View. Adding an instance adds all the probe-able points available in the instance to Live Probes, Active Probes, and Probe Insertion.

The **Netlist View** displays a flattened net view of all the probe-able points present in the design, along with the associated cell type.

This section demonstrates the abilities of setting Live Probes, Active Probes, and reading/writing from/to the fabric SRAM.



The Debug FPGA Array can be accessed from the SmartDebug window, as shown in Figure 10. On the **SmartDebug** window, click **Debug FPGA Array** to display the **Debug FPGA Array** window, as shown in Figure 14. The Debug FPGA Array window has a left and right pane. The left pane has two tabs that allow you to toggle between the **Hierarchical** View and **Netlist** View debug points in the design. This information is read into SmartDebug from the Libero SoC design database.



e/Active Probes Selection	B × FPGA Array debug data
Hierarchical View Netlist View	Live Probes Active Probes Memory Blocks Probe Insertion
Filter: Search	Delete Delete Al
Instance(s): Add	Name Type
Instance Tree	
Fabric_Debug_0	
SERDES_Debug_0	
	Assign to Channel A ->
	Assign to Channel B ->
	Assign to Channel B ->
	Assign to Channel B ->
	Assign to Channel B ->

The following steps describe how to use the Live Probes, Active Probes, and the Memory Block debugging features:

1.6.3.1 Specifying Live Probe Points in Libero

With Live Probe, two dedicated probes can be configured to observe a probe point, which is any output of a register. The probe data can be sent to the two dedicated probe pins (PROBE_A and PROBE_B). You can connect an oscilloscope to the probe pins and monitor the signals status. The probe points location can be changed without recompiling or reprogramming the design. The probes can capture data at a speed of up to 100 MHz.

The PROBE_A and PROBE_B pins are dedicated dual-purpose pins. These pins are regular I/Os, if not used by the Live Probes channels. These pins can be reserved for probing by selecting **Reserve Pins** for **Probes** in the **Project Settings** window, as shown in Figure 15.

Figure 15 • Reserving Probe Pin for Probes

O Project Settings	
Device Selection Device Settings Design Flow Analysis Operating Conditions Simulation Options DO File Waveforms	I/O Settings Default I/O Technology:

In addition, the probe pin on your package can be identified from the pin description document for that particular package. Another option is to check the Function column in the Package Pins tab of the **I/O Editor** in the Libero SoC software, as shown in Figure 16.

Y10 and W10 are the two dedicated probe pins in M2GL010T and M2S090T in the 484 FBGA package, which can be used for probing, as shown in Figure 16.



Figure 16 • Identifying Probe Pins using Package Viewer Inside Libero I/O Editor

Po	rts Package Pi	ns Package	/iewer				
	Pin Number 💌	Port Name 💌	Macro Cell 💌	Function	Ļ	Locked	*
381	AA10	Unassigned		MSIO122PB4			
382	AB10	Unassigned		MSIO122NB4			
383	W10			MSIO121PB4/PROBE_A			
384	Y10			MSIO121NB4/PROBE_B			
385	W9	Unassigned		MSIO120PB4			-
•	III					۱.	

Note: The probe pins, PROBE_A/PROBE_B, are not exposed and not accessible on the IGLOO2 Evaluation Kit Rev C board. These pins are accessible on the IGLOO2 Evaluation Kit board Rev D and SmartFusion2 M2S090TS Security Evaluation Kit Rev D on J29 and J30 jumpers.

Figure 17 shows an example of setting two probe points: coutA[23]:Q and coutA[24]:Q to be probed on ChannelA and ChannelB respectively. The Live Probes tab shows the probe point name and pin type (SRAM, Logic, or I/O). When a probe point is selected, it can be assigned to either ChannelA (PROBE_A) or ChannelB (PROBE_B) as follows:

- 1. Select the **point** to be probed, as shown in Figure 17.
- 2. From the **Netlist View**, select the Net to be probed, and click Add to that Net to the FPGA Array debug data.
- 3. Click Assign to Channel A or Assign to Channel B.
- 4. Click Close.

A message is displayed in the Log window of Libero SoC, showing the signals that are assigned to be probed, as follows:

Live probe has been set:

PROBE_A:

Channel A: Fabric_Debug_0/count_0/coutA[23]:Fabric_Debug_0/count_0/coutA[23]:Q

PROBE_B:

Channel B: LED1_c:Fabric_Debug_0/count_0/coutA[24]:Q.

After setting the channels, SmartDebug configures the ChannelA and ChannelB I/Os to monitor the desired probe points. On the SmartFusion and IGLOO2 Evaluation Kit Rev D boards, the PROBE_A and PROBE_B pins are exposed on the J29 and J30 connectors. An oscilloscope can be connected to these probe points to monitor the signals that are assigned to be probed. The maximum number of simultaneous probes is two internal signals. A filter box is provided to filter out the Net Names.

Note: The Active Probes WRITE overwrites the settings of the Live Probe channels, if any.



Figure 17 • Live Probes Channels Assignments

bug FPGA Array	₽×	FPGA Array debuq data	
Herarchical View Netlist View Step 1: Search for Filter: *coutA[24]*	desired net	Live Probes Active Probes Memory Blocks Probe Insertion Delet	te Delete All
Net(s):	Add	Name	Туре
Name Type		Fabric_Debug_0/count_0/coutA[23]:Fabric_Debug_0/count_0/coutA[23]:Q	DFF
LED1_c:Fabric_Debug_0/count_0/coutA[24]:Q DFF		LED1_c:Fabric_Debug_0/count_0/coutA[24]:Q	DFF
Step 2: Select desired net from list and click Add	d.	Step 3: Assign Added net to desired Channel fro debu	g
		Assign to Channel A -> Fabric_Debug_0/count_0/coutA[23]:Fabric_De	ebug_0/count_0/coutA[23]:C
		Assign to Channel B -> Fabric_Debug_0/count_0/coutA[23]:Fabric_De	ebug_0/count_0/coutA[23]:ς
		Unassign Channels	
Help			Close

Note: Click the **Unassign Channels** button to clear the live probe names to the right of the channel buttons, and to also discontinue the live probe function during debug.

1.6.3.2 Active Probes

Active Probe allows dynamic asynchronous read and write to a flip-flop or probe point. It enables you to observe the output of the logic internally or to experiment on how the logic is affected by writing to a probe point. The following steps describe how to select a specific set of probe pins by reading the current value and then writing different values.

1.6.3.2.1 Selecting Active Probes

- 1. On the Debug FPGA Array window, click the Active Probes tab.
- 2. Add search filter to find desired net to add probe., as shown in Figure 18.

Figure 18 • Selecting Active Probes From the Design

Debug FPGA Array		
; v		
Live/Active Probes Selection	5 ×	FPGA Array debug data
Herarchical View Netlist View		Live Probes Active Probes Memory Blocks Probe Insertion
Filter: *could[2* Step 1: Search for desired nets for probe Net(p): Step 2: Highlight desired nets from list below and click Add.	Search Add	Example Save Laad Delete Delete Al Name IED1_cFebric_Debug_count_0(count_0(count_0)count_0(coun
Name	Type ^	
Fabric_Debug_0/count_0/coutA[21]:Fabric_Debug_0/count_0/coutA[21]:Q	DFF	
Fabric_Debug_0/count_0/coutA[22]:Fabric_Debug_0/count_0/coutA[22]:Q	DFF	
Fabric_Debug_0/count_0/coutA[23]sFabric_Debug_0/count_0/coutA[23]:Q	DFF	
Fabric_Debug_0/coutA_net_0[2]:Fabric_Debug_0/count_0/coutA[2]:Q	DFF	
LED1_c:Febric_Debug_0/count_0/coutA(24):Q	DFF	
LED2_c:febric_Debug_0/count_0/coutA[25]:Q	DFF	
LED3_c:Fabric_Debug_0/count_0/count4[26]:Q	DFF +	Read Active Probes Write Active Probes
Heb		Close

A window that shows all the available probe points in the design opens. In this tutorial, the following points are monitored:

- Three bits of the counter output coutA—coutA[24]:Q, coutA[25]:Q and coutA[26]:Q.
- The monitoring signal error, which is also connected to the LED (H5) on the board. If the LED is ON, it indicates that the RAM count and the expected value mismatch.

To find these points in the list of available probe points, use the Filter control, as shown in Figure 19.

Note: As Active Probe only deals with individual signals, the coutA bus segment is broken up into three separate probe lines.



- 3. Select the desired points and click **Add** to move to the **Selected Probe Points** window and click **Read Active Probes**, as shown in Figure 19.
- **Note:** The coutA bus counts constantly. As a result, the value that you read may be different from the value shown. Also, the error signal must be High (LED H5 is OFF), which indicates that there are no errors in the counting pattern.

Debug FPGA Array								
Ţ								
Live/Active Probes Selection \blacksquare ×	FPGA Array debug data							
Hierarchical View Netlist View	Live Probes Active Probes Memory Blocks	Probe Insertion						
Filter: *error:Q Search		Save	Load	Delete	Delete All			
Net(s): Add	Name	Туре	Read Value	Write Value				
Add	LED1_c:Fabric_Debugcount_0/coutA[24]:Q	DFF	1					
Name	LED2_c:Fabric_Debugcount_0/coutA[25]:Q	DFF	0					
error_c:Fabric_Debug_0/count_chk	LED3_c:Fabric_Debugcount_0/coutA[26]:Q	DFF	0					
endi_endire_bebdg_oyeount_enk	error_c:Fabric_Debug_0/count_chk_0/error:Q	DFF	1					
Read current state of Active Probe								
< ۲	Read Activ	ve Probes	Write Active Probes					
Неір		K	2		Close			

Figure 19 • Selecting Desired Points to Read and Reading the Values

Note: The "+" and "-" icons expand or collapse the bus or group present in the Active Probes UI. In Figure 19, there is no bus or group, as a result, these buttons are not enabled.

1.6.3.3 Writing Active Probes

The write operation is similar to the read operation. After specifying points you can define new write values that are applied to the device, when **Write Active Probes** is selected. Figure 20 shows the results of a first write of the design.





Figure 20 • Active Probe Writing

Debug FPGA Array									
ve/Active Probes Selection 🛛 🗗 🗙	FPGA Array debug data								
Hierarchical View Netlist View	Live Probes Active Probes Memory Blocks	Probe Insertion							
Filter: *error:Q Search		Save	Load	Delete	Delete All				
Net(s): Add	Name	Туре	Read Value	Write Value					
	LED1_c:Fabric_Debugcount_0/coutA[24]:Q	DFF	1	0	<u> </u>				
Name	LED2_c:Fabric_Debugcount_0/coutA[25]:Q	DFF	0		<u> </u>				
error_c:Fabric_Debug_0/count_chk	LED3_c:Fabric_Debugcount_0/coutA[26]:Q	DFF	0						
	error_c:Fabric_Debug_0/count_chk_0/error:Q	DFF	1		<u> </u>				
Changing to state by wring new value									
Read Active Probes Write Active Probes									
Help					Close				

Note: To toggle the states between High and Low, select a new Write Value from the drop-down menu and click Write Active Probe to update the state.

Use the Save button to save a set of Active probes, and to save them to a file. Use the Load button to load a saved active probe setup. This allows the user to use various setups while debugging without needing to recreate the active probe settings.

The coutA bus counts constantly, therefore, the value that you read may be different from the value shown in Figure 20.

Also, the error signal must be **High (LED H5 is OFF)**, indicating that there are no errors in the counting pattern.

The Probe grouping feature is available with Active Probes. This feature is useful to manage large designs with many signals. This feature gathers multiple signals as a single entity. Probe nets with the same name are automatically grouped in a bus when they are added to the Active Probes tab. Create Custom probe groups by manually selecting and adding probe nets of a different name into the group.

1.6.3.4 Fabric SRAM Memory Debug

To view the content of the Large SRAM in this design, click the **Memory Blocks** tab, as shown in Figure 21.



Figure 21 • Memory Blocks Tab

Debug FPGA Array	
Memory Blocks Selection	FPGA Array debug data
Memory Blocks: Select	Live Probes Active Probes Memory Blocks Probe Insertion
Fabric_Debug_0/DPSRAM_0/Fabric_Debug_DPSRAM_0_DPSRAM_ROC	Current Memory Block: Data bit Mode:
۲ <u>ااا</u>	Read Block Write Block
Help	Close

This design contains a single Large SRAM, named DPSRAM_0, and it is the only one available on the left side window that shows the list of all the available RAM blocks in your design. If your design has more RAM blocks, the RAM blocks are shown on this left side panel window. Highlight the memory block from the left panel, and double-click or click **Select** to make it the "**Current Memory Block**" to debug. After selecting the block, click on **Read Block**.

The contents of the DPSRAM_0 is displayed, as shown in Figure 22. See the counting pattern that is loaded into the RAM.

Ŧ	K																	
emory Blocks Selection	PGA Arra Live Pro Current Data bit	bes Memo	Activ	/e Prob			ry Bloc D/DPSR		Probe /Fabric			RAM_0	_DPSR	AM_R	DC0/IN	ST_RA	M1K1	3_IP
Step 1: Select desired memory block from list and click Select	0000	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	-
	0010	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F	
	0020	020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	
	0030	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F	
	0040	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	
	0050	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F	
	0060	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	-
۲ m							Read	Block		Writ	e Block	:						
Helo							o 2: C nory		Read ent	Block	k to c	aptu	re cu	rrent				Close

Figure 22 • DPSRAM_0 Contents

Note: The left pane displays all the memory blocks contained in the design. The right pane only displays the current memory block that is selected.

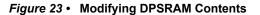


1.6.4 Writing to Fabric SRAM Blocks

The design reads the contents of the DPSRAM and compares it with a synchronized counter in the checker, which looks for errors. If the content of the DPSRAM is modified, it breaks the count pattern and causes an error in the checker.

The following steps describe how to modify the RAM content and force an error:

- 1. Read the memory content, as shown in Figure 22.
- 2. Select an entry and double-click. Each entry is 9-bits wide.
- 3. Modify the value from the current value to break the count pattern. An example is shown in Figure 23.
- **Note:** The counter writes to the SRAM constantly. To prevent the overwrite of the changes that are forced into the SRAM, the writing is stopped by forcing A_WEN LOW through Switch2 (SW2). This drives a SELECT of a mux that selects between High and Low inputs. When SW2 is pressed, A_WEN becomes low, which prevents any write from the counter to the SRAM block.
 - 4. Press and hold SW2 and click Write Block to write the modified value to the SRAM.
 - 5. The error LED(H5) light turns ON, indicating an error in the counting pattern.
 - 6. Release SW2 to resume the write operation from the counter to the SRAM. This overwrites the error that was injected into the SRAM. The content of the SRAM can be rechecked by clicking **Read Block**.



Debug FPGA Array								((
Memory Blocks Selection	₽× Select		rray debu Probes	-	ve Prot)es	Memo	ry Bloc	ks	Probe	Insert	ion							
Fabric_Debug_0/DPSRAM_0/Fabric_Deb	ug_DPSRAM_0_DPs		nt Memo bit Mode		k: Fa	abric_D	ebug_(D/DPSF	AM_0/	Fabric	_Debug]_DPSI	RAM_0	_DPSR	AM_R	DCO/IN	IST_RA	M1K18	B_IP
		000	000	001	002	003	004	OBB	006	007	008	009	00A	00B	00C	00D	00E	00F	^
		001	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F	
		002	0 020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	
		003	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F	
		004	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	
		005	0 050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F	
		006	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	-
								Read	Block		Write	e Block							
Help																			Close

1.6.5 **Probe Insertion**

Probe insertion is a post-layout process that enables you to insert probes into the design and bring signals out to the FPGA package pins to evaluate and debug the design. Probe insertion enables you to select internal nets anywhere in the design, connect those nets to unused pins, and then run layout incrementally to manage the physical connection to the pin. Nets are selected and assigned using the SmartDebug Probe Insertion feature. For more information, refer to the *FPGA On-Chip Debug Tools.*

The following steps describe how to probe a net:

- 1. On the **Debug FPGA Array** window, click the **Probe Insertion** tab and click **Add Probe**, as shown in Figure 24.
- In the Filter field, enter the *couta* signal, as shown in Figure 24, and click Search. Select signal Fabric_Debug_0/count_0/coutA_s[24]. The goal is to add a probe by routing the counter bit 24 signal out into the E1 LED and check if it toggles.



- 3. Click Add.
- 4. In the **Probe Insertion** window, assign **Package Pin E1**, as shown in Figure 24.

Figure 24 • Assigning Package Pin and Running the Flow

erarchical View Netlist View		Live Probes	Active Probes	Memory Blocks	Probe Insertion			
ter: *coutA_s*	Search						Delete	Delete All
et(s):	Add	Ne	t I		Driver		Package Pin	Port Name
Name	Type ^	Fabric_Deb	ug_0/cou Fabric_De	bug_0/count_0/cou	tA_cry[24]:S		E1	Probe_Insert0
abric_Debug_0/count_0/coutA_s[20]:Fabric_Debug_0/count_0/coutA_cry[20]:S	1BIT				Step 1: Assig	n probe to package pi	n	
abric_Debug_0/count_0/coutA_s[21]:Fabric_Debug_0/count_0/coutA_cry[21]:S	1BIT							
abric_Debug_0/count_0/coutA_s[22]:Fabric_Debug_0/count_0/coutA_cry[22]:S	1BIT							
abric_Debug_0/count_0/coutA_s[23]:Fabric_Debug_0/count_0/coutA_cry[23]:S	1BIT							
abric_Debug_0/count_0/coutA_s[24]:Fabric_Debug_0/count_0/coutA_cry[24]:S	1BIT					Step 2: Click Run		
abric_Debug_0/count_0/coutA_s[25]:Fabric_Debug_0/count_0/coutA_cry[25]:S	1BIT	•			111			
abric_Debug_0/count_0/coutA_s[26]:Fabric_Debug_0/count_0/coutA_s[26]:S	1BIT +					Insert probe(s) an	id program the device	Run

5. Click Run.

The place and route tool is run incrementally in the background re-routing the coutA_s[24] signal to package pin E1, which is the LED on the board. The LED E1 on the board starts toggling when the incremental place and route is completed, which indicates that the counter output bit[24] is routed to the E1 package pin.

6. Click Close to exit the Debug FPGA Array window.

Note: The Probe Insertion tab is not available with stand-alone SmartDebug.

1.6.6 SERDES Debug

This SmartDebug SERDES tutorial helps the FPGA and board designers to perform SERDES real-time signal integrity testing and tuning in a system that:

- Provides real-time access to SERDESIF block control and status registers
- Provides testing functions with pseudo-random binary sequence (PRBS) pattern generators and checkers
- Runs link tests with various loop back options
- Provides overview for tuning many combinations of physical medium attachment (PMA) analog settings to find the optimal set for a SERDES channel





The following steps describe how to perform SERDES debug:

1. On the SmartDebug window, click Debug SERDES, as shown in Figure 25.

Figure 25 • Debug SERDES Operation Selection

SmartDebug		
<u>File V</u> iew <u>H</u> elp		
Device: [M2GL010T (M2GL010T)	Programmer: 94782 (usb94782) v	
ID code read from device: F8031CF		
View Device Status	Debug FPGA Array	
View Flash Memory Content	Debug SERDES	
Log I Messages 😵 Errors 🗼 Warnings 👔 Info	6 ×	

The Configuration tab is displayed as shown in Figure 26. The **Configuration** tab auto-identifies and populates SERDESIF and the lanes used in the design. The status of each lane and the programmed lane mode are displayed. This example demonstrates the use of SERDESIF_0 block and the lock status of TxPLL and RxCDR.

2. Click Refresh Report, to update the data.



Figure 26 • SERDES Configuration Tab

Debug SERDES		? X
SERDES I	SERDES Block: SERDESIF_0 O Lane 0 Lane 1 Lane 2 Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset Lane 3 Reset	
Debug SERDES	Configuration Report:	
Configuration Tests PRBS Test Loopback Test	Serdes Block SERDESIF_0 : Lane 0 : Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked RxPLL status : Locked Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked RxPLL status : Locked RxPLL status : Locked Lane 2 : Lane mode : Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked RxPLL status : Locked Lane 3 : Locked Lane mode : EPCS (custom) PMA Ready : True TxPLL status : Locked RxPLL status : Locked RxPL status : Locked SerDES Register Read or Write: Script:	Refresh Report
Help		Close

3. The PRBS Test tab provides several capabilities for each lane of the SERDES block. Based on the selected SERDES lane, information is provided for each channel. For example, select Lane 0, Nearend Serial Loopback, PRBS7, and click Start, as shown in Figure 29. This test generates and checks PRBS7 data without going off-chip. The green LEDs indicate the lock status of TxPLL and RxCDR for the selected lane.





Figure 27 • SERDES Test Tab

Debug SERDES	? ×
Debug SERDES Step 2: Select Lane to SERDES Debug SERDES Configuration Tests PRBS Test Loopback Test Step 1: Select PRBS Test	? X
Help	Close

In this example setup, the data stream is expected to have zero errors as the datapath does not go off-chip while using the Near-end Serial Loopback as shown in Figure 27.

The Data Rate value is entered optionally based on the actual targeted data rate of the design. This rate is entered in Gbps, and is used to derive the bit-error rate (BER). When the Data Rate is entered, the bit-error rate is calculated based on the following formula:

BER = (1 + Error count) / (data rate * seconds)

If the Data Rate is left blank, BER is not calculated. The **Reset** button clears the Cumulative Error Count and the Bit-Error Rate.





Figure 28 • SERDES Link Status

Ø Debug SERDES	
	SERDES Block: SERDESIF_0 SERDES Lane 0 Lane 1 Lane 2 Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset Lane 3 Reset
Debug SERDES	Lane 0 status: RxPLL TxPLL Lock to data
Configuration Tests PRBS Test Loopback Test	Test Type: Status indicators of PLLs and CDR data
Help	Close

Note: Lane 0 is the PCIe[®] lane. This lane is connected to the PCIe edge fingers of the Evaluation board.

4. Click **Stop** and select **Serial Data** (**Off-Die**). Click **Start** and observe that the **Lock to data** status indicator is red. This indicates that the data is no longer looping between Tx and Rx and Lane 0 is not looped together on the PCB.



Figure 29 • Sending Serial Tx Data Off-Die

3

Debug SERDES	? **
	SERDES Block: SERDESIF_0 v SERDES Lanes: O Lane 1 Lane 2 Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset Lane 3 Reset Lane 3 Reset Lane 3 Reset Lane 4 Reset Lane 4 Reset Lane 4 Reset Lane 5 Reset La
Debug SERDES	Lane 0 status: RxPLL 🔵 TxPLL 🔍 Lock to data 🔴
Configuration Tests PRBS Test	Test Type: Status indicators show failure due to open channel connection Near End Serial Loopback (On-Die) Serial Data (Off-Die)
Loopback Test	Pattern: PRBS 7 PRBS 11 PRBS 23 PRBS 31 Cumulative Error Count Data Rate Bit Error Rate NA Gbps NA Reset Stop
Help	Close

5. The Evaluation Kit board connects Lane 1 on the PCB to loop back Tx and Rx. This loopback demonstrates a complete path with data transmitted and received. For example, select Lane 1, Serial Data (Off-Die), PRBS7, and click Start, as shown in Figure 32. This test generates and checks PRBS7 data going off-chip and folded back on the PCB to the receiver.



Figure 30 •	I ane 1 Transmittin	g Data Through	On-Board Loopback
		g Data Initagi	

3

Debug SERDES	? <mark>×</mark>
Debug SERDES	SERDES Block: SERDESIF_0 Lane 0 Lane 1 Lane 2 Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset Lane 3 Reset Lane 1 status: RxPLL TxPLL Lock to data
Configuration Tests PRBS Test	Test Type: Near End Serial Loopback (On-Die)
Loopback Test	PRBS7 PRBS11 PRBS 23 PRBS 31 Cumulative Error Count Data Rate Bit Error Rate 0 Start 0 Data Rate Bit Error Rate 0 Data Rate 0 Data Rate Bit Error Rate 0 Data Rate 0
Help	Close

6. The Tx and Rx channels of Lane 2 can be interconnected in a loopback configuration using coaxial cables. In this example, as shown in Figure 33 and Figure 34, after connecting a pair of high-quality 50 Ω SMA cables to the SMA connections on the Evaluation Kit board, SERDES debug can be used to send data off-board and check for errors. Select Lane 2, Serial Data (Off-Die), PRBS7, and click Start.

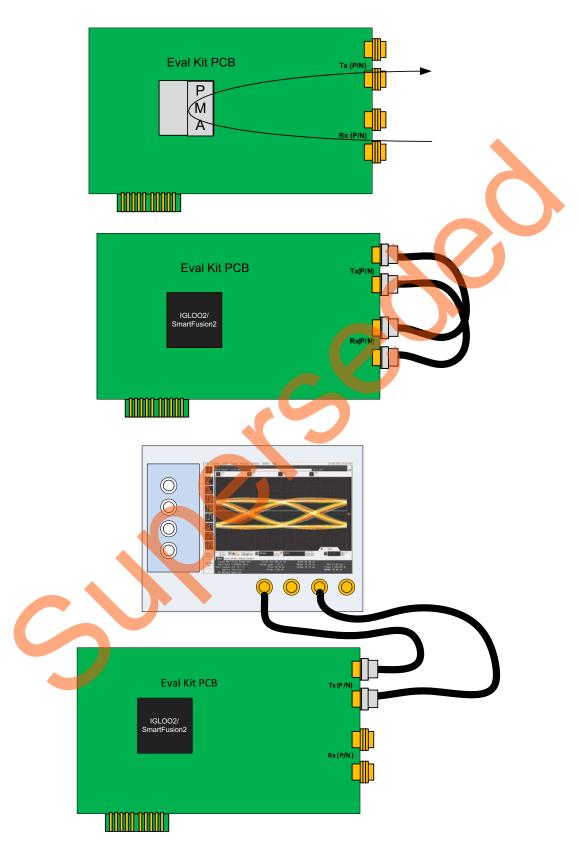


Figure 31 • External Cable Loopback

Debug SERDES	
	SERDES Block: SERDESIF_0 *
	◯ Lane 0 ◯ Lane 1 🔘 Lane 2 ◯ Lane 3
	SERDES Lanes:
Debug SERDES	Lane 2 status: RxPLL TxPLL Lock to data
Configuration	Test Torse
▲ Tests	Test Type: Near End Serial Loopback (On-Die) Near End Serial Loopback (On-Die)
PRBS Test	
Loopback Test	Pattern:
	PRBS7
	PRBS11
	PRBS 23
	O PRBS 31
	Start
	Cumulative Error Count Data Rate Bit Error Rate 0 Gbos NA Reset Stop
	0 Gbps NA Reset Stop
Help	Close
нер	Cose
2	
0	



Figure 32 • Evaluation Kit Board with External Coax Loopback Setup





- 7. The Lane 2 SMA test connections can be used for interconnecting with high-speed coaxial cables to test equipment or other test fixtures like test backplanes. In the example shown in Figure 35, when the Lane 2 test is started without any means to connect the Tx and Rx together, **Lock to data** status goes red as the link is broken between the pattern generator and the checker. This setup sends a data pattern of the board for analysis on the test equipment.
- **Note:** SMA Male-to-SMA Male Precision Cables, such as Pasternack Industries part number PE39429-12 (or equivalent), are recommended.

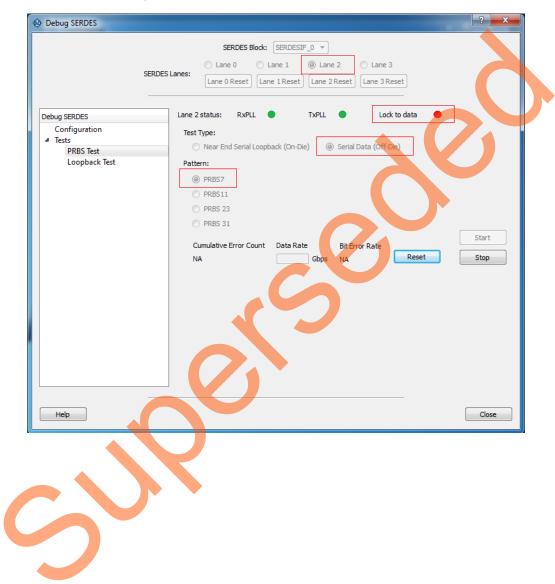
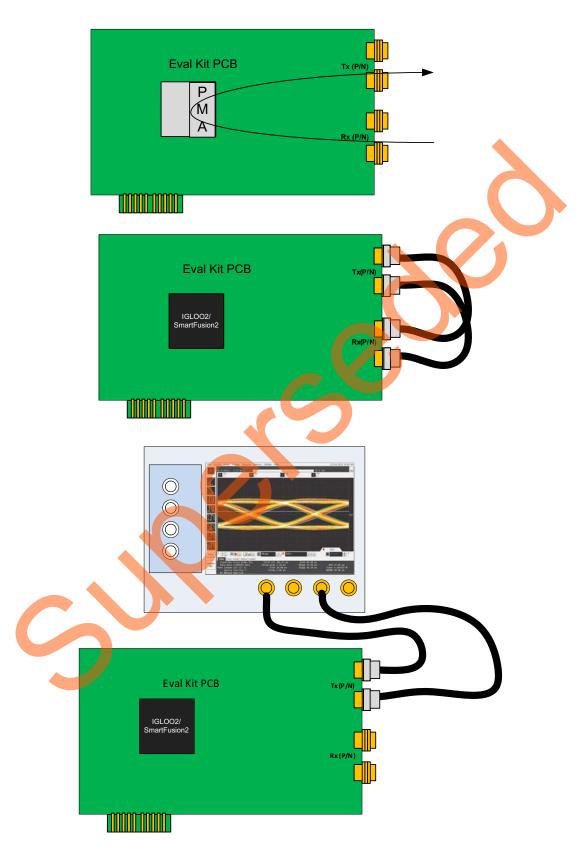


Figure 33 • Lane 2 Transmitting Data Off-Board



Figure 34 • Connecting Lane 2 to the Test Equipment





Several test patterns are available from the test pattern generator. PRBS7 is a very typical pattern for testing signal integrity in communication applications.

Bit error rate (BER) is the count of the number of errors over time to provide a level of confidence for a high-speed link. For a 2.5 Gbps test, it takes about three minutes with zero errors to achieve a BER of 10e-12. The SmartDebug SERDES provides an error counter that can be used for BER test.

1.6.7 Far-End Loop Back Support

Far-end loopback is supported from the **Loopback Test** tab. From this tab, you can receive data from a far-end source and fold the received data (Rx) back out of the transmitter (Tx).

In the example shown in Figure 37 and Figure 38, by using the Evaluation Kit board, data is received from a far-end transmit source, such as a device or test equipment. It is received into Lane 2 and looped back out of the transmitter.

This is performed by selecting SERDES Lane 2, PCS Far End PMS Rx to Tx Loopback Test Type, and clicking Start.

Data entering the SMA connectors on Lane 2 of the Evaluation Kit board is observed coming off the board on the Tx SMA connectors.

Note: In this test, the IGLOO2 Evaluation board or SmartFusion2 Evaluation Kit board must use the same SERDES reference clock as the far-end device that is sending and receiving the data. The datapath through the SERDEIF goes through the CDR and reclocks the data to the local REFCLK. This requires 0 ppm difference between the far-end clock source and the Evaluation Kit clock source. For this, use the SMA inputs (designators J17 and J21) of the board as the input for the SERDES REFCLK.

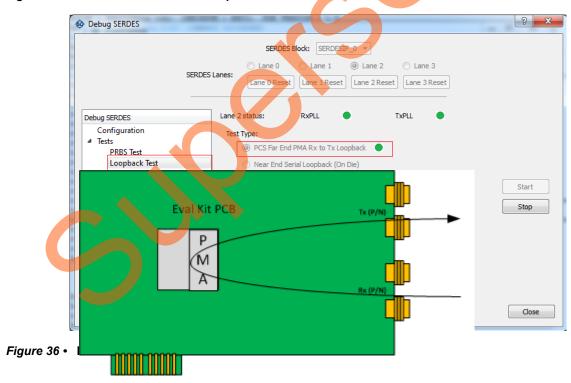


Figure 35 • PCS Far-End Rx to Tx Loopback



1.6.8 Near-End Serial Loopback

The Near-end Serial Loopback Test feature, as shown in Figure 37, includes a loopback that folds back the TX to the RX. This feature requires the FPGA design to verify the correct operation of the looping data stream.

Use this feature to allow an FPGA application to send a data stream into the SERDES, and to bring the data stream back into the FPGA from the SERDES. This operation is done at the device pins without leaving the device. All data generation and checking is done in the FPGA application design.

Figure 37 • Loopback Test Feature

		SERDES Block: SERDESIF_0 *	
	SERDES Lanes:	Lane 0 Lane 1 Image: Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset	
Debug SERDES	Lane	2 status: RxPLL 🔵 TxPLL 🦲	
Configuration Tests PRBS Test	Test	Type: PCS Far End PMA Rx to Tx Loopback	
Loopback Test		Near End Serial Loopback (On Die)	Start
			Stop
		6	_
Help			Close
	Q		



1.6.9 Tcl Support

The SERDES Debug tool set permits execution of Tcl scripts. This allows customized writes and reads of the entire SERDES register base. Tcl can be used to update or check status of the SERDES system, PCle system, and SERDES lane registers.

Tcl command syntax is:

```
read register -addr <RegisterAddress >
write register -addr <RegisterAddress> -value <RegisterValue>
where RegisterAddress is 8 hex character (with optional 0x prefix) example:
0x4002200C
RegisterValue is 1-8 hex character (with optional 0x prefix)
                                                                   example: 0x1,
0x1F
Example:
read_register -addr 0x4002200C
write register -addr 0x4002E008 -value 0x3
Address for the SERDES blocks are as follows:
                                    0x40028000 - 0x4002A3FF
SERDESIF 0
SERDESIF 1
                                    0x4002C000 - 0x4002E3FF
SERDESIF 2
                                    0x40030000 - 0x400323FF
                                    0x40034000 - 0x400363FF
SERDESIF 3
Within each SERDES block, the memory map is as follows:
```

Name – Offset from the base address (example, for SERDESIF_0 the base address is 0x40028000).

PCle Core register map	0x0000 – 0x0FFF
Lane 0 registers	0x1000 – 0x13FF
Lane 1 registers	0x1400 – 0x17FF
Lane 2 registers	0x1800 – 0x1BFF
Lane 3 registers	0x1C00 – 0x1FFF
SERDESIF system register map	0x2000 – 0x23FF

Example Tcl applications:

- 1. To access the Tx Impedance Ratio register for lane 2 in SERDESIF_1, the address is 0x4002C000 (SERDESIF_1 base) + 0x1800 (lane 2 offset) + 0x0C (register offset) = 0x4002D80C
- 2. To access the PRBS Control register for lane 0 in SERDESIF_0, the address is 0x40028000 (SERDESIF_0 base) + 0x1000 (lane 0 offset) + 0x190 (register offset) = 0x40029190

For register map details, refer to the UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide.

Read only the lanes that are programmed by the design. Also, read the PCIe registers only if any of the lanes have PCIe protocol.



Example:

The Tcl script below is used to alter the TX_PST (Transmit Post Emphasis) setting of Lane 0 of SERDESIF_0.

Serdes block 0

Set the config_phy_mode_1 value by separately running the following Tcl
command "" in separate script and write the value without '0x' prefix

set config_phy_mode_1 80f

set config_phy_mode_1

scan \$config_phy_mode_1 %x phyMode1Val

set CONFIG_REG_LANE_SEL for this lane
set lane0PhyMode [expr { (\$phyMode1Val & 255) | 256
scan [format %x \$lane0PhyMode] %s lane0PhyMode
write_register -addr 0x4002a028 -val \$lane0PhyMode
puts "Serdes lane0 registers"

write_register -addr 0x40029028 -val 0x1a
puts "TX_PST_RATIO"

read register -addr 0x40029028

#Reset the config_phy_mode_1 value to original value
write_register -addr 0x4002a028 -val \$config_phy_mode_1

The value of the CONFIG_PHY_MODE_1 register must be known in the example shown above. This register contains the value of the CONFIG_REG_LANE_SEL, which defines the lanes accessed in the design. In this example, reading the CONFIG_PHY_MODE_1 register and passing its value and the associated offset targets the correct lane.

Note: Some SERDES PMA register settings are updated only after the assertion of a PHY_RESET or writing to the UPDATE_SETTINGS register.

Tcl commands and syntax are found in the SmartFusion2 and IGLOO2 FPGAs Tcl for SoC – Tcl Documentation.

From the **Debug SERDES Configuration** tab, an executable Tcl script can be imported. Browse to the Tcl script file and click **Execute**, as shown in Figure 39. The script contains commands to write or read registers using a flattened top for most address mapping.



Figure 38 • Tcl Script Execution User Interface

Debug SERDES	२ <mark>×</mark>	
	SERDES Block: SERDESIF_0 Clane 0 Lane 1 Lane 2 Lane 3 Lane 0 Reset Lane 1 Reset Lane 2 Reset Lane 3 Reset	
Debug SERDES	Configuration Report:	
Configuration Tests PRBS Test Loopback Test	Serdes Block SERDESIF_0: Lane 0: Lane mode: EPCS (custom) PMA Ready : True TXPLL status : Locked Lane i: Lane mode: Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked Lane i: Lane mode: Lane z: Lane divertex Lane z: Lane divertex Lane z: Locked Lane z: Locked Lane z: Lane divertex Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked Lane 3: Locked Lane 3: Lane divertex Lane mode : EPCS (custom) PMA Ready : True TXPLL status : Locked RxPLL status : <td< td=""><td></td></td<>	
	Script: artdebug_liberov11p7_tu_df/m2gl_SmartDebug_Tutorial/serdes0_config.td Execute	
Help	Close	

After execution of the Tcl SERDES access, the log of the access is displayed in the SmartDebug Console Log pane, as shown in Figure 40.

Figure 39 • SERDES Access Log

1.09
Messages 😵 Errors 🗼 Warnings 🕕 Info
Messages S Erors A Warnings Info The 'write_register' command succeeded. Serdes lane0 registers Register Address: 0x40029000, Value: 0x80 Ine 'read_register' command succeeded. CRO Register Address: 0x40029004, Value: 0x20 The 'read_register' command succeeded. ERRCNT_DEC Register Address: 0x40029008, Value: 0xf8 The 'read_register' command succeeded. RXIDLE_MAX_ERRCNT_THR Register Address: 0x4002900c, Value: 0x80 The 'read_register' command succeeded. IMPED_RATIO Register Address: 0x40029010, Value: 0x00 The 'read_register' command succeeded. PLL_F_PCLK_RATIO Register Address: 0x40029014, Value: 0x13 The 'read_register' command succeeded. PLL_F_NN

Refer to "Appendix" on page 45 for more Tcl examples.



1.6.10 Executing SERDES Debug from SmartDebug Tcl

1.6.10.1 PRBS

User-level command: Used in PRBS test to start, stop, reset the error counter, and read the error counter value.

prbs_test [-deviceName <device_name>] -start -serdes <num> -lane <num> [near] -pattern <PatternType> [-value <PatternValue>]

prbs_test [-deviceName <device_name>] -stop -serdes <num> -lane <num>

prbs_test [-deviceName <device_name>] -reset_counter -serdes <num> -lane
<num>

prbs test [-deviceName <device name>] -read counter -serdes <num> -lane <num>

-deviceName <device_name>: Parameter is optional, if only one device is available in the current configuration or set for debug (see the SmartDebug User Guide, for details).

-start: To start PRBS test.

-stop: To stop PRBS test.

-reset_counter: To reset the PRBS error count value to 0.

-read_counter: To read and print the error count value.

-serdes < num>: SERDES block number. Must be between 0 and 4 and varies between dies.

-lane <num>: SERDES lane number. Must be between 0 and 4.

-near: Corresponds to near-end (on-die) option for PRBS test. Not specifying this option implies off-die.

-pattern <PatternType>: The pattern sequence to be used for the PRBS test. It can be one of the following:

prbs7 or prbs11 or prbs23 or prbs31

custom

user

-value < PatternValue>: Specifies the pattern type value for cases other than PRBS* sequences. It can be one of the following:

If custom is selected above, then it must be one of all_zeros, all_ones, alternated, or dual_alternated.

If **user** is selected above, then it must be 20 hexadecimal characters.

Example:

```
prbs_test -start -serdes 1 -lane 0 -near -pattern prbs11
prbs_test -start -serdes 2 -lane 2 -pattern custom -value all_zeros
prbs_test -start -serdes 0 -lane 1 -near -pattern user -value
0x0123456789ABCDEF0123
```



1.6.10.2 Loopback

User level command: Used to start and stop the loopback tests.

```
loopback_test [-deviceName <device_name>] -start -serdes <num> -lane <num> -
type <LoopbackType>
```

```
loopback test [-deviceName <device name>] -stop -serdes <num> -lane <num>
```

deviceName <device_name>: Parameter is optional, if only one device is available in the current configuration or set for debug (see the SmartDebug User Guide, for details).

start: To start loopback test.

stop: To stop loopback test.

serdes <*num*>: SERDES block number. Must be between 0 and 4 and varies between dies.

lane <num>: SERDES lane number. Must be between 0 and 4.

type <LoopbackType>: Specifies the loopback test type. Must be one of the following:

- 1. plesio (PCS Far End PMA Rx to Tx Loopback)
- 2. parallel
- 3. meso (PCS Far End PMA Rx to Tx Loopback)

Example:

loopback_test	-start	-serdes	1	-lane 1	type	meso
loopback_test	-start	-serdes	0	-lane () -type	plesio
loopback_test	-start	-serdes	1	-lane 2	2 -type	parallel
loopback_test	-stop -	-serdes		lane 2		

Tcl scripting for SERDES SmartDebug can be used in batch mode without launching SmartDebug. The following is an example batch script:

open_project -project {D:/my_serdes_design/my_serdes.pro}

set_debug_device -name {M2S/M2GL050(T|S|TS)}

read_id_code

```
set_programming_file -name {M2S/M2GL050(T|S|TS)} -file {./
SERDES1_REFCLK1_EPCS_MODE_SF2_DEV_KIT/SERDES1_REFCLK1_EPCS_MODE/designer/
SERDES_LOOPBACK_top/export/SERDES_LOOPBACK_top.stp}
```

run selected actions

set_debug_device -name {M2S/M2GL050(T|S|TS)}

//Place serdes tcl commands after here

1.7 Stand-Alone SmartDebug

SmartDebug is offered as a stand-alone utility. This allows SmartDebug to be used on other host computer systems without the full installation of the Libero SoC Software. The stand-alone SmartDebug flow requires the user to create standalone SmartDebug project.

There are two ways to create a stand-alone SmartDebug project:

- Import DDC files from Libero
- Construct automatically



The following procedure describes how to import a DDC file from Libero:

- 1. Enable the appropriate debug features such as probe insertion of the targeted devices in the Libero design project prior to creating the DDC file.
- 2. Double-click Export SmartDebug Data to generate the DDC file from the Libero SoC design flow.

Figure 40 • Export SmartDebug Data

esigr	n Flo	DW				₽×]
Smar	tDe	bug_top	-	0		¢۶	
Тоо	d						
\triangleright	•	Create Design					
\triangleright	•	Create Constraints					
\triangleright	•	Implement Design				~	
\triangleright	•	Program and Debug Design					
\triangleright	•	Handoff Design for Production					
⊿	•	Handoff Design for Debugging				V	
		🕸 Export SmartDebug Data				~	
₹.		III					
Desi	gn i	Flow Design Hierarchy Stimulus Hier	archy	Cat	alog	Files	

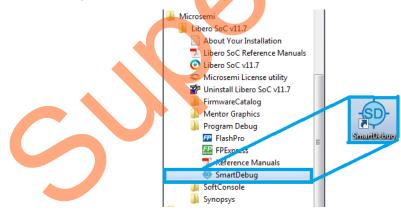
The exported DDC file is located at: <project path>\designer\Project\export\Project_top.ddc

The exported DDC file and programming file need to be transferred to a stand-alone PC for debug sessions.

The following procedure describes how to create a SmartDebug project:

- 1. Connect a FlashPro programmer to a valid hardware device.
- Start SmartDebug stand-alone utility. The Standalone SmartDebug is found in the Program Debug program group of the Microsemi Libero SoC v11.7 program group, as shown in Figure 41. You can also find it as an icon on your desktop.





3. Click New.



Figure 42 • New SmartDebug Project

Project View Tools	
🕒 🚰 🖽 🧶	
SmartDebug Projects	
New Open	
Recent Projects	
Log	ð ×
🔳 Messages 🔯 Errors 🗼 Warnings 🌗 Info	
create SmartDebug Project window is displayed.	

- 4. Enter the name of the SmartDebug project.
- 5. Browse to the desired directory location and select the DDC file related to the Libero SoC project.
- 6. Click **OK**.

The

Figure 43 • Create SmartDebug Project

🐵 Crea	ate SmartDebug Project
Name:	: m2gl_sd
Locatio	on: D:/Microsemiprj/m2s_m2gl_smartdebug_liberov11p7_tu_df/m2gl_SmartDebug_Tutorial
- Cons	struct JTAG chain for the project connected programmers: 81446 Import DDC File: rtDebug_df/designer/SmartDebug_top/export/SmartDebug_top.ddc Design debug data will be imported with JTAG chain Construct Automatically
	Help OK Cancel

The SmartDebug project is created. At this point SmartDebug works exactly the same as when it is launched from Libero. See the prior sections for operation. The Standalone SmartDebug UI is shown in Figure 44.



Figure 44 • Standalone SmartDebug UI

Project View Tools			
Device: M2S090T (M2S090T)	▼ Programme	er: 94782 (usb94782)	
ID code read from device: F8031CF			
View Device Status		Debug FPGA Array	
View Flash Memory Content		Debug SERDES	
			S
g			₽×
🔳 Messages 🔞 Errors 🔺 Warnings 🌗 Info			
Driver : 3.0.0 build 1 programmer '94782' : FlashPro4			^
The project "m2gl_sd" is created.			-

1.8 Conclusion

This tutorial demonstrated the capabilities of SmartDebug. SmartDebug provides the capabilities to observe and analyze many embedded device features. Live Probe gives real-time access to device test points and internal logic states can be easily accessed using Active Probes. The SmartDebug SERDES utility assists FPGA and board designers to validate signal integrity of high-speed serial links in a system and improve board bring-up time. This is completed in real-time without any design modifications. Adjustments and tuning the PMA analog settings for optimal link performance is easily accomplished to match the design to the system. Using the SmartDebug utility with the Evaluation Kit board provides designers a good understanding of its features and capabilities.





2 Appendix

2.1 Tcl Script Examples

2.1.1 Example 1: Change M/N/F registers for Lane1 and Lane2 of SERDESIF 0

set CONFIG_REG_LANE_SEL write_register -addr 0x4002a028 -val 20F read register -addr 0x4002a028 write register -addr 0x40029410 -val 0x0 puts "PLL F PCLK RATIO Lane1" write register -addr 0x40029414 -val 0x13 puts "PLL M N Lane1" write_register -addr 0x40029600 -val 0x1 puts "UPDATE SETTINGS Lane1" puts "Serdes lane1 registers" # set CONFIG_REG_LANE_SEL write_register -addr 0x4002a028 -val 40F write register -addr 0x40029810 -val 0x0 puts "PLL F_PCLK_RATIO_Lane2" write register -addr 0x40029814 -val 0x13 puts "PLL_M_N_Lane2" write register -addr 0x40029a00 -val 0x1 puts "UPDATE_SETTINGS_Lane2"

puts "Serdes lane2 registers"



2.1.2 Example 2: Change RX LEQ registers Lane2 of SERDESIF_0

set CONFIG_REG_LANE_SEL
write register -addr 0x4002a028 -val 40F

write_register -addr 0x4002981c -val 0x00
puts "RE_AMP_RATIO_Lane2"

write_register -addr 0x40029820 -val 0x00
puts "RE_CUT_RATIO_Lane2"

write_register -addr 0x40029a00 -val 0x1
puts "UPDATE SETTINGS Lane2"

2.1.3 Example 3: Change TX De-emphasis registers Lane2 of SERDESIF_0

set CONFIG_REG_LANE_SEL
write register -addr 0x4002a028 -val 40F

write_register -addr 0x40029828 -val 0xa
puts "TX_PST_RATIO_Lane2"

write_register -addr 0x4002982c -val 0x0
puts "TX_PRE_RATIO_Lane2"

write_register -addr 0x40029a00 -val 0x1
puts "UPDATE SETTINGS Lane2"



3 Revision History

The following table shows the important changes made in this document for each revision.

Date	Version	Page
Revision 8 (April 2016)	Updated the document for Libero v11.7 software release (SAR 75567).	NA
Revision 7 (October 2015)	Updated the document for Libero v11.6 software release (SAR 68374).	NA
Revision 6 (January 2015)	Updated the document for Libero v11.5 software release (SAR 62936).	NA
Revision 5 (October 2014)	Updated the document for SERDES core change (SAR 61612).	NA
Revision 4	Updated the document for Libero v11.4 software release (SAR 59069).	NA
(September 2014)	Updated the document for M2S025 Evaluation Kit board details (SAR 59069).	NA
	Updated the document for M2GL010 Evaluation Kit board details (SAR 59069).	NA
Revision 3 (April 2014)	Added Note in "Specifying Live Probe Points in Libero" section(SAR 56593).	17
Revision 2	Updated the software version from 11.2 SP1 to 11.3 (SAR 56012).	NA
(March 2014)	Updated design files using the latest 11.3 SERDES core (SAR 56012).	NA
Revision 1 (January 2014)	Initial release.	NA



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Revision 8



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