Implementing JESD204B Interface Using SmartFusion2 - Libero SoC v11.7

DG0611 Demo Guide

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1 Preface

1.1 Purpose

The demo describes the use of SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) serializer/de-serializer (SERDES) and JESD204B Tx/Rx IP cores for JESD204B data converter interface. This demo uses the CoreJESD204BTx and CoreJESD204BRx IP cores in a loop-back configuration and operates as a standalone demo for JESD204B data converter interface that can be used with the SmartFusion2 Security Evaluation Kit board. A testbench is also provided to simulate the CoreJESD204BTx/Rx cores. Instructions are provided on how to use the corresponding demo as a reference design for JESD204B applications.

1.2 Intended Audience

This document is intended for:

- FPGA designers
- Embedded designers
- System-level designers

1.3 References

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: *http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#documents*

The following documents are referred in this demo guide.

- *CoreJESD204BRX*
- *CoreJESD204BTX*
- *UG0451: IGLOO2 and SmartFusion2 Programming User Guide*
- *UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide*

2 Implementing JESD204B Interface Using SmartFusion2

2.1 Introduction

The SmartFusion2 SoC and IGLOO®2 FPGA family devices have embedded high-speed SERDES blocks that can handle data rates from 1 Gbps to 5 Gbps. The SERDES module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA. JESD204B is a high-speed serial interface standard for data converters from the JEDEC committee. It reduces the number of data inputs and outputs between the high-speed data converters and receivers. Microsemi® has both JESD204B Rx/Tx IP cores compliant with the JESD204B standards. These cores are easy to integrate with JESD204B based data converters for developing high bandwidth applications such as wireless infrastructure transceivers, software defined radios, medical imaging systems, and radar and secure communications.

The SmartFusion2 and IGLOO2 JESD204B Rx/Tx IP cores support link widths of x1, x2, and x4 up to 3.2 Gbps per lane using subclass 0, 1, and 2. This demo guide describes how to use the SmartFusion2 SERDES blocks, JESD204B Rx/Tx IP cores for interfacing subclass0 JES204B based data converters with the data rates up to 2 Gbps. This demo does not use any analog-to-digital converter (ADC) or digital-to-analog converter (DAC) devices, but operates in a loop-back to provide an example of these IP cores in a working design. This demo design works only on SmartFusion2 devices, not on IGLOO2 devices.

- Refer to the *JESD204B standard from JEDEC* for information on JESD204B interface.
- Refer to the *UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide* for more information on SERDES blocks.

2.2 Design Requirements

Table 1 lists the design requirements.

Table 1 • **Design Requirements**

Design Requirements	**Description**
Hardware Requirements	
SmartFusion2 Security Evaluation Kit • 12 V - 2 A wall mounted power supply • FlashPro4 JTAG Programmer • USB 2.0 A-male to mini-B for UART • 2 SMA to SMA cables[1]	Rev D or later
Host PC or Laptop	Any Windows 64-bit
Software Requirements	
Libero® System-on-Chip (SoC)	v11.7
SoftConsole	v3.4 SP1[2]
FlashPro Programming Software	v11.7

Table 1 • **Design Requirements *(continued)***

Design Requirements	Description
Host PC Drivers for FlashPro5	USB to UART drivers

Note:

1. SmartFusion2 Security Evaluation Kit does not include the 2 SMA cables. The user needs to obtain the cables to run this demo.
2. For this demo guide, SoftConsole v3.4 SP1 is used. For using SoftConsole v4.0, see the *TU0546: SoftConsole v4.0 and Libero SoC v11.7 Tutorial*.

2.3 Demo Design

2.3.1 Introduction

The demo design files are available for download from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_liberov11p7_df*

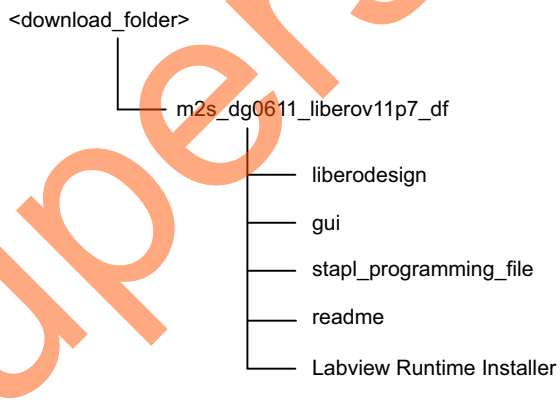
The demo design files include:

- Libero SoC software project
- STAPL programming file
- Graphical User Interface (GUI)
- Sample programming files
- Labview Runtime Installer

For more information, see the `readme.txt` file.

Figure 1 shows the top-level structure of the design files.

Figure 1 • **Top-Level Directory Structure**



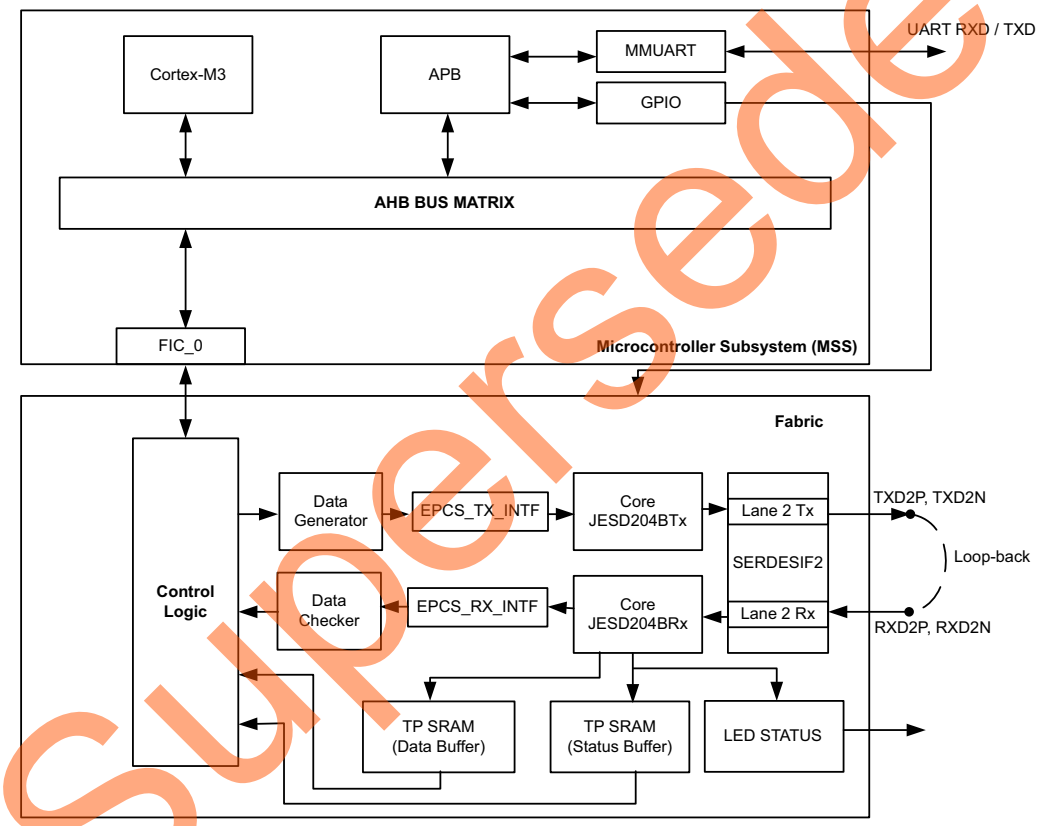
2.3.2 Features

The SmartFusion2 JESD204B demo is a standalone reference design developed for interfacing JESD204B compliant data converters with the SmartFusion2 devices. In this demo design, the SERDES lanes are looped back and the data generator pattern is checked by data checker after traversing through both the JESD204B Tx/Rx IP cores. A user friendly GUI is provided to control and monitor the status signals. Figure 2 shows the JESD204B demo design block diagram implemented in the SmartFusion2 device.

This reference design describes the following:

- Hardware demonstration by externally looping back the SERDES Tx/Rx lanes externally on SmartFusion2 Security Evaluation Kit
- Simulation by looping back the SERDES Tx/Rx lane internally on a test bench to verify the mode of operation

Figure 2 • **Hardware Implementation Block Diagram**



2.3.3 Description

2.3.3.1 Hardware Design

The hardware design for the JESD204B demo implementation includes the following:

- Data Generator
- JESD204BTx IP core
- JESD204BRx IP core
- Data Checker
- SERDESIF
- Control Logic
- MMUART for console communications
- Fabric Interface Controller

Figure 2 on page 8 shows the block diagram for the design implementation. Refer to the Block Descriptions for more information.

2.3.3.2 Block Descriptions

2.3.3.2.1 Data Generator

The data generator has a PRBS generator and waveform generator. The PRBS generator can generate PRBS9, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode is also implemented in the PRBS generator, which inserts an error in to the PRBS sequence for checking. The waveform generator generates sine wave, saw tooth wave, triangle wave, and square wave. The data generator feeds the 16-bit test pattern to CoreJESD204BTx core for transmitting data for SEREDESIF.

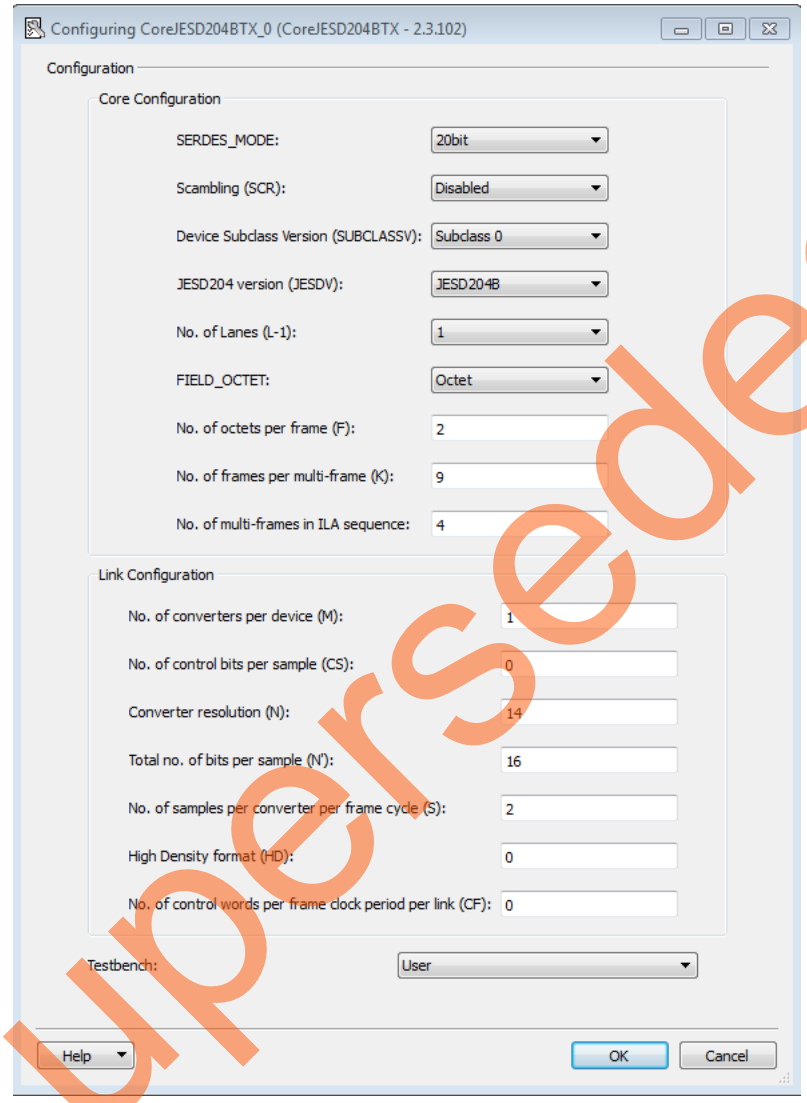
2.3.3.2.2 Data Checker

The data checker receives 16-bit data output from the CoreJESD204BRx IP core and checks for the correctness of the received data. It generates both an error count and status signal, which is sent to the GUI for status indication. It only checks the PRBS sequences of the data generator.

2.3.3.2.3 Core JESD204B Tx

The CoreJESD204BTx is compatible with the JEDEC JESD204B standard. For this demo design, the IP core is configured, as shown in Figure 3.

Figure 3 • **Core JESD204B Tx Configuration**

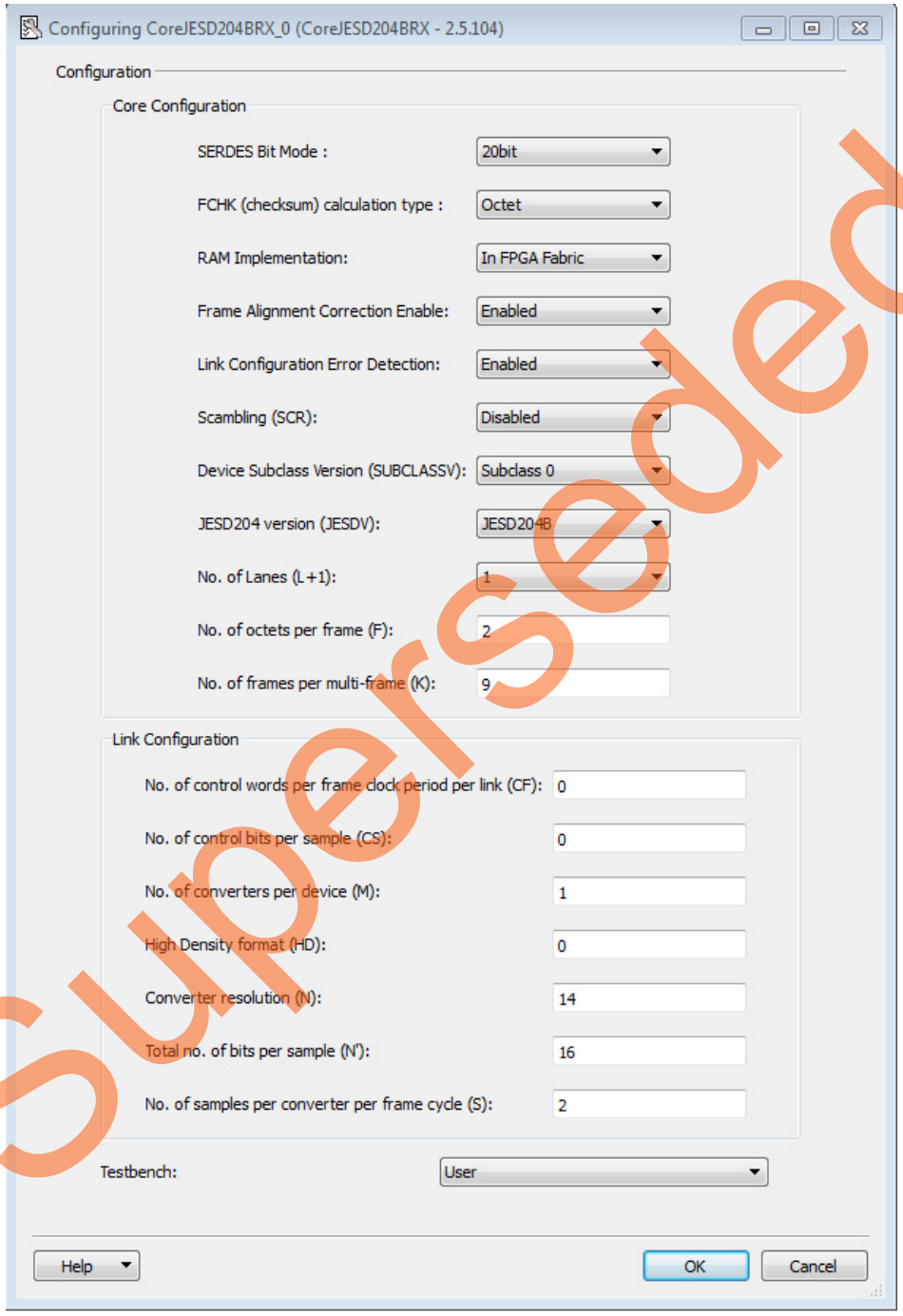


Refer to the *IP Core Configuration Guide* for more information on settings.

2.3.3.2.4 Core JESD204B Rx

The Core JESD204B Rx is compatible with the JEDEC JESD204B standard. The IP core is configured, as shown in Figure 4.

Figure 4 • **Core JESD204B Rx Configuration**



Refer to the *IP Core Configuration Guide* for more information on settings.

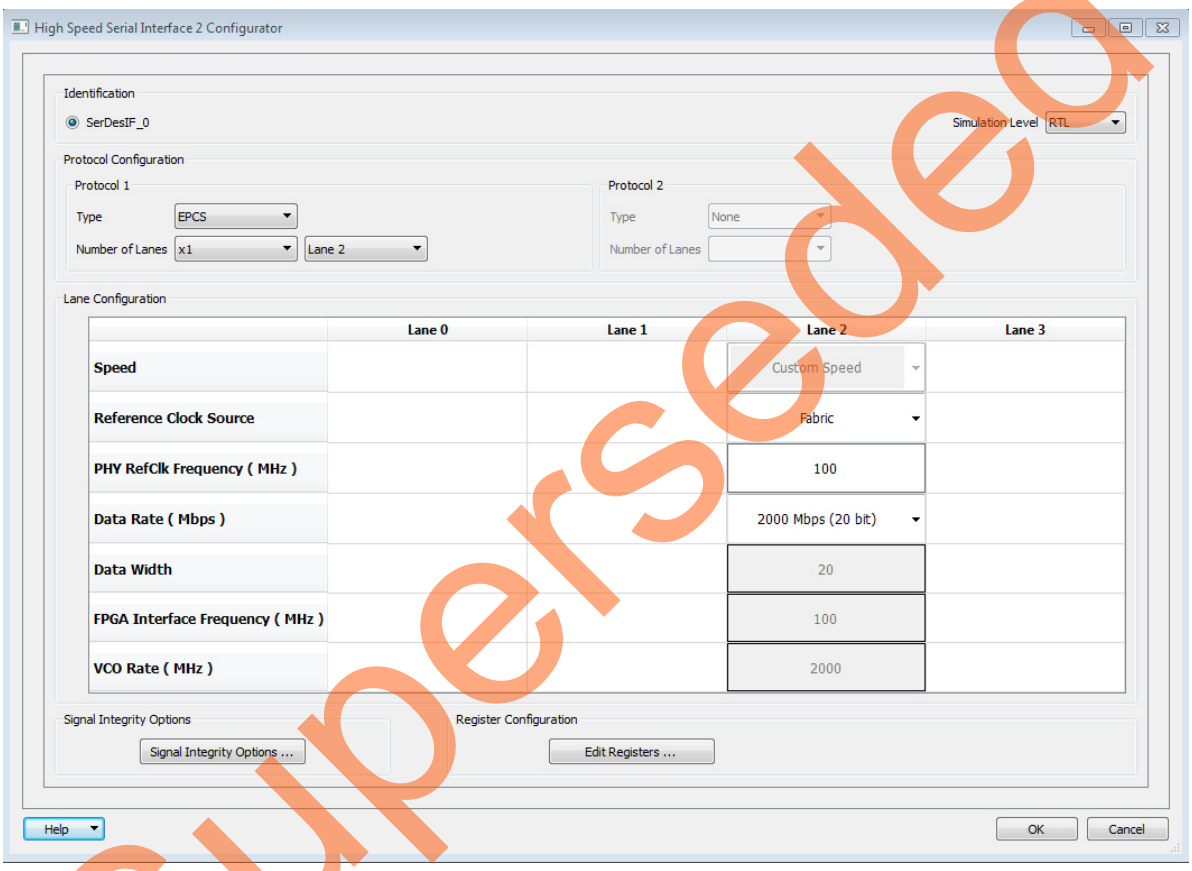
2.3.3.2.5 SERDESIF

The SmartFusion2 SoC FPGA high-speed SERDES is a hard IP block on chip that supports the high-speed data rates up to 5 Gbps. The SERDESIF EPCS mode is used for JESD204B providing a data path directly to the PMA.

Refer to *UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide* for more information on the SERDES block.

In this demo, the SERDESIF2 block is configured in EPCS mode on lane 2 to interface JESD204B IP cores, with reference clock 100 MHz from fabric to support 2 Gbps data rate. Figure 5 shows the SERDES block configuration details.

Figure 5 • **SERDESIF2 Configuration**



Note: The M2S090/M2GL090 and M2S060/M2GL060 devices use the SERDESIF2 module. All the other SmartFusion2 and IGLOO2 devices use the SERDESIF module.

2.3.3.2.6 MSS Block

The microcontroller subsystem (MSS) block sends and receives the data between host PC (GUI interface) and fabric logic. The MMUART interface is used to communicate with the host PC. The FIC_0 interface (APB master) is used to communicate with the fabric user logic.

2.3.3.2.7 TPSRAM IP

TPSRAM IP is an LSRAM module and is used for loading status and data signal, and is configured as follows:

- Status data Buffer (Depth: 1024, Width: 32)
- Output data Buffer (Depth: 1024, Width: 32)

2.3.3.2.8 Control Logic

The control logic implemented in the fabric consists a APB slave FSM to communicate with a MSS APB master, and also controls operations such as reading and writing status and output data buffers.

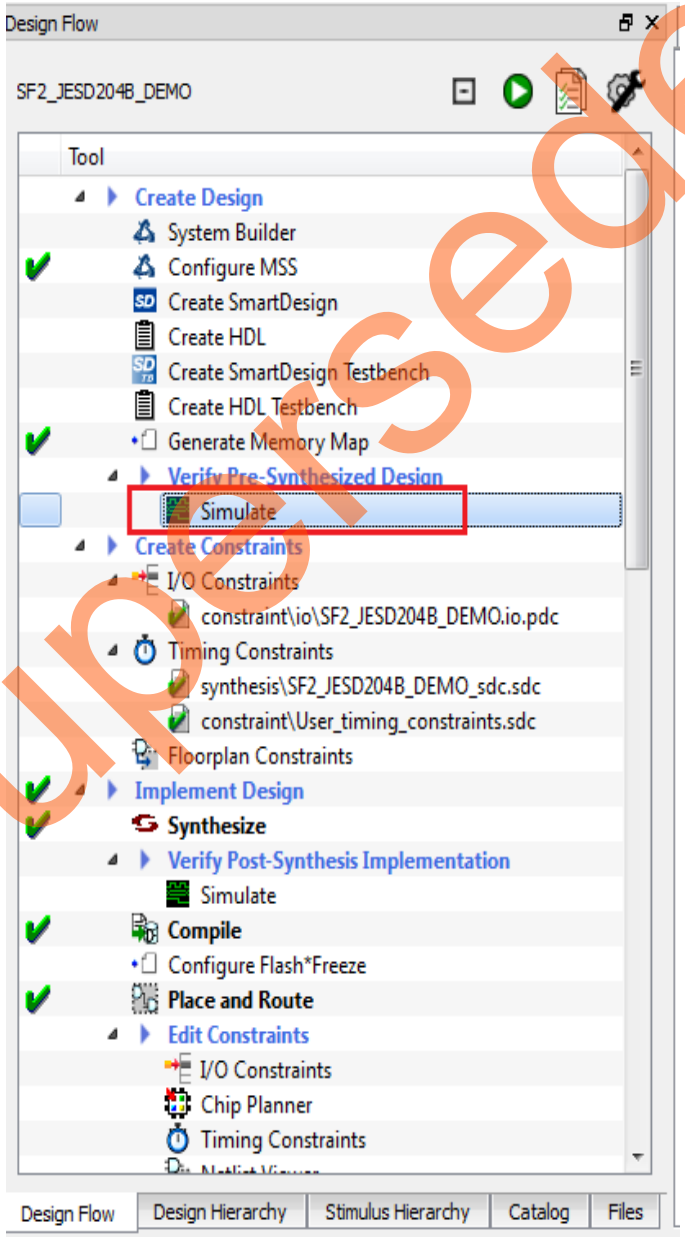
2.4 Simulating the Design

The design is simulated using the provided testbench. The testbench simulates the JESD204B demo design for PRBS pattern and waveform selection.

To run the simulation,

- Double-click **Simulate** under **Verify Pre-Synthesized Design** in the **Design Flow** tab of the Libero project, as shown in Figure 6.
- Or right-click and select **Simulate** to invoke the simulator.

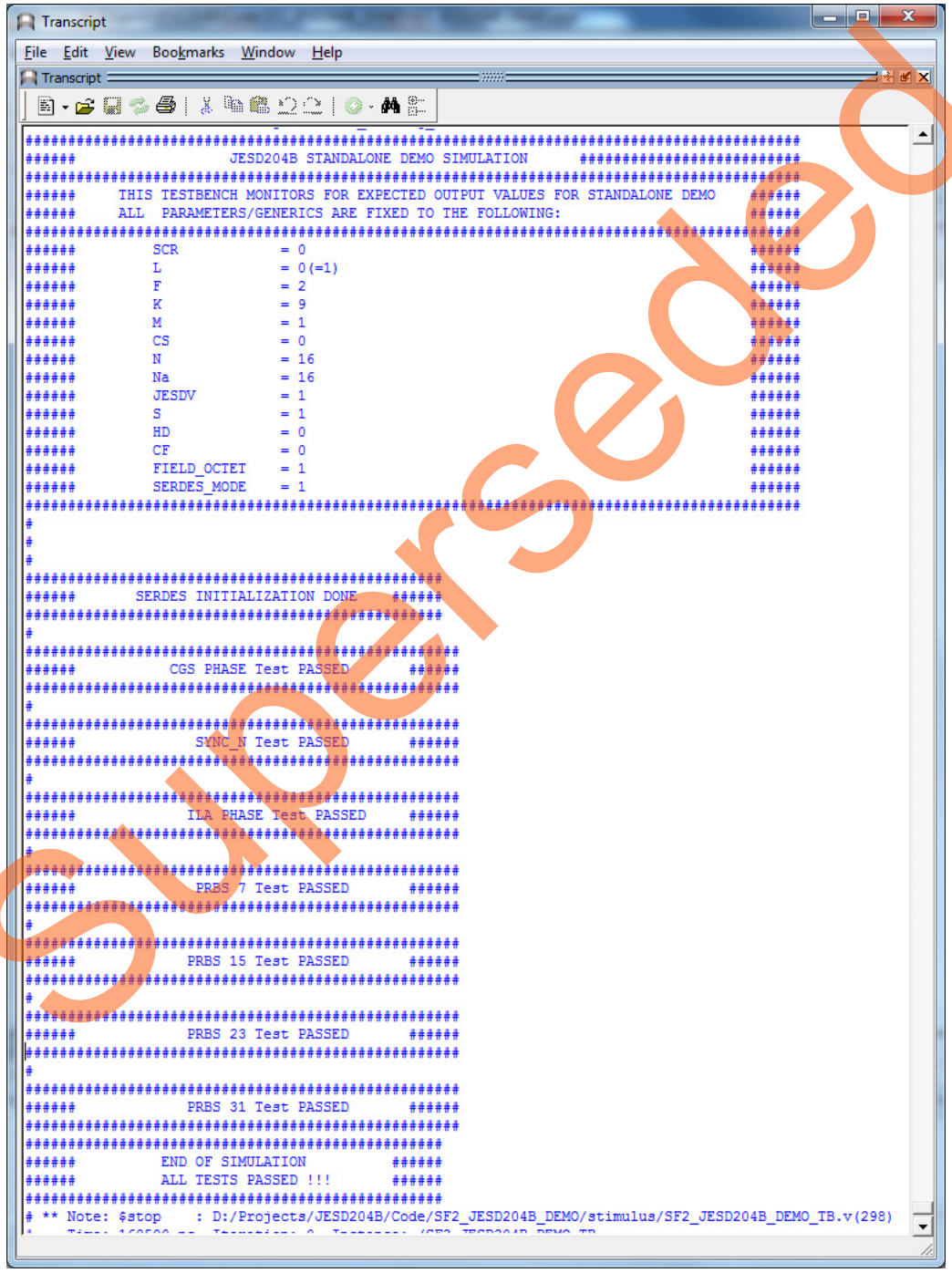
Figure 6 • **Simulating the Design**



The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and sine wave for waveform input. It also monitors the JESD204B output status signals (SYNC_N, ALIGNED, and CGS_ERR) for the verification of JESD204B phases, and PRBS checker output status signals for the correctness of the Input PRBS pattern (PRBS7, PRBS15, PRBS23, and PRB31).

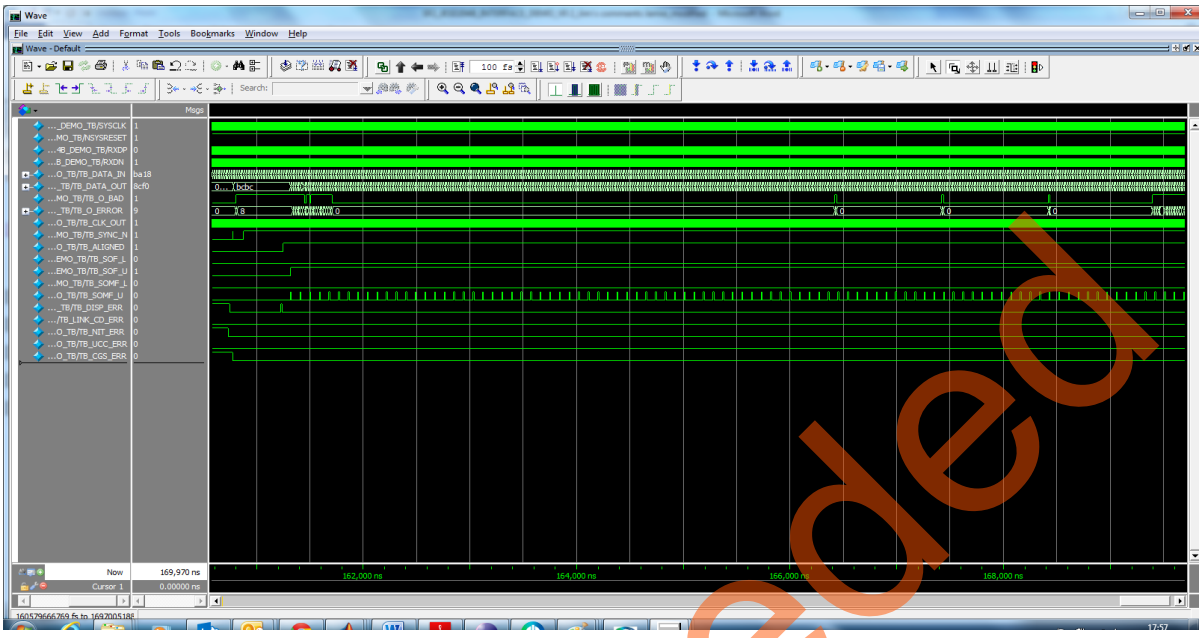
The simulation ends after executing all the test cases. The status of the test cases is shown in the **Modelsim Transcript** window, as shown in Figure 7.

Figure 7 • **Transcript Window**



After simulation, the **Simulation Waveform** window is displayed, as shown in Figure 8.

Figure 8 • **Simulation Waveform Window**



2.5 Setting Up the Demo Design

The following steps describe how to set up the demo design:

1. Connect the FlashPro4 programmer to the FlashPro header on the SmartFusion2 Security Evaluation Kit, as shown in Figure 9.
2. Connect the J18 connector and host PC using the mini-B cable.
3. Ensure that the USB to UART bridge drivers are automatically detected (can be verified in the Device Manager).
4. Loop-back the SERDES Lane 2 (TxD2P <-> RxD2P, TxD2N <-> RxD2N) using two SMA-SMA cables, as shown in Figure 9.
5. Connect the 12 V power adapter that shipped with the FPGA development board to the power jack J6, and switch on the power supply.

Figure 9 • **Hardware Setup**

Note: SERDES Lane 1 is looped back from transmit to receive data on the board. If the SMA cables are not available, the user can reconfigure the SERDESIF2 to Lane 1.

2.6 Programming the Device

The following steps describe how to program the device:

1. Download the design files from *http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_liberov11p7_df*
   The Programming file (STAPL/PDB) is located in the Programming_File folder.
2. Connect the **FlashPro4** programmer to the **SmartFusion2 Security Evaluation Kit**.
3. Connect the jumpers to the **SmartFusion2 Security Evaluation Kit** board as shown in Table 2.

Table 2 • **SmartFusion2 Security Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J3	1	2	Default
J8	1	2	Default

CAUTION: Ensure that the power supply switch SW7 is switched OFF while connecting the jumpers to the SmartFusion2 FPGA Security Evaluation Kit.

4. Program the SmartFusion2 device with the downloaded programming file as in step 1 using FlashPro v11.7.

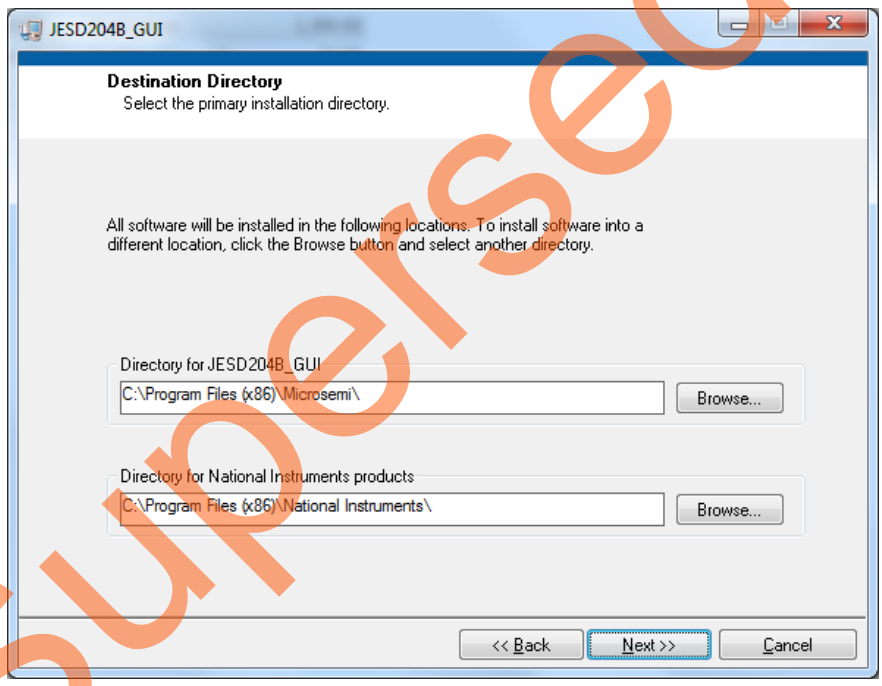
2.7 Installing the GUI

The JESD204B demo is provided with a user friendly GUI that runs on the host PC to communicate using an UART with the SmartFusion2 Security Evaluation Kit.

The following steps describe how to run the installer if the GUI is used for the first time:

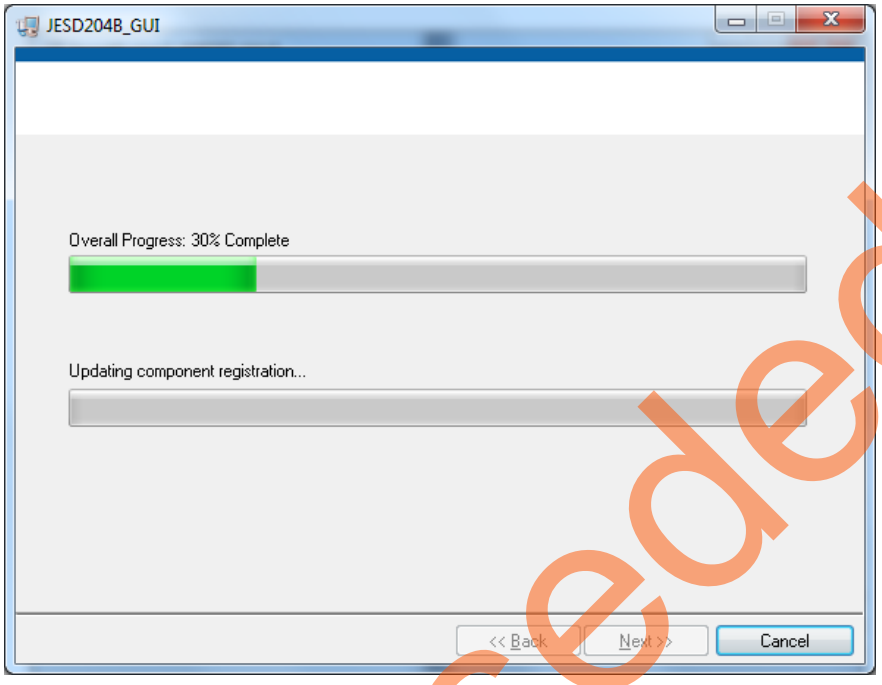
1. Download the design files from *http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_liberov11p7_df*
2. Open and run **Labview Runtime Installer** > **setup.exe** before installing JESD204B GUI. Restart host PC if necessary.
3. Open **GUI_Installer > Volume > setup.exe**.
4. Click **Yes** for any message from **User Account Control**. The Destination Directory window is displayed with the default locations, as shown in Figure 10.
5. Click **Next**.

Figure 10 • **GUI Set Up Window**



6. Follow the instructions in the GUI to start the installation.
   A progress bar appears, which shows the progress of installation as shown in Figure 11.

Figure 11 • **GUI Set Up Progress Bar**



7. Wait for the installation to complete. After successful installation, the Installation Complete message is displayed.
8. Click **Finish**.
9. Restart the host PC before using the installed GUI.

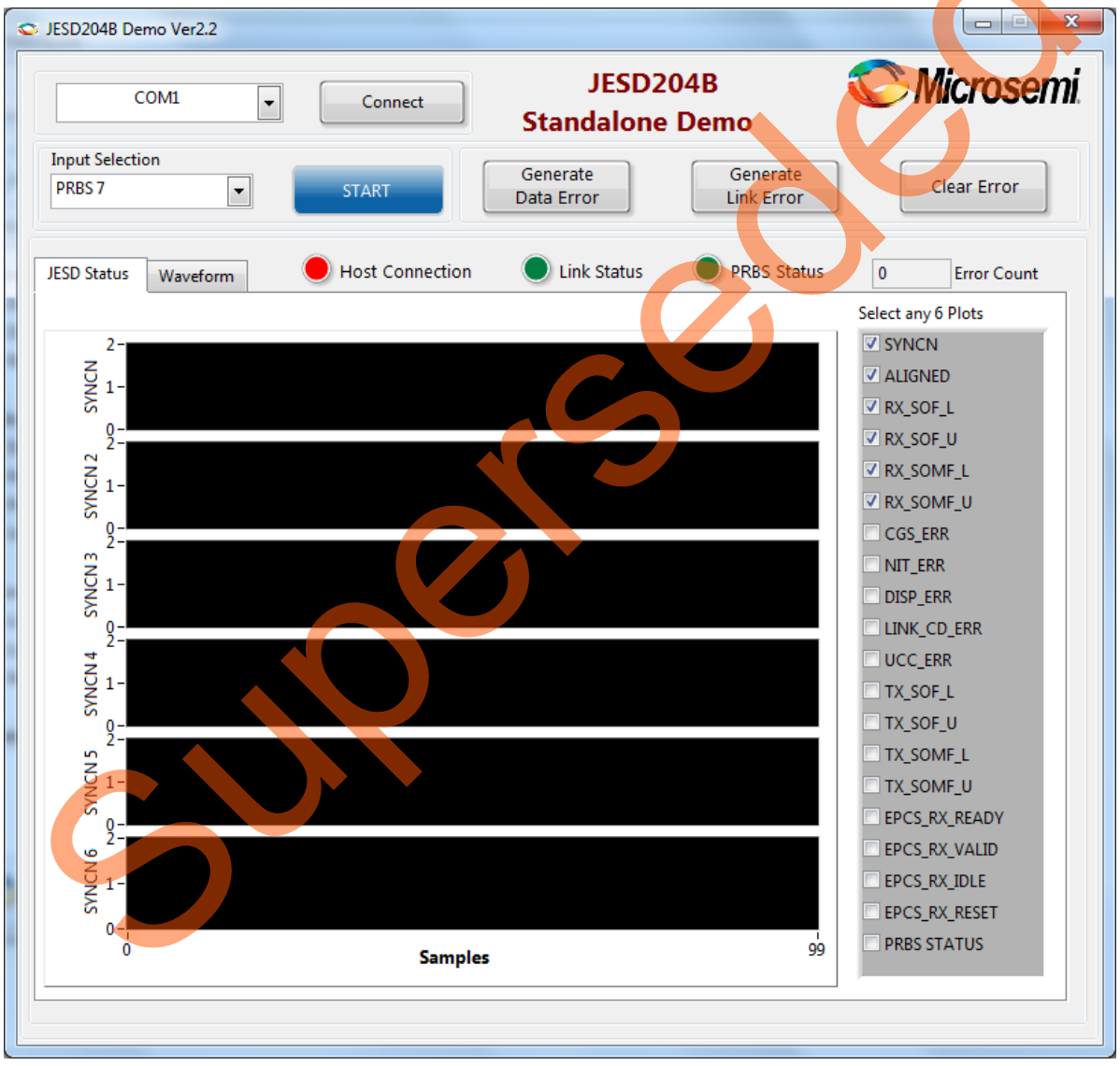
2.8 Running the Demo Design

This section describes how to use the GUI for selecting the test patterns and monitoring the loop-back data for the demo design. It provides an interactive GUI for selection of different PRBS test patterns as a demo input, and observes the JESD204B status signals and PRBS status collected from the board. It also shows the output waveform samples collected from the board during waveform selection on the waveform tab.

The following steps describe how to run the demo design:

1. Open **Programs > SF2_JESD204B Demo**.
   Figure 12 shows the GUI window.

Figure 12 • **SmartFusion2 JESD204B Demo GUI Window**



The drop-down list for ports has the list of serial ports available on the host PC. The working ports are enabled and the unavailable ports are grayed out.

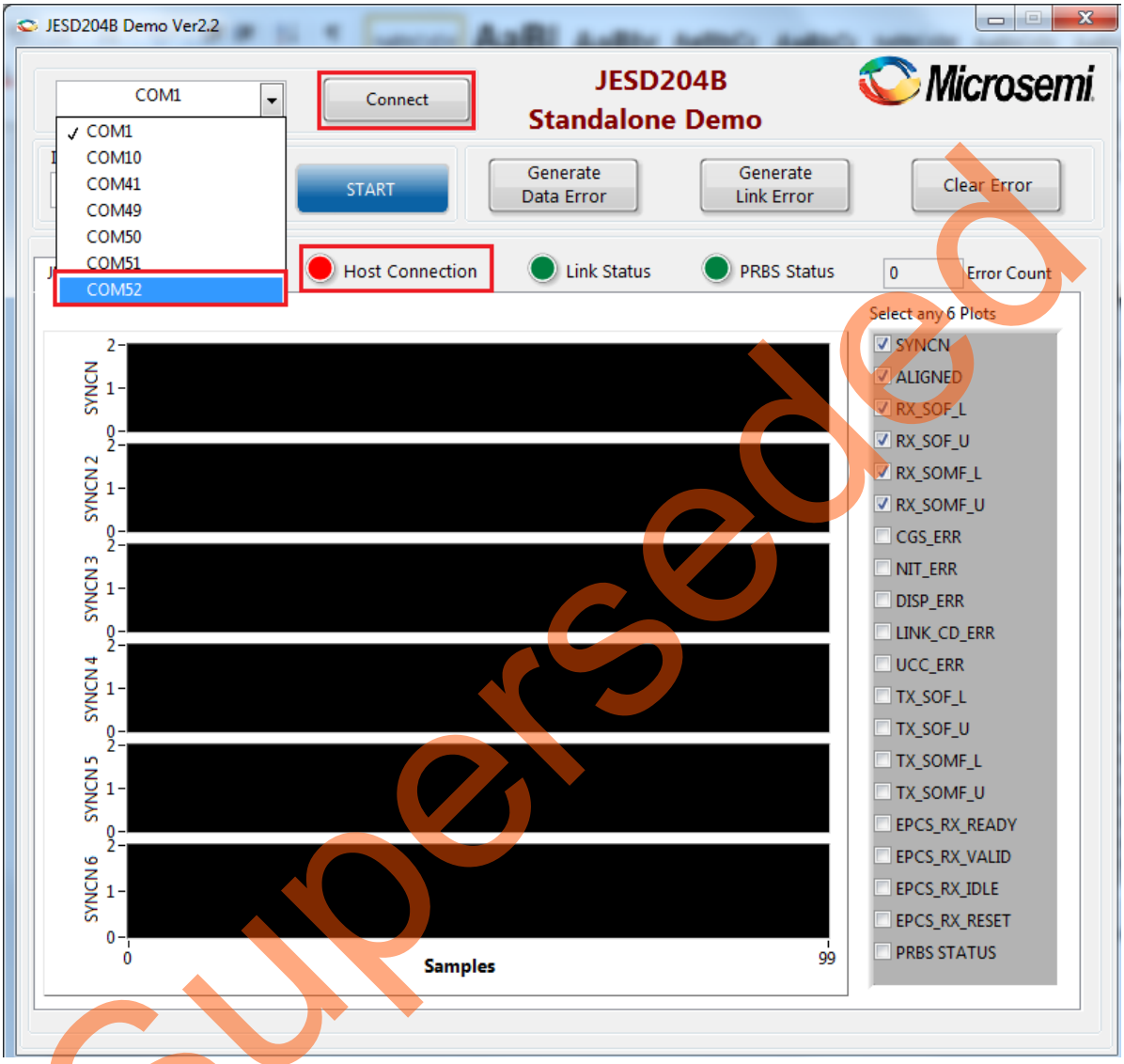
Note: The default settings for the design are 115200 baud, no flow control, one stop, and no parity.

2. Select the COM port number that is detected to configure the serial port.

3. Click **Connect** to connect the host PC to the hardware through the selected port, as shown in Figure 13.

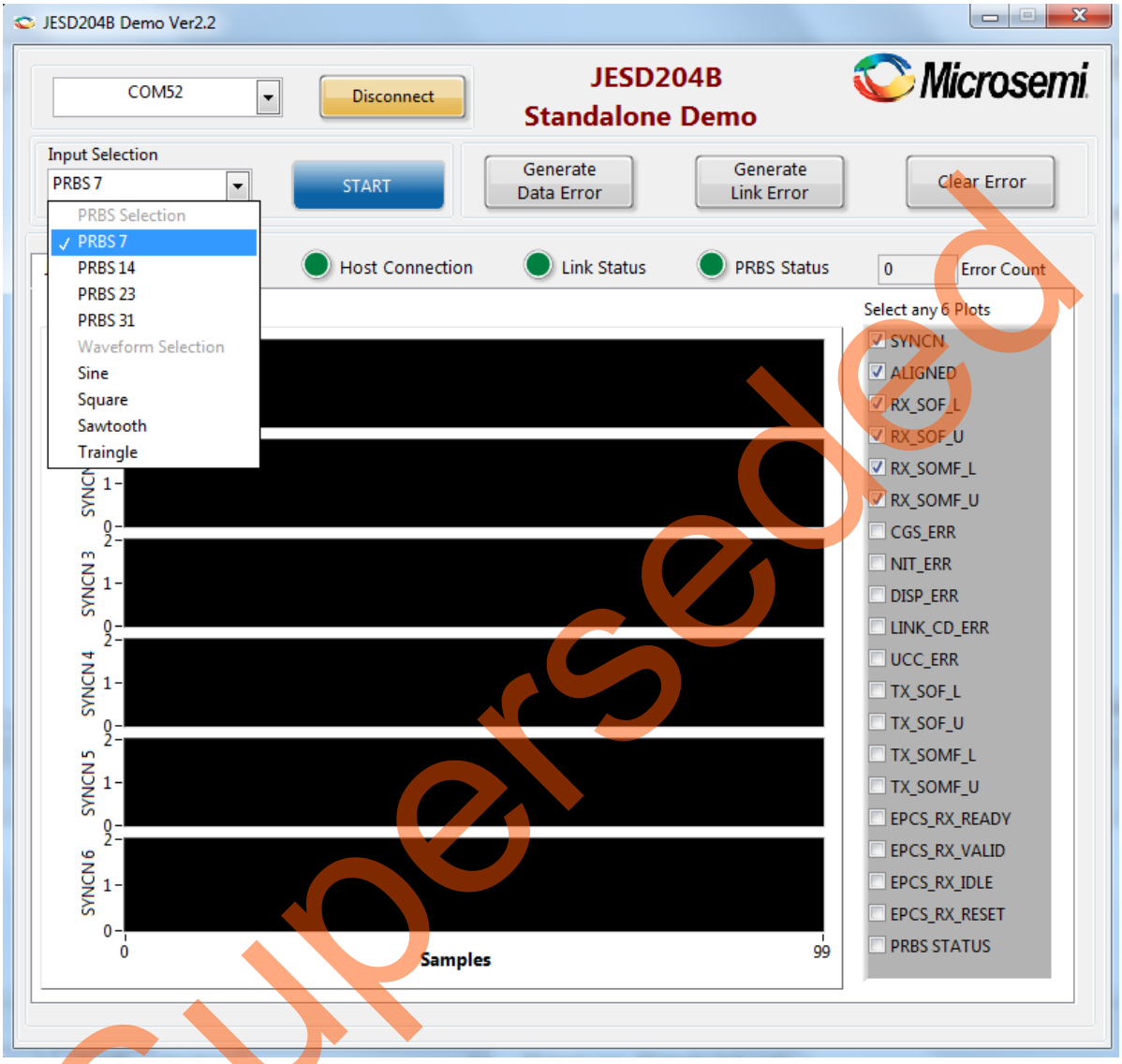
Note: Port numbers may vary. Select the correct port number from the list.

Figure 13 • **Serial Port Configuration**



4. Select the pattern to be transmitted using the **Input selection**. Select one of the patterns in PRBS selection, Select **PRBS 7** as shown in Figure 14.

Figure 14 • **PRBS Pattern Selection**

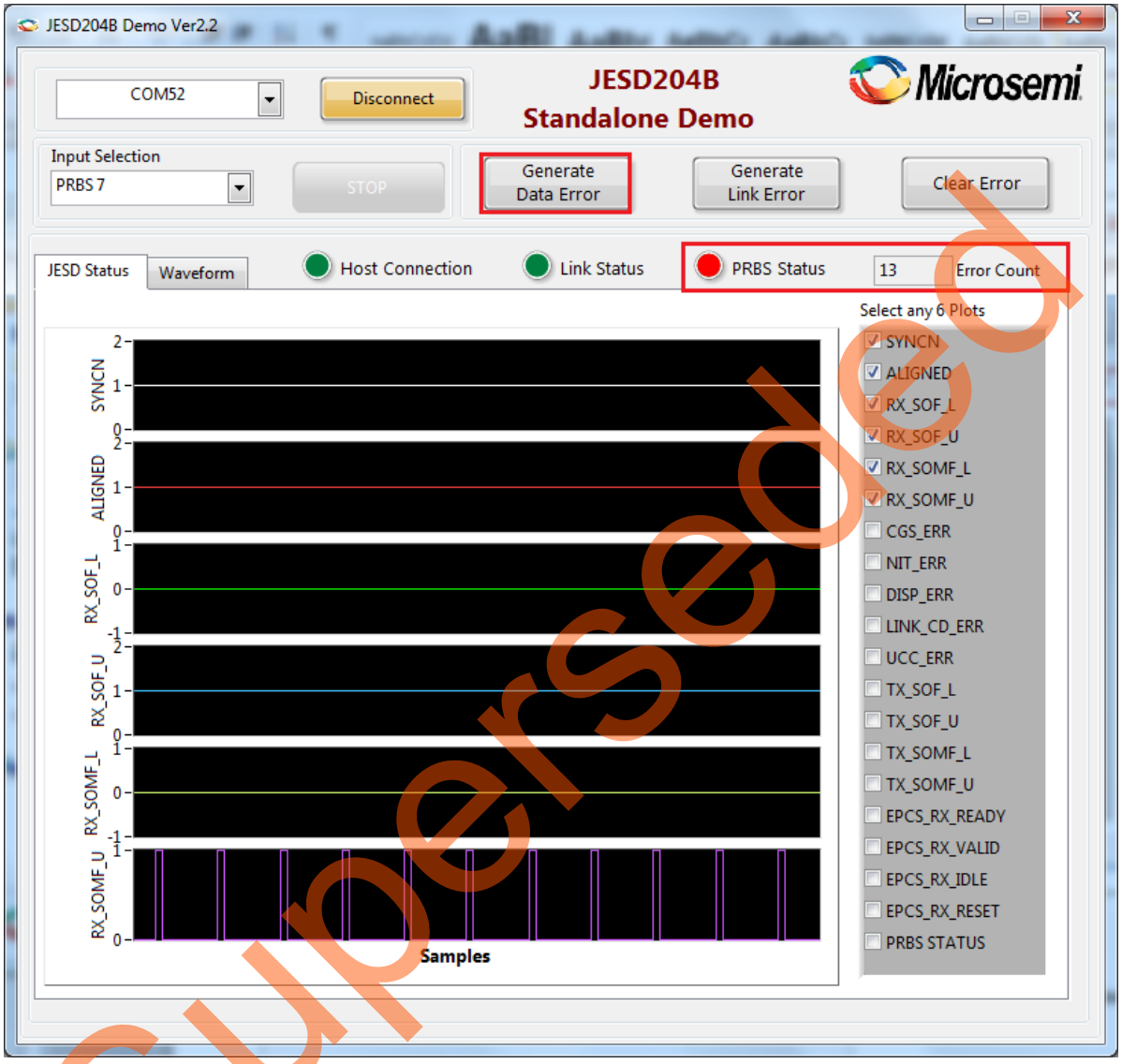


5. Click **START** to start the JESD204B demo. The selected pattern is sent over serial transmit link. The looped back data is received by the receiver and checked for any errors. The status can be monitored using the status signals in the GUI at any time.

Note: Select any six signal check boxes on the right side panel to view the status of the signals. If the count is more than six, de-select the selected signals before selecting any new signals.

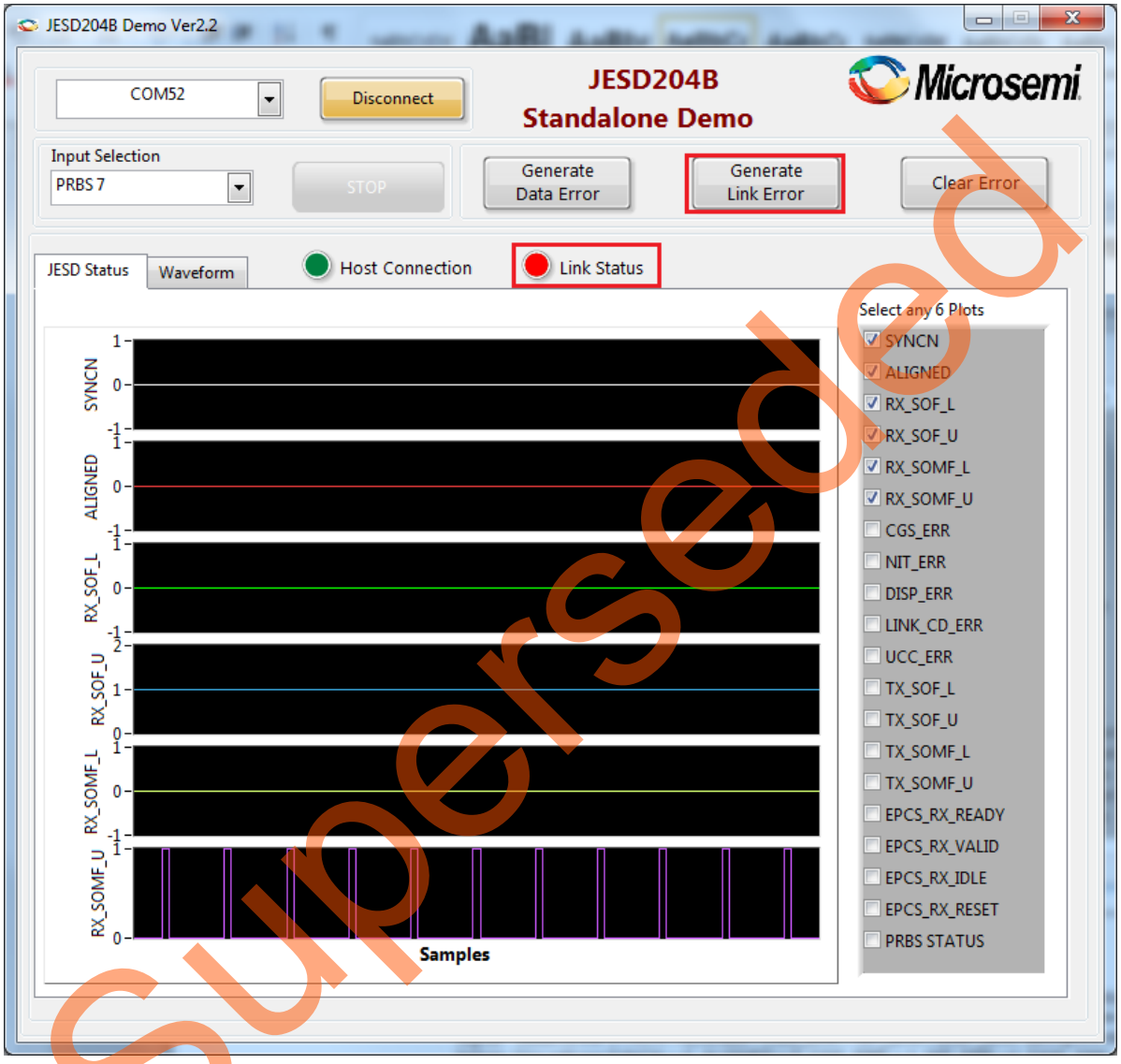
6. Click **Generate Data Error** and observe error status using GUI. Figure 15 shows the Host Connection, Link Status, PRBS Status, and Error Count.

Figure 15 • **Data Error Generation**



7. Click **Clear Error** to stop generating the error data **PRBS Status** turns green, and **Error Count** is displayed as 0.
8. Click **Generate Link Error** to generate error in 20 bits SERDES lane. Figure 16 shows the **Link Status** changed to RED on link error.

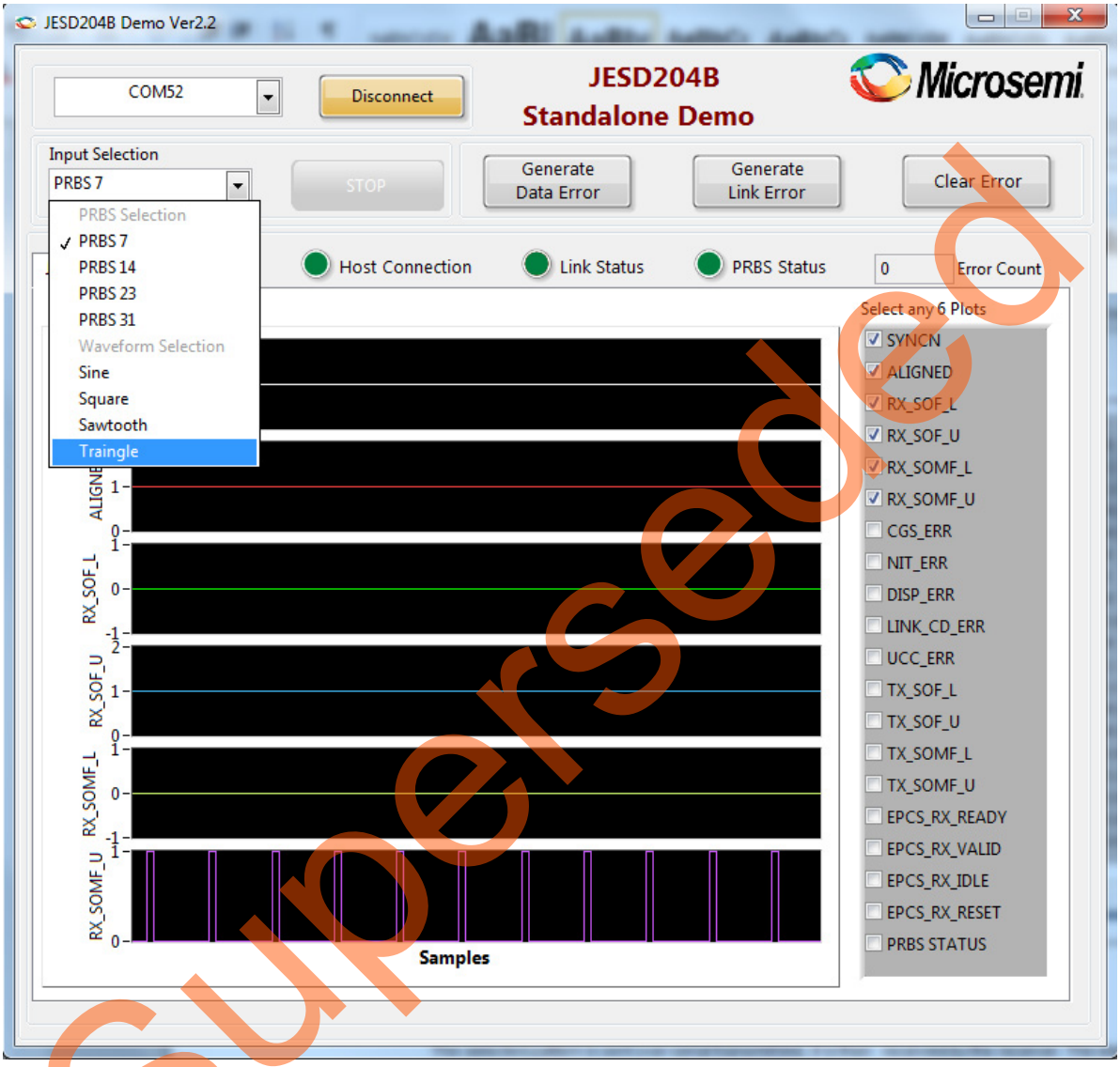
Figure 16 • **Data Error Generation**



Note: Select any six signal check boxes on the right side panel to view the status of the signals. De-select the selected signals before selecting any new signals if the count is more than six. The SYNCN, ALIGNED, CGS_ERR, NIT_ERR, DISP_ERR, and EPCS_RX_VALID signals are enabled during Link Status failure.

9. Click **Clear Error** to stop generating the error data and observe the **Link Status** turn to green.
10. Select **Triangle** as Input selection to change the pattern and view the status link, as shown in Figure 17.

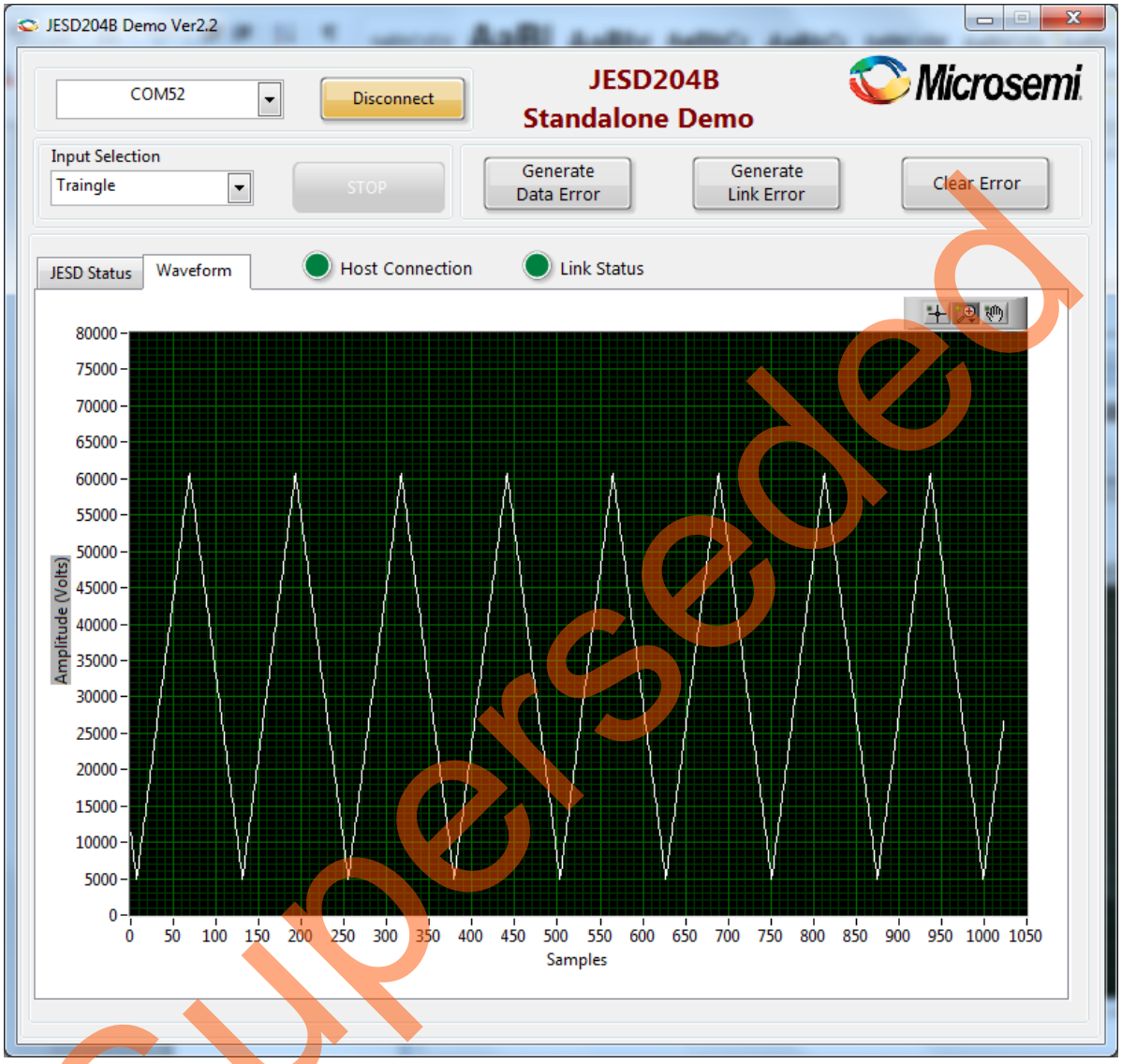
Figure 17 • **Waveform Pattern Selection**



The selected pattern is sent over the serial transmit link. It is then received by the receiver. The status can be monitored using **Status Signals** in the GUI.

11. Click the **Waveform** tab to view the **Triangle** waveform received from the JESD204BRx IP core, as shown in Figure 18.

Figure 18 • **Waveform Tab**



12. Click **Stop**.

3 Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 3 (May 2016)	Updated the demo guide for Libero v11.7 software release changes (SAR 78042).
Revision 2 (September 2015)	Updated the demo guide for Libero v11.6 software release changes (SAR 71756).
	Updated the labview runtime installer instruction in the "Installing the GUI" section on page 17 (SAR 68588).
Revision 1 (May 2015)	Initial release

4 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

4.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

4.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

4.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

4.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

4.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

4.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

4.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

4.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

4.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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