Libero SoC PolarFire v1.1

Release Notes

4/2017

Microsemi
Power Matters.™

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About Microsemi
Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at **www.microsemi.com**.

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1 Revision History

1.1 Revision 1.0

This is the initial release of these Release Notes.

1.2 Revision 2.0

Updated Paragraph 3.3 CCC Known Issues/Limitations

Updated Paragraph 3.7 Transceiver Known Issues

Reference Documents

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide (Updated 02/2017)

PO0137: PolarFire FPGA Product Overview (02/2017)

DS0141: PolarFire FPGA Datasheet (02/2017)

UG0680: PolarFire FPGA Fabric User Guide (02/2017)

UG0684: PolarFire FPGA Clocking Resources User Guide (02/2017)

UG0686: PolarFire FPGA User I/O User Guide (02/2017)

UG0677: PolarFire FPGA Transceiver User Guide (02/2017)

UG0685: PolarFire FPGA PCI Express User Guide (02/2017)

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide (02/2017)

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide (Updated 02/2017)

UG0676: PolarFire FPGA DDR Memory Controller User Guide (02/2017)

UG0748: PolarFire FPGA Low Power User Guide (02/2017)

UG0743: PolarFire FPGA Debugging User Guide (02/2017)

UG0714: PolarFire FPGA Programming User Guide (02/2017)

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide (02/2017)

UG0726: PolarFire FPGA Board Design User Guide (02/2017)

UG0752: PolarFire FPGA Power Estimator User Guide (02/2017)

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide (02/2017)

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide (02/2017)

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide (02/2017)

DG0755: PolarFire FPGA JESD204B Interface Demo Guide (02/2017)

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2 Libero SoC PolarFire™ v1.1 Software Release Notes

The Libero® system on chip (SoC) PolarFire™ v1.1 release is a production release of the Libero SoC software for designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about the Libero SoC PolarFire devices, see the Microsemi website.

2.1 What's New in this Release

This release includes the following new features and enhancements:

- Timing data update to be consistent with ES devices which yield improved Fmax.
- Design and Memory Initialization Tool in Design Flow
    - Initialization of PCIe/Transceiver blocks and fabric RAMs at power up
    - uPROM content update
    - sNVM content update
    - SPI flash content definition for IAP and auto-update programming use models
- JTAG Programming Flow support

2.2 Limitations of this Release

This release has the following limitations:

- Post-synthesis and post-layout simulations are not supported.
- IBIS generation is not supported.
- Design Block Flow (bottom-up design reuse methodology) is not supported.
- Transceiver initialization support is limited. Contact Microsemi Technical Support for assistance with bringing up transceiver solutions with ES devices.
- Identify is not supported.

2.3 System Requirements

- Windows 7 OS or Windows 8.1 OS
- RHEL 5 and RHEL 6, CentOS 5 and CentOS 6
- 64-bit OS
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC on Red Hat Enterprise Linux OS are available on the Libero SoC Documents Web page.

2.4 Timing and Power Data

The Timing and Power reports use data based on “Advance” Data. Max Delay Slacks and Clock Frequencies reported in the Timing Reports may be pessimistic and slower than the actual timing performance of the PolarFire device.

2.5 Device Support

Table 1 Libero SoC PolarFire Device Support

Device	Package	Speed Grade	Core Voltage	Required License
MPF200TS_ES	Fully bonded package	-1	1.0 /1.05V	Eval/Gold/Platinum
MPF300T_ES	FCG1152E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG484E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG784E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484E	-1, STD	1.0/1.05V	Eval/Platinum
MPF300TS_ES	FCG1152E	STD	1.0 /1.05V	Eval/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCG484E	STD	1.0 /1.05V	Eval/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum

See the Licensing Web page for details.

2.6 Design Migration

Place and Route will be invalidated for designs created with earlier releases.

- If the design has not changed, run incremental Layout (**Design Flow Window> Place and Route > Configure Options > Incremental Layout**) and continue with the design process.

Design containing CCCs will be invalidated.

- You must upgrade the CCC core to the current version (1.1.104) available in the IP Catalog.
- See CCC Known Issues/Limitations for details.

Microsemi recommends that you upgrade to the latest core version available in the IP Catalog for the following cores:

- DDR3, DDR4, PCI Express and Transceiver Interface.

3 Known Issues and Limitations

3.1 RAM Initialization

- RAM initialization at Power Up is only supported for the PolarFire Dual-Port Large SRAM, Two-Port Large SRAM and Micro SRAM cores.
- RAM initialization at Power Up is not supported for the PolarFire SRAM (AHBLite) core.
- RAM initialization at Power Up is not supported for RAMs inferred during Synthesis.
- The RAM initialization tool does not support the import of a memory file with a space in the file path.

3.2 Design Initialization

In the 'Design and Memory Initialization' tool, the second stage start address must be aligned to a 256 word boundary if the memory type is uPROM. The software does not check this rule.

3.3 CCC Known Issues/Limitations

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.
- In the PLL configurator, output clock frequencies should always be in descending order with the highest clock frequency assigned to the first enabled output clock to obtain an optimal solution.
- In DLL Phase Generation Mode, the secondary output clocks are not getting the correct phase in simulations.

3.4 DDR3/4 Known Issues/Limitations

Known issues/limitations described in the Libero SoC PolarFire Software Release Notes also apply to this release.

3.5 IOD CDR and IOD Generic Known Issues and Limitations

Known issues/limitations described in the Libero SoC PolarFire Software Release Notes also apply to this release.

3.6 PCIe Known Issues:

The AXI interface minimum clock frequency is 125 MHz. If operating at a frequency lower than 125 MHz is required, use the CoreAXI4Interconnect to interface between the PCIe core and the AXI subsystem connected to that core.

Additionally, Libero SoC PolarFire Release Notes also apply to this release.

3.7 Transceiver Known Issues

In 8b10b mode the RX_SLIP port is enabled by default. This port should not be used in the 8b10b mode. The user should tie this port low in their design. It will be removed in a future release

Additionally, Libero SoC PolarFire Release Notes also apply to this release.

In the latest version of the PF_XCVR transceiver core, the LANE#_ARST_N [1:0] port was removed as it is only a factory test signal and not a user signal.

3.8 I/O and I/O Bank Known Issues

See the Libero SoC PolarFire Release Notes.

3.9 Placement DRC Rules

See the Libero SoC PolarFire Release Notes.

3.10 Miscellaneous Known Issues

All known issues in the Libero SoC PolarFire Release Notes apply to this release, unless otherwise stated.

4 Download Libero SoC PolarFire v1.1 Software

The following are available for download:

Libero SoC PolarFire v1.1 for Linux or Windows: Download here

Note: Installation requires administrative privileges.