

Application Note
Design Recommendations for SiC MOSFETs

Released



Contents

1	Revision History	1
1.1	Revision 1.0	1
2	Designing with SiC MOSFETs	2
2.1	Device Model	2
2.2	SPICE Model	3
2.3	Threshold Voltage and Source Inductance	3
2.4	Miller Effect and Gate Drive Impedance	6
2.5	Positive Gate Drive	7
2.6	Characteristics of the Body Diode	8
2.7	RDS(on) vs. Temperature	13
2.8	Gate Drive	15
2.9	DC Bus Items	15
2.10	References	16

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in February 2017. It was the first publication of this document.

2 Designing with SiC MOSFETs

This application note provides recommendations for designing with SiC MOSFETs. It highlights the characteristics of SiC MOSFETs that differ from previous technologies and the resulting design recommendations. It assumes that the designer is familiar with power switching terminology and techniques.

SiC MOSFETs are coming into prominence in select power switching applications above ½ kV, especially in those that benefit from the high-speed capability of SiC MOSFETs. This application note focuses on optimization for speed to minimize switching losses and to get the full benefit of the devices.

There are many similarities between SiC MOSFETs and Si MOSFETs: they are both enhancement mode devices with body diodes; they are much faster than IGBTs; the $R_{DS(on)}$ of a SiC MOSFET increases with temperature like with a Si MOSFET (although not by as much); and the switching speed of both is governed mostly by the speed at which the gate charge is removed or added, with a speed limit set by the output capacitance and the ability of the devices to source high currents.

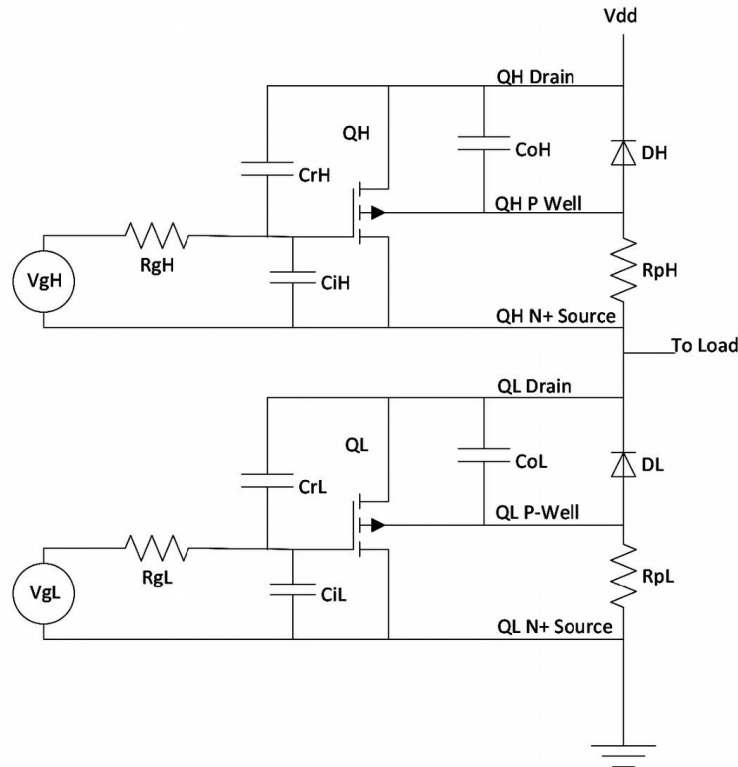
Some important differences include the following:

- SiC MOSFETs have a lower $R_{DS(on)}$ than Si MOSFETs. They are normally driven at a higher gate voltage, typically –5 V to 20 V, to enhance $R_{DS(on)}$ and switching speed.
- The body diode of a SiC MOSFET has a high voltage drop (about 4 V), but a low minority carrier lifetime. They have a significantly faster recovery and a lower recovery charge than that of Si MOSFETs.
- The output switching current (di/dt) is significantly higher with SiC MOSFETs than with Si MOSFETs. This affects DC bus ringing, EMI, and output stage losses.
- The slew rate at the output of a SiC half bridge can be much higher than with Si half bridge. SiC power stages can switch at a dV/dt of 30 kV/ μ s to 50 kV/ μ s. This should be considered in the design of gate-drive signal isolation, gate-power isolation, and EMI mitigation.
- There is no need to limit the output slew rate with Microsemi SiC MOSFETs. They are not susceptible to conduction in the parasitic NPN.
- By design, Microsemi SiC MOSFETs have excellent unclamped inductive switching (UIS) capability.

This application note will cover these in detail while concentrating on half-bridge power stages. Half-bridge configurations are commonly used and tend to stress the devices more than most other configurations. Simulated sample designs are used to demonstrate the design concepts.

2.1 Device Model

Throughout this document, references will be made to the following illustration, which shows two MOSFETs in a half bridge. It shows the internal parasitic devices of the MOSFETs. The FET body diode is represented by DL and DH through the P-wells RpL and RpH respectively. The nonlinear reverse transfer capacitance is represented by CrL and CrH. The nonlinear output capacitance is represented by CoL and CoH.

Figure 1 • Detailed Half Bridge

The parasitic NPN is not shown. The parasitic NPN is associated with the slew rate limit of the device. The slew rate limit is of no concern due to the SiC's wide bandgap and the structure of Microsemi SiC MOSFETs.

2.2 SPICE Model

Microsemi is releasing Berkeley SPICE models for all SiC MOSFET devices. These are high-accuracy models representing typical performance. Temperature dependence is well represented in these models, which are in subcircuit form and should be compatible with all variations of SPICE. In addition, symbol files are available for LTspice IV.

SiC MOSFETs have a very high transconductance and are capable of switching at a high dI_{DS}/dt . For this reason, it is beneficial to be able to accurately simulate device behavior to predict system performance.

Throughout this application note, simulation is used in order to illustrate various concepts.

2.3 Threshold Voltage and Source Inductance

One of the challenges faced by the designers of SiC MOSFETs was the control of the gate threshold voltage. Early SiC MOSFETs exhibited problems with threshold stability. There was a problem with threshold shift due to soaking at a bias condition. Continuous operation with a negative gate bias at an elevated temperature resulted in a negative threshold shift; similarly soaking with a positive gate bias resulted in a positive shift. There also was a dependence upon the switching current history. Both of these problems have since been resolved. This was never a problem with Microsemi devices but this question should be addressed when considering other vendors.

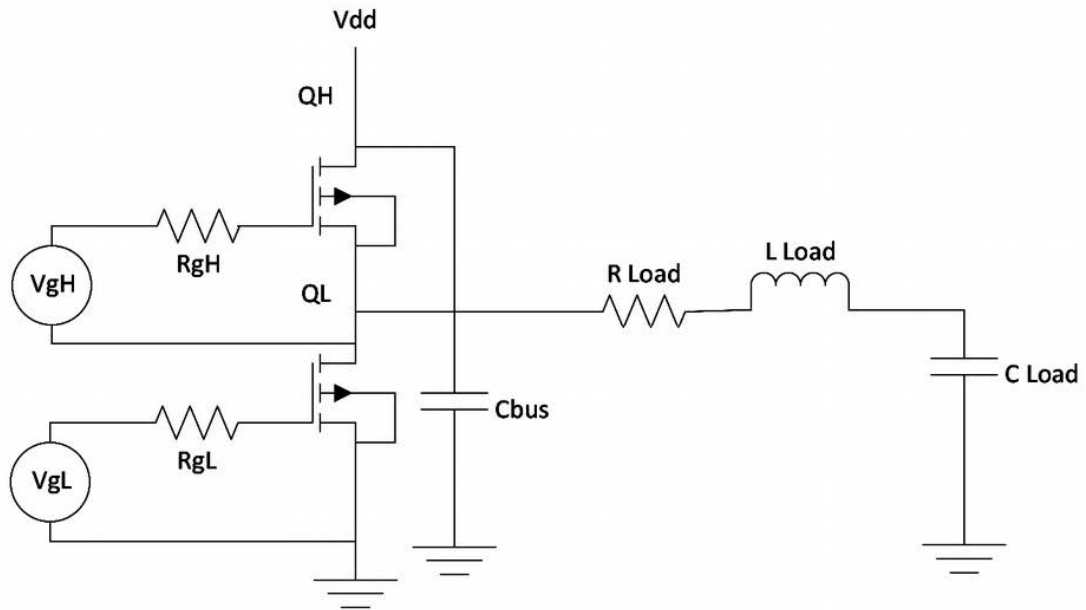
Microsemi SiC MOSFETs have a minimum threshold voltage of 1.7 V at 25 °C. The typical temperature coefficient of the threshold voltage is $-6 \text{ mV}/^\circ\text{C}$. Operation at an elevated junction temperature of 175 °C results in a threshold shift to roughly $1.7 \text{ V} - (175-25) * 6 \text{ mV} = 0.8 \text{ V}$. This threshold voltage is by design as a compromise between noise immunity and $R_{DS(on)}$. The temperature dependence is nonlinear, so the specified threshold is typically closer to 1 V at 175 °C.

It is highly recommended to use a negative gate drive with SiC MOSFETs in switching applications. The threshold voltage is designed above zero to keep a device OFF when there is no active switching. With slower devices, such as silicon MOSFETs and IGBTs, a negative gate drive is commonly used in power applications. There are two reasons for this:

- Gate Drive Impedance—The gate driver's function is to turn the MOSFET on and off (usually quickly) in order to reduce losses. To avoid cross conduction losses due to the Miller effect or due to slow switching with some loads, it is important for the driver to assert the off state with a lower impedance than the on-state drive on the opposing transistor. The negative gate drive margin plays an important part in reducing these losses. This is covered in more depth in the following section.
- Source Inductance—This is the inductance shared by the gate driver current loop and the output current loop. The negative gate drive voltage margin combined with the source lead inductance have a direct effect on the switching speed of the output under load. This is due to the source degeneration effect of the source inductance (the source lead inductance couples the output switching current back to the gate drive, slowing the gate drive).

Consider the circuit below but add an inductor to the source of QL. When the gate of QL is driven negative, the drain current of QL is reduced. Inductance in the source results in the source going below ground. This reduces the effective drive to the gate of QL, reducing the speed of the switching event.

Figure 2 • Half Bridge with Load



As an example, the APT40SM120B (TO-247) package has an internal source inductance of approximately 0.5 nH. Adding 1 cm of source wire will add about 5 nH to the three leads. Consider switching under the following conditions:

$$F_{sw} = 100 \text{ kHz}, T = 25 \text{ }^\circ\text{C}$$

$$R_{G(on)} = 5 \text{ } \Omega, R_{G(off)} = 1.7 \text{ } \Omega$$

$$\text{DC bus inductance} = 50 \text{ nH}$$

$$V_{G(on)} = 20 \text{ V}, V_{G(off)} = -5 \text{ V}$$

The following table has the losses calculated in QL using SPICE and the Microsemi device model. Microsemi SPICE models reference the lead-to-body interface; they do not include wire inductance external to the package. In most cases, the circuit lead inductance will dominate due to the need to offset the package from the PCB in order to allow for alignment to a heat sink.

Table 1 • Sample Half Bridge Losses in QL

QL Loss	Additional $L_{G(nH)}$ and $L_{S(nH)}$	Loss (W)	TO247 Mounting
1 mH inductive load	0	2.01	Flush
	5	1.98	1 cm off of a PCB
No load	0	12.02	Flush
	5	11.67	1 cm off of a PCB
20 A resistive load	0	18.58	Flush
	5	19.72	1 cm off of a PCB
40 A resistive load	0	69.09	Flush
	5	76.06	1 cm off of a PCB

The second line in the previous table shows the losses with no load on the bridge. This introduces a switching loss, best represented by the following: power supply energy → output capacitance energy → heat. The first two results show how a light inductive load results in very low power loss in the transistors. There is essentially no conduction loss, and the inductor exchanges energy with the transistor capacitance resulting in no switching loss.

The next two set shows the loss with resistive loads. Notice that the loss becomes sensitive to the source inductance. Most of the loss is from conduction, but a portion of the loss is caused by slow switching due to the source inductance.

Microsemi offers SiC MOSFETs in the SOT-227 package for higher performance applications. This offers two significant benefits:

- A SOT-227 provides internal electrical isolation. The thermal resistance is quite a bit lower than can be obtained with a TO-247 when considering an isolated heat sink. The TO-247 is best with a nonisolated (electrically hot) heat sink.
- A SOT-227 has a source inductance of approximately 0.6 nH, but there is no additional inductance wire inductance when wired to a PCB.

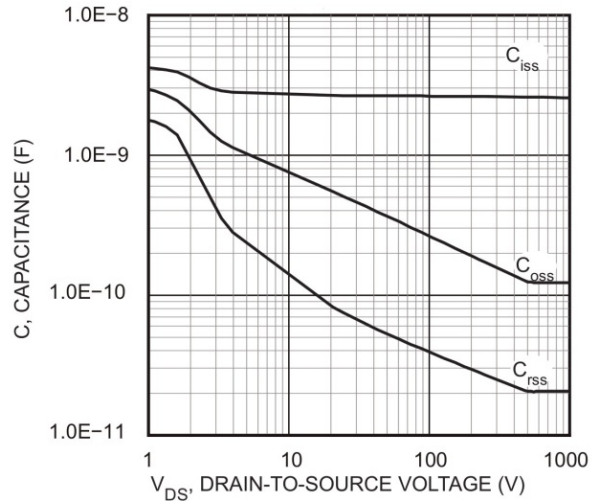
Operation above the specified DC limit is allowed in pulsed operation. As an example, the 40 A rating of the APT40SM120 device is a thermal rating, not a limit imposed by the device alone. A TO-247 package directly coupled to an electrically hot heat sink should be considered in the highest power applications.

The exception to the requirement for negative gate drive may be flyback supplies. SiC MOSFETs have an advantage over Si MOSFETs in some high-voltage flyback applications without a negative gate drive. The switching loss induced by Miller capacitance and the resulting channel conductance can be reduced by limiting the drain slew rate. A designer should evaluate the design at high temperatures with low-threshold devices to verify the suitability of a SiC MOSFET in the application.

2.4 Miller Effect and Gate Drive Impedance

In a switching application, it helps to understand the effect of nonlinearities of the Miller effect to fully understand the requirements of a gate driver. Figure 3 shows the capacitance curves for an APT40SM120B.

Figure 3 • APT40SM120B/J C/V Curve



With hard switching, a MOSFET must turn ON in order to switch the output voltage. By this definition, a half bridge with no load is on the border of hard switching because it must switch the capacitance of the drive transistors themselves, but there is no excess body diode charge or load to switch. A half bridge with no load is considered here. Only one edge is considered where the output transitions from +800 V to 0 V. See Figure 1 under the following conditions:

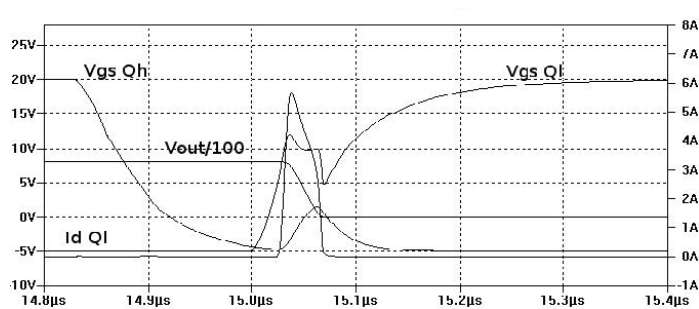
- 10 Ω gate drive at +20 V and -5 V
- 30 ns rise/fall time on the gate drive
- 100 ns dead time

The gate drive impedance is symmetrical (10 Ω ON, 10 Ω OFF) in order to demonstrate the need for an asymmetrical gate drive impedance.

The following figure shows 600 ns around a falling edge at the output. Starting at 14.84 μ s, the QH gate drive is switching QH OFF. The channel of QH, is fully OFF by 15.0 μ s as shown on the V_{GS} QH graph. When that happens, the following is true:

- The channel of QH is blocked.
- There is no significant change in the output voltage; it is still near V_{DD} at 800 V.
- CrH has almost no voltage across it. It will be between 2 nF and 200 pF, depending upon the load during the dead time.
- CrL has the full V_{DD} across it at about 20 pF.

Note that due to the output voltage, the switching event starts with CrH much larger than CrL.

Figure 4 • Half Bridge Falling Edge

The interesting part of the switching event is between 15.03 μ s and 15.07 μ s, when R_{gL} is sourcing the charge into the gate of QL and the Miller capacitance is sinking it. Also during that time, the graph shows the Miller plateau on the QL gate voltage ($V_{GS QL}$ in the graph) at about 10 V. Then during the Miller plateau, assuming an approximate 20 V gate drive, the following is true:

$$C_{rL} * dV_o/dt = I_g = (\text{Gate Drive Voltage} - \text{Gate Plateau Voltage})/R_g = (20 - 10)/R_g$$

During the first half of the switching process (15.03 μ s to 15.05 μ s), the upper device (QH) has less voltage across it than the lower device, and therefore it is more capacitive. The slew rate is set by the lower device's Miller capacitance. The effect is that the drain current ($I_{d QL}$ in the graph) peaks during the first half of the switching process at about 5.5 A in this case. This current is through QH capacitances C_{oh} and C_{rh} into the DC bus. The portion that is C_{rh} is the Miller capacitance of the upper device.

The result is a Miller voltage bump on V_{GS} of QH of about 7 V that peaks at about 15.06 μ s. This drives the upper device back into conduction and can greatly increase losses.

If only one gate resistor sets the gate drive both ON and OFF, there is no solution. Increasing the gate drive resistor of QL (turning on the lower device) spreads the event out over time. If the drive were symmetrical, however, it would require raising it on QH, which brings the Miller bump back to roughly the same amplitude.

The solution is that the resistance of the gate drive turning the device on must be much higher than that the one holding the opposing transistor off. A typical ratio might be anywhere from 2:1 to 4:1. It is just as important that the device is properly held off. There is no need for a Miller clamp as long as there is a sufficient negative gate drive margin to keep the devices held off, which ties back to the requirement for the negative drive.

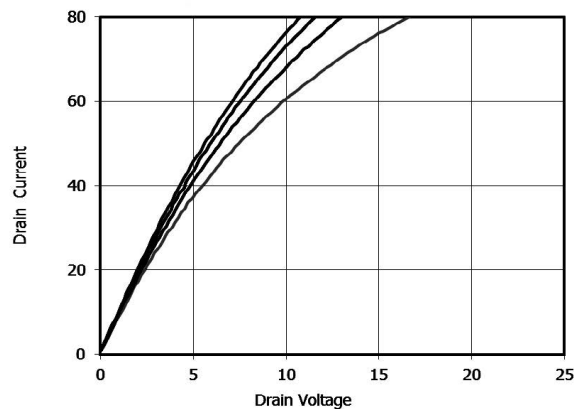
Figure 4 was simulated with a gate drive dead time of 150 ns. It has quite a bit of margin. If the dead time is of concern when designing a gate driver, the propagation variability (skew) of the gate driver should be considered. Analog Device ADuM4135 is a very low-skew driver.

There are no limitations on gate current. Switching losses are minimized by using the fastest possible ON and OFF drive subject to the condition that there is no excessive overshoot on the drive and the Miller effect mentioned above does not contribute excessively to losses. Overshoot and ringing of a few volts are expected and unavoidable.

2.5 Positive Gate Drive

When driving the gate, a positive 20 V drive is recommended. This can be reduced to +18 V or less, but there will be a penalty of increased conduction loss. SiC MOSFETs show more dependence upon gate voltage at the recommended gate drive voltage than silicon devices. This can be seen in the APT40SM120 output curves below with gate voltages ranging from 14 V to 20 V.

Figure 5 • APT40SM120 Transfer Curve ($V_{gs} = 20\text{ V}, 18\text{ V}, 16\text{ V}, 14\text{ V}$)



The positive gate drive voltage is reduced sometimes to increase device reliability, especially at elevated temperatures.

2.6 Characteristics of the Body Diode

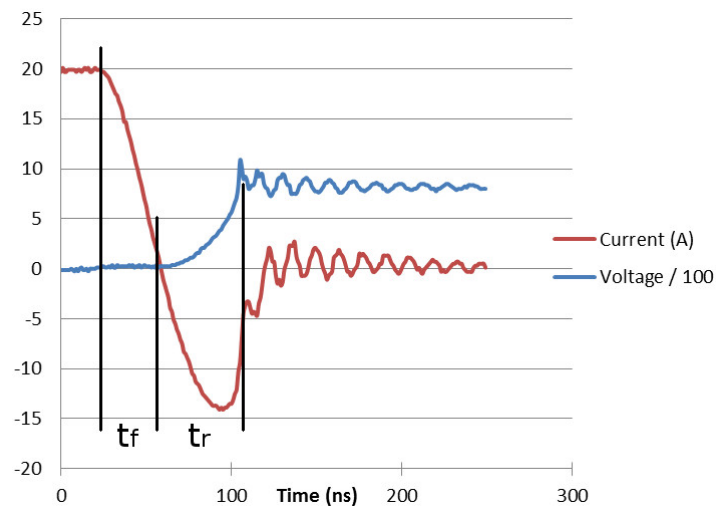
There are no restrictions on the use of the body diode with Microsemi SiC MOSFETs. There is no significant change in the body diode over time due to stacking faults. This is not true with all SiC MOSFET manufacturers, so it should be considered when comparing devices.

SiC is a wide bandgap semiconductor. For that reason, the body diode forward voltage drop is a little over 4 V. Any conduction loss will be high compared to the silicon variant due to the 4 V overhead. Generally, this does not matter because the body diode is normally used in such a way that the diode has a very short conduction time.

In a half-bridge arrangement, some loads place the diode in forward conduction during dead time followed by switching OFF with a high di_{DS}/dt . This is the definition of hard switching. Under these conditions, the recovery characteristics of the body diode are very important when calculating losses. A SiC MOSFET body diode has a very fast recovery and performs well under these conditions. Some applications operate continually with a hard-switched load. In that case, a shunt SiC Schottky diode may be considered. The following information will help with this decision.

The recovery current waveform of a SiC MOSFET body diode is different than that of silicon fast-recovery diode. With SiC, the N⁻ drain region doping is very low. Also, the carrier lifetime in the P⁺ P-well source region and the N⁺ drain region is very short. For this reason, the following are true:

- Above approximately 300 V with the 1200 V devices or above 200 V with 700 V devices, the depletion region has formed across the whole drain N⁻ region and cannot expand. Instead, the N⁻ electric field increases. In that state, the device acts as a parallel plate capacitor with constant capacitance. This can be seen in [Figure 3](#), where C_{OSS} and C_{RSS} are constant from 300 V to 1000 V.
- At most forward currents in the forward direction, the diode is in a high-level injection condition. The charge in what will later be the depletion region is a function of the forward current and temperature.
- The short carrier lifetime in the P⁺ and N⁻ regions means that the current rapidly drops to zero once the depletion region has formed.

Figure 6 • Body Diode Recovery

Body diode recovery can be seen in the switching characteristics. Figure 6 is a reverse recovery plot of an APT40SM120 body diode measured at 30 A forward current, where $dI_{DS}/dt = 500 \text{ V}/\mu\text{s}$, and the source is 800 V.

The standard JEDEC method used to measure recovery charge works very poorly because of the extremely high dV_{DS}/dt across the diode in relation to dI_{DS}/dt . This was recognized previously with fast recovery diodes. All SiC MOSFET body diode measurements in the data below were taken using the method described by Catt [1] [2].

The general shape of this waveform is representative of the recovery of the SiC body diode over a wide range of forward currents, current slew rates, temperature, and device voltage ratings. The interval t_r is the time over which the depletion region is being cleared of charge starting when the current crosses zero. The late edge of the t_r time interval marks where the voltage slewing stopped. Note that the current dropped to zero roughly 10 ns to 15 ns after the voltage clamped, a small current tail beyond t_r ; but by far the bulk of the recovery charge comes while the drain/source voltage is slewing.

The reverse recovery charge Q_{rr} is a function of temperature and the current profile leading into the event. Unlike a silicon diode, there is no current tail, hence the concept of a recovery time does not apply well. The effect of temperature on switching loss has been observed [3]. This effect is important when determining the need for a shunt Schottky diode.

The following graphs are the result of measurements of Q_{rr} at 25 °C, 100 °C, and 150 °C. They serve as a guide in estimating Q_{rr} for Microsemi 1200 V devices. These baseline measurements were taken with APT40SM120.

Figure 7 • APT40SM120 Body Qrr at Approximately 400 A/μs

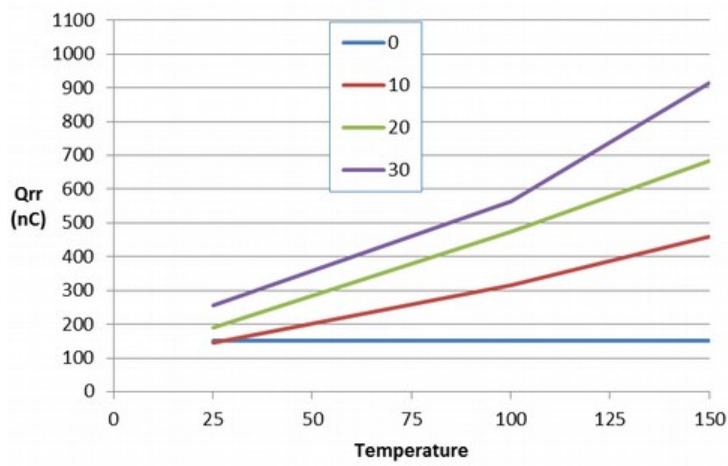


Figure 8 • APT40SM120 Body Qrr at Approximately 150 A/μs

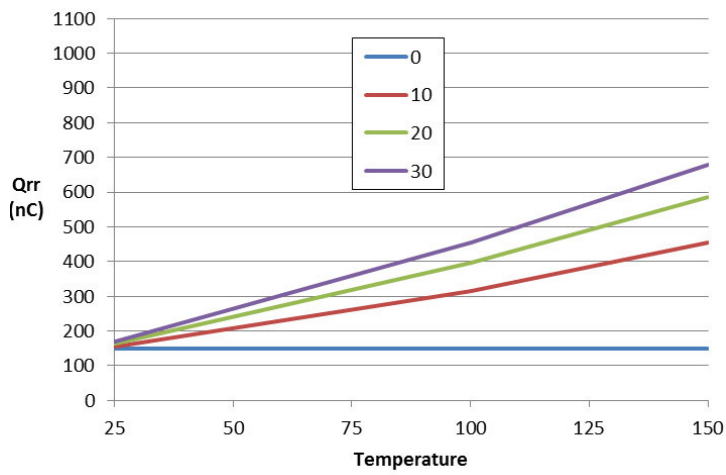
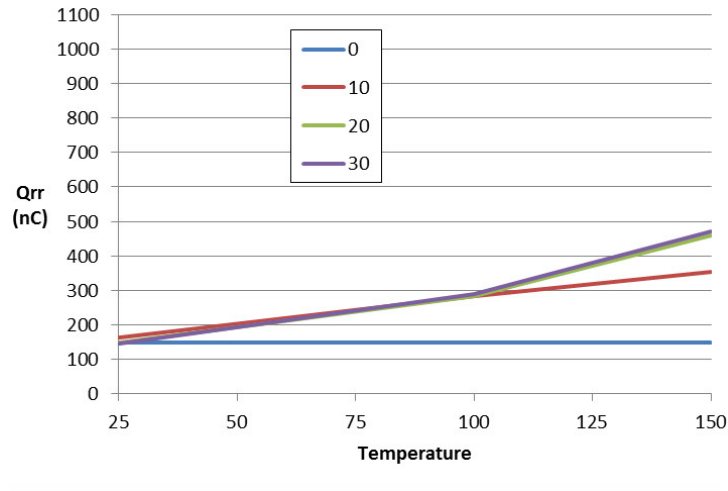


Figure 9 • APT40SM120 Body Qrr at Approximately 50 A/ μ s



APT25SM120 is half the die size as APT40SM120. To estimate Qrr in an application with APT25SM120, double the current I and double the rate dI_{DS}/dt . Reference the graphs above and then divide the resulting Qrr by two.

APT80SM120 is twice the size of APT40SM120. Divide the current I_{DS} and dI_{DS}/dt by two to reference the graphs and then multiply Qrr by two.

The following is recovery taken on APT35SM70. Being a 700 V device the temperature dependence is slightly different.

Figure 10 • APT35SM70 Body Qrr at Approximately 80 A/ μ s

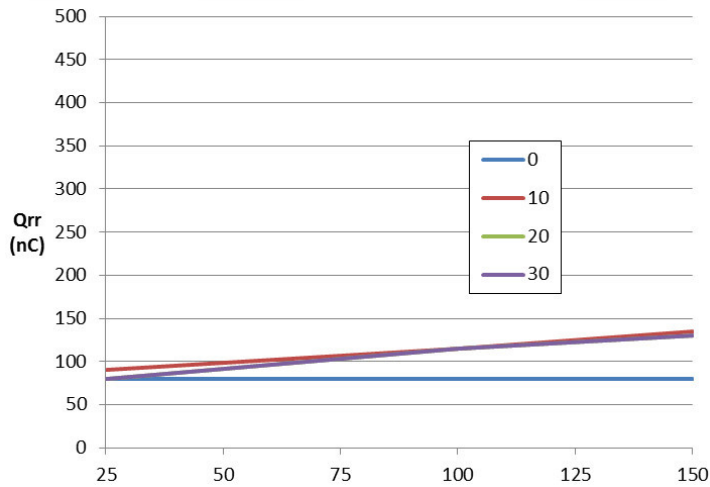


Figure 11 • APT35SM70 Body Qrr at Approximately 250 A/μs

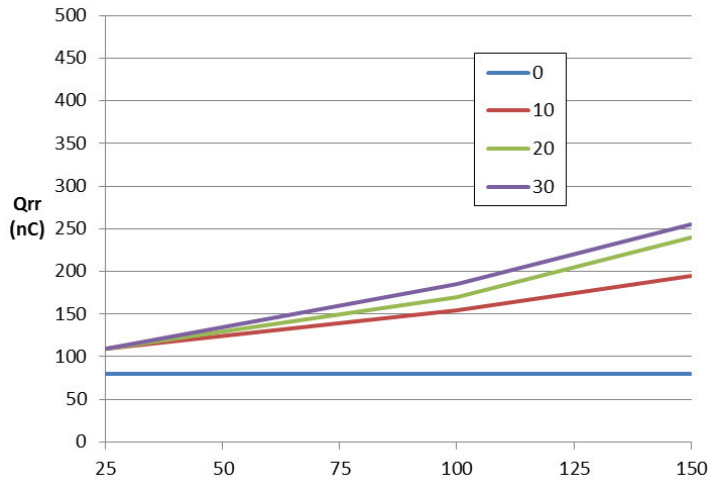
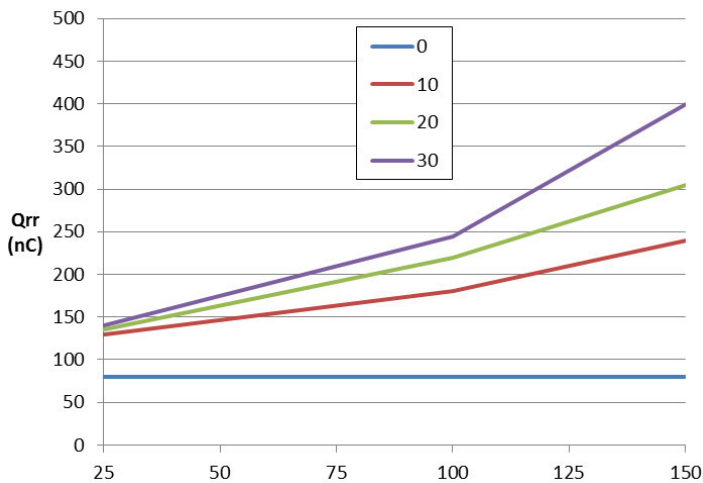


Figure 12 • APT35SM70 Body Qrr at Approximately 550 A/μs



Again, APT70SM70 has a die twice the size of APT35SM70. Divide the application current by two to reference the graphs, then multiply Qrr by two.

APT130SM70 has a die four times the size. Divide the application current by four to reference the graphs, then multiply Qrr by four.

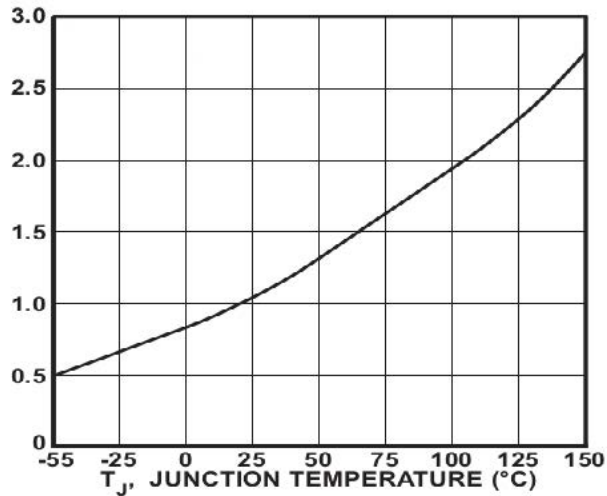
Each of these graphs has a baseline zero current plot. This is the value of Qrr predicted by capacitance measurements. The Microsemi SPICE models include this capacitance. The models do not include the additional charge due to high-level injection.

A shunt SiC Schottky diode should be considered when the additional energy penalty due to the capacitance of the Schottky diode and cost is less than the energy penalty from high-level injection without the diode and the higher voltage drop/conduction loss. Silicon Schottky diodes generally should not be used with SiC MOSFETs due to their limited di/dt capability and the possibility of dynamic avalanche in their termination structure.

2.7 RDS(on) vs. Temperature

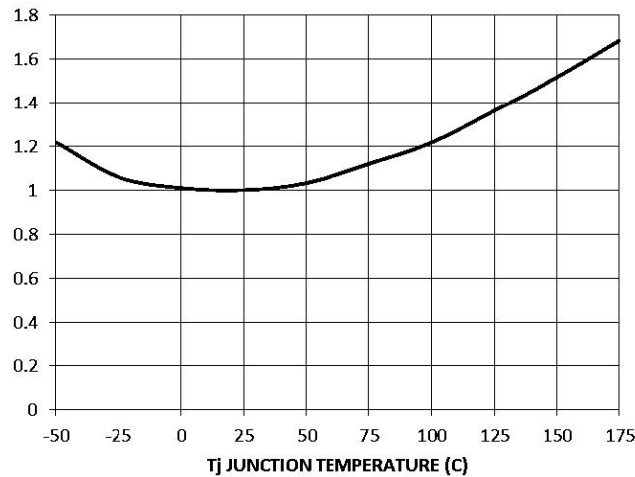
The following three graphs illustrate the difference in $R_{DS(on)}$ over temperature between Si and SiC MOSFETs. The temperature dependence of $R_{DS(on)}$ with Si MOSFETs is independent of the voltage rating of the device. This is because electron mobility in silicon MOSFETs is dominated by thermal scattering. They tend to show similar to the one in the following graph.

Figure 13 • RDS(on) vs. Temperature, Silicon



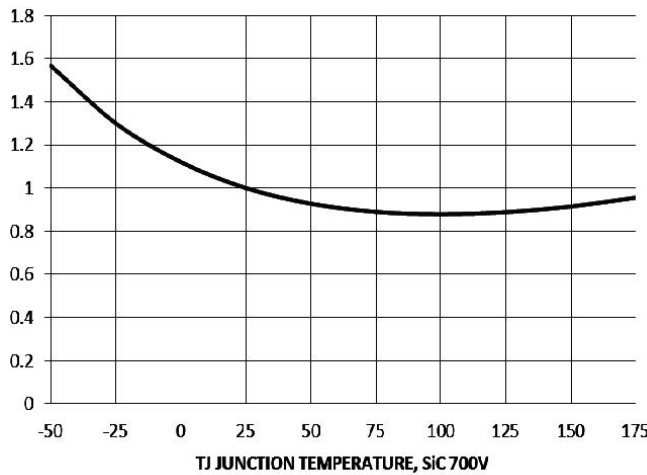
Note that from 25 °C to 150 °C, $R_{DS(on)}$ increases by a ratio of approximately 2.7 to 1. The following graph is typical of a Microsemi 1200 V SiC MOSFET.

Figure 14 • RDS(on) vs. Temperature, SiC 1200 V



There are two scattering mechanisms affecting electron mobility with the resulting benefit that from 25 °C to 175 °C, normalized $R_{DS(on)}$ varies typically by a ratio of approximately 1.5 to 1.8. Microsemi 700 V SiC MOSFETs have a different curve, as shown in the following graph.

Figure 15 • Rds(on) vs. Temperature, SiC 700 V



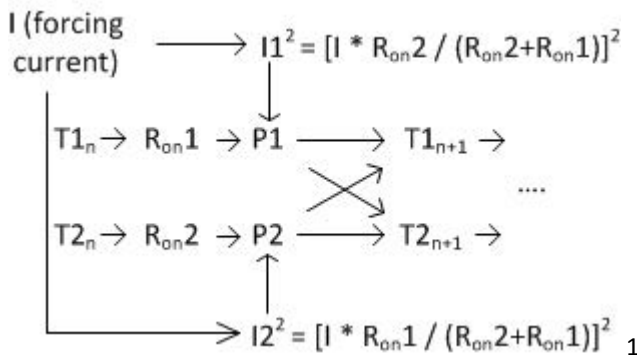
Parallel operation of SiC MOSFETs is used in higher current switching applications. A positive R_{DS(on)} vs. temperature slope may result in a negative feedback effect in current sharing. Likewise, a negative slope of R_{DS(on)} vs. temperature may result in a slight increase in the temperature imbalance. As an example, if two parallel transistors were on separate heat sinks with differing power levels or differing heat sinks, then a positive slope will tend to balance the heating. Two dies on a water-cooled heat sink also results in devices that are thermally decoupled. In most cases, there is thermal coupling because the devices must be close for electrical and practical reasons.

The following equation describes the relationship between the power dissipated in the devices and the resulting temperature. R_{hs11} is the sum of the junction to heat sink and heat sink to ambient thermal resistance for device 1. R_{hs12} is the heating induced in device 1 by device 2. This is a fraction of the heat sink to ambient thermal resistance. In all cases, the long time-constant thermal resistances should be considered.

$$\begin{bmatrix} R_{hs11} & R_{hs12} \\ R_{hs21} & R_{hs22} \end{bmatrix} \begin{bmatrix} P1 \\ P2 \end{bmatrix} = \begin{bmatrix} T1 \\ T2 \end{bmatrix}$$

With separate heat sinks, R_{hs12} = R_{hs21} = 0. With a perfectly coupled heat sink, all four terms are equal.

The following equation describes the feedback effect at a higher level by breaking it into an iterative equation.



P1 and P2 are the power dissipation of the devices and are multiplied by the respective $R_{DS(on)}$. The relation between the temperatures T1 and T2 and the resulting $R_{DS(on)}$ should be described by a second order polynomial.

Simulation of the sharing process will show that at lower ambient temperatures, the device temperatures will diverge more than at higher temperatures. However, the divergence is less than the absolute temperature resulting from the lower ambient temperature. For this reason, it is almost impossible to create a situation where the negative temperature coefficient will significantly affect a circuit reliability if the circuit is designed for a maximum operating temperature of greater than 25 °C. Current sharing could be an issue with cryogenic designs.

2.8 Gate Drive

The design of a SiC MOSFET gate driver is much like the design of a standard IGBT or silicon FET driver. Most of the features and practices carry forward, including the following:

- Asymmetrical high-current gate drive keeps switching losses down, as mentioned above.
- Secondary side power monitoring could be considered.
- Desat (short circuit) protection could be considered.

Due to the higher speed of SiC MOSFETs, consider the following:

- The capacitance of the gate drive interface should be kept to a minimum. At 50 V/ns, 5 pF of interface capacitance results in 250 mA current pulses. On the control side, these current pulses should be directed away from cables or control electronics using bypassing to a chassis or other filtering structures.
- The gate drive power supply should be rated for at least 50 V/ns. Most are not. Recom RxxP22005D DC/DC supplies are targeting the SiC market and are an economical solution. They currently do not have a dV/dt rating but probably will eventually. Another solution used on the Microsemi SiC Dual Driver Reference Design is the LT3999 unregulated with a custom transformer at the interface.
- Recommended gate drivers are ADuM4135 by Analog Devices; 1EDI(05,20,40,60)112AF drivers by Infineon; Si8271-8275 by Silicon Labs; and ISO5851 and ISO5852 by TI. As stated earlier, any gate driver should be capable of bipolar drive and capable of sustained operation at greater than 50 V/ns.
- With parallel operation it is very important to include series gate resistors with each device. Without these resistors, differential oscillation can develop rapidly during the switching process that can be destructive to the gate oxide.
- Microsemi has a dual-gate driver reference design available to aid in product development (part number: MSCSICMDD/REF1).

Due to the combination of the insulation requirement and high slew rate, the design of the gate supply is not trivial. In many supplies, the coupling from the secondary to the primary will interfere with the current control of the primary side controller. The Microsemi design avoids this problem by passing power over the insulation interface with an unregulated switcher.

2.9 DC Bus Items

The design of most power stages is driven by a number of requirements, including the following:

- Optimization and thermal performance
- Low DC bus inductance
- Insulation, clearance, and creepage requirements
- Manufacturability

It is beyond the scope of this application note to cover the details of design optimization. In the previous sections, the following topics were discussed:

- The role of source inductance in switching.
- The reason for negative gate drive and asymmetrical gate drive current.
- How the gate drive voltages are roughly determined.

There are a number of common design practices that should be implemented, including the following:

- To minimize losses, keep the bus loop inductance to a minimum using a wide parallel plate DC bus (laminated bus) with minimized layer spacing between the switching stages and the supporting film capacitors. The switching currents using SiC MOSFETs with hard switching will generate a higher di/dt across the bridge and DC bus than Si MOSFETs and Si IGBTs.
- Film or ceramic capacitors absorb the switching currents, and electrolytic capacitors fill in the charge behind. It is much better to use multiple small film capacitors than a few large ones in order to minimize the effect of capacitor inductance.
- As with other types of devices, when higher power levels are involved, it is recommended to minimize the DC bus inductance and the source inductance in the modules.
- In most designs, electrolytic capacitors will take part of the switching currents. At low temperatures, the devices switch faster but the electrolytic capacitors have a much higher equivalent series resistance (ESR). Designs must be evaluated at startup at the minimum operating temperature if electrolytic capacitors are involved.

2.10 References

[1] Catt, Jamie. “An Improved Method for Ultra Fast Recovery Diode Testing” (presented at the ninth annual Applied Electronics Conference and Exposition (APEC)), February 13–17, 1994.

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