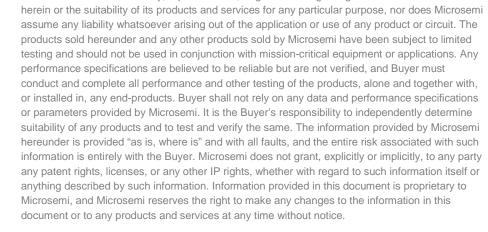
## SmartTime for Libero SoC v11.8 (Classic Constraint Flow) SmartFusion2, IGLOO2, and RTG4

### **User Guide**

NOTE: PDF files are intended to be viewed on the printed page; links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.







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## Welcome to SmartTime

### About SmartTime

SmartTime is a gate-level static timing analysis (STA) tool for the SmartFusion2, IGLOO2, and RTG4 families. With SmartTime, you can enter timing constraints and perform complete timing analysis of your design to ensure that you meet all timing constraints and that your design operates at the desired speed with the right amount of margin across all operating conditions.

Note: SmartTime in the Enhanced Constraint Flow has changed. Creation and Editing of timing constraints are now handled in a separate Timing Constraints Editor. See the Timing Constraints Editor for help with creating and editing timing constraints in the Enhanced Constraints Flow.

#### Static Timing Analysis (STA)

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements.

The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms as it reports all possible paths, including false paths, in the design. False paths are timing paths in the design that do not propagate a signal. To get a true and useful timing analysis, you need to identify those false paths, if any, as false path constraints to the STA tool and exclude them from timing considerations.

#### **Timing Constraints**

SmartTime supports a range of timing constraints to provide useful analysis and efficient timing-driven layout. SmartTime also includes a constraint checker that validates the constraints in the database.

#### **Timing Analysis**

SmartTime provides a selection of analysis types that enable you to:

- Find the minimum cycle time that does not result in a timing violation
- Identify paths with timing violations
- Analyze delays of paths that have no timing constraints
- Perform inter-clock domain timing verification
- · Perform maximum and minimum delay analysis for setup and hold checks

To improve the accuracy of the results, SmartTime evaluates clock skew during timing analysis by individually computing clock insertion delays for each register.

SmartTime checks the timing requirements for violations while evaluating timing exceptions (such as multicycle or false paths).

#### SmartTime and Place and Route

Timing constraints impact analysis and place and route the same way. As a result, adding and editing your timing constraints in SmartTime is the best way to achieve optimum performance.

#### See Also

Starting and Closing SmartTime



Starting and Closing SmartTime (Enhanced Constraint Flow) <u>SmartTime Components</u> <u>Components of SmartTime Timing Analyzer</u> <u>Changing SmartTime Preferences</u>

### **Design Flows with SmartTime**

You can access SmartTime in Libero SoC either implicitly or explicitly during the following phases of design implementation:

- After <u>Compile</u> Run SmartTime to add or modify timing constraints or to perform pre-layout timing analysis. In the Libero SoC Design Flow window, expand **Implement Design > Place and Route >** Timing Constraints. Choose Open Interactively to enter Timing Constraints.
- During <u>Place and Route</u> When you select timing-driven place-and-route, SmartTime runs in the background to provide accurate timing information.
- After <u>Place and Route</u> Run SmartTime to perform post-layout timing analysis and adjust timing constraints. In the Libero SoC Design Flow window, expand Implement Design > Verify Post-Layout Implementation. Right-click Verify Timing and choose Open Interactively.
- During <u>Back-Annotation</u> SmartTime runs in the background to generate the SDF file for timing simulation.

You can also run SmartTime whenever you need to generate timing reports, regardless of which design implementation phase you are in.

#### See Also

<u>Compile</u>

Layout

Back-Annotation

### Starting and Closing SmartTime - SmartFusion2, IGLOO2, RTG4

You must complete the layout of your design before using SmartTime. If you have not completed layout, the software executes the layout step for you before starting SmartTime.

To edit timing constraints in SmartTime, in the Design Flow window under **Constrain Design** double-click **Edit Timing Constraints**.

## To verify timing, in **Implement Design > Verify Post Layout Implementation** right-click **Open SmartTime** and choose **Open Interactively**.

SmartTime reads your design and displays post- or pre-layout timing information.

To close SmartTime, from the File menu, choose Exit.

To save changes to your design, from the File menu, choose Commit.

#### See Also

Importing Files Compiling your design Running Layout

### SmartTime Components

SmartTime is composed of two main tools:

- <u>The SmartTime Constraints Editor</u> enables you to view and edit timing constraints in your design. Constraints are sorted by category (requirements and exceptions) and by constraint type.
- The Maximum Delay Analysis View 🕍 and the Minimum Delay Analysis View 📐 enable you to analyze your design



With SmartTime, you can:

- Browse through your design's various clock domains to examine the timing paths and identify those that violate your timing requirements
- Add and modify timing requirements and exceptions
- Set constraints on a specific pin or a specific set of paths
- Create customizable timing reports
- · Navigate directly to the paths responsible for violating your timing requirements

# SmartTime Constraint Scenario - SmartFusion2, IGLOO2, RTG4 (Classic Constraint Flow Only)

A constraint scenario is an independent set of constraints. By default a scenario is created as *Primary Scenario* to hold all timing constraints defined by the user. This scenario is used during both analysis and TDPR. You can create multiple scenarios. The scenario used for analysis and the scenario used for TDPR can be selected from a list. Only one scenario can be used for analysis at a time. If multiple scenarios are created they are displayed in separate Constraint Editor windows.

The scenarios window lists all timing constraints scenarios available for the current design.

To create a new scenario, from the Constraints Editor, choose Tools > Scenarios > New Scenarios.

The icon indicates it is the Primary Scenario. It is the default scenario when the Constraints Editor opens.

The new scenario option is also available from Tools> Scenario > New Scenario.

You may click the undock icon at the upper right hand corner to undock a scenario window.

New scenarios are named Scenario\_1, Scenario\_2 and so on by default when they are first created. From the scenarios window you can select a scenario and from the right-click menu, select:

- Use for Analysis: : to use the selected scenario for Timing Analyzer. This command is also available from the Advanced tab in the SmartTime Options dialog box
- Use for TDPR: : to use the selected scenario for Timing-driven Layout. This command is also available from the Advanced tab in the SmartTime Options dialog box.
- Clone scenario: to create a new scenario with a set of constraints based on an existing scenario
- Delete scenario: to delete the selected scenario
- Rename scenario: to rename the selected scenario
- New Scenario: to create a new scenario

### Setting SmartTime Options - SmartFusion2, IGLOO2, RTG4

You can modify SmartTime options for timing analysis by using the <u>SmartTime Options</u> dialog box.

#### To set SmartTime options:

- 1. From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools> Options**. The **SmartTime Options** dialog box has three categories: **General**, **Analysis** and **Advanced**.
- 2. In the **General** category, select the settings for the operating conditions. SmartTime performs maximum or minimum delay analysis based on the Best, Typical, or Worst case.
- 3. Check or uncheck whether you want SmartTime to use inter-clock domains in calculations for timing analysis.
- 4. Click **Restore Defaults** only if you want the settings in the General pane to revert to their default settings.
- 5. Click Analysis to display the options you can modify in the Analysis view.
- 6. Enter a number greater than 1 to specify the maximum number of paths to include in a path set during timing analysis.



- 7. Check or uncheck whether to filter the paths by slack value. If you check this box, you must then specify the slack range between minimum slack and maximum slack.
- 8. Check or uncheck whether to include clock network details.
- 9. Enter a number greater than 1 to specify the number of parallel paths in the expanded path.
- 10. Click **Restore Defaults** only if you want the settings in the Analysis View pane to revert to their default settings.
- 11. Click Advanced to display advanced options.
- 12. Check or uncheck whether to use loopback in bidirectional buffers (bibufs) and/or break paths at asynchronous pins. Check or uncheck whether to disable non-unate arcs in the clock path. If using **Scenarios**, pick the appropriate scenario for timing analysis and timing driven place- and- route.
- 13. Click **Restore Defaults** only if you want the settings in the Advanced pane to revert to their default settings.
- 14. Click OK.

Option Categories	General
Select a category:     General	Operating Conditions
Analysis Advanced	Perform maximum delay analysis based on WORST
	Perform minimum delay analysis based on BEST
	Clock Domains
	✓ Include inter-dock domains in calculations for timing analysis.
	Enable recovery and removal checks.
	Restore Defaults

Figure 1 · SmartTime Options Dialog Box – General Options



Option Categories	Analysis View	
<ul> <li>Select a category: General</li> </ul>	Display of Paths	
Analysis	Limit the number of paths shown in a path set to:	100
Advanced	Filter the paths by slack value Slack range from: ns to: Slock network details in expanded path	ns
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults

Figure 2  $\cdot$  SmartTime Options Dialog Box – Analysis Options

Option Categories	Advanced	
<ul> <li>Select a category: General Analysis</li> <li>Advanced</li> </ul>	Special Situtations Use loopback in bi-directional buffers(bibufs)  Break paths at asynchronous pins  Disable non-unate arcs in dock network  Scenarios Use this scenario for timing analysis : Use this scenario for timing-driven place-and-route:	Primary •
	and the second second second second	
		Restore Defaults

Figure 3 · SmartTime Options Dialog Box – Advanced Options

#### See Also

SmartTime Options Dialog Box



# SmartTime Tutorial - Libero SoC for SmartFusion2, IGLOO2, and RTG4

The following tutorials explore common SmartTime features with example designs:

#### • Tutorial 1 - 32-Bit Shift Register with Clock Enable

**Goal:** Learn how to apply a clock constraint, perform maximum delay analysis & minimum delay analysis. Also, use the feature to dynamically update timing analysis by changing constraints in the constraints editor.

#### • Tutorial 2 – Count16 Counter

**Goal**: Import timing constraints file (SDC)/Add Clock Constraint, add input delay and output delay constraints. Create filters abd user sets to isolate design paths for analysis in SmartTime.

#### • Tutorial 3 - Design Using Both Clock Edges

**Goal**: Learn how to apply a clock constraint, perform maximum delay analysis for a design using both edges of the clock (rising & falling). Generate a custom timing report using SmartTime.

#### • Tutorial 4 - False Path Constraints

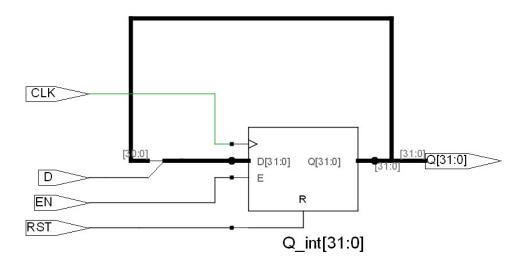
Goal: Add false path constraints to identify non-timing critical design paths.

#### • Tutorial 5 - Cross Clock Domain Analysis

Goal: Analyze the timing results for a design with cross clock domain paths.

### Tutorial 1 - 32-Bit Shift Register with Clock Enable

This tutorial section describes how to enter a clock constraint for the 32-bit shift register shown. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.



#### Figure 4 · 32-bit Shift Register

Use the links below to go directly to a topic:

- Add a Clock Constraint
- Run Place and Route



- Maximum Delay Analysis with Timing Analyzer
- Minimum Delay Analysis with Timing Analyzer
- <u>Changing Constraints and Observing Results</u>

#### To set up your project:

- 1. Invoke Libero SoC. From the Project menu, choose New Project.
- 2. Enter shift32 for your new project name and browse to a folder for your project location.
- 3. Select **Verilog** as the Preferred HDL Type.
- 4. Leave all other settings at the default values.

ew project				
oject details Specify project details				
Project Details	Project name:	sf2_shfit32		
Device Selection	Project location:	d. (actelprj		Browse
Device Settings	Description:			
Design Template	Preferred HDL type	Contraction of the second		
Add HDL Sources	Enable block or	eation		
Add Constraints				
Help			< Back Next >	Finish Cancel

Figure 5 · New Project Creation - 32 Bit Shift Register

- 5. Click Next to go to Device Selection page. Make the following selection from the pull-down menu:
- Family: SmartFusion2
- Die: M2S090TS
- Package: 484FBGA
- Speed:STD
- Core Voltage: 1.2 V
- Range: COM
- 6. Click the M2S090TS-1FG484 part number and click Next.



	Part filter										
Project Details	Family:	SmartFu	ision2	•	Die:	M2S090TS	•	Package:	484 FBGA	•	
	Speed:	+1		•	Core voltage:	1.2	•	Range:	COM	•	
Device Selection									Res	et filters	
Device Settings	Search part:										
	Part Numb	er	4LUT		DFF	User I/Os	uSRAM	IK	LSRAM 18K	Math (18x18)	PLLs and
Design Template	M25090TS-1	LFG484	86184		86184	267	112		109	84	6
Add HDL Sources											
Add Constraints											
ibero	4		111		-						

- 7. Accept the default settings in the Device Settings page and click Next.
- 8. Accept the default settings in the Design Template page and click Next.
- 9. In the Add HDL source files page, click **Import file** to import the source file, Navigate to the location of the source Verilog file for the 32-bit shift register you have downloaded from the <u>Microsemi website</u>. Click to select the source file and click **Open**. After project creation, the source Verilog file you import will appear in the project's hdl folder under the File tab.

ew project			
<b>Id HDL source files</b> Specify HDL files to import/link to your	project.		Selected part: M2S090T5-1FG4
Project Details	ort file		Delete
	File type	File name	File location
Device Selection	Imported	shift_reg32.v	D:/shift_reg32/hdl
Device Settings			
Design Template			
Add HDL Sources			
Add Constraints			
Help		< E	lack Next > Finish Cancel

- 10. Click Next to go to the Add Constraints Page.
- 11. We are not adding any constraints. Click **Finish** to exit the New Project Creation wizard.
- 12. After you have created the project, confirm that the imported Verilog source file appears in the Files window, as shown in the figure below.



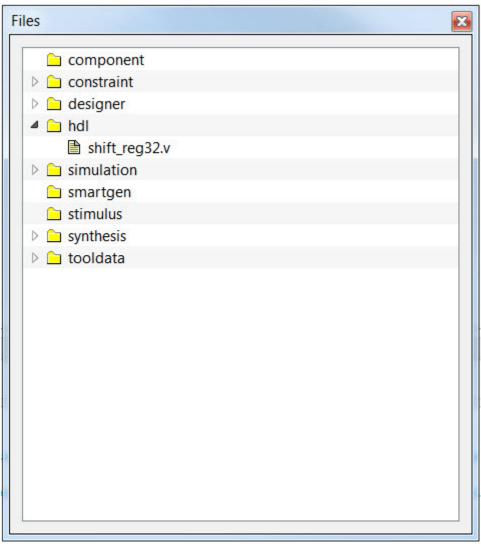


Figure 6 · HDL File shift\_reg32.v in the Libero SoC File Window

13. Confirm that the shift\_reg32 design appears in the Design Hierarchy window, as shown in the figure below.



Design Hierarchy	×
Show: Components 💌	
🔺 í work	
shift_reg32 (shift_reg32.v)	
•	4

Figure 7 · shift\_reg32 in the Design Hierarchy Window

- 14. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
- 15. Double-click **Compile** in the Design Flow window to run Compile with default settings. A green check mark appears next to Compile when it completes successfully (as shown in the figure below).



Design Flow shift_reg32 Tool Create Constraints Tool Create Constraints Timing C	⊕ × ● ♥ Design = _sdc.sdc	shift_re Synthesize Synplift shi run_op Compile shift_re shift_re	eports 2 eg32_pinrpt eg32_pinrpt	The 'set The 'set	0 Errors ( 0 War t_compile_info	o' command o' command	i succeeded i succeeded	
Tool         4       Verify Pre-Synthesized         Simulate         4       Create Constraints         *       I/O Constraints         *       Timing Constraints         *       Timing Constraints         *       Timing Constraints         *       Floorplan Constraints         *       Implement Design         *       Synthesize         *       Verify Post-Synthesis In         Simulate       Compile         *       Configure Flash*Freeze	Design =	<ul> <li>shift_reg3</li> <li>shift_reg</li> <li>shift_reg</li> <li>shift_reg</li> <li>Synthesize</li> <li>synthesize</li> <li>synthift</li> <li>\$\u00e4</li> </ul>	2 232_pinrpt 232_pinrpt 2 4.log ft_reg32.srr tions.txt 232_rwnetl ft_reg32_co 232_compi	The 'set The 'set	t compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info t_compile_info	o' command o' command	i succeeded i succeeded	
bearg Dearg	e Catalog				cute Script co 'st_shell.exe	ommand suc	cceeded.	-
G ■ Messages S Errors ▲ Warnings The 'set_compile_info' comma The 'set_compile_info' comma	and succeeded and succeeded and succeeded and succeeded and succeeded and succeeded and succeeded and succeeded and succeeded was specifie eded.	4. 4. 4. 4. 4. 4. 4.						8

Figure 8 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

### Add a Clock Constraint - 32 Bit Shift Register

To add a clock constraint to your design:

1. In the Design Flow window, expand **Edit Constraints** and double-click **Timing Constraints** to open the Constraints Editor (as shown in the figure below.)



SmartTime - [Constraints Editor for scer	nario P	rimary]										
File Edit View Constraints Too	ols He	elp										_ 8 ×
📕 🖸 🗅 🕉 🗲 e 🕷	e 14	¥. ¥_	84 - 84	WN 56	n (n )	n D.						
	UL HAA	10 <b>1</b> 101	00	nn 💊	147° - 440° -	a. 🗆						
🔄 🖸 Constraints Editor for scenario Primar	v											
Constraints Editor for scenario Primary	·											
constraints cutor for scenario Prinary												
▲ Constraints											-	
<ul> <li>Requirements</li> </ul>		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File	Comments
Clock				1999-1997	(113)	(1112)	(70)		(			
Generated Clock	1	Click here to	add a const	raint								
Input Delay												
Output Delay												
<ul> <li>Exceptions</li> </ul>												
Max Delay												
Min Delay												
Multicycle												
False Path												
<ul> <li>Advanced</li> </ul>												
Clock Source Latency												
Disable Timing												
Clock Uncertainity												
4		•							_		_	- F
										Temp: 0	85 C Volt	t: 1.14 - 1.26 V Speed: -1

Figure 9 · SmartTime Constraints Editor

2. In the left pane, under Constraints> Requirements, right-click **Clock** and choose **Add Clock Constraint** to open the Create Clock Constraint dialog box (as shown in the figure below).

Create Clock Constraint		? X
Clock Name : my_clk	Clock Source : CLK 🔹 🛄	
H Period	ns Mhz	
Offset :         ▶ <         Duty cycle         ▶            0.000         ns         50.0000         %		
Comment :		
Help	OK Cancel	

Figure 10 · Create Clock Constraint Dialog Box

- 3. From the **Clock Source** drop-down menu, choose the CLK pin.
- 4. Enter my\_clk in the Clock Name field.
- 5. Set the Frequency to 800 MHz (as shown in the figure below) and leave all other values at the default settings. Click **OK** to continue.



Clock Name : my_clk	Clock Source :	· ···
Image: Period : 1,25         Image: Period : 1,25 <td>ns 🔸 or Fr</td> <td>requency: 800 Mhz</td>	ns 🔸 or Fr	requency: 800 Mhz
Comment : Help		OK Cancel

Figure 11 · Add a 800 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).

	<u> </u>	Syntax	Clock	Clock	Period	Frequency	Dutycycle	First Edge	Offset	Waveform	File	Comments	
A Requirements		Syncax	Name	Source	(ns)	(MHz)	(%)	rusetuge	(ns)	wavelonin	THE	comments	
Clock		2.11	2002/20	1									
Generated Clock		Click here to add	a constraint										
Input Delay	2	W	my_clk	CLK	1.250	800.000	50.0000	rising 🚽	0.000	0 0.625	GUI		
Output Delay	e -												
4 Exceptions													
Max Delay													
Min Delay													
Multicycle													
False Path	- L												
Advanced													
Clock Source Latency	-												

Figure 12 · 800 MHz Clock Constraint in the Constraint Editor

- 6. From the File menu, choose Save to save the constraints.
- 7. From the SmartTime File menu, choose Exit to exit SmartTime.

### **Run Place and Route**

Constraints Editor for scenario Primary

- 1. Right-click **Place and Route** and choose **Configure Options**.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.



Layout Options	? ×
Timing-driven	
Power-driven	
High Effort Layout	
Repair Minimum Delay Violations	
<ul> <li>Incremental Layout</li> <li>Use Multiple Passes</li> </ul>	
Configure	
Help ОК	Cancel

Figure 13 · Layout Options Dialog Box

3. Double-click Place and Route inside the Design Flow window to start the Place and Route.

A green check mark appears next to Place and Route after successful completion of Place and Route.

# Maximum Delay Analysis with Timing Analyzer- 32-Bit Shift Register Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

#### To perform Maximum Delay Analysis:

1. Right-click **Verify Timing** in the Design Flow window and choose **Open Interactively** to open SmartTime. The Maximum Delay analysis window appears. A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays:

- Maximum operating frequency for the design
- External setup and hold requirements
- Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 609.75 MHz.



1 2	2 🚨 🦻 🎽 🖌 🖉 🖉 🗮									
mum Dela	ay Analysis View									
<b>A</b>	Analysis for scenario				00					
MAX	Primary	Design Family		shift_reg						
- 81		A		M2S090	and state of the second se					
4 .	<ul> <li>✓ my_clk</li> <li>✓ Register to Register</li> </ul>	Die			1.20					
	External Setup	Package		484 FBC						
	Clock to Output Register to Asynchronous	Temperatur		0 - 85 C						
	External Recovery	Voltage Ra		1.14 - 1	26 V					
	Asynchronous to Register	Speed Gra		STD						
	E Pin to Pin Input to Output	Design Sta	te	Post-La						
-	alput to output	Data sourc	0	Producti						
		Min Operat	ing Conditio	ns BEST -	1.26 V - 0 C					
		Max Opera	ting Condition	ans WORST	- 1.14 V - 85 C					
		Scenario fo	r Timing An	alysis Primary						
of paths	Select a set of paths to see its slack distribution.	Summa Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Out (ns)
*		my_clk	1.640	609.756	1.250	800.000	1.258	0.429	3.823	9.486
			Territoria		-					
	J	-		elay (ns) Max	Delay (ns)					
	slack distribution(ns)	Input to Ou	tput N/A	N/A						

Figure 14 · Maximum Delay Analysis - Summary

- 2. Expand my\_clk to display the Register to Register, External Setup and Clock to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations

Primary		ron =					TO *					
d Summary	- L									E ante		1
4 vi my_clk		Oustomize table								Apply	Filter Store Filter	Reset Filter
🖌 Register to Register			1					_	1	212		
External Setup Clock to Output		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Hinimum Perio (ns)	d g	Skew (ns)	
Register to Asynchronous	1	Q_int[18]:CLK	Q_int[19]:D	0.716	0.159	4.810		0.298			0.077	
External Recovery		d befrahory	d hid rate	0.715	0.139	4.020	3,202	0.230	1,05	-	0.077	
Asynchronous to Register	2	Q_int[25]:CUK	Q_int[20]:0	0.754	0.164	4.809	4.973	0.298	101	6	0.054	E
Input to Output	3	a lutrit av	0.1-11-12-0	0.688	0.174	4.823	4.997	0.298	1.07		0.090	
🖂 User Sets	3	Q_int[11]:QUK	Q_int[12]:D	0.688	0.1/4	4.823	4.997	0.298	1.03	- C	0.090	
	4	Q_int[5]:CLK	Q_int(6):D	0.712	0.177	4.832	5.009	0.298	1.07	73	0.053	
		1.00000000		0.000	01572	10/102		0.000	1000			
	5	Q_Int[7]:CLK	Q_int[8]:D	0,706	0.182	4.827	5.009	0,298	1.06	58	0,054	
	6	Q_int[19]:OLK	Q_int[20]:D	0.701	0.219	4.777	4.995	0.298	1.03	31	0.032	
30	7	Q_int[26]:CUK	Q_int[27]:D	0.673	0.245	4.753	4.998	0.299	1.00	05	0.033	
		ame		Туре	Net			Ma	cro Op	Delay Tot	tal Fanout Edge	1
24	1	Summary data required tin								4.9	73	
		data arrival time								4.8		
		slack								0.1	64	
18		Data_arrival_time_c	alculation									
		my_clk								0.000 0.0		6
		CLK		Clock source	CLK				-	0.000 0.0		
		CLK_ibuf/U0/U_I		net	CLK					0.000 0.0		
12		CLK_ibuf/U0/U_J		cell	CLK ibu	2		ADL	LIB:IOPAD_IN +	0.197 2.3		
		CLK_ibuf_RNIVQ		net	CLK_ibu				LIB:GBM +	0.197 2.3		
		CLK_ibuf_RNIVQ		cell	-			AUL	LIB:GBM +	0.691 3.1		
			M/U0_RGB1_RGB1:An		CLK_ibu	RNIVQ04/U0_	YWn					
			04/U0_RGB1_RGB1:VL						LIB:RGB +	0.372 3.4		
6		Q_int[25]:CLK		net	CLK_ibu	_RNIVQ04/U0_	RGB1_RGB1_rg			0.612 4.1		
				cell				ADI	LIB:SLE +	0.102 4.2		
		Q_int[25]:Q							+	0.602 4.8	109 r	
		Q_int[25]:Q Q_int[26]:D		net	Q_c[25]							
6		Q_int[25]:Q Q_int[26]:D data arrival time		net	Q_c[25]					4.8	09	
6	1.445 <i>•</i>	Q_int[25]:Q Q_int[26]:D	calculation	net Clock Constra						4.8		

Figure 15 · SmartTime Register to Register Delay

4. Double-click a path row to open the Expanded Path window. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).

**Note:** The Timing Numbers in these reports may vary slightly with different versions of the Libero Software, and may not be exactly the same as what you will see when you run the tutorial.



	@ X										
mmary for path mm Q_mt[25]:CLK Q_mt[26]:D ita Required Time (ns) Data Arrival Ti 973 4.809	me (ns) Slack (ns) 0.164	1								Path Profile Cel Delay 0.00%	
		a									
ame	Type	Net	Macro	Op	Delay	Total	Fanout Edge				
Data_arrival_time_calculation											
my_clk					0.000						
CLK	Clock source			+	0.000						
CLK_ibuf/U0/U_JOPAD:PAD	net	CLK		+	0.000						
CLK_ibuf/U0/U_IOPAD:Y	cell		ADLIB:JOPAD_IN	4 +	2.128						
CLK_ibuf_RNIVQ04:An	net	CLK_ibuf		+	0.197						
CLK_ibuf_RNIVQ04:YWn	cell		ADLIB:GBM	+	0.105						
CLK_ibuf_RNIVQ04/U0_RGB1_RGB1	:An net	CLK_ibuf_RNIVQ04/U0_YWn		+	0.691						
CLK_ibuf_RNIVQ04/U0_RGB1_RGB1			ADLIB:RGB	+	0,372	3,493	6 r				
Q_int[25]:CLK	net	CLK_ibuf_RNIVQ04/U0_RGB1_RGB1_rgbl_net_	Providence of the second	+	0.612	4.105	r				
Q_int[25]:Q	cell		ADLIB:SLE		0.102	4.207	2 1				
Q_int[26]:D	net	Q_c[25]		+	0.602						
data arrival time		100 B 100				4.809					
		D_IN EN YWO	CLK_buf_R	NIV			-	RGB _int[25]	-	ALN 	
				An ENn	n Y RGB	R –	-0 -0			SLE	

Figure 16 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 3**. The Input Arrival time from the EN pin to Q\_int[27]:EN is 4.547 ns (as shown in the figure below).

	nalysis View														
	Analysis for scenario														
	Primary	Fri	- m						TO *						
		_ 2									-				
	mmary	0	ustomize table								6	Apply Pi	iter	Store Fil	ter Reset Filte
* 46	w my_clk	_				_	_		-	-		_	_	_	
	<ul> <li>Register to Register</li> </ul>		Source Pin	Sink	-	Delay	Slack	Arrival	Required	Setup	External				
	External Setup	_	Source Pin	SIRK	rm .	(ns)	(ns)	(ns)	(ns)	(ns)	Setup (ns)				
	Clock to Output Register to Asynchronous	1	EN	Q_int[31]:EN		4.547		4.547	-	0.399	1.258				
	External Recovery			and the second	S										
	Asynchronous to Register	2	EN .	Q_int[30]:EN		4.547		4.547		0.399	1.248				
4 50	Pin to Pin						_								
	Input to Output	- 1									1.248				
- 25	User Sets														
		4	EN	Q_int[29]:EN		4.547		4.547		0.399	1.248				
			EN	O int/281:EN		4.547		4,547	÷	0.399	1.248				
		plane (	and the second se	10 mit 281:EN		- North Color		4.54/	-	0.3991					
		Na			Туре	N	et				Macro	Op	Delay	Total F	anout Edge
			Summary												
			data required time											N/C	
<ul> <li>E</li> </ul>		1	data arrival time											4.547 N/C	
- 1			slack											N/L	
- 1			Data_arrival_time_calcu EN	alation									0.000	0.000	
- 1			EN_IBUE/UD/U_JOPAD	DAD	net	E							0.000		
- 1			EN_ibuf/U0/U_IOPAD		cell	E					ADLIB:JOPAD IN		2.720		11
- 1			EN_ibuf/U0/U_IOINF		net	E	jibuf/00	/VIN1			Horabiotelo an	+	0.000		1
- 1			EN_ibuf/U0/U_IOINF		cell			000000			ADUBIOINEE BYPAS	55 +	0.106		32 f
- 1			Q_int[27]:EN		net	ET	4_c						1.721		1
- 1	The set of the set of the		data arrival time											4.547	
	This set has no path.		Data_required_time_cal	lculation											
- 1			my_clk										N/C		
- 1			CLK		Clock source							+	0.000		r
			CLK_ibuf/U0/U_IOPA		net	C	ж					+	0.000		r
- 1			CLK_ibuf/U0/U_IOPA		cell						ADLIB:JOPAD_IN	+	1.915		2 /
- 1			CLK_ibuf_RNIVQ04:A		net	C	K_ibuf					+	0.177		f
- 1			CLK_ibuf_RNIVQ04:V		cell	12					ADLIB:GBM	•	0.095		5 f
- 1			CLK_ibuf_RNIVQ04/L			C	K_ibuf_R	NEVQ04/U0	_Y1Wn		(hereite en	+	0.623		.1
- 11			CLK_ibuf_RNIVQ04/U	JO_HGB1_RGB3;YL					0.004 0.000		ADLIB:RGB	*	0.335		5 .
			Q_int[27]:CLK		net		R IDUT R	MINQ04/00	RGB1_RGB3_	rgus net 1	ADUB-SLE		0.399		
			Q_int[27]:EN		Library setup	time					ADUBISCE	-	0.399	Le.C	

Figure 17 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 1. The maximum clock to output time from Q\_int[16]:CLK to Q[16] is 9.486ns.



-	2 3 2 6 0 ×													
rum Delay	Analysis View													
~	0.077104 00													
	Analysis for scenario Primary													
AX		Fre	HI *					то •						
	immary	0	ustomize table								Apply	Filter 1	itore Pilter	Reset Pilter
4 44	🕑 my_clk	_												
	<ul> <li>Register to Register</li> </ul>		Source Pin	Sink		Delay	Slack	Arrival (ns)	Required (ns)	Clock to 0		a		
	External Setup Clock to Output	_	Source ras	Serve		(ns)	(ns)	Arrivat (its)	(ns)	CIOCK LO C	une (une	.,		
	Register to Asynchronous	1	Q_int[16]:CUK	Q[16]				9.486				374	6	
	External Recovery													1
	Asynchronous to Register	2	Q_int[15]:CLK	Q[15]		5.354		9,461				9.4	1	
4 7	Pin to Pin		0.1.1707.0.1	0.5201										
	Input to Output	3	Q_int[28]:CLK	Q[28]		3.946		8.054				8.05	4	
3		4	Q_int[4]:CLK	Q[4]		3.817		7.937				7.9	7	
		1	of infidience	91.75		3.01/		1.337				1.2.		+
		Nat	me		Type	Net				Macro	On 1	Delay Tota	I Fanout E	doe
			Summary								op			.1.
_		_	data required time									N/	c	
			data arrival time								÷.	9.48	6	
			sløck									N/	С	
- 1			Data_arrival_time_calc	ulation										
- 1			my_clk									0.000 0.00		
- 1			CLK	2012	Clock source							0.00 000.0		
- 1			CLK_ibuf/U0/U_IOP		net	CLK						0.000 0.00		
- 1			CLK_ibuf/U0/U_IOP CLK_ibuf_RNIVQ04:		cell	CLK_ibuf				ADLIB/JOPAD_IN		0.197 2.32		
- 1			CLK_ibuf_RNIVQ04:		cell	CERCIDOR				ADUR-GRM		0.105 2.43		
- 1			CLK_ibuf_RNIVQ04/			CLK ibuf	PARIOOA	ALL MADE		AD LID. JOWI		0.687 3.11		
- 1			CLK_ibuf_RNEVQ04/			CCK_INGS	in an offer	/w_1111		ADLIB:RGB		0.372 3.48		
	This set has no path.		Q_int[16]:CLK	00_11002_11000.11	net	CLK ibuf	RNIV004	/U0_RGB1_RGB0		HELENIOP		0.618 4.10		
			Q_int[16]:Q		cell					ADUB:SLE	+	0.127 4.23	4 2 f	
			Q_obuf[16]/U0/U_K	OUTFF:A	net	Q.c[16]					+	1.671 5.90	5 f	
			Q_obuf[16]/U0/U_K	OUTFF:Y	cell					ADLIB:JOOUTFF_BYPASS		0.403 6.30		
- 1			Q_obuf[16]/U0/U_K	PAD:D	net	Q_obuf[1	5]/U0/DO	UT			+	0.000 6.30	8 f	
- 1			Q_obuf[16]/U0/U_K	PAD:PAD	cell					ADLIB-JOPAD_TRJ		3.178 9.48		
- 1			Q[16]		net	Q[16]					+	0.000 9.48		
- 1			data arrival time									9.48	δ	
		1	Data_required_time_ca	liculation										
		-	my_clk									N/C N/		
			CLK		Clock source						+	0.000 N/		
	slack distribution(ns)		Q(16)									N/	· · ·	

Figure 18 · SmartTime Clock to Output Path Analysis

### Minimum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

- 1. From the SmartTime Constraints Editor Tools menu, choose Minimum Delay A
- 2. Analysis. The Minimum Delay Analysis View appears, as shown in the figure below.



1 2	2 2 3 2 K 8 @ X									4
um Dela	ıy Analysis View									
3	Analysis for scenario	Desig			shift reg32					
min	Primary				SmartFusion2					
	Summary	A	ry -							
	v⊕ my_clk ✓ Register to Register	Die			M2S090TS					
	External Hold	Pack			484 FBGA					
	Clock to Output	Temp	erature F	tange	0 - 85 C					
	Register to Asynchronous External Removal	Volta	ge Range		1.14 - 1.26 V					
	Asynchronous to Register	Spee	d Grade		STD					
43	🔀 Pin to Pin	Desig	n State		Post-Layout					
	Input to Output	* Data	source		Production					
		Min C	Operating	Conditions	BEST - 1.26 V -	0 C				
	30. 2	Max	Operating	g Conditions	WORST - 1.14 V	- 85 C				
				iming Analysis	Primary					
# of paths	Select a set of paths to see its slack distribution.	Cloc		riod Frequer	cy Required	Required	External	External	Min Clock-To-	
2 b		Dom	ain (ns	) (MHz)	Period (ns)	Frequency (MHz)	Setup (ns)	Hold (ns)	Out (ns)	To-Out (ns)
4		my_c	lk 1.6	40 609.756	1.250	800.000	1.258	0.429	3.823	9.486
				Min Delay	ns) Max Delay (I	15)				
		Input	to Outpu	t N/A	N/A					
	slack distribution(ns)									

Figure 19 · SmartTime Minimum Delay Analysis View- Summary

- 3. Expand **my\_clk** to display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Register path sets.
- 4. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
- 5. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.

le Edit View Tools Help															-
m Delay Analysis View															
															_
Analysis for scenario Min Pristary		om •					то								
and Summary ar v@ my_clk		Lustomize table								Apply	Filter	Store	Filter.	Reset Fill	ter
✓ Register to Register															-
External Hold Clock to Output		Source Pin	Sink	Pin f	elay	Slack	Arrival	Required	Hold	Skew					
Register to Asynchronous		0.000000000000000			(ns)	(ns)	(ns)	(ns)	(ns)	(ns)					
External Removal	1									0.036					12
Asynchronous to Register A 🏹 Pin to Pin	2	Q_int[28]:CLK	Q_jnt[29]:D		0.289	0.253	2.442	2, 189	0.000	0.036					-
Input to Output St User Sets	3	Q_int[15]:OLK	Q_int[16]:D		0.293	0.257	2.446	2.189	0.000	-0.036					
	4	Q_int[16]:CUK	Q_int[17]:D		0.296	0,260	2.449	2, 189	0.000	0.036					
	5	Q_int[27]:O.K	Q_int[28]:D		0.297	0.261	2.450	2.189	0.000	-0.036					
6227	6	Q_int[10]=OLK	Q_jnt[11]:0	1	0.307	0.262	2.467	2.205	0.000	-0.045					
30	N	ime	-	Туре	Ne	t		_	-	Macro	Op	Delay	Total Fa	nout Edg	je -
65 C	-	Summary													
24		data arrival time											2.439		
		data required time slack									- 1		0.250		
		Data arrival time calco	lation												
18		my_clk										0.000	0.000		1
		CLK		Clock source							+	0.000	0.000		
22		CLK_ibuf/U0/U_JOPA	D.PAD	net	CU	K:					+	0.000	0.000	1	
		CLK_ibuf/U0/U_JOP/	D:Y	cell						ADUB:IOPAD J	N +	1.109		2 1	
12		CLK_ibuf_RNIVQ84;4		net	CU	Kjbuf.					+	0.104		1	
		CLK_ibuf_RNIVQ04:1		cell						ADLIB:GBM	+	0.055		5 f	
		CLK_ibuf_RNIVQ04/			CU	K_ibuf_RN	EVQ04/U0_	YWn			+	0.363		1	
6		CLK_ibuf_RNIVQ04/	IO_RGB1_RGB3:VL							ADLIB:RGB	+	0.197		5 1	
		Q_int[29]:CLK		net	CU	Cibuf_RN	INQ04/U0_	RGB1_RGB3_r	gbl_net_1		*	0.325		. 1	
		Q_int[29]:Q		cell		-				ADLIB:SLE	•	0.057		2 r	
		Q_int[30]:D data arrival time		net	0.	c[29]							2,439		
0 0.1985 0.25 0.3015 0.353 0.40		Data required time ca	in dation										2.439		
		usu_required_time_ca	c snation				10								. "
slack distribution(ns)							110								

Figure 20 · SmartTime Minimum Delay Analysis



# Changing Constraints and Observing Results - 32-Bit Shift Register Example

You can use SmartTime to adjust constraints and view the results in your design. To do so:

- 1. Open the SmartTime Constraints Editor (**Tools > Constraints Editor**).
  - The Constraints Editor displays the clock constraint at 800 MHz that you entered earlier, as shown in the figure below.

File Edit View Constrai			1000									-
l 🛃 🎦 💱 🏂 ᡬ traints Editor for scenario Primar		n i	<b>ia is</b> is in its in its is its it	2 1 1	s (3° %	) Au D						
Constraints     Requirements	*		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File
₹ Clock Generated Clock		1	Click here to add a	constraint								
Input Delay	ik E	2	7	my_clk	CLK	1,250	800.000	50.0000	rising 👻	0.000	0 0.625	GUI
Output Delay A Exceptions												
Max Delay												
Max Delay Min Delay												
Max Delay	J											
Max Delay Min Delay Multicycle	J											

Figure 21 · Clock Constraint Set to 800 MHz

- Select the second row. Right click on it and select Edit Clock Constraint. This will open the Edit Clock Constraint dialog box. Change the clock constraint from 800 MHz to 1000 MHz and click green check mark to continue.
- 3. From the View menu choose Recalculate All to recalculate the delays using your new clock constraint.
- 4. From the Tools menu choose Maximum Delay Analysis View to view the max delay analysis.
- 5. Expand **my\_clk** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the slacks decrease after you increase the frequency and recalculate. You may see the slacks go negative indicating Timing Violations. Negative slacks are shown in red.

Note: The actual timing numbers you see may be slightly different.



-	slay Analysis Ve					-												
AX	Analysis for Primary	r scenario				Pre	-					10 *						
	Summary					a	ustomize table								i.	Apply Filter	Store Filter	Reset Filter
	Regist	ter to Regi	ster			_				_					-		-	
	External S Clock to						Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	linimum Peri (ns)	bo	Skew (ns)		
		to Asynch Recovery	ronous			1	Q_HI[18:CIX	Q_Htt[19]40	0.726	0.091	4.810	4.729	0.288		91		0.077	2
	Asynchro	onous to P	legister			2	Q_Ht[25]-CLK	Q_int[26]:0	0.704	-0.086	4.809	4,723	0.298	1.4	186		0.084	
1	Pin to Pin Input to I				11	-	Q_HH[11]:CLK	Q_int[12]:0	0.688	-0.076	4,823	4,747	0.298	1.4	126		0.090	
	X User Sets	5				1												
						*	Q_Htt[\$]:CLK	Q_int[6]:0	0.712	-0.073	4.832	4.759	0.298	1.4	73		0.063	
						5	Q_int[7]:CLK	Q_int(8):0	0.706	-0.068	4,827	4.759	0.298	1.4	68		0.064	
						6	Q_int[19].CLK	Q_int[20]10	0.701	-0.031	4.777	4.746	0.298	- 14	31		0.032	
_					- 1	7	Q_H1[26]:CLK	Q_H1[27]:0	0.673	0.005	4.753	4,748	0.299	1.4	05		0.033	
						5	Q_int[30]:CLK	Q_nt[31]:0	0.587	0.043	4.695	4.738	6.299	0.4	67		0.071	
						9	Q_int[9]:CLK	Q_int[10]:0	0.576	0.048	4.711	4.759	0.298	0.5	152		0.078	
					111	10	Q_int[17]:CLK	Q_int[18]:0	0.577	0.052	4.684	4.736	0.298	0.9	940		0.073	
14	4		-		11	11	Q_int[12]:CLK	Q_int[13]:0	0.571	0.058	4.678	4.736	0.298	0.5	142		0.073	
					111		Q_HIT[2]:CUK	Q_H1(3):D	0.577	0.061	4.712	4,773	0.298	0.5	(79		0.064	
- 1				-	11		Q_mt[3]:CLK	Q_Ht[40	0.563	0.061	4.698	4.759	0.298	0.4	(39)		0.078	
					111	-		1							-		1	
	2				11	Nar	Summary		Туре	Net			Macr	0	p Delay	Total Fanos	it Edge	1
1	-				11		data required tim data arrival time	se .								4.719 4.810		
					1.11		slack									-0.091		
					1.11		Data_arrival_time_c	alculation							4.03			1
1					1.11		my_clk CLK		Clock source							0.000		
							CLK_ibut/00/U_J	OPAD PAD	net	CLK						0.000	-	
							CLK ibut/00/U 1		cell	550			ADUE	SOPAD IN +			21	
۰,							CLK_ibuf_RNIVQ		net	CLKjbu	KS					2.325	1	
1	-0.091 (	0	0.0045	0.1	0.195		CLK, but, RNIVQ		cell				ADUE				51	
		ock distrib					CLK and RNR/O	04/U0_RGB1_RGB0:Ar	n net	CIK ibut	RNI/Q04/U0_	YWin			0.687	3.117	1	

Figure 22 · Maximum Delay Analysis After Setting Clock Constraint to 1000 MHz

6. Close SmartTime. Click No when prompted to save changes.

### Tutorial 2 - Adding an \*.sdc File to Constrain Clock

This tutorial uses the 4-bit count16 example to step you through the process of entering constraints and analysing the timing performance of the design. Two options of entering clock constraints are covered: using SmartTime's Constraint Editor and importing an \*.sdc file into Libero SoC.

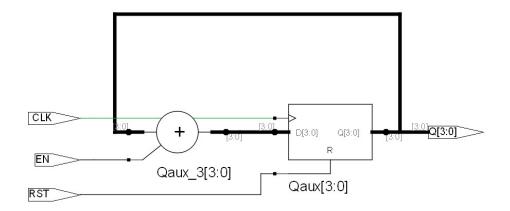


Figure 23 · Tutorial 2 – 4-bit Counter

- 1. From the Project menu, choose New Project to create a new Libero project.
- 2. Name the project **smarttime\_tutorial** and set the project location according to your preferences. Enter the following values for the new project:
- Family: SmartFusion2
- Die: M2S050



- Speed: STD
- Die Voltage: 1.2 V
- Package: 484 FBGA
- Range: COM
- 7. Click Finish to create the new project.
- Import the count16\_behave.v into your project (File > Import > HDL Source Files) from the folder where you have downloaded the tutorial files (link to tutorial files).
- 9. Double-click **Compile** in the Design Flow window to run both Synthesis and Compile with default settings.

Refer to the Compile and Layout help topics for more information.

You are ready to create your clock constraints.

### Creating a Clock Constraint

You may create a Clock Constraint in one of two ways:

- Option 1 Add Clock Constraint in the Constraint Editor
- Option 2 Import an \*.sdc file that contains the Clock Constraint

**Option 1 - Create a clock constraint in the Constraint Editor:** 

1. In the Design Flow window, expand Edit Constraints and right click on Timing Constraints > Open Interactively to start SmartTime and open the SmartTime Constraints Editor (as shown in the figure below).

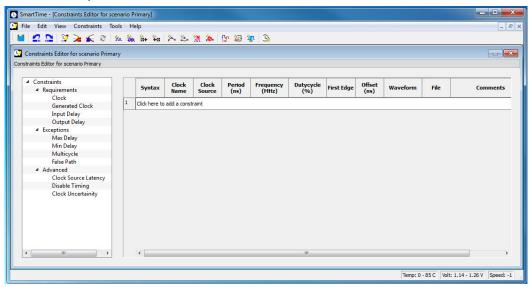


Figure 24 · SmartTime Constraints Editor

- 2. Add a clock constraint in one of the followng three ways:
- Click the New Clock Constraint icon
   in the SmartTime toolbar.
- Double-click Clock under Requirements in the Constraints Pane.
- Right-click Clock and choose Add Clock Constraint

The Create Clock Constraint dialog box appears (as shown below).



Create Clock Constraint			8	23
Clock Name :	Clock Source :		•	
Period :	ns	or Frequency:		Mhz
: <u>*</u>				
- Offset : Duty cycle :	I			
0.000 ns 50.0000 %				
Comment :				
Help		ОК	Cancel	

Figure 25 · Create Clock Constraint Dialog Box

- 3. Select the **CLK** pin from the pull-down menu in the **Clock Source** field, or click the **Browse** button to open the Select Source Pins for Clock Constraint dialog box, select the **CLK** pin and click **OK**.
- 4. Enter my\_clk under Clock Name. The name of the first clock source is provided as default.
- 5. Type 100 in the Period field of the Create Clock Constraint box and accept all other default values.
- 6. Click **OK** to close the dialog box.

The clock constraint appears in the SmartTime Constraints Editor.

SmartTime - [Constraints Editor fo File Edit View Constraints												— Θ Σ _ #
🐸 🙋 🎦 😏 🍝 e	1 - <b>%</b> n	🍇 🗱 🌠 🏅	5 🔈 🕅	10. [s	🧐 🛄	3						
nstraints Editor for scenario Primary												
Constraints			c1 1	<i>a</i> 1	n : 1	-						
A Requirements		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform		File
Clock					(	(****=)	50.0000		0.000		GUI	
Generated Clock	1	Click here to add a c	c				50.0000	rising 🔫				
Input Delay	2	<b>Y</b>	my_clk	CLK	100.000	10.000	50.0000	rising 👻	0.000	0 50	GUI	
Output Delay		1.										
A Exceptions												
Max Delay												
Min Delay												
Multicycle												
False Path												
<ul> <li>Advanced</li> </ul>												
Clock Source Latency												
Disable Timing												
Clock Uncertainity												
۰ III ا		•			m							Þ
										Temp: 0 - 85	i C Volt: 1.14 - 1.2	5 V Speed: STD

#### **Option 2 - Import a Timing Constraint \*.sdc File**

The SDC file contains a Clock Constraint of 10.0 ns for the CLK.

- 1. From the File menu choose Import > Timing Constraint (SDC) Files.
- 2. Navigate to the folder that contains the file count16.sdc that you have downloaded. Click to select it and click **Open**.
- 3. A pop-up dialog appears to ask if you want to organize the constraint files for your current root (count16) for (Compile). Click **Yes** to continue.
- 4. In the Libero SoC Files window, check that the count16.sdc file appears in the constraint directory.



C Libero - D:\2Work\G4_SmartTime_UG\count16\count16.prjx*				
Project File Edit View Design Tools Help				
Files & ×	Reports 🗗 🗙 StartPage	₽ × count16_behave.v* ₽ ×	count16.sdc 🗗 🗙	Ŧ
component     constraint     constraint     constraint     fp     fp     fo     designer     count16 behave.v     b     count16 behave.v     b     simulation     simatigen     simatigen     simatigen     synthesis     b     tooldata	¢ = 3	name (my_olk) -period 10 -	waveform (0 5) [get	ports (CLK)]
Desi Desig Stimulu Catalog Files HDL	< III			•
Log				₽×
🔳 Messages 😵 Errors 🗼 Warnings 🏮 Info				
The count16 project was created.				
Log Message Cores				
X X Find: Clock  Next Replace with: CLK Replace		Search in: Current Open Text Editor	Match case M	atch whole word 📄 Regular Expression
			Fam: Smar	tFusion2 Part: M2S050-FG484 Verilog

Figure 26  $\cdot$  count16.sdc under the Constraints folder in Files tab

### Adding an Input Delay Constraint

Add an input delay constraint for Inputs EN and RST in one of the following three ways:

- Click the Add Input Delay Constraint icon
- Double-click Input Delay under Requirement in the Constraint pane.
- In the Constraint pane, right-click Input Delay and choose Add Input Delay Constraint.

The Add Input Delay Constraint dialog box appears.



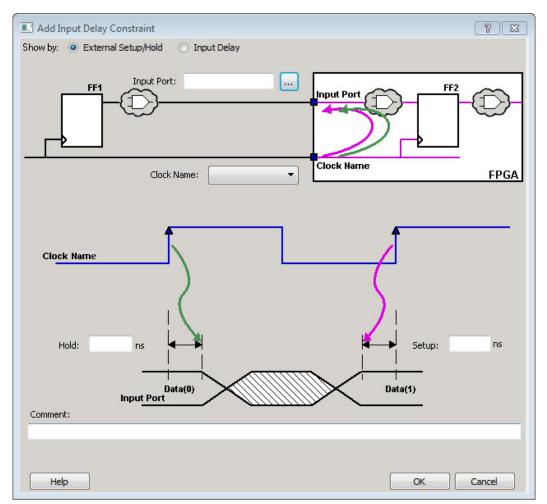


Figure 27 · Add Input Delay Constraint Dialog Box

- 1. In the Show by field, select External Setup/Hold.
- Click the Browse button in the Input Port field to select the ports for the external setup constraints. The Select Ports for Input Ports dialog box appears and displays the input ports in the design.

Available Pins: CLK EN RST	6	Add Add All Remove Remove All	Assigned Pins	
Filter available				 Help
Pin Type :	Input Ports			 ОК

Figure 28 · Select Ports for Input Delay Dialog Box

- 3. Select the ports **EN** and **RST**, and then click **Add** to move the pins from the **Available Pins** list to the **Assigned Pins** list. Click **OK** to close the Select Ports for Input Delay dialog box.
- 4. Enter the following values in the Set Input Delay Constraint dialog box:
  - Clock Name: Select my\_clk from the Clock Name drop-down list.
- Hold Delay: 1 ns
- Setup Delay: 8 ns
- 5. Add text in comment field if required for better readability.
- 6. Click **OK** to close the Set Input Delay Constraint dialog box.

The Input Delay constraints appear in the SmartTime Constraint Editor. Note that the Timing Constraints Editor View displays the external setup/hold requirement.

traints Editor for scenario Primary										
Constraints     A Requirements		Input Ports	Clock	Setup (ns)	Hold (ns)	Max Delay (ns)	Min Delay (ns)	Clock Edge	File	Comments
♥ Clock Generated Clock	1		-					rising -	GUI	
Tinput Delay	2	[get_ports { EN RST }]	my_cik 🗸	8.000	1.000			rising -	GUI	
Output Delay	-	Cardina Carrier 11		51000	11000					
<ul> <li>Exceptions</li> </ul>										
Max Delay										
Min Delay										
Multicycle										
False Path										
Advanced										
4 Advanced										
<ul> <li>Advanced</li> <li>Clock Source Latency</li> </ul>										

Figure 29 · SmartTime Constraints Editor with Input Delay Constraint Continue to add an output delay constraint.

### Adding an Output Delay Constraint

Add an output delay constraint in one of three ways:

• Click the Add Output Delay Constraint icon 🐜 in the SmartTime toolbar.

- Double-click Output Delay in the Requirement pane.
- Right-click Output Delay and choose Add Output Delay Constraint.

The Set Output Delay Constraint dialog box appears.

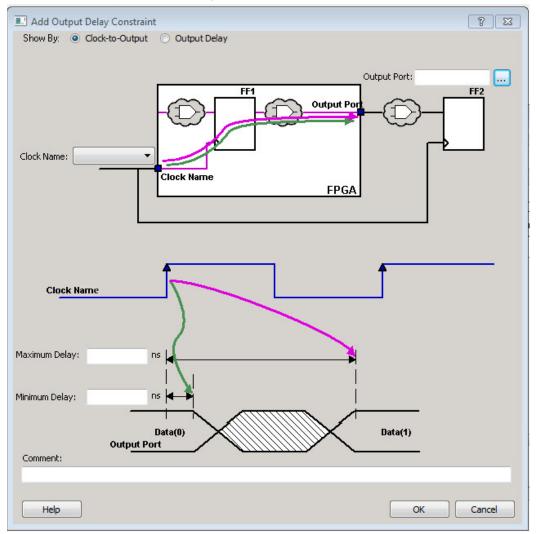


Figure 30 · Add Output Delay Constraint Dialog Box

- 1. In the Show by field, select Clock-to-Output.
- 2. Click the **Browse** button in the **Output Port** field to select the ports for the output delay constraint. The Select Ports for Output Delay dialog box appears and displays the output ports in the design.



vailable Pins:			
		Assigned Pins:	
Q Q[0] Q[1] Q[2] Q[3]		Add All	
		Remove	
		Remove All	
ilter available pir	ns :		Help
Pin Type :	Output Ports		• OK

Figure 31 · Select Ports for Output Delay Dialog Box

- 3. Click Add All to select all the output ports. SmartTime moves the output pins from the Available Pins list to the Assigned Pins list.
- 4. Click **OK** to close the Select Ports for Output Delay dialog box.
- 5. Click **OK** to close the Select Ports for Output Delay dialog box.
- 6. Select my\_clk from the Clock Name drop-down list in the Add Output Delay Constraint dialog
- 7. Enter 10 in the Maximum Delay field and 8 in the Minimum Delay field.
- 8. Add comments if required (optional)
- 9. Click **OK** to close the Set Output Delay Constraint dialog box. After the dialog box closes, the clk-toout delay constraints appear in the SmartTime Constraint Editor.

💌 🔼 🗊 🏊 🏑 4		ls Help	第 25 25 18 26 19 28	1 <b>%n</b>   D.						
aints Editor for scenario Primary				· • · •						
Constraints		Syntax	Output Ports	Clock	Clk To Out	Clk To Out	Max Delay	Min Delay	Clock	File
Requirements     Clock		- Junar	output to b	circu	Max(ns)	Min(ns)	(ns)	(ns)	Edge	
Generated Clock	1	Click here to							rising 👻	GUI
* Input Delay	2		[get_ports { Q Q[0] Q[1] Q[2] Q[3] }]	my_dk ▼	10.000	8.000			rising -	GUI
* Output Delay		<u>1</u>	b 5 ccurararan		22.00	20000			(	
Exceptions										
Max Delay										
Min Delay										
Multicycle										
False Path										
4 Advanced										
Clock Source Latence										
Disable Timing										
Disable Timing Clock Uncertainity										
Disable Timing Clock Uncertainity										

Figure 32 · SmartTime Constraints Editor with Output Delay Constraint

- 10. Click the Save icon in the SmartTime toolbar to save your constraints.
- 11. Exit (File -> Exit) the SmartTime tool.



### Place and Route Your Design

#### To run Place and Route:

- 1. Right-click Place and Route in the Design Flow window and choose Configure Options.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings. Click **OK** to close the Layout Options dialog box.
- 3. Right-click Place and Route and choose Run.

A green check mark appears next to Place and route when it completes successfully.

You are now ready to analyze your design.

### Analyzing the Maximum Operating Frequency

The Maximum Delay Analysis View indicates the maximum operating frequency for a design and displays any setup violations.

#### To perform the Maximum Delay Analysis:

Right-click Verify Timing and choose Open Interactively to open the Maximum Delay Analysis View.

Alternatively, you may click the Max Delay Analysis icon to open the SmartTime Maximum Delay Analysis View.

A green flag next to the name of the clock indicates there are no timing violations for that clock domain (as shown below).

The SmartTime Maximum Delay Analysis View displays the maximum operating frequency for a design and any setup violations.

Constrainter (Maximum Delay Analysis View)     File Edit View Tools Help     Constraints     Constraints     Analysis for scenario     MAX     Prany     Sommay     Sommay     Cosk to Register     Constraints     Const										
ile E	Analysis for scenario Primary     Constraint Original     Constraint Ori									-
Acalysis for scenario     MAX     Acalysis for scenario     Acad. filter     Acad. fi	2 🖸 😏 🍡 候 🕲 🛪									
Analysis View  Analysis for scenario Primary  Analysis for scenario Primary  Analysis for scenario Primary  Analysis for scenario Primary  Analysis for scenario Primary Prima	av Analysis View									
		_								
-	Analysis for any state									
<u>R</u>	Primary	svew  for scenario  for scenar		count16						
	Analysis for scenario Pennary      Clock to Dougle      Package      Temperature Range      Votage Range      Speed Grade      Design      Temperature Range      Votage Range      Speed Grade      Data source      Max Operating Condition      Max Operating Condition      Scenario for Timing Anal	SmartFu	ision2							
		Die		M2S050						
				484 EBC	4					
		anario  to Register  ter  ter  ter  ter  ter  ter  ter								
		Besign control of the second sec								
	y Analyns Vere Analyns for scenario Primary *** Register to Register Qaud, Offer ** External Setup ** Clock to Output Register to Asynchronous ** External Recovery Asynchronous to Register ** External Recovery Asynchronous to Register ** External Recovery Asynchronous to Register ** External Recovery Asynchronous to Register ** User Sets ** User Sets ** Qaud, filter				26 V					
	elay Analysis View Analysis for scenario Primary Summary  Case of the scenario Primary  Case of filter  Earnal Setup  Clock to Output Register to Asynchronous  Earnal Recovery Asynchronous to Register  Spin to filt Input to Output  Spin to Output  Cust Set S  Quad_filter  Quad_filter  Quad_filter	Speed Grad	e	STD						
	Delay Analysis View Analysis for scenario Premary 3 Summary 4 * Offine, Caudo Enter Quado Enter Quado Enter Quado Enter Caudo Duput Pegister to Asynchronous * Detranal Recovery Asynchronous to Register * Sprint Pin Input to Output * Cluck to Output * Starta Starts * Quad, Enter * Quad, Enter * Quad, Enter	Design Stat	e	Post-Lay	out					
-		Data source		Producti	on					
4	User Sets	Min Operation	ng Condition	BEST -	1.26 V - 0 C					
		Max Operat	ing Condition	s WORST	- 1.14 V - 85 C					
	Constant Constan									
	- Quas_ma	Contanto Ior	Titling Anal	yolo I minary						
	Select a set of paths to see	_	Period	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Ou (ns)
	its slack distribution.	my_clk	1.983	504.286	100.000	10.000	1.384	0.253	3.788	7.517
							1000			
			Min De	ay (ns) Max	Delay (ns)					
		Input to Out	put N/A	N/A						
	slack distribution(ns)									
		-								
_	X									
	63								Temp: 0 - 85 C Volt:	1.14 - 1.20 V Speed:

Figure 33 · SmartTime Maximum Delay Analysis View Summary

The Summary in the Maximum Delay Analysis View displays the maximum operating frequency for the design, the required frequency if any, the external setup and hold requirements, and the maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 504 MHz.

You can now View Register-to-Register paths as part of the Maximum Delay Analysis.

#### See Also

Analyzing Your Design

### Viewing Register-to-Register Paths

#### To view register to register paths:

- 1. Expand my\_clk domain in the Domain Browser and display the Register to Register, External Setup, and Clock to output path sets.
- Click Register to Register to display the register to register paths in the Paths List. It displays a list of register-to-register paths at the top of the Path List and detailed timing analysis for the selected path in the Path Details. Note that all the slack values are positive, indicating that no setup time violations exist.

n Delay Analysis View													
Analysis for scenario AX	Fre	m *				то	-						
Summary ▲ ✓ my_clk	0	ustomize table							Apply Fi	ter	Store Filter	Reset Filt	ter
Register to Register     External Setup     Clock to Output		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns) Mi	nimum Period (ns)		Skew (n	s)	
Register to Asynchronous		Qaux[0]:CLK	Qaux[3]:D	1.619	98.017	5.629	103.646	0.298	1.983			0.066	
✓ External Recovery												0.000	
Asynchronous to Register	2	Qaux[2]:CLK	Qaux[3]:D	1.213	98.433	5.213	103.646	0.298	1.567	1		0.056	
Pin to Pin													
District User Sets	3	Qaux[0]:CLK	Qaux[2]:D	1.145	98.491	5.155	103.646	0.298	1.509			0.066	
	4	Qaux[0]:CLK	Qaux[1]:D	1.059	98.587	5.069	103.656	0.298	1.413	1		0.056	
	5	Qaux[1]:CLK	Qaux[1]:D	0.900	98,745	4,911	103.656	0.298	1.255			0.057	
	1	Sanv[1].cer	Same 1-110	0.000	30.713		100.000	0.200	112.00			0.005	
	6	Qaux[3]:CLK	Qaux[3]:D	0.856	98.790	4.856	103.646	0.298	1.210			0.056	
	7	Qaux[1]:CLK	Qaux[2]:D	0.765	98.870	4.776	103.646	0.298	1.130			0.067	
	8	Qaux[1]:CLK	Qaux[3]:D	0.765	98.870	4.776	103.646	0.298	1.130	1		0.067	
	Na	me		Type	Net			Macro	On	Delay	Total F	anout Edge	
10	4	Summary								,			
		data required tim	ie								103.646		
8		data arrival time							-		5.629		-
		slack									98.017		
6	-	Data_arrival_time_c	alculation							0.000	0.000		
		my_clk CLK		Clock source						0.000	0.000		
4		CLK ibuf/U0/U I	OPAD-PAD	net	CLK					0.000	0.000	r	
		CLK_ibuf/U0/U_I		cell	CEN			ADLIB-1	OPAD IN +	2.128	2.128	2 1	
2		CLK_ibuf_RNIVQ0		net	CLK_ibut			Più Liui	+	0.352	2,480	f	
		CLK ibuf RNIVQ0		cell				ADLIB:0	SBM +	0.105	2.585	2 f	
0			04/U0 RGB1 RGB0:An		CLK ibut	RNIVQ04/U0	YWn		+	0.507	3.092	f	
97.529 98.017 98.505 98.993 99.48			04/U0_RGB1_RGB0:YL					ADLIB:F	RGB +	0.372	3.464	1 r	
slack distribution(ns)		Qaud01:CLK		net	CLK ibut	RNIVO04/U0	RGR1 RGR0 ra			0.546			

Figure 34 · SmartTime Register to Register Paths List

3. Double-click a path row to open the Expanded Path View (see figure below). The top of the view shows a calculation of the required and arrival times. A schematic of the path is shown at the bottom of the view.



mmary for path m::Qaux[0];CLK Qaux[3]:D ata Required Time (ns) Data Arriva 13.646 5.629	l Time (ns) Slack (ns) 98.017							Path Profile	5
ame	Туре	Net	Macro	Op	Delay	Total	Fanout Edge		
Data arrival time calculation									
my_clk					0.000	0.000			
CLK	Clock source			+	0.000	0.000	r		
CLK_ibuf/U0/U_IOPAD:PAD	net	CLK		+	0.000	0.000			
CLK ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	2.128	2.128	2 1		
CLK_ibuf_RNIVQ04:An	net	CLK ibuf		+	0.352	2.480	4		
CLK_ibuf_RNIVQ04:YWn	cell		ADLIB:GBM		0.105	2.585	2 f		
CLK_ibuf_RNIVQ04/U0_RGB1_RC		CLK ibuf RNIVQ04/U0 YWn	ALD COM		0.507	3.092	1		
CLK_ibuf_RNIVQ04/U0_RGB1_RC		CEN_IDDI_NINVQ04/00_TWN	ADLIB:RGB	-	0.372	3.464	1 1		
Qaux[0]:CLK		CLK_ibuf_RNIVQ04/U0_RGB1_RGB0_rgbl_net_1	ADLIDINGB	-	0.546	4.010			
	net	CEN_IDUI_KINIVQU4/UU_KOB1_KOB0_rgb1_net_1	ADUBCLE	*	0.540	4.010	5 r		
Qaux[0]:Q	cell	0 101	ADLIB:SLE	+		4.112	21		
Qaux_3_1.CO0:A	net	Q_c[0]		+	0.659		, r		
Qaux_3_1.CO0:Y	cell		ADLIB:CFG2	+	0.088	4.859	1 r		
Qaux_3_1.SUM[3]:B	net	Qaux_3_1_CO0		+	0.496	5.355			
Qaux_3_1.SUM[3]:Y	cell		ADLIB:CFG4	+	0.186	5.541	1 r		
Qaux[3]:D	net	Qaux_3[3]		+	0.088	5.629	r		
data arrival time						5.629			
	J <u>o/U_</u> IOPAD C Y	GBM CLK_lbuf_RNIVQ04/L An	YR	ADn	ux[0] Q		Qaux_3_1.CO0 A y B CFG2	CLK,buf,RNNQQQ4(U0,RG81) Qaux[3] Hon Rc	_

Figure 35 · SmartTime Expanded Paths View

- Tip: Left-click and drag the mouse to zoom in or out in the schematic window.
- 4. Close the Expanded Paths View.

### Viewing External Setup Paths

To view External Setup paths, click **External Setup** in the Domain Browser to display the external setup timing (as shown below). Note that the slack is positive in the tutorial example, indicating there are no timing violations.

mum Delay Analysis View	-													-
Analysis for scenario toming_analysis	From *							TO *						
의 Summary 응 →평 my_clk	Customize table											Apply Filter	Store Filter	Fiter
Register to Register     Sectoring Comment     Cock to Output	Source Pi	n Sink Pir	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	External Setup (ns)						
Register to Asynchronous	1 EN	Qaue(3) D	5.307	90.051	13.397	193.358	0.298	1.949						
<ul> <li>SC Pin to Pin Input to Output</li> </ul>	2 EN	Qaux(0):D	5.134	90.212	13,134	103.346	0.298	1.788						
X User Sets	3 EN	Qaux[2]:D	4.660	90.681	12.660	103.341	0.298	1 319						
	a. 1741	00 101.D		00.336	43,643	143.333		1.344						
	Name		Туре		Net				Macro	Op Dela	y Total	Fanout Edge		
4	Summary data required data arrival ti slack										103.35 13.30 90.05	7		
	Data_arrival_tit	ne_calculation										-		
3	my_clk EN		Inout Delay	Constania							000 0.00	0		
	EN Ibut/U0/U	IOPAD PAD	net	Constraint	EN.						000 8.00			
	EN_ibut/U0/U		cell						ADLIB:IOPAD_IN		993 10.99			
	EN_But/U0/U		net		EN_but	U0/11N1					000 10.99			
2	EN_but/U0/U Oaux 3 1.00		cell		ENC				ADLIB.IOINFF_BIFASS	* 0	106 11.09			
	Qitua 3 1.00		cell		EN,C				ADUB-CFG2		102 11.80			
	Qaux 3 1.50	MIST-B	net		Oaux 3	1 000			HOUSERER	+ 0	262 12.06	4 /		
	Qeux 3 1.SU	MOLY	cell						ADLIB:CFG4		173 12.23			
1	Qiiux[3].D		net		Qaux 3	3)				+ 1	070 13.30	7 1		
	data arrival ti	me									13.30	7		
		time_calculation	3.50.00070							1000				
0	my_ck CLK		Clock Constr Clock source								000 100 00			
89.7185 90.051 90.3835 90.716 91.0	CLK BURDON	L LODAD BAD	net		CLK						000 100.00			

Figure 36 · SmartTime External Setup Path List



### Viewing Clock-to-Output Paths

To view Clock-to-output paths, click **Clock to Output** in the Domain Browser to display the register to output timing. Again, the slack is positive in the tutorial example, indicating there are no timing violations.

Source Pin         Sink Pin         Delay         Sink Pin         Other Pin         Class of the Pin <thclass of="" pin<="" th="" the=""></thclass>	r Reset filter
Spinnery         Customize table         Customize table         Apply filter         Store Fill           4 Spinnery              • Register to Register • Extend Store • Extend Store • Extend Store • Extend Store • Cover(s) table               Source Pin • Sink Pin • Cover(s) •	r Reset Filter
✓ Register to Register               Source Pin          Delay          Stack          Arrival          Register          Source            > Cotext to CAput          > Cotext to CAput          (ns)	
Count to Dudpid         Source Prin	
Cstemal Recovery     1 Quox(0) CLK Q(0) 4.451 81.471 8.529 90.000 8.529     Anynchronous to Register     Z Dawa(3) CLK Q(3) 3.369 82.570 7.430 90.000 7.430	
Z Pin to Pin 2 Oauxi31:CLK 0(3) 3.369 82.570 7.430 90.000 7.430	
mput to cutput 2 Wurd Sets 3 Qaux[1]:CLK Q[1] 3.370 82.596 7.404 90.000 7.404	
4 Qaux[2]:CLK Q[2] 3.322 82.635 7.365 90.000 7.365	
Name         Type         Net         Macro         Op         Delay         Table         Fanout         Edge           2         Sammary         diat required time         90.000         diat annual time         90.000         diat annual time         90.000         diat annual time         90.000         diat annual time         0.000         diatanual time         0.000<	
Data arrival time calculation	
B Data arrival time calculation         0.000         0.000           -my_cfk         0.000         0.000         r           -CK         Clock source         +         0.000         r	

Figure 37 · SmartTime Clock to Output Paths List

### Using Filters and Creating Analysis Sets

Filters can be used and saved to display analysis sets in the Maximum Delay Analysis window and the Minimum Delay Analysis window.

#### To create a filter:

- 1. When the Place and Route step is complete, click Verify Timing > Open Interactively.
- 2. In the Maximum Delay Analysis View, select the Register to Register path. Enter the following in the Filter fields (as shown in the figure below), then click **Apply Filter**:

From: Qaux[0]:CLK To: \*:D



mum (	n Delay Analysis View														
~															
MA	Analysis for scenario Primary	Fr	om Qaux[0]:CLK				то	*:D							
	& Summary	6	ustomize table							Apply	Filter	Stor	e Filter	Reset Filte	er
	4 √(1) my clk														_
	<ul> <li>Register to Register</li> </ul>						in an an an	Required		Minimum P	horized				Т
	✓ External Setup		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	(ns)	Setup (ns)	(ns)	enou		Skew	(ns)	
	✓ Clock to Output		Qaux[0]:CLK	Qaux[3]:D	1.619	8.017	5.629	13.646	0.298		1.983			0.06	56
	Register to Asynchronous														~
	✓ External Recovery Asynchronous to Register	2	Qaux[0]:CLK	Qaux[2]:D	1.145	8.491	5.155	13.646	0.298	1	1.509			0.06	56
	4 55 Pin to Pin														
	Input to Output	3	Qaux[0]:CLK	Qaux[1]:D	1.059	8.587	5.069	13.656	0.298		1.413			0.05	56
	5 User Sets				-										_
		4	Qaux[0]:CLK	Qaux[0]:D	0.743	8.904	4.753	13.657	0.298		1.096			0.05	55
-			ime		Туре	Net			Ма	cro	Op I	Delay	Total F	anout Edge	e
	10		ime Summary		Туре	Net			Ma	cro	Op I	Delay	Total F	anout Edge	e
	10		Summary data required tin		Туре	Net			Ma	cro	Op I		13.646	anout Edge	e
	10		Summary data required tin data arrival time		Туре	Net			Ma	cro	Op I		13.646 5.629	anout Edge	e
	8	*	Summary data required tin data arrival time slack		Туре	Net			Ma	cro	Op 1		13.646	anout Edge	e
		*	Summary data required tin data arrival time slack Data_arrival_time_c		Туре	Net			Ma	cro			13.646 5.629 8.017	anout Edge	e
		*	Summary data required tin data arrival time slack Data_arrival_time_o my_clk			Net			Ма	cro		0.000	13.646 5.629 8.017 0.000		e -
	8	*	Summary data required tim data arrival time slack Data_arrival_time_c my_clk CLK	alculation	Clock source		_		Ма	cro		0.000	13.646 5.629 8.017 0.000 0.000	r	e
		*	Summary data required tim data arrival time slack Data_arrival_time_c my_clk CLK CLK_ibuf/U0/U_1	calculation		Net					•	0.000 0.000 0.000	13.646 5.629 8.017 0.000		e
	8	*	Summary data required tim data arrival time slack Data_arrival_time_c my_clk CLK	OPAD:PAD OPAD:Y	Clock source net		f			cro LIB:IOPAD_IN	- + +	0.000 0.000 0.000 2.128	13.646 5.629 8.017 0.000 0.000 0.000	r	e
	6	*	Summary data required tim data arrival time slack Data_arrival_time_o my_clk CLK CLK_ibuf/U0/U_J CLK_ibuf/U0/U_J	OPAD:PAD OPAD:Y OPAD:Y 04:An	Clock source net cell	CLK CLK_ibut			AD		- + + + + +	0.000 0.000 2.128 0.352 0.105	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585	r r 2 r f 2 f	e :
	8	*	Summary data required time data arrival time_c my_clk CLK CLK_ibuf/U0/U_J CLK_ibuf/U0/U_J CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ	alculation OPAD:PAD OPAD:Y 04:An 04:Wn 04/Wu_RGB1_RGB0:An	Clock source net cell net cell net	CLK CLK_ibut	f f_RNIVQ04/U0_	YWn	AD AD	LIB:IOPAD_IN LIB:GBM	- + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092	r 2 r f 2 f f	e
or paths	6	*	Summary data required tin data arrival time slack Data_arrival_time_c my_clk CLK_ibuf/V0/VJJ CLK_ibuf/V0/VJ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ	OPAD:PAD OPAD:PAD OPAD:Y 04:An 04:YWn	Clock source net cell net cell net cell	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0_		AD AD AD	LIB:IOPAD_IN	- + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464	r 2 r f 2 f f 1 r	e
or parties	6	*	Summary data required tin data arrival time slack Data_arrival_time_c my_cik CLK_ibud/U0/UJ CLK_ibud/U0/UJ CLK_ibud_RNIVQ CLK_ibud_RNIVQ CLK_ibud_RNIVQ Qax(0):CLK	alculation OPAD:PAD OPAD:Y 04:An 04:Wn 04/Wu_RGB1_RGB0:An	Clock source net cell net cell net cell net	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0_	YWn RGB1_RGB0_rgt	AD AD al_net_1	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372 0.374	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010	r r 2 r f 2 f f 1 r	e
# of paths	6	*	Summary data required tin data arrival time, c slack Data, arrival, time, c my, clik CLK, ibud, FNIVQ CLK, ibud, FNIVQ CLK, ibud, FNIVQ CLK, ibud, FNIVQ Qaux(0):CLK	alculation OPAD:PAD OPAD:Y 04:An 04:Wn 04:Wu 04:VU0_RGB1_RGB0:An 04/U0_RGB1_RGB0:YL	Clock source net cell net cell net cell net cell	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0_		AD AD al_net_1	LIB:IOPAD_IN LIB:GBM	- + + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372 0.546 0.102	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010 4.112	r r 2 r f 2 f f 1 r r 5 r	e
# of paths	8 6 4	*	Summary data required tin data arrival time dack my_cfk CLK CLK bd//J00/JJ CLK,bbd//J00/JJ CLK,bbd//J00/JJ CLK,bbd//RNIQ CLK,bbd/RNIQ CLK,bbd/RNIQ Qau(0):CLK Qau(0):Q Qau(0):CLK Qau(0):Q Qau(3):CLK	alculation OPAD:PAD OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:Y OPAD:PAD OPAD:PAD OPAD:PAD OPAD:PAD OPAD:PAD OPAD:Y	Clock source net cell net cell net cell net cell net	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0_		AD AD I_net_1 AD	LIB:IOPAD_IN LIB:GBM LIB:RGB LIB:SLE	- + + + + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372 0.546 0.102 0.659	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010 4.112 4.771	r r 2 f f 2 f f 1 r 5 r r	e -
# of paths	8 6 4	*	Summary data required tin data arrival time data arrival time data my, cik CLK, bud/VU0/UJ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ Qaux(0):CLK Qaux(0):QD Qaux(3).COB/Y	alculation OPAD:PAD OPAD:Y 04:An 04:VU0_RGB1_RGB0:An 04/VU0_RGB1_RGB0:YL	Clock source net cell net cell net cell net cell net cell et	CLK CLK_ibut CLK_ibut CLK_ibut Q_c[0]	f_RNIVQ04/U0_ f_RNIVQ04/U0_		AD AD I_net_1 AD	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + + + + + + + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372 0.546 0.102 0.659 0.088	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010 4.112	r r 2 r f 2 f f 1 r r 5 r r 1 r	e .
# of paths		*	Summary data required tim data arrival time c Data_arrival_time_c my_cik CLK Data_arrival_time_c CLK_ibid_NUVJ CLK_ibid_RNIVQ CLK_ibid_RNIVQ CLK_ibid_RNIVQ CLK_ibid_RNIVQ CLK_ibid_RNIVQ Qatu[0]:CLK CLK Qatu[0]:CLK CLK CLK CLK CLK CLK CLK CLK CLK CLK	alculation OPAD:PAD OPAD:Y O4:An 04:7VWn 04:7VWn 04:7VW, RGB1_RGB0:An 04:7VW, RGB1_RGB0:YL	Clock source net cell net cell net cell net cell net	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0_ f_RNIVQ04/U0_		AD AD J_net_1 AD AD	LIB:IOPAD_IN LIB:GBM LIB:RGB LIB:SLE	- + + + + + + + + + + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.507 0.372 0.546 0.102 0.659 0.088 0.496	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010 4.112 4.771 4.859	r r 2 f f 2 f f 1 r 5 r r	e
# of paths	8	*	Summary data required tin data arrival time data arrival time data my, cik CLK, bud/VU0/UJ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ CLK, ibud/RNIVQ Qaux(0):CLK Qaux(0):QD Qaux(3).COB/Y	alculation OPAD:PAD OPAD:Y O4:An 04:7VWn 04:7VWn 04:7VW, RGB1_RGB0:An 04:7VW, RGB1_RGB0:YL	Clock source net cell net cell net cell net cell net cell net	CLK CLK_ibut CLK_ibut CLK_ibut Q_c[0]	f_RNIVQ04/U0_ f_RNIVQ04/U0_ 1_CO0		AD AD J_net_1 AD AD	LIB:JOPAD_IN LIB:GBM LIB:RGB LIB:SLE LIB:CFG2	- + + + + + + + + + + + + + + + + + +	0.000 0.000 2.128 0.352 0.105 0.505 0.546 0.102 0.659 0.659 0.088 0.496 0.186	13.646 5.629 8.017 0.000 0.000 2.128 2.480 2.585 3.092 3.464 4.010 4.112 4.771 4.859 5.355	r r 2 r f 2 f f 1 r r 5 r r r r r	e

Figure 38 · Applying a Filter in the Maximum Delay Analysis View

3. Click **Store Filter** to save the filter. Enter **Qaux0\_filter** in the Name field of the Create Filter Set dialog box. The set will be visible in the Maximum Delay Analysis View under Register to Register, as shown in the figure below.

n Delay Analy		S 2															
n Delay Analy			100 ×														
_	sis View																
				_													
2				- I.													
Analysis for scenario						From * TO *											
AX Prina	,				Fre	om -					10 -						
🕅 Summa	rv			A	a	ustomize table								oply Filte	Store	Filter R	Reset Filter
⊿ √@ m					_												
▲ ✓ Register to Register									Required		Minimum Period						
Qaux0_filter ✓ External Setup				Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	(ns)		Skew (ns	)			
				Qaux[0]:CLK	Qaux[3]:D	1.619	8.017	5.629	13.646	0.298	1.983	0.0		0.066			
✓ Clock to Output			1											0.000			
Register to Asynchronous			2	Qaux[0]:CLK	Qaux[2]:D	1.145	8,491	5.155	13.646	0.298	1.509			0.066			
✓ External Recovery			1	donifolioni	donufatio												
Ana	chronour to	Desirter			3	Qaux[0]:CLK	Qaux[1]:D	1.059	8.587	5.069	13.656	0.298	1.413	1		0.056	
					4	Qaux[0]:CLK	Qaux[0]:D	0.743	8.904	4.753	13.657	0.298	1.096			0.055	
4																	
3			_	- II													
				1.11	-									_			
1					Na	me		Туре	Net			Mag	ro Op	Delay 1	Total Fand	ut Edge	
2					4 Summary												_
						data required ti									13.646		
1				- U		data arrival tim	e								5.629		
					slack										8.017		
						Data_arrival_time_calculation											
0		8,4605				my_clk									0.000		
7.5735	8.017	8.4605	8.904	9.347		CLK		Clock source					+	0.000		r	
slack distribution(ns)					CLK_ibuf/U0/U_IOPAD:PAD			net	CLK				+	0.000	0.000	r	

Figure 39 · Qaux0\_filter Path Set

- 4. Click Reset Filter.
- 5. Right-click Register to Register and choose Add Set to open the Add Path Analysis Dialog box.



Add Path Analysis Set	?
Name :-   Source pins:	Trace from :-      Source to sink      Sink to source     Sink Pins:
Qaux[0]:CLK Qaux[1]:CLK Qaux[2]:CLK Qaux[3]:CLK	
Select All Filter source pins: Pin Type: Registers by pin names * Filter	Select All       Filter sink pins:       Pin Type:       Registers by pin names       *       Filter
Help	OK Cancel

Figure 40 · Add Path Analysis Set Dialog Box

6. Use the values in the table below to add timing path sets.

From	То	Name
Qaux[1]:CLK	*:D	Qaux1_filter
Qaux[2]:CLK	*:D	Qaux2_filter
Qaux[3]:CLK	*:D	Qaux3_filter

The path sets appear under User Sets in the Maximum Delay Analysis View, as shown in the figure below.



6	Summary	
4	✓ my_clk	
	<ul> <li>Register to Register</li> </ul>	
	✓ Qaux0_filter	
	<ul> <li>External Setup</li> </ul>	
	<ul> <li>Clock to Output</li> </ul>	
	Register to Asynchronous	
	<ul> <li>External Recovery</li> </ul>	
	Asynchronous to Register	
4	🔁 Pin to Pin	
	Input to Output	
4	🔁 User Sets	
	✓ Qaux1_filter	
	Qaux2_filter	
	Qaux3_filter	

7. Close SmartTime and Libero SoC.

# Tutorial 3 - Design Using Both Clock Edges

This tutorial example analyzes SmartTime reports that include both rising and falling edges of a clock in the same design. The design (see the figure below) consists of a 16-bit serial-in parallel-out (SIPO) shift register. The shift register tmp1 is clocked on the rising edge of the clock. The output register tmp2 is clocked on the falling edge of the clock.

You will import the RTL verilog file shiftreg16.v and enter a clock constraint of 100 MHz. After routing the design, you will analyze the timing to determine the maximum operating frequency and export a timing report.



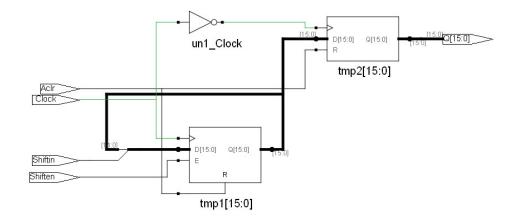


Figure 41 · Example Design that Uses Both Clock Edges

### Set Up Your Example Design Project

- 1. Open Libero and create a new project (from the Project menu choose New Project).
- 2. Name the project shiftreg16 and set the project location according to your preferences. Enter the following values for your new project:
- Family: SmartFusion2
- Die: M2S090TS
- Package: FG 484
- Speed: STD
- Die Voltage: 1.2 V
- Range: COM
- 3. Click Finish to create the project.

# Import the Verilog Source File - Design Uses Both Clock Edges

You must import the shiftreg16.v Verilog file into your design for this tutorial. Download the design files from the Microsemi website (URL to location of tutorial files).

#### To import the Verilog source file:

- 1. From the File menu, choose Import > HDL Source Files.
- 2. Browse to the location of the shiftreg16.v file you have downloaded and select it. Click **Open** to import the file.
- 3. Verify that the file appears in your project, as shown in the figure below.



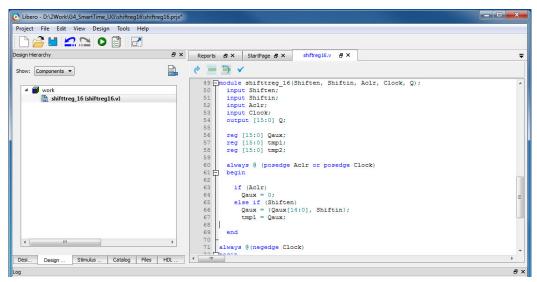


Figure 42 · shiftereg.v in the Design Hierarchy

# Add a Clock Constraint - Design Uses Both Clock Edges

To add a clock constraint to your example design:

1. In the Design Flow window, expand Edit Constraint and choose Timing Constraints > Open Interactively.

This triggers the synthesis and compile steps to run.

The SmartTime Constraints Editor opens when the compile step is completed.

- 2. In the Constraints pane, right-click Requirements > Clock and choose Add clock constraint.
- 3. Enter a constraint with Clock Source (Clock), Clock Name (my\_clk) of 100 MHz at a 50% duty cycle.

Create Clock Constraint			8 23
Clock Name : my_clk	Clock Source :	Clock	•
Period : 10	ns	or Frequency:	100 Mhz
← Offset : → ← Duty cycle : → ← 0.000 ns 50.0000 %			
Comment :			
Help		OK	Cancel

Figure 43 · Add 100 MHz Clock Constraint

The new constraint appears in the Constraints Editor, as shown in the figure below.



			Primary]									
ile Edit View Constraint	s To	pols	Help									-
🛛 🕰 😫 😏 🏹 🖌	0	m 1	in in in in	25 19 2	. Cr %	a 💁 🖪						
raints Editor for scenario Primary												
Constraints				Clock	Clock	Period	Frequency	Dutycycle		Offset		
A Requirements			Syntax	Name	Source	(ns)	(MHz)	(%)	First Edge	(ns)	Waveform	File
* Clock		1	-			100.00	2.177.2					
Generated Clock		1	Click here to add a	constraint								
Input Delay		2	1 m	my_clk	Clock	10.000	100.000	50.0000	rising 👻	0.000	0 5	GUI
Output Delay												
<ul> <li>Exceptions</li> </ul>	=											
Max Delay												
Min Delay												
Multicycle												
False Path												
<ul> <li>Advanced</li> </ul>												
Clock Source Latence	3											
Disable Timing	-											
			•				m					
	_											

100 MHz Clock Constraint in the Constraint Editor

- 4. Save the constraints (File > Save).
- 5. Exit SmartTime Constraints Editor (File > Exit).

# Run Place and Route for a Design that Uses Both Clock Edges

#### To run Place and Route on the design 'shiftreg\_16':

- 1. In the Design Flow window, click **Place and Route** and choose **Configure Options**.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings. Click **OK** to exit the Layout Options Dialog box.
- 3. Right-click Place and Route and choose Run.

A green check mark appears next to Place and Route to indicate successful completion of Place and Route.

# Maximum Delay Analysis - Design Using Both Clock Edges

The SmartTime Maximum Delay Analysis window displays the design's maximum operating frequency and lists any setup violations.

#### To perform Maximum Delay Analysis:

1. In the Design Flow window, click **Verify Timing > Open Interactively** to open SmartTime. The Maximum Delay Analysis View window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.



SmartTime - [Maximum Delay Analysis View]									
File Edit View Tools Help									-
해 요구 있는 것가 않는 것이 600 또 The	Design			nifttreg 16					
MAX	Family			martFusion2					
Summary	Die		-	2S090TS					
<ul> <li>✓ my_clk</li> <li>✓ Register to Register</li> </ul>				2509015 34 FBGA					
External Setup	Package								
Clock to Output	Temperatu			- 85 C					
Register to Asynchronous External Recovery	Voltage Ra	•		14 - 1.26 V					
Asynchronous to Register		Speed Grade		TD					
Fin to Pin     Input to Output	Design Sta	Design State		ost-Layout					
St User Sets	Data source	Data source		roduction					
	Min Operating Conditions		ditions B	EST - 1.26 V - 0 C					
	Max Opera	ting Con	ditions M	/ORST - 1.14 V - 8	5 C				
	Scenario f	or Timing	Analysis P	rimary					
	Clock		Frequency (MHz)	y Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)
Select a set of paths to see	my_clk	1.980	505.051	10.000	100.000	5.457	0.955	4.311	9.127
its slack distribution.		Mi	n Delay (ns)	Max Delay (ns)			1	1	
slack distribution(ns)	Input to Ou	itput N//	Ą	N/A					
v							Ter	mp: 0 - 85 C Volt: 1.	14 - 1 26 V Speed:

Figure 44 · Maximum Delay Analysis for Design Shifter

The Summary in the Maximum Delay Analysis View window indicates the maximum operating frequency for this design is 505.05 MHz.

- 2. Expand my\_clk to display the Register to Register, External Setup and Clock to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.
- 4. Click to select row 1 and study the timing analysis (resize the Maximum Delay Analysis View window as required). The path is from register tmp1 to register tmp2. Note that SmartTime uses 5 ns in the data required calculation (circled in red in the figure below). This is because the source flip flop uses the rising edge of the clock and the destination flip-flop uses the falling edge of the clock.

n Delay Analysis View												
Analysis for scenario Primary		From =				то	•					
Summary		Customize table							Apply Filter	Store Filter	Reset Filter	2
⊿ √@ my_clk	11 .								(			-
<ul> <li>Register to Register</li> </ul>		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required	Setup (ns)	Minimum Period	<i>a i</i>		
External Setup		Source Pin	SINK PIN	Delay (ns)	Slack (ns)	Arrival (ns)	(ns)	Setup (ns)	(ns)	Skew (r	5)	
Clock to Output Register to Asynchronous		tmp1[8]:CLK	tmp2[8]:D	0.574	4.159	5.554	9.713	0.298	1.682		-0.031	-
External Recovery												
Asynchronous to Register		tmp1[0]:CLK	tmp2[0]:D	0.574	4.160	5.553	9.713	0.298	1.680		-0.032	
4 35 Pin to Pin		tmp1[10]:CLK	tmp2[10]:D	0.562	4,170	5,543	9,713	0.298	1.660		-0.030	
Input to Output		timp1[10]:CLK	tmp2[10]:D	0.562	4.1/0	5.543	9.713	0.298	1.660		-0.030	
🗮 User Sets	1	tmp1[2]:CLK	tmp2[2]:D	0.573	4.172	5.552	9.724	0.298	1.656		-0.043	
		tmp1[9]:CLK	tmp2[9]:D	0.571	4.172	5.552	9.724	0.298	1.656		-0.041	
		Name		Туре	Net			N	1acro Op	Delay Total	Fanout Edg	
		Clock_ibuf_RNIH	ISID/U0_RGB1_RGB0	An net	Clock	ibuf_RNIHSID/U	0_YWn		+	0.714 3.984	f	
			ISID/U0_RGB1_RGB0	:YL cell					DLIB:RGB +	0.372 4.356	12 r	
		tmp1[8]:CLK		net	Clock	ibuf_RNIHSID/U	0_RGB1_RGB0		+	0.624 4.980	r	
		tmp1[8]:Q tmp2[8]:D		cell	tmp1[8	1		A	DLIB:SLE +	0.102 5.082 0.472 5.554	2 r	(T
20		data arrival time		net	tmp1[a	u			•	5.554	,	
16		4 Data required time								5.554		
12		my_clk		Clock Const	raint					5.000 5.000	>	u
8		Clock		Clock sourc					+	0.000 5.000	f	
		Clock_ibuf/U0/U	IOPAD:PAD	net	Clock				-	0.000 5.000	f	
1.696 4.159 6.622 9.085 1	.54	Clock_ibuf/U0/U	IOPAD:Y	cell				A	DLIB:IOPAD_IN +	2.993 7.993	2 f	*
slack distribution(ns)		(				.111						

Figure 45 · Slack Calculation in Maximum Delay Analysis View



# Generate a Timing Report - Design Uses Both Clock Edges

Timing reports can be generated from SmartTime. Timing reports enable you to quickly determine if there are any timing problems. The timing report lists the following information:

- Design information including device, speed grade and operating conditions.
- Design performance summary (maximum frequency, external setup and hold, minimum and maximum clock-to-out)
- Clock domain details
- Inter clock domain details
- Pin to pin timing

The timing report can be printed and saved.

#### To generate a Timing Report:

1. From the **Maximum Delay Analysis View** menu, choose **Tools > Reports > Timer** to open the Timing Report Options dialog box, as shown in the figure below.

Option Categories	Display of paths	
<ul> <li>Select a category: General</li> <li>Paths</li> <li>Sets</li> </ul>	☑ Include detailed path information in this report	
Clock Domains	Limit the number of paths per section to:	5
	Limit the number of expanded paths per section to:	1
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults

Figure 46 · Timing Report Options Dialog Box

2. Click the **Paths** category. Limit the number of reported paths to **5** (default), and click **OK**. The timing report opens in a new window, as shown in the figure below.



File Actions Help		
Timing Report Max Delay Ar	nalysis	
SmartTime Version v11.6		
Microsemi Corporation - Mi	icrosemi Libero Software Release v11.6 (Version 11.6.0.15)	
Date: Mon Apr 27 09:10:59	2015	
Design: shifttreg_16		
Family: SmartFusion2		
Die: M2S090TS Package: 484 FBGA		
Temperature Range: 0 - 85		
Voltage Range: 1.14 - 1.26		
Speed Grade: STD		
Design State: Post-Layout		
Data source: Production		
Min Operating Conditions:	BEST = 1.26 V = 0.0	
Max Operating Conditions:		
Scenario for Timing Analys		
sociality for finding marin	and removel	
SUMMARY		
Clock Domain:	my clk	
Period (ns):	1.980	
Frequency (MHz):	505.051	
	10.000	
Required Frequency (MHz):		
External Setup (ns):	5.457	
External Hold (ns):	0.955	
	4.311	
Max Clock-To-Out (ns):	9.127	
	Input to Output	
Min Delay (ns):	N/A	
Max Delay (ns):	N/A	

Figure 47 · Timing Report for shifter

The timing report contains the following sections:

- Header
- Summary
- Clock domain details for my\_clk and expanded path information
- External setup information
- Clock to output delay information
- 6. Save the timing report (File > Save As) as shifter\_timing.rpt and close the report window.
- 7. Close SmartTime and Libero.

### **Tutorial 4 - False Path Constraints**

This section describes how to enter false path constraints in SmartTime. You will import an RTL source file from the design shown below. After routing the design, you will analyze the timing, set false path constraints, and observe the maximum operating frequency in the SmartTime Timing Analysis window.



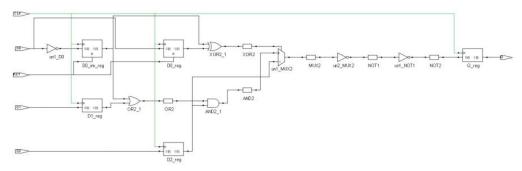


Figure 48 · Example Design with False Paths

### Set Up Your False Path Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **false\_path** and set the project location according to your preferences. Click **Next**. Enter the following values for your Device Selection settings:
- Family: SmartFusion2
- Die: M2S050
- Package: 484 FBGA
- Speed: STD
- Die Voltage: 1.2 V
- Range: COM
- 3. Click Finish to create the new project.
- 4. At the pop-up window, click **Use Enhanced Constraint Flow** in the New Project Information dialog box.

New Project Information	×
Libero SoC v11.7 introduces an enhanced constraint flow aimed at simplifying the management of all constraints for your design:	ĥ
• I/O, timing, floor planning and netlist optimization constraints can be created, imported, edited, checked and organized in a single view.	ł
<ul> <li>Timing constraints can be entered using standard SDC format and the same set of constraints can be automatically applied to both Synopsys' Symplify synthesis, Timing Driven Place and Route and Timing Verification.</li> </ul>	
• A new SDC clock group constraint is also introduced and can be used to ease the specification of related and unrelated clocks.	E
• Timing constraints for known hardware blocks and IPs can be derived automatically; examples of such constraints are:	I
<ul> <li>SERDES-EPCS, MSS/HPMS and internal oscillator clock sources</li> </ul>	I
• Fabric CCCs generated clocks	ĩ
• Fabric CCCs clock sources	
<ul> <li>CoreConfigP false paths, min and max delay constraints</li> </ul>	
Note that this first release of the enhanced constraint flow has the following limitations:	
The block flow is not enabled	
The design separation methodology is not enabled	÷
Remember my choice and do not show me again.     Use Classic Constraint Flow Use Enhanced Constraint Flow	w

Figure 49 · New Project Information Dialog Box

# Import the false\_path Verilog File and Add Constraints

You must import the false\_path.v Verilog source file into your design for this tutorial. Download the design files from the Microsemi website (URL link).

#### To import the Verilog Source File:

1. From the File menu, choose Import > HDL Source Files.



- 2. Browse to the location of the false\_path.v where you have downloaded from the Microsemi website and select it. Click **Open** to import the file.
- 3 1 2 2 0 1 2 € × Reports € × StariPage € × false\_path.v € × . - - v ø ts = false path (false path.v) reg reg reg reg Q reg: ssign 0 - 0 reg ways @ (posedge CLK or posedge RST if (RST) begin <= 1'b0; reg <= 1'b0; inv reg; Stimulus Hierarchy Catalog Files
- 3. Verify that the file appears in your project, as shown in the figure below.

Figure 50 · false\_path Design in Design Hierarchy

- 4. In the Design Flow window, double-click **Synthesize** to run synthesis. A green check mark appears when the Synthesis step completes successfully.
- 5. In the Design Flow window, double-click **Compile** to Compile with default settings. A green check mark appears next to Compile to indicate that it has completed successfully.
- 6. Expand Edit Constraints. Right-click Timing Constraints and choose Open Interactively.
- 7. In the SmartTime Constraints Editor, right click on **Requirements > Clock** and choose **Add clock constraint** under the Constraints pane on the left.
- 8. Enter a constraint for the clock source (CLK) with clock name (my\_clk) of 100 MHz (50% duty cycle), as shown in the figure below.

traints Editor for scenario Prima	ary										
Constraints     Requirements		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	
Clock	1	Click here to add a									
Generated Clock						1		r	-v		
Input Delay Output Delay	2	1	my_clk	CLK	10.000	100.000	50.0000	rising -	0.000	0 5	GUI
Max Delay Min Delay Multicycle & False Path Advanced Clock Source La Disable Timing Clock Uncertain											

Figure 51 · Clock Constraint of 100 MHz in false\_path design

9. Save your changes (File > Save) and close SmartTime (File > Close).



# Place and Route Your FALSE\_PATH Design

#### To run Place and Route on false\_path design:

1. In Libero SoC, right-click Place and Route and choose Configure Options.

Layout Options	? 🔀
Timing-driven	
Power-driven	
High Effort Layout	
Repair Minimum Delay Violations	
<ul> <li>Incremental Layout</li> <li>Use Multiple Passes</li> <li>Configure</li> </ul>	
Help	Cancel

Figure 52 · Layout Options Dialog Box

- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings. Click **OK** to close the Layout Options dialog box.
- 3. Right-click Place and Route and choose Run.

A green check mark appears next to Place and Route in the Design Flow window when Place and Route completes successfully.



alse_pa	th	🗆 🕒 🎑	ø
	Tool		*
	4	Create Design	
		🖧 System Builder	
		🖧 Configure MSS	
		D Create SmartDesign	
		Create HDL	
		😨 Create SmartDesign Testbench	
		Create HDL Testbench	
		• 🗋 Generate Memory Map	
		Verify Pre-Synthesized Design	
		Simulate	
	4	Create Constraints	
		→ I/O Constraints	
		🖞 💆 Timing Constraints	
		synthesis\false_path_sdc.sdc	III
		Proorplan Constraints	
	4	Implement Design	
1		Synthesize	
	1	Verify Post-Synthesis Implementation	
1		Rompile	
		• Configure Flash*Freeze	
1		Place and Route	
		Edit Constraints	
		➡ I/O Constraints	
		苬 Timing Constraints	
		🚱 Floorplan Constraints	
		Verify Post Layout Implementation	
	4	Edit Design Hardware Configuration	
		Programming Connectivity and Interface	
		🔊 Programmer Settings	
		Device I/O States During Programming	
		Configure Security and Programming Options	-

Figure 53 · Synthesize, Compile and Place and Route Successful Completion

# Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis View displays the design maximum operating frequency and lists any setup violations.

#### To perform Maximum Delay Analysis:

1. Expand Verify Post Layout Implementation. Right-click Verify Timing and choose Open Interactively to open SmartTime. The Maximum Delay Analysis View appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at a maximum frequency of 442.48 MHz.

Note: You may see a slightly different maximum frequency with a different Libero software version.



	x @ \$ <b>} &amp; {</b> ? @ x									
n Dela	y Analysis New									
2	Analysis for crenario									
	Analysis for scenario Primary	Design		false_path						
	Summary	Family		SmartFusio	n2					
	ny_dk	Die		M2S050						
	<ul> <li>Register to Register</li> <li>External Hold</li> </ul>	Package		484 FBGA						
	Clock to Output	Voltage Range Speed Grade		0 - 85 C						
	Register to Asynchronous			1.14 - 1.26	v					
	External Removal Asynchronous to Register			STD						
<ul> <li>Pin to Pin Input to Output</li> </ul>				Post-Layout	ť.					
Input to Output				Production						
		Min Operating Conditions		BEST - 1.26	V-0C					
_		Max Operating Conditions		s WORST - 1	14 V - 85 C					
		Scenario for Timing Analysis Primary								
		Scenario fo	Timing Analy	sis Primary						
	[]	Scenario fo	Timing Analy	ysis Primary						
		Scenario fo	Timing Analy	ysis Primary						
		Scenario fo		ysis Primary						
			ry Period	Frequency	Required Period (ns)	Required Frequency	External Setup (ns)	External Hold (ns)	Min Clock-To-Out	Max Clock-To-Out (ns)
	Select a set of paths to see	Summa	ry		Required Period (ns) 10.000	Required Frequency (MHz) 100.000	External Setup (ns) -0.025	External Hold (ns) 0.753	Min Clock-To-Out (ns) 5.117	Max Clock-To-Out (ns) 9.781
	Select a set of paths to see its sied: detribution.	Summa Clock Domain	Period (ns) 2.260	Frequency (MHz) 442.478	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)
	Select a set of paths to see its slad, debbutton,	Summa Clock Domain my_clk	Period (ns) 2.260 Min Del	Frequency (MHz) 442.478 ay (ns) Max De	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)
	Select a set of paths to see its also debbufus.	Summa Clock Domain	Period (ns) 2.260 Min Del	Frequency (MHz) 442.478	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)
	Select a set of paths to see the slact distribution.	Summa Clock Domain my_clk	Period (ns) 2.260 Min Del	Frequency (MHz) 442.478 ay (ns) Max De	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)
	Select a set of paths to see its sleck detribution.	Summa Clock Domain my_clk	Period (ns) 2.260 Min Del	Frequency (MHz) 442.478 ay (ns) Max De	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)
	Select a set of paths to see its dark definition.	Summa Clock Domain my_clk	Period (ns) 2.260 Min Del	Frequency (MHz) 442.478 ay (ns) Max De	(ns) 10.000	(MHz)	(ns)	(ns)	(ns)	(ns)

Figure 54 · Maximum Delay Analysis Summary

- 2. Expand my\_clk to expand the display and show the Register to Register path sets.
- 3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
- 4. Click to select the row in the path list with the path is from the CLK pin of flip-flop D0\_inv\_reg to the D input of flip flop Q\_reg. Note that the path goes through the S input of multiplexer un1\_MUX2.

Figure 48 shows that the S input of un1\_MUX2 will always be logic 1; consequently, all the paths through the 0 input of un1\_MUX2 and the S input of un1\_MUX2 are false paths. You must set a false path on these paths to determine the true maximum operating frequency.

5. To set the path from D0\_inv\_reg:CLK to Q\_reg :D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint** (as shown in the figure below). The Set False Path Constraint dialog box appears.

🖬 🗅 🕉 🗶 🖉 🐵 ≍											
Delay Analysis View											
Analysis for scenario Primary 3) Summary ∞ ™ my_clk ♥ Register to Register		om *					то	•		Apply Filter	Store Filter Reset Filter
External Setup Clock to Output Register to Asynchronous External Recovery		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
Asynchronous to Register	1	D0_inv_reg:CLK	Q_reg:D	1.906	7.740	5.887	13.627	0.298	2.260	0.056	
<ul> <li>Fin to Pin</li> </ul>	2	D0_reg:CLK	Сору		7.882	5.745	13.627	0.298	2.118	0.066	
Input to Output T User Sets		D0_reg:CLK	Print		7.002	5.745	13.02/	0.290	2.118	0.005	
S. User Sets	3	D1_reg:CLK	Add False Path	Constraint	7.896	5.731	13.627	0.298	2.104	0.067	
	4	D2_reg:CLK	Add Max Delay Add Min Delay	Constraint <table-cell></table-cell>	8.294	5.333	13.627	0.298	1.706	0.067	
			Add Multicycle	Path Constraint							
			Expand selected	naths							

Figure 55 · Right-Click > Add False Path Constraint



Set False Path Constraint		? 🔀
From :		
þ0_inv_reg:CLK	A	
	-	
K	F	
Through :		
	*	
	-	
	F	
То:		
Q_reg:D	A	
	+	
4	*	
Comment :		
Help	ОК Са	ancel

Figure 56 · Set False Path Constraint Dialog Box

- 6. Click OK to close the Set False Path Constraint dialog box.
- 7. From the View menu, choose Recalculate All to recalculate the delays.
- 8. There are a total of three register-to-register false paths in this design (see table below). Repeat steps 5 through 8 to set the false path constraint on the other two false paths (#2 and #3) using the values shown in the table.

	From	То
False Path #1	D0_inv_reg:CLK	Q_reg:D
False Path #2	D0_reg:CLK	Q_reg:D
False Path #3	D1_reg:CLK	Q_reg:D

9. Open the Constraint Editor (**Tools > Constraints Editor**) and click **Exceptions > False Path** (in the left pane under Constraints). The three False Path constraints are listed as shown in the figure below.



0	Syntax	From	Through	То	File	Commer
6	22.24					
					GUI	_
_	Click here to add a constrair				10.020	
	٣	D0_inv_reg:CLK		Q_reg:D	GUI	
	~	D0 reg:CLK		O reg:D	GUI	
-	<b>`</b>					-
1	<b>x</b>	DI_reg:CLK		Q_regio	GOI	
its of	f this kind are correct and	i valid.				
		r r	P D0_reg:CLK	©0_reg:CLK	OD_reg:CLK         Q_reg:D           P         D1_reg:CLK         Q_reg:D	D0_rep:OX         Q_rep:D         GUI           V         D1_rep:OX         GUI         V

Figure 57 · False Path Constraints in the SmartTime Constraint Editor

 View the summary in the Maximum Delay Analysis View (Tools > Max Delay Analysis). Note that SmartTime now reports the maximum operating frequency as 586.17 MHz, as shown in the figure below.

Note: The maximum operating frequency may vary slightly with a different version of the Libero software.

	×⊛ S <b>≥ ≤</b> 2										
num Delay	Analysis View										
	Analysis for scenario										
MAX	Primary	Design		fa	alse_path						
a 👌 Su		Family		S	martFusion2						
	immary	Die		N	12S050						
	✓ Register to Register	Package		4	84 FBGA						
	External Setup Clock to Output	Temperatu	re Range	0	- 85 C						
	Register to Asynchronous	Voltage Ra	ange	1	.14 - 1.26 V						
	External Recovery Asynchronous to Register	Speed Gra	ide	S	TD						
4 25	Pin to Pin	Design St	ate	F	Post-Lavout						
	Input to Output	Data source	e	F	Production						
2	User Sets		ting Conditi		EST - 1.26 V - 0 C						
			ating Condit		VORST - 1.14 V - 85 C						
			or Timing A	100							
		Scenario	or rinning A	alysis F	minary						
	,										
		Summa	ITV								
	2										
	Select a set of paths to see its slack distribution.	Clock Domain	Period (ns)	Freque (MHz)	ncy Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)	
# of paths		my_clk	1.706	586.166	10.000	100.000	-0.025	0.753	5.117	9.781	
4					Max Delay (ns)						
			MIN I	Jelay (ns	) Max Delay (ns)						

Figure 58 · Maximum Delay Analysis View - Summary

11. Select the Register to Register set for my\_clk. Observe that only one path is visible, from D2\_reg: CLK to Q\_reg:D. This is the only path that propagates a signal (as shown in the figure below).



	2 0	37 泽	👟 R	~ ~												
um De	elay Analysis			-												
and the second																
A	Drimary	for scenario				From *				TC						
	Summary				_	Customize table								Apply Filter	Store Filter	Reset Filter
	von my_					CONTRACT ODAC								Apply I stor	Storerito	Nedectifier
	✓ Reg	gister to Reg al Setup	ister			Source Pin	Sink Pi	n Delay (ns	) Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimu	m Period	Skew (n	5)
		to Output				1 D2_reg:CLK	Q_reg:D	1.34	1 8.294	5.333	13.627	0.29	-	1.706		0.067
		ter to Asynch				a begregitette										0.007
	Extern	al Recovery			_											
	Async	hronous to	Register													
	Async St Pin to	Pin	Register													
•	Async R Pin to Input	Pin to Output	Register													
	Async St Pin to	Pin to Output	Register													
	Async R Pin to Input	Pin to Output	Register													
	Async R Pin to Input	Pin to Output	Register			Name		Туре	Net		Macro	Op	Delay To	al Fanout	Edge	
	Async R Pin to Input	Pin to Output	Register			4 Summary		Туре	Net		Macro	Op			Edge	
	Async Pin to Input User S	Pin to Output	Register			<ul> <li>Summary data required time</li> </ul>	e	Туре	Net		Macro	Op	13	527	Edge	
	Async Pin to Input User S	Pin to Output	Register			<ul> <li>Summary data required time data arrival time</li> </ul>	ė	Туре	Net		Macro	Op	13	527 333	Edge	E
	Async Pin to Input User S	Pin to Output	Register			<ul> <li>Summary data required time data arrival time slack</li> </ul>		Туре	Net		Macro	Op -	13	527	Edge	E
	Async Pin to Input User S	Pin to Output	Register			Summary data required time data arrival time slack     Data_arrival_time_ca		Туре	Net		Macro	Op -	13 5 8	527 333 294	Edge	E
3	Async Pin to Input User S	Pin to Output	Register			Summary data required time data arrival time slack     Data_arrival_time_ca my_clk			Net		Macro	Op -	13 5 8 0.000 0	527 333 294		E
3	Async Pin to Input User S	Pin to Output	Register			<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_ca my_clk CLK</li> </ul>	alculation	Clock source			Macro	Op - +	13 5 8 0.000 0 0.000 0	527 333 294 000	r	, E
3	Async Pin to Input User S	Pin to Output	Register			Summary data required time data arrival time slack     Data_arrival_time_ca my_clk CLK CLK CLK,	alculation	Clock source net	Net			-	13 5 8 0.000 0 0.000 0 0.000 0	527 333 294 000 000	r	E
3	Async Pin to Input User S	Pin to Output	Register			<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_ca my_clk CLK CLK_ibuf/U0/U_JC CLK_ibuf/U0/U_JC</li> </ul>	alculation DPAD:PAD DPAD:Y	Clock source net cell	CLK		Macro ADLIB:JOPA	-	13 5 8 0.000 0 0.000 0 0.000 0 2.128 2	527 333 294 000 000 100 128 2	r t t	a E
3	Async X Pin to Input X User S	Pin to Output	Register			<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_ca my_clk CLK_ibuf/U0/U_JC CLK_ibuf/U0/U_JC CLK_ibuf/NU/VQU</li> </ul>	alculation DPAD:PAD DPAD:Y 14:An	Clock source net cell net			ADLIB:IOPA	+ + + + + +	13 5 8 0.000 0 0.000 0 0.000 0 2.128 2 0.352 2	527 333 294 000 000 128 2 480	r r f	E
3	Async Pin to Input User S	Pin to Output jiets		9,794	10.79	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_ca my_clk</li> <li>CLK</li> <li>CLK_ibuf/U0/U_JC</li> <li>CLK_ibuf/U0/U_JC</li> <li>CLK_ibuf/N0/U_JC</li> <li>CLK_ibuf_NNVQ0</li> <li>CLK_ibuf_NNVq0</li> </ul>	alculation DPAD:PAD DPAD:Y 14:An 14:YWn	Clock source net cell net cell	CLK CLK_ibuf			+ + + + + +	13 5 8 0.000 0 0.000 0 0.000 0 2.128 2 0.352 2 0.105 2	527 333 294 000 000 128 2 480 585 1	r r f f	-
3	Async X Pin to Input X User S	Pin to Output	Register	9.294	10.29	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_ca my_clk CLK_ibuf/U0/U_JC CLK_ibuf/U0/U_JC CLK_ibuf/NU/VQU</li> </ul>	alculation DPAD:PAD DPAD:Y M:An M:YWn M:YWn	Clock source net cell net cell net	CLK	Q04/U0_YWn	ADLIB:IOPA	+ + + + + +	13 5 8 0.000 0 0.000 0 0.000 0 2.128 2 0.352 2	527 333 294 000 000 128 2 480 480 551	r r f f	E

Figure 59 · Maximum Delay Analysis View - Register to Register

- 12. Close SmartTime.
- 13. Close Libero SoC.

# Tutorial 5 - Cross Clock Domain Analysis

SmartTime performs inter-clock domain timing checks for designs that contain functional paths that cross two clock domains (the register launching the data and the register capturing the data are clocked by two different clock sources). Accurate specification of both clocks is required to allow a valid inter-clock domain timing check.

SmartTime analyzes each inter-clock domain by determining a common period equal to the least common multiple of the two clock periods.

For setup check, the tightest launch-capture time period is considered to ensure that the data arrives before the capture edge (as shown in the figure below). The hold check verifies that a setup relationship is not overwritten by a following data launch.



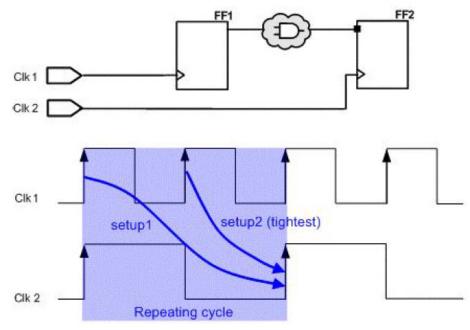


Figure 60 · Tightest Launch - Capture Relation for Setup Check in SmartTime In this tutorial you will:

- 1. Create a new Libero project.
- 2. Import a Verilog Source for the design shown in the figure below.
- 3. Enter timing constraints for the two clock domains.
- 4. Use SmartTime to analyze the inter-clock domain timing.

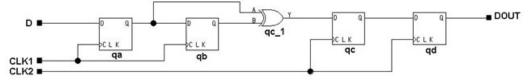


Figure 61 · Inter-Clock Domain Example Design Diagram

### Set Up Your Cross Clock Domain Analysis Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **multi\_clocks** and set the project location according to your preferences. Enter the following values for your new project:
- Family: SmartFusion2
- Die: M2S050
- Package: 484 FBGA
- Speed: STD
- Core Voltage: 1.2 V
- Range: COM

Leave all other fields at their default values.



New project										
Device selection Select a part for your project	from the part nur	nber list							Selected part	: M25050-FG484
Project Details	Part filter Family: Speed:	SmartFu	sion2 •		M2S050	•	Package: Range:	484 FBGA	•]	
Device Selection	Speed.	510		Core voltage.	1+6		Konge.		set filters	
Device Settings	Search part:									
	Part Numb	er	4LUT	DFF	User I/Os	uSRAM 1	К	LSRAM 18K	Math (18x18)	PLLs and
Design Template	M25050-FG	484	56340	56340	267	72		59	72	6
Add HDL Sources										
Add Constraints										
	•		111							•
Help							< Bac	k Next	t > Finish	Cancel

Figure 62 · multi\_clocks Project Settings

3. Click **Finish** to create the new project.

### Import Verilog Source File and Run Compile for Cross Clock Domain Analysis Example

You must import the multi\_clk.v file into your design for this tutorial. Download the design files from the Microsemi website (Url link to tutorial file) .

To import and constrain the Verilog source file:

- 1. From the File menu choose Import > HDL Source Files.
- 2. Choose HDL Source Files from the file type drop-down list in the Import Files dialog box.
- 3. Browse to the location of the **multi\_clk.v** file you have downloaded and select it. Click **Open** to import the file.
- 4. Verify that the file appears in the Design Hierarchy window of your project, as shown in the figure below.



n Hierarchy	ē×	Reports	θ×	StartPage 🗗 🗙	multi_ck.v 🖪 🗙	
v: Components -		0 =				
		17			///////////////////////////////////////	
🖌 🎒 work		18	1			
test (multi_clk.v)		19				
		20 21	modure	test (D, CLK1,	CLR2, DUUI);	
		22	input	D:		
		23	input	CLR1;		
			input	CLK2 ; DOUT ;		
		25 26	output	0001;		
		27	reg	qa;		
		28	reg	; dip		
		29 30	reg	qc; qd;		
		31	reg	da:		
			wire	qc_1;		
		33				
		34 35		qc_1 = qa ^ q DOUT = qd;	b1	
		36	assign	boot - dat		
		37		@ (posedge CLK	1)	
			begin	1.		
		39 40	ga gb	<= D; <= ga;		
		41	end	( day		
		42				
		43	always begin	8 (posedge CLK	2)	
		45	gc	<= qc_1;		
		46	gd	<= qc;		
		47	end			
m	•	48	endmod	110		
ign F Design Hierar Stimulus Hierar Catalog	Files HDL Templa	a ( m				
Design meran Sumulas meran Catalog	ries rise rempio	C.C. Harrison				
Messages 🔯 Errors 🗼 Warnings 🌒 Info						

Figure 63 · multi\_clocks Design in the Design Hierarchy Window and HDL Editor

5. Double-click **Compile** in the Design Flow window to run Synthesis first and then Compile with default settings. A green check mark appears next to Synthesize and Compile when they have run successfully, as shown in the figure below.



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test				🗆 🕒 📄 🧯	r
	Too	ы			-
	4	•	Cre	ate Design	1
			4	System Builder	
			4	Configure MSS	
			SD	Create SmartDesign	
			ľ	Create HDL	
			SD	Create SmartDesign Testbench	
				Create HDL Testbench	=
			•	Generate Memory Map	
		4		Verify Pre-Synthesized Design	
				Simulate	
	4		Cre	eate Constraints	
			-+	I/O Constraints	
		4	Ö	Timing Constraints	-
				synthesis\test_sdc.sdc	
			₽.	Floorplan Constraints	
	4		Im	plement Design	
1			S	Synthesize	
		4		Verify Post-Synthesis Implementation	
				Simulate	
14				Compile	
			•	Configure Flash*Freeze	
			0 <sub>lo</sub>	Place and Route	
		4		Edit Constraints	
				→ I/O Constraints	
				Timing Constraints	
				P: Floorplan Constraints	
		4		Verify Post Layout Implementation	
				Ganarata Dack Annatatad Ellar	-
•	_				
Catalog	9	De	si	Design Hi Stimulus Hi Files HDL T	e

Figure 64 · Design Flow Window – Synthesize and Compile Successful

# Enter Timing Constraints for the Cross Clock Domain Analysis Example

#### To add a clock constraint to your example design:

- 1. In the Design Flow window, expand **Edit Constraints**. Right-click on Timing Constraints and choose **Open Interactively** to open the SmartTime Constraints Editor.
- 2. In the Constraint Browser, expand **Requirements** and double-click **Clock** to enter the following clock constraints:
- Clock Source: CLK1, Clock Name: my\_clk1, Frequency:250 MHz
- Clock Source: CLK2, Clock Name: my\_clk2, Frequency:100 MHz



3. Verify that your new constraints are listed in the Constraints Editor, as shown in the figure below.

e Edit View Constrain			MIRE COL	. 9 <b>9</b> 2	. fr 55	3 <b>30</b> 3									-
traints Editor for scenario Primary															
Constraints A Requirements	^		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First E	dge	Offset (ns)	Waveform		File	Comments
Clock Generated Clock		1	Click here to add a cc					50.0000	rising	-	0.000	0.0	GUI		
Input Delay		2	<b>*</b>	my_clk1	CLK1	4.000	250.000	50.0000		•	0.000	0 2	GUI		
Output Delay Exceptions Max Delay	н	3	States .	my_clk2	CLK2	10.000	100.000	50.0000	rising	•	0.000	0 5	GUI		
Min Delay															
Multicycle															
False Path	1.00														
<ul> <li>Advanced</li> </ul>															
Clock Source Latency	*														

Figure 65 · Clock Constraints in the SmartTime Constraints Editor

- 4. Click Save to save your constraints.
- 5. Open the Max Delay Analysis View (Tools > Max Delay Analysis).
- 6. Choose **Tools > Options**. Ensure that the checkbox to Include inter-Clock domain analysis in calculations for timing analysis is enabled (default) as shown in the figure below.

SmartTime Options	? ×
Option Categories Select a category: General Analysis Advanced	General         Operating Conditions         Perform maximum delay analysis based on         WORST <ul> <li>case</li> <li>Perform minimum delay analysis based on</li> <li>BEST</li> <li>case</li> </ul> Clock Domains <ul> <li>Include inter-clock domains in calculations for timing analysis.</li> <li>Enable recovery and removal checks.</li> </ul>
Help	Restore Defaults OK Cancel

Figure 66 · Inter-Clock Domain Analysis Enabled in the SmartTime Options Dialog Box

7. Exit SmartTime (File > Exit).

### Place and Route Your Cross Clock Domain Analysis Example

#### To run Place and Route on multi\_clocks:

- 1. Right-click Place and Route in the Design Flow window and choose Configure Options.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings, as shown in the figure below. Click **OK** to close the Layout Options dialog box.
- 3. Right-click Place and Route and choose Run.

A green check mark appears next to Place and route when it completes successfully.



Layout Options	? ×
Timing-driven	
Power-driven	
High Effort Layout	
Repair Minimum Delay Violations	
Incremental Layout	
🔲 Use Multiple Passes	
Configure	
HelpOK	Cancel

Figure 67 · Layout Options - multi\_clocks

### Analyze Inter-Clock Domain Timing

Inter-clock domain timing enables you to analyze timing for designs that contain functional paths that cross two clock domains.

#### To analyze inter-clock domain timing:

- 1. Right-click Verify Timing and choose Open Interactively to open the Maximum Delay Analysis View.
- Expand the my\_clk2 path in the Maximum Delay Analysis View. Click to select the my\_clk1 to my\_clk2 path and observe the inter-clock domain path timing (as shown in the figure below).



																	_
6	Analysis for scena	io															
MA	Y Primary				From	n *				TO *							
_	4 √(0) my_clk2			1	6	stomize table						Apply Fil		e Filter		et Filte	-
	✓ Register to F	enister			Cus	stomize table						Арріу ні	ter	e ritter	Ke	etrite	
	External Setup	1						ourses 1	Delay	Slack	Arrival	Required	Setup		_	_	-
	Clock to Outpu Register to Asy					Source Pin	5	Sink Pin	(ns)	(ns)	(ns)	(ns)	(ns)				
	External Recov				1	ga:CLK	qc:D		0.739	1.351	4.788	6.13	9 0.298				
	Asynchronous												1				
	✓ my_clk1 to r			=	2	qb:CLK	qc:D		0.747	1.353	4.786	6,13	9 0.298				
	4 🔀 Pin to Pin																
	Input to Outpu	t															
	S User Sets																
				*													
				-										0.	Dul	Tabl	
				-	Nam			Туре	Net	_		Ma	cro	Op	Delay	Total	1.4
	3					Summary		Туре	Net	_		Ма	cro	Ор	Delay		14
	3					Summary data required time		Туре	Net			Ma	cro	Op		6.139	1*
	3			]		data required time data arrival time		Туре	Net	_	_	Ma	cro	Ор		6.139 4.788	1*
	3				- 5	Summary data required time data arrival time slack	ululia	Туре	Net			Ma	cro	Ор		6.139	-
	3				- 5	Summary data required time data arrival time slack Data_arrival_time_calc	ulation	Туре	Net			Ma	cro	Op -		6.139 4.788 1.351	E
	3				- 5	data required time data arrival time slack Data_arrival_time_calc my_clk1	ulation		Net			Ma	cro	-	0.000	6.139 4.788 1.351 0.000	E
					- 5	data required time data arrival time slack Data_arrival_time_calc my_clk1 CLK1		Clock source				Ma	cro	Ор -	0.000	6.139 4.788 1.351 0.000 0.000	E
					- 5	data required time data arrival time slack Data_arrival_time_calc my_clk1 CLK1 CLK1_ibuf/U0/U_IO	PAD:PAD		Net					•	0.000	6.139 4.788 1.351 0.000 0.000 0.000	E
ě					- 5	data required time data arrival time slack Data_arrival_time_calc my_clk1 CLK1_ibuf/U0/U_JO CLK1_ibuf/U0/U_JO CLK1_ibuf/U0/U_JO	PAD:PAD PAD:Y	Clock source net		ibuf			cro LIB:IOPAD_IN	•	0.000 0.000 0.000	6.139 4.788 1.351 0.000 0.000 0.000 2.128	E
paces	2				- 5	data required time data arrival time slack Data_arrival_time_calc my_clk1 CLK1 CLK1_ibuf/U0/U_IO	PAD:PAD PAD:Y 7:An	Clock source net cell	CLKL	ibuf		ADI		•	0.000 0.000 0.000 2.128	6.139 4.788 1.351 0.000 0.000 2.128 2.441	E
F of paths					- 5	data required time data arrival time slack Data_arrival_time_calc my_clkl CLKL_ibuf/U0/U_JO CLKL_ibuf/V0/U_JO CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD:	PAD:PAD PAD:Y 7:An 7:YWn	Clock source net cell net cell	СЦКІ		BD7/U0 YV	ADI	LIB:JOPAD_IN	•	0.000 0.000 0.000 2.128 0.313	6.139 4.788 1.351 0.000 0.000 2.128 2.441 2.650	E E
# of paths	2				- 5	data required time data arrival time slack Data_arrival_time_calc my_clkl CLKL CLKL_ibuf/U0/U_JO CLKL_ibuf/U0/U_JO CLKL_ibuf,RNIGBD7	PAD:PAD PAD:Y 7:An 7:YWn 7/U0_RGB1:An	Clock source net cell net cell net	СЦКІ		BD7/U0_W	ADI ADI Vn	LIB:JOPAD_IN	•	0.000 0.000 0.000 2.128 0.313 0.209	6.139 4.788 1.351 0.000 0.000 2.128 2.441 2.650 3.132	F.
# of paths	2				- 5	data required time data arrival time slack Data arrival_time_calc my.clkl CLKL_ibuf/U0/U_IO CLKL_ibuf/U0/U_IO CLKL_ibuf,RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD:	PAD:PAD PAD:Y 7:An 7:YWn 7/U0_RGB1:An	Clock source net cell net cell net	сікі, сікі,	ibuf_RNIG	BD7/U0_YV BD7/U0_RG	ADI ADI Vn ADI	LIB:IOPAD_IN LIB:GBM	- + + + + + + + + + +	0.000 0.000 0.000 2.128 0.313 0.209 0.482	6.139 4.788 1.351 0.000 0.000 2.128 2.441 2.650 3.132 3.504	E
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# of paths	2				- 5	data arquired time data arrival time slack Data arrival_time_calc my_ciki CLKL_ibuf/U0/U_JO CLKL_ibuf/U0/U_JO CLKL_ibuf/RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD:	PAD:PAD PAD:Y 7:An 7:YWn 7/U0_RGB1:An	Clock source net cell net cell net cell net	сікі, сікі,	ibuf_RNIG		ADI ADI Vn ADI iB1_VR	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + + + + + + + + + + + + + +	0.000 0.000 2.128 0.313 0.209 0.482 0.372 0.545 0.127 0.409	6.139 4.788 1.351 0.000 0.000 2.128 2.441 2.650 3.132 3.504 4.049 4.176 4.585	H
# of paths	2	1.352	1.353	1.354	- 5	data required time data arrival time slack Data, arrival time_calc my_clkl CLKL_ibuf/U0/U_IO CLKL_ibuf/U0/U_IO CLKL_ibuf,RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD: CLKL_ibuf_RNIGBD: qa:CLK qa:Q	PAD:PAD PAD:Y 7:An 7:YWn 7/U0_RGB1:An	Clock source net cell net cell net cell net cell	стка <sup>т</sup> стка <sup>т</sup>	ibuf_RNIG		ADI ADI Vn ADI iB1_YR ADI	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + + + + + + + + + + + + + +	0.000 0.000 2.128 0.313 0.209 0.482 0.372 0.545 0.127 0.409	6.139 4.788 1.351 0.000 0.000 2.128 2.441 2.650 3.132 3.504 4.049 4.176	H



The Paths list shows the detailed timing analysis. The longest reported path is from qa:clk to qc:d, as shown in the figure below. This path has a slack of 1.351 ns. The clock edges used in the calculation are shown in the timing diagram below.

Note: The actual slack value may vary with different die size and different Libero SoC versions.

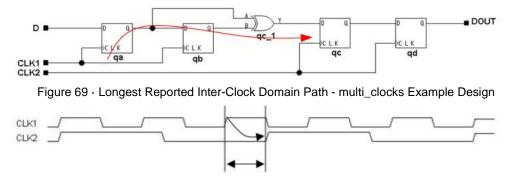


Figure 70 · Clock Edges Used in Inter-Clock Domain Max Delay Calculation - multi\_clocks Example Design

- 3. Click Tools and choose Minimum Delay Analysis.
- 4. Expand the CLK2 paths in the Minimum Delay Analysis View. Click to select **my\_clk1 to\_my\_clk2** path and observe the inter-clock domain path timing, as shown in the figure below.

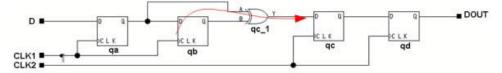


num Delay Analysis View												
NAT:												
Analysis for scenario												
Primary												
	From *				TO	) =						
	·							-			-	_
✓ w my_clk1	Customize ta	ble					1	Apply Fit	er Sti	ore Filter	Reset Fit	er
<ul> <li>Register to Register</li> </ul>												
External Hold			Service Service	Delay	Slack	Arrival R	equired	Hold				
Clock to Output Register to Asynchronous	5	Source Pin	Sink Pin	(ns)	(ns)	Arrival K (ns)	(ns)	(ns)				
External Removal	1 03:CK											
Asynchronous to Register	E 1 qa:CLK	qc:D		0.364	0.118	2.486	2.368	0.000				
<ul> <li>✓ my_clk2</li> </ul>	2 ab:CLK	qc:D		0.380	0.129	2.497	2.368	0.000				
<ul> <li>Register to Register</li> </ul>	a quican				0.147			0.000				
External Hold								-				
Clock to Output												
Register to Asynchronous												
External Removal												
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External Removal	* Name		Туре	Net			Macro		Op De	lav Total	Fanout E	dc ^
External Removal Asynchronous to Register			Туре	Net			Macro	2	Op De	lay Total	Fanout E	dç ^
External Removal Asynchronous to Register	4 Summar		Туре	Net			Macro	1	Op De	lay Total 2.497		dç ^
Estemal Removal Asynchronous to Register	4 Summar data a	y arrival time required time	Туре	Net			Macro	2	Op De			dç ^
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Estemal Removal Asynchronous to Register ✓ my_clk2 to my_clk2	✓ Summar data data slack	arrival time	Туре	Net			Macro	2		2,497		d <u>s</u> *
Estemal Removal Asynchronous to Register ✓ my_clk2 to my_clk2	✓ Summar data data slack	arrival time required time ival_time_calculation	Туре	Net			Macro		-	2.497 2.368 0.125		d <u>s</u> ^
Estemal Removal Asynchronous to Register ✓ my_clk2 to my_clk2	Summar data data slack     Data_arri	arrival time required time ival_time_calculation	Type Clock source				Macro	2	- 0. + 0.	2,497 2,368 0,125 000 0,000	r	d <u>s</u> ^
Estemal Removal Asynchronous to Register v my_clkl to my_clk2	Summar data data slack Data_arri my_c CLK1 CLK3	rrival time required time ival_time_calculation Ik1 _ibuf/U0/U_IOPAD:PAD	Clock source net	Net			Macro		- 0. + 0. + 0.	2.497 2.368 0.125 000 0.000 000 0.000	f	ds *
Asynchronous to Register	Summar data i data i slack     a Data_arii my_cl CLN1 CLN1 CLN1	rrival time required time ival_time_calculation lk1 _ibuf/U0/U_IOPAD:PAD _ibuf/U0/U_IOPAD:Y	Clock source net cell	CLKI				IOPAD_IN	- - + 0. + 0. + 1.	2.497 2.368 0.125 000 0.000 000 0.000 000 0.000 109 1.105	r r 2 r	ds *
Asynchronous to Register	Summar, data : data : slack Data arri my.c CIM CIM CIM CIM CIM	rrival time required time ival_time_calculation lk1 _ibuf/U0/U_IOPAD:PAD _ibuf/U0/U_IOPAD:Y _ibuf_RNIGBD7:An	Clock source net cell net		buf		ADLIB:	IOPAD_IN	- - + 0. + 0. + 1. + 0.	2.497 2.368 0.125 000 0.000 000 0.000 000 0.000 109 1.105 166 1.275	r r 2 r	dg *
Asynchronous to Register	Summar data : data : slack Data_arri my_c CLU CLU CLU CLU CLU CLU CLU CLU CLU	rrival time required time ival_time_calculation Ik1 _ibuf/U0/U_IOPAD:PAD _ibuf/U0/U_IOPAD:Y _ibuf_RNIGBD7:YWn	Clock source net cell net cell	СІКІ				IOPAD_IN	- + 0. + 0. + 1. + 0. + 0.	2.497 2.368 0.125 000 0.000 000 0.000 000 0.000 109 1.105 166 1.275 110 1.385	f r 2 r r 1 f	dg ≜ E
Asynchronous to Register W my_clk2 to my_clk2	Summar data data slack     Data_arri my.c CLC CLC CLC CLC CLC CLC CLC CL	rrival time required time ival_time_calculation lk1 _ibuf/U0/U_IOPAD:PAD _ibuf/U0/U_IOPAD:Y _ibuf_RNIGBD7:An _ibuf_RNIGBD7:YWn _ibuf_RNIGBD7:YWn	Clock source net cell net cell An net	СІКІ		807/U0_YWn	ADLIB:	IOPAD_IN GBM	- + 0. + 0. + 1. + 1. + 0. + 0. + 0.	2.497 2.368 0.125 000 0.000 000 0.000 000 0.000 109 1.105 166 1.275 110 1.385 253 1.638	r r 2 r r 1 f	E
Estemal Removal Asynchronous to Register y my_ciki to my_cik2	Summar, data ; data, dat	rrival time required time ival_time_calculation II. jbuf/U0/U_JOPAD:PAD jbuf/U0/U_JOPAD:Y jbuf_RNIGBD7:An jbuf_RNIGBD7:YWn jbuf_RNIGBD7/U0_RGB1:	Clock source net cell net cell An net YR cell	сікі сікі, сікі,	buf_RNIGE		ADLIB: ADLIB: ADLIB:	IOPAD_IN GBM	- + 0. + 1. + 1. + 0. + 1. + 0. + 0. + 0.	2.497 2.366 0.125 000 0.000 000 0.000 000 0.000 109 1.109 166 1.275 110 1.385 253 1.638 196 1.834	r 2 r 1 f 2 r	E
External Removal Asynchronous to Register	Summar, data slack     Data.arm my.c CLKLL CLKLL CLKLL CLKLL CLKLLL CLKLLL CLKLLL CLKLLL CLKLLL CLKLLL CLKLLLL CLKLLLL CLKLLLL CLKLLLLL CLKLLLLLLL CLKLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	rrival time required time ival_time_calculation II. jbuf/U0/U_JOPAD:PAD jbuf/U0/U_JOPAD:Y jbuf_RNIGBD7:An jbuf_RNIGBD7:YWn jbuf_RNIGBD7/U0_RGB1:	Clock source net cell net cell An net YR cell net	сікі сікі, сікі,	buf_RNIGE	807/U0_YWn 807/U0_RG81_	ADLIB: ADLIB: ADLIB: VR	IOPAD_IN GBM RGB	- - - - - - - - - - - - - -	2.497 2.366 0.125 000 0.000 000 0.000 000 0.000 109 1.109 166 1.275 110 1.385 253 1.638 196 1.834 283 2.117	r 2 r 1 f f 2 r r r r r r r r r r	
External Removal Asynchronous to Register w my_clkl to my_clk2	Summar, data ; data, dat	rrival time required time <b>ival_time_calculation</b> lid jbuf/U0/U_JOPAD:PAD jbuf/RIGBD7:An jbuf_RNIGBD7:YWn jbuf_RNIGBD7/U0_RGB1: jbuf_RNIGBD7/U0_RGB1: Jbuf_RNIGBD7/U0_RGB1:	Clock source net cell net cell An net YR cell	сікі сікі, сікі,	buf_RNIGE		ADLIB: ADLIB: ADLIB:	IOPAD_IN GBM RGB	- + 0. + 0. + 1. + 0. + 0. + 0. + 0. + 0. + 0.	2.497 2.366 0.125 000 0.000 000 0.000 000 0.000 109 1.109 166 1.275 110 1.385 253 1.638 196 1.834	r 2 r 1 f f 7 r 1 r	



The Paths list shows the detailed timing analysis. The shortest reported path is from qb:clk to qc:d, as shown in the figure below. This path has a positive slack of 0.129 ns. The clock edges used in the calculation are shown.

Note: The actual slack value may vary with different die sizes and different versions of Libero SoC.



Shortest Reported Inter-Clock Domain Path - multi\_clocks Example Design

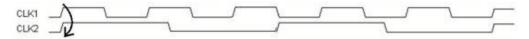


Figure 72 · Clock Edges Used in Inter-Clock Domain Min Delay Calculation - multi\_clocks Example Design

- 5. Exit SmartTime (File > Exit).
- 6. Exit Libero (**Project > Exit**).

### **Editable Constraints Grid**

The Constraints Editor allows you to add, edit and delete constraints directly from the Constraints Editor View.



Constraints Editor     Constraints     Generated Clock     Generated Clock     Min Delay     Min Delay     Multicycle     False Path     Clock Source Latency     Disable Timing     Clock Uncertainty

Figure 73 · Constraints Editor View

#### To add a new constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Enter the constraint values in the first row and click **OK**. Click the Save icon.
- 3. The new constraint is added to the Constraint List. The green syntax flag indicates that the syntax check on the constraint was successful.

#### To edit a constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Select the constraint, edit the values and click **Save**. The green syntax flag indicates that the syntax check for the constraint was successful.

#### To delete a constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Select the constraint you want to delete and from the right-click menu, select Delete Constraint.



# **SmartTime Constraints Editor**

### Components of the SmartTime Constraints Editor

SmartTime Constraints Editor is a tool in the Libero software that enables you to create, view, and edit timing constraints of the selected scenario for use with SmartTime timing analysis and timing-driven optimization tools. This editor includes powerful visual dialogs that guide you toward capturing your timing requirements and timing exceptions quickly and correctly. In addition, it is closely connected to the SmartTime Timing Analysis View, which enables you to analyze the impact of constraint changes.

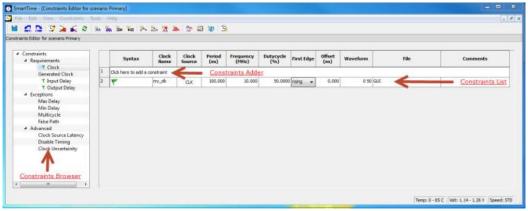


Figure 74 · SmartTime Constraints Editor View

#### **Constraint Hierarchy Browser**

The SmartTime Constraints Editor window is divided into a Constraint Browser and a Constraint List. The Constraint Browser categorizes constraints based on requirements, exceptions and advanced categories, while the Constraint List provides details about each constraint and enables the user to add, edit and delete constraints.

You can perform the following tasks in the SmartTime Constraints View:

- Select a constraint type from the Constraint Browser and create or edit the constraint.
- Add a new constraint and check the syntax.
   To add a constraint, double-click on the constraint type. To edit a constraint, select the constraint from the constraint list, right-click and choose Edit Constraint.
- Select a row and right-click to display the shortcut menu, which you can use to edit, delete, or copy the selected constraint to a spreadsheet.
- Select the entire spreadsheet and copy it to another spreadsheet.

#### See Also

Editable Grid and Quick Adder SmartTime scenarios

### **Constraint Wizard**

The SmartTime Constraint Wizard enables you to quickly and easily create clock and timing I/O constraints for your design.

To open the Constraint Wizard (shown below) from the SmartTime Tools menu, click the Constraint

Wizard icon \_\_\_\_\_. This window can be resized.



### **Constraint Wizard**

Constraint Wizard		×
	ion to SmartTime Constraint Wizard will assist you in creating constraints for clocks and I/Os in your design.	
Introduction Overall clock constraint Overall VO constraint Specific clock constraints Generated clock constraints Specific input constraints Specific output constraints Summary	The constraints created by the Wizard can be modiified later from the Constraints Editor. You can use the Wizard sequentially by clicking Next at each screen. Alternatively, you can access each individual step in the Wizard by clicking a step in the Constraint Wizard flow, available on the left column of this window. All steps in this Wizard are optional. Click Finish at any time to skip the remaining steps.	
Help	< Back Next > Cancel	

#### Figure 75 · Constraint Wizard

This window provides information about the Constraint Wizard and how to use it. Check the **Don't show this introduction again** box to skip this window next time you use this wizard.

Press **Next** to continue to the next step in the wizard.

Note: All steps in this Wizard are optional; click Finish to exit the wizard.



### **Overall Clock Constraint**

Constraining explicit clocks         You can set a constraint for all explicit clocks in your design.         Introduction         Overall clock constraint         Overall NO constraint         Specific clock constraints         Generated clock constraints         Specific input constraints         Specific input constraints         Specific clock constraints         Specific output constraints         Specific output constraints         Specific output constraints         Summary	Constraint Wizard	
constraints       The constraint above will apply to all explicit clocks that are not constrained yet. You will be able to override this constraint for any specific clock in a later step of this Wizard.         Specific output constraints	Constraint You can set a Introduction Overall LOCK constraint Overall I/O constraint Specific clock constraints Generated clock constraints	ng explicit clocks a constraint for all explicit clocks in your design.
Help < Kip Finish Cancel	constraints Specific output constraints Summary	override this constraint for any specific clock in a later step of this Wizard.

Figure 76 · Constraint Wizard – Overall Clock Requirements

In this window you can set a default required period or frequency for all explicit clocks in your design. Clocks that already have a constraint will not be affected.

To set a constraint for all explicit clocks, enter the **Period** or the **Frequency**, and click **Next** to go to the next step or **Finish** to exit the wizard.



### **Overall I/O Constraint**

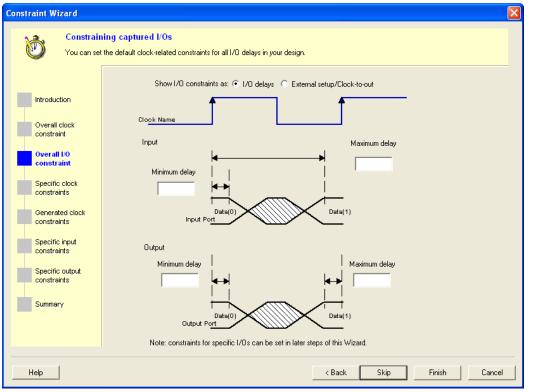


Figure 77 · Constraint Wizard – Overall I/O Constraint

In this window you can set a default constraint for all I/O's in the design. Constraints will be applied with respect to clocks related to the I/O's. This constraint will not override existing I/O constraints.

**Show I/O constraints** enables you to display I/O constraints as I/O delays (minimum and maximum delays for input and output) or external setup/clock-to-out.

#### To set a constraint for all I/Os:

- 1. Enter the Maximum and/or Minimum delays for the Input and/or Output.
- 2. Click Next to go to the next step or Finish to exit the wizard.



### **Specific Clock Constraints**

Constraint Wizard									X
You can set constraining in									
Introduction	Syntax	Clock Name	Period (ns)	External Setup (ns)	External Hold (ns)	Max Input Delay (ns)	Min Input Delay (ns)	Max Clock-to-out (ns)	Min Clock-I (ns)
Overall clock constraint				potential cloci	< pin				
constraint		CLK_IN	4.000						
Overall I/O		DATA_REG_	2.000						
constraint _		SM_RD:Q	4.000						
Specific clock	Ÿ	step[1]:Q	2.000						
constraints         Generated clock constraints         Specific input constraints         Specific output constraints         Summary	<								3
V	√aming:Some∣	ootential clock	s in your d	esign are not c	constrained.				
Help						< Back	Next >	Finish	Cancel

Figure 78 · Constraint Wizard – Specific Clock Constraints

In this window you can set a period and I/O timing constraints for a specific clock domain. All I/Os within the domain will be affected by the I/O timing constraints. You can modify the constraints from the grid.

#### To add a constraint for a potential clock:

- 1. Click the first row in the grid, enter the constraint information, and click the green check mark.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is a potential clock in your design.



### **Generated Clock Constraints**

Constraint Wizard		
You can set constrain	nerated clocks nts for generated clocks.	
Introduction	Syntax Clock Pin Reference Pin Multiplier Divider External Setup (ns) External Hold (ns) Delay (ns) Delay (ns)	Clo
Overall clock constraint	Click here to add a constraint on a potential clock pin	_
Overall I/O constraint		
Specific clock constraints		
Generated clock constraints		
Specific input constraints		
Specific output constraints		
Summary		
J≤ ₩	Jarning: Some potential clocks in your design are not constrained.	>
Help	< Back Next > Finish Canc	;el

Figure 79 · Constraint Wizard – Generated Clock Constraints

In this window you can set a period and I/O timing constraints for a specific generated clock domain. You can modify the constraints from the grid.

#### To add a constraint for a generated clock:

- 1. Click the first row in the grid, enter the constraint information, and click the green check mark.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is a generated clock in your design.



### **Specific Input Constraints**

Constraint Wizard									×
You can set const									
Introduction	Syntax	Port Name	Clock	External Setup (ns)		Max Input Delay (ns)	Min Input Delay (ns)		^
	- P	CPUADD[0]	CLK_IN					1	9
Overall clock constraint	- <b>F</b>	CPUADD[1]	CLK_IN						
Constraint	- <b>F</b>	CPUADD[2]	CLK_IN						
Overall I/O	- <b>F</b>	CPUADD[3]	CLK_IN						
constraint	- <b>F</b>	CPUADD[4]	CLK_IN						
	- <b>F</b>	CPUADD[5]	CLK_IN						
Specific clock constraints	- <b>P</b>	CPUADD[6]	CLK_IN						
constraints	- <b>P</b>	CPUDATA[0]	CLK_IN						
Generated clock	- <b>7</b>	CPUDATA[10]	CLK_IN						
constraints	- <b>Y</b>	CPUDATA[11]	CLK_IN						
		CPUDATA[12]	CLK_IN						
Specific input		CPUDATA[13]	CLK_IN						
constraints		CPUDATA[14]	CLK_IN						
Specific output	- <b>P</b>	CPUDATA[15]	CLK_IN						
constraints	- <b>P</b>	CPUDATA[1]	CLK_IN						
	- <b>7</b>	CPUDATA[2]	CLK_IN						
Summary		CPUDATA[3]	CLK_IN					1	
,		CPUDATA[4]	CLK_IN						
		CPUDATA[5]	CLK_IN						
		CPUDATA[6]	CLK_IN						~
	· ¬ ·							1	
Help					< Back	Next>		nish	Cancel
Trop					< Dack	Next>		riisri	Cancel

Figure 80 · Constraint Wizard – Specific Input Constraints

In this window you can set constraints for specific input pins. You can modify the constraints from the grid.

#### To set a constraint for an input pin:

- 1. Set the maximum and/or minimum input delay for selected pin in the grid.
- 2. Click Next to go to the next step or Finish to exit the wizard.

Note: This option is available only when there is an input pin in your design.

Double-click the **Port Name** or **Clock** header in the table to change the sorting order by input port name or clock name.



### **Specific Output Constraints**

ATT N	g individual ou nstraints for specific							
Introduction	Syntax	Port Name	Clock	Max Clock-to-out (ns)	Min Clock-to-out (ns)	Max Output Delay (ns)	Min Output Delay (ns)	
Overall clock		BYPASS	CLK_IN					1
constraint		CPUDATA[0]	CLK_IN					1
Overall I/O		CPUDATA[10]	CLK_IN					1
constraint		CPUDATA[11]	CLK_IN					
		CPUDATA[12]	CLK_IN					
Specific clock		CPUDATA[13]	CLK_IN					1
constraints		CPUDATA[14]	CLK_IN					1
		CPUDATA[15]	CLK_IN					
Generated clock constraints		CPUDATA[1]	CLK_IN					1
Constraints		CPUDATA[2]	CLK_IN					
Specific input		CPUDATA[3]	CLK_IN					
constraints		CPUDATA[4]	CLK_IN					1
		CPUDATA[5]	CLK_IN					1
Specific output constraints		CPUDATA[6]	CLK_IN					
constraints		CPUDATA[7]	CLK_IN					1
		CPUDATA[8]	CLK_IN					
Summary	1 V	CPUDATA[9]	CLK_IN					1
		CPU_NREADY	CLK_IN					
		CRC32_SRAM	CLK_IN					
		CDC00 CDAM	CLV IN					

Figure 81 · Constraint Wizard – Specific Output Constraints

In this window you can set constraints for specific output pins. You can modify the constraints from the grid.

#### To set a constraint for an output pin:

- 1. Set the maximum and/or minimum output delay for selected pin in the grid.
- 2. Click Next to go to the next step or Finish to exit the wizard.

Note: This option is available only when there is an output pin in your design.

Double-click the **Port Name** or **Clock** header in the table to change the sorting order by output port name or clock name.



### Summary

Constraint Wizard		×
Summary	fully completed the Constraint Wizard. te the constraints listed below.	× .
Help	< Back Finish Cancel	

Figure 82 · Constraint Wizard – Summary

This window summarizes the requirements specified in the wizard and information about all clock and I/O constraints in the design.

Click Finish to create the constraints.

#### See Also

Editable Constraints Grid

### **Using Clock Types**

Clock constraints enable you to specify your clock sources and clock requirements, such as the frequency and duty cycle. SmartTime detects possible clocks by tracing back the design from the clock pins of all sequential components until it finds an input port, the output of another sequential element, or the output of a PLL. SmartTime classifies clock sources into three types:

- Explicit Clocks
- Potential Clocks
- <u>Clock Networks</u>

Grouping clocks into these three types helps you manage clock domains efficiently when you add a new clock domain for analysis or when you create a new clock constraint using the Select Source Pins for Clock Constraint dialog box (as shown below).



Select Source Pins for Clock Constraint			
Specify pins 💿 by explicit list	C by keyword and wild	dcard	
Available Pins:		Assigned Pins:	
CPUCIk VidRefClk	Add >		
	Add All >		
	< Remove		
	< Remove All		
, Filter available objects:		,	
Pin Type: Explicit clocks	•		
*	Filter		
Help		ОК	Cancel

Figure 83 · Select Source Pins for Clock Constraint Dialog Box

#### See Also

Select Source Pins for Clock Constraint Dialog Box Understanding Explicit Clocks Understanding Potential Clocks Understanding Clock Networks

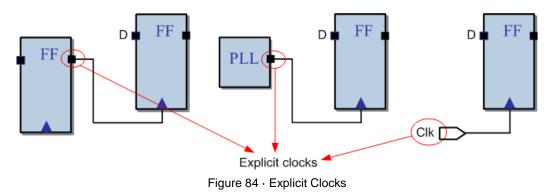
# **Understanding Explicit Clocks**

Explicit clocks are pins or ports connected to the clock pin of one or more sequential component, and where each clock is one of the following:

- The output of a PLL
- · An input port that does not get gated between the source and the clock pins it drives
- The output pin of a sequential element that does not get gated between the source and the clock pins it drives
- Any pin or port on which a clock constraint was specified

By default, SmartTime displays domains with explicit clocks in the Timing Analysis View. You can browse these domains in the Domain Browser of the Timing Analysis View.



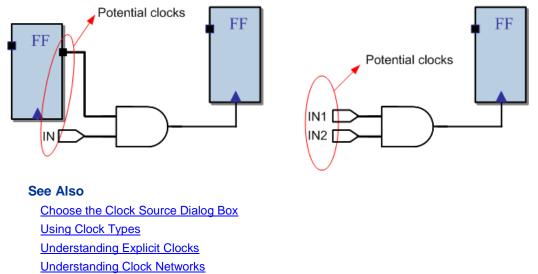


#### See Also

Choose the Clock Source Dialog Box Using Clock Types Understanding Potential Clocks Understanding Clock Networks

### **Understanding Potential Clocks**

Potential clocks are the clock sources that could be either enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks. When associated with gated clocks, SmartTime cannot differentiate between the enabled sources and clock sources. Both sources appear in the potential clocks list and not the explicit clocks list.



# **Understanding Clock Networks**

Clock networks are internal clock network pins used as a clock source. With this network type, you can set the clock constraint on any pin in the clock network. You may want to do this to eliminate clock network pessimism by short-cutting a reconvergent combinational logic on the clock network (as shown below). Clock network pessimism triggers an overestimation of the clock skew, making the timing analysis inaccurate.



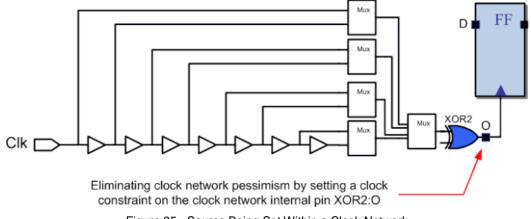


Figure 85 · Source Being Set Within a Clock Network

#### See Also

<u>Choose the Clock Source Dialog Box</u> <u>Using Clock Types</u> <u>Understanding Potential Clocks</u> Understanding Clock Networks

# **Specifying Clock Constraints**

Specifying clock constraints is the most effective way to constrain and verify the timing behavior of a sequential design. Use clock constraints to meet your performance goals.

#### To specify a clock constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Create Clock Constraint</u> dialog box using one of the following methods:
  - Click the icon in the Constraints Editor.
  - Right-click the Clock in the Constraint Browser and choose Add Clock Constraint.
  - Double-click Clock in the Constraint Browser.

The Create Clock Constraint dialog box appears (as shown below).

Create Clock Constraint			? X
Clock Name :	Clock Source :		•
I <del>≪</del> Period : [	ns	or Frequency:	Mhz
Offset : Duty cyde :			
0.000 ns 50.0000 %			
Comment:			
Help		ОК	Cancel

Figure 86 · Create Clock Constraint Dialog Box



2. Select the pin to use as the clock source. You can click the **Browse** button to display the <u>Select</u> <u>Source Pins for Clock Constraint Dialog Box</u> (as shown below).

Note: Do not select a source pin when you specify a virtual clock. Virtual clocks can be used to define a clock outside the FPGA that it is used to synchronize I/Os.

Use the Choose the Clock Source Pin dialog box to display a list of source pins from which you can choose. By default, it displays the explicit clock sources of the design. To choose other pins in the design as clock source pins, select **Filter available objects - Pin Type** as **Explicit clocks**, **Potential clocks**, **All Ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. To display a subset of the displayed clock source pins, you can create and apply a filter. Multiple source pins can be specified for the same clock when a single clock is entering the FPGA using multiple inputs with different delays.

Click **OK** to save these dialog box settings.

- 3. Specify the **Period** in nanoseconds (ns) or **Frequency** in megahertz (MHz).
- 4. Modify the Clock Name. The name of the first clock source is provided as default.
- 5. Modify the Duty cycle, if needed.
- 6. Modify the **Offset** of the clock, if needed.
- 7. Modify the first edge direction of the clock, if needed.
- 8. Click OK. The new constraint appears in the Constraints List.

Note: When you choose File > Save, SmartTime saves the newly created constraint in the database.

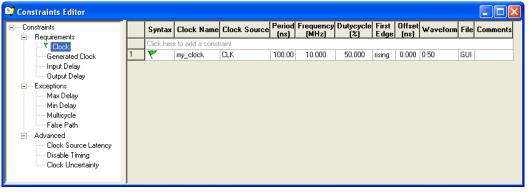


Figure 87 · SmartTime Timing Constraint View

#### See Also

**Clock** definition

Create a Clock

Create Clock Constraint Dialog Box

### Specifying Generated Clock Constraints

Specifying a generated clock constraint enables you to define an internally generated clock for your design and verify its timing behavior. Use generated clock constraints and <u>clock constraints</u> to meet your performance goals.

#### To specify a generated clock constraint:

- 1. Open the Create Generated Clock Constraint dialog box using one of the following methods:
  - Click the Micon.
  - Right-click the GeneratedClock in the Constraint Browser and choose Add Generated Clock.
  - Double-click the Generated Clock Constraints grid. The Create Generated Clock Constraint dialog box appears (as shown below).



Create Generated Clock Constraint
Clock Reference:
Clock Port FPGA
Generated Clock Name
The generated frequency is such as
f(clock) = f(reference) × 1 / 1 Get Pre-Computed Factors
The generated waveform is the same as 💌 the reference waveform
Comment:
Help OK Cancel

Figure 88 · Create Generated Clock Constraint

 Select a Clock Pin to use as the generated clock source. To display a list of available generated clock source pins, click the Browse button. The <u>Select Generated Clock Source</u> dialog box appears (as shown below).



Select Generated Clock Source	$\mathbf{X}$
Select a pin:	
XCMP33/U0/U2_DDR 1:Q XCMP33/U0/U2_DDR 2:Q pll 1:CLK1 pll 1:CLK2	
Filter available objects:	
Type: Explicit clocks	
Filter:	
* Filter	
Help OK Cancel	

Figure 89 · Select Generated Clock Source Dialog Box

- 3. Modify the Clock Name if necessary.
- 4. Click **OK** to save these dialog box settings.
- 5. Specify a **Clock Reference**. To display a list of available clock reference pins, click the **Browse** button. The <u>Select Generated Clock Reference</u> dialog box appears.
- 5. Click OK to save this dialog box settings.
- 6. Specify the values to calculate the generated frequency: a multiplication factor and/or a division factor (both positive integers).
- 7. Specify the first edge of the generated waveform either same as or inverted with respect to the reference waveform.
- 8. Click OK. The new constraint appears in the Constraints List.
- Tip: From the File menu, choose Save to save the newly created constraint in the database.

#### See Also

Design Constraint Guide: <u>Clock</u> Design Constraint Guide: <u>Create a Clock</u> Create Clock Constraint Dialog Box

### Using Automatically Generated Clock Constraints

If your design uses a static PLL, SmartTime automatically generates the required frequency at the output of the PLL, provided you have supplied the input frequency. When you start SmartTime, a generated clock constraint appears in the Constraints List with the multiplication and division factor extracted from the PLL configuration. The **File** column specifies this constraint as **auto-generated** (as shown below).



									_ [
	Syntax	Clock Name	Clock Pin	Reference Pin	Multiplier	Divider	Waveform	File	Comments
	Click here	e to add a constra	int						
1	7	\$1155/Core:GLA	\$1155/Core:GLA	\$1155/Core:CLKA	8	8	synchronized	auto-generated	
2	2	\$1156/Core:GLA	\$1156/Core:GLA	\$1156/Core:CLKA	8	8	synchronized	auto-generated	
	1	Click here	Click here to add a constra State of the state of the st	Syntax Clock Name Clock Pin Click here to add a constraint \$1155/Core:GLA \$1155/Core:GLA \$1156/Core:GLA \$1156/Core:GLA	Click here to add a constraint           1         Y         \$1155/Core:GLA         \$1155/Core:CLKA	Click here to add a constraint           1              \[	Click here to add a constraint           1              \\$             1155/Core:GLA \$1155/Core:GLA \$1155/Core:CLKA 8 8	Click here to add a constraint V \$1155/Core:GLA \$1155/Core:GLA \$1155/Core:CLKA 8 8 synchronized	Click here to add a constraint           Click here to add a constraint         ¥1155/Core:GLA \$1155/Core:GLA \$1155/Core:CLKA         8         8         synchronized         auto-generated

#### Figure 90 · Constraints Editor

Note: SmartTime does not automatically create a Generated Clock constraint if you have already set a constraint on the PLL output.

If you delete the automatically generated clock constraint, SmartTime does not regenerate it the next time you open the design. However, you can easily create it again by using the following steps:

- 2 23 Create Generated Clock Constraint Clock Pin: Ŧ .... Reference Pin: Clock Conditioning Circuitry Clock Port FPGA Generated Clock Name The generated frequency is such as  $f(clock) = f(reference) \times 1$ / 1 Get Pre-Computed Factor The generated waveform is the same as Ŧ the reference waveform Comment: OK Cancel Help
- 1. Open the Create Generated Clock Constraint dialog box (as shown below).

Figure 91 · Create Generated Clock Constraint

- 2. Select the PLL output as the Clock Pin source for the generated clock.
- 3. Select the PLL input clock as the **Clock Reference** for the generated clock.
- 4. Click Get Pre-Computed Factors. SmartTime retrieves the factor from the static PLL configuration.
- 5. Click OK.

# Specifying an Input Delay Constraint

Use the input delay constraint to define the arrival time of an input relative to a clock.

#### To specify an input timing delay constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the **Set Input Delay Constraint** dialog box using one of the following methods:
  - From the SmartTime Actions menu, choose Constraints > Input Delay.
  - Click the icon.
  - Right-click the Input Delay in the Constraint Browser.
  - Double-click any field in the Input Delay Constraints grid.

The Set Input Delay Constraint dialog box appears (as shown below).

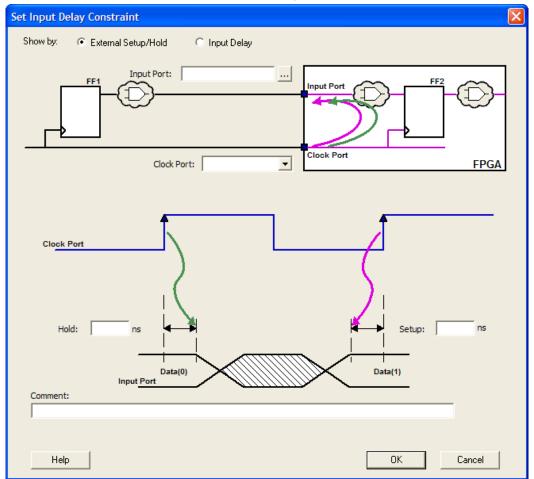


Figure 92 · Set Input Delay Dialog Box

- 2. Select either External Setup/Hold or Input Delay.
  - External Setup/Hold enables you to enter an input delay constraint by specifying the timing budget inside the FPGA using the external setup and hold time. This is the default selection.
  - Note: The external hold information is currently used for analysis only and not by the optimization tools. For the basic timing analysis flow of a simple design, select External Setup/Hold.
  - **Input Delay** enables you to enter an input delay constraint by specifying the timing budget outside the FPGA. You can enter the Maximum Delay, the Minimum Delay, or both.

Note: The Minimum Delay is currently used for analysis only and not by the optimization tools.

When you change values in one view, SmartTime automatically updates the other view.

3. Specify the **Input Port** or click the **Browse** button to display the **Select Ports for Input Delay** dialog box.

Select Ports for Input Delay			
Specify pins ( by explicit list	C by keyword and wildo	ard	
Available Pins:		Assigned Pins:	
Aclr Clock Enable	Add >		
	< Remove		
	< Remove All		
Filter available pins:			
Pin Type: Input ports	•		
*	Filter		
Help		OK	Cancel

Figure 93 · Select Ports for Input Delay Dialog Box

- 3. Select the name of the input pin(s) from the **Available Pins** list. Choose the **Pin Type** from the dropdown list. You can use the filter to narrow the pin list. You can select multiple ports in this window.
- 4. Click Add or Add All to move the input pin(s) from the Available Pins list to the Assigned Pins list.
- 5. Click OK.

The Set Input Delay Constraint dialog box displays the updated Input Port information.

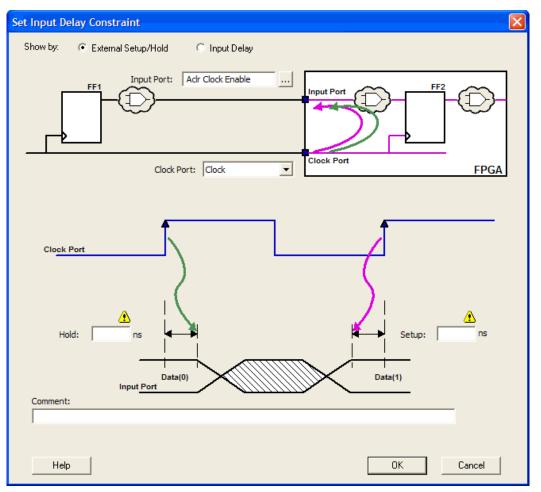


Figure 94 · Updated Set Input Delay Constraint Dialog Box

- 4. Select a clock from the Clock Port drop-down list.
- 5. If you selected **Show by: External Setup/Hold**, specifythe External Setup. If you selected **Show by: Input Delay**, specify the Maximum Delay value.
- 6. If you selected **Show by External Setup/Hold**, specify the External Hold. If you selected **Show by: Input Delay**, specify the Minimum Delay value.
- 7. Click **OK**.

SmartTime adds this constraint to the Constraints List in the SmartTime Constraints Editor.

#### See Also

Set Input Delay Constraint dialog box Select Source or Destination Pins for Constraint dialog box

### Specifying an Output Delay Constraint

Use the output delay constraints to define the output delay of an output relative to a clock.

#### To specify an output delay constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the **Set Output Delay Constraint** dialog box using one of the following methods:
  - From the SmartTime Actions menu, choose Constraints > Output Delay.
  - Click the icon.



- Right-click the **Output Delay** in the Constraint Browser.
- Double-click any field in the Output Delay Constraints grid.

The Set Output Delay Constraint dialog box appears.

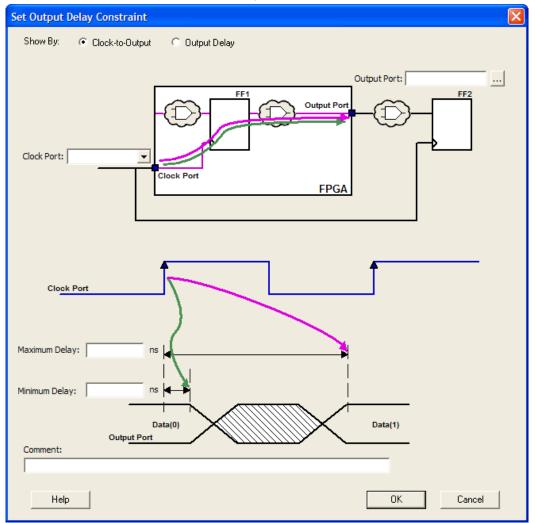


Figure 95 · Set Output Delay Constraint Dialog Box

Specify either Clock-to-Output or Output Delay.

• **Clock-to-Output** enables you to enter an output delay constraint by specifying the timing budget inside the FPGA. This is the default selection.

Note: The Minimum Delay value is currently used for analysis only and not by the optimization tool.

• **Output Delay** enables you to enter an output delay constraint by specifying the timing budget outside the FPGA. You can enter either the Maximum Delay, the Minimum Delay, or both.

Note: The Minimum Delay is currently used for analysis only and not by the optimization tools.

When you change values in one view, SmartTime automatically updates the values in the other view.

3. Enter the name of the **Output Port** or click the Browse button to display the **Select Ports for Output Delay** dialog box.



Select Ports for Ou	ıtput Delay			
Specify pins (	by explicit list	🔘 by keyword and wild	lcard	
Available Pins:			Assigned Pins:	
Q(0) Q(1) Q(10)	^	Add >		
Q(11) Q(12) Q(13) Q(14)		Add All >		
Q(15) Q(2) Q(3)		< Remove		
Q(4) Q(5) Q(6) O(7)	~	< Remove All		
Filter available pin:	s:			
Pin Type:	Output ports	•		
*		Filter		
Help			ОК	Cancel

Figure 96 · Select Ports for Output Delay Dialog Box

- 4. Select the output pin(s) from the **Available Pin** list. Choose the **Pin Type** from the drop-down list. You can use the filter to narrow the pin list. You can select multiple ports in this dialog box.
- 5. Click Add or Add All to move the output pin(s) from the Available Pins list to the Assigned Pins list.
- 6. Click **OK**. The **Set Output Delay Constraint** dialog box displays the updated representation of the Output Port graphic.
- 7. Select a clock port from the Clock Port drop-down list.
- 8. Enter the Maximum Delay value.
- 9. Enter the Minimum Delay value.
- 10. Click OK. SmartTime adds this constraint to the Constraints List in the Constraints Editor.

#### See Also

Set Output Delay Constraint dialog box Select Source or Destination Pins for Constraint dialog box



# **SmartTime Timing Analyzer**

### Components of the SmartTime Timing Analyzer

Use the SmartTime Timing Analyzer to visualize and identify timing issues in your design for the selected scenario. In this view, you can evaluate how far you are from meeting your timing requirements, create custom sets to track, set timing exceptions to obtain timing closure, and cross-probe paths with other tools.

The timing analysis view includes:

Demois Desures

- Domain Browser: Enables you to perform your timing analysis on a per domain basis.
- Path List: Displays paths in a specific set in a given domain sorted by slack.
- Path Details: Displays detailed timing analysis of a selected path in the paths list.
- Analysis View Filter: Enables you to filter the content of the paths list.

• Path Slack Histogram: When a set is selected in the Domain Browser, the Path Slack Histogram displays a distribution of the path slacks for that set. Selecting one or multiple bars in the Path Slack Histogram filters the paths displayed in the Path List.

You can copy, change the resolution and the number of bars of the chart from the right-click menu.

-	ximum Delay Analysis Vi	ew									
Co	à	From	*			То	*				
<b>м</b> А	Summary						Apply	Filter	Store Filter	Res	et Filter
ļ	St Datashee♥ ×⊕ CLK8M		Source Pin		Sink Pin		Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Mini
	<ul> <li>Register to Regi.</li> </ul>	1	J_SBI/U3/rwra:CLK	U_SB	I/U3/WR:D	5.658	53.655	7.916	61.571	0.668	
	External Setup     Clock to Output	2 L	J_TOPM031/U_CORE/c _2[2]:CLK	on U_SB	1/U4/bram_a[12]:D	48.407	70.731	50.722	121.453	0.867	
	<ul> <li>Register to Asynchrc</li> <li>External Recovery</li> </ul>	3 L		on U_SB	1/U4/bram_a(1):D	47.470	71.611	49.785	121.396	0.867	
	Asynchronous to Re	4 L	J_TOPM031/U_CORE/c _1[3]:CLK	on U_SB	1/U4/bram_a(12):D	47.412	71.726	49.727	121.453	0.867	
T	× Register to Regi.	5 L		on U_SB	1/U4/bram_a[14]:D	47.183	71.910	49.498	121.408	0.867	
<b></b>		6 L	J_TOPM031/U_CORE/c _0_0[2]:CLK	on U_SB	1/U4/bram_a(12):D	47.269	71.915	49.538	121.453	0.867	
11	10	<									>
	00-		)etails for path from: U_SBI/U3/rwra	CLK							
	90-	ĺ	o: U_SBI/U3/WR:D								
1	90	ļ	o: U_SBI/U3/WR:D Pin Name		Туре	Net I	Name	Cell Na	ame Op De	lay (ns) T	otal (r
:		i	o: U_SBI/U3/WR:D		Туре	Net I	Name	Cell Na	me Op De	lay (ns) T	otal (r
1	80		o: U_SBI/U3/WR:D		Туре	Net I	Name	Cell Na	me Op De	lay (ns)  T	
1	80		io: U_SBI/U3/WR:D Pin Name		Туре	Net I	Name	Cell Na	ame Op De	lay (ns)  T	61.5
1	80		I o: U_SBI/U3/WR:D Pin Name lata required time		Туре	Net I	Name	Cell Na	me Op De	lay (ns) T	61.5
# of paths	80 - 70 - 60 -		to: U_SBI/U3/WR:D Pin Name lata required time lata arrival time lack		Type	Net I	Name	Cell Na	me Op De	ilay (ns)  T	61.5 7.9
# of paths	80 - 70 - 60 - 50 - 40 -		To: U_SBI/U3/WR:D Pin Name lata required time lata arrival time lack Data arrival time calqu	lation	Туре	Net I	Name	Cell Na	nme Op De		61.5 7.9 53.6
# of paths	80 - 70 - 60 - 50 -		In the second se	ulation		Net I	Name	Cell Na	*	0.000	61.5 7.9 53.6 0.0
# of paths	80 - 70 - 60 - 50 - 40 -		Iata required time lata arrival time Lack Data arrival time calc LK8M LK8M	ulation	Clock source		Name		·	0.000	61.5 7.9 53.6 0.0 0.0
# of paths	80 - 70 - 60 - 50 - 40 - 30 - 20 -		In the second se		Clock source net C	CLK8M			+ +	0.000	61.5 7.9 53.6 0.0 0.0 0.0
# of paths	80		In the second se	F:PAD	Clock source net C				+ + +	0.000 0.000 0.000 0.000 0.000	61.5 7.9 53.6 0.0 0.0 0.0 0.0
# of paths	80 - 70 - 60 - 50 - 40 - 30 - 20 -		In the second se	F:PAD F:GL	Clock source net C net C cell	CLK8M J_IO_BUFFE		ADLIB:6	+ + +	0.000	61.5 7.9 53.6 0.0 0.0

Path Slack Histogram

Path Details



#### See Also

SmartTime Constraint Scenario



# Analyzing Your Design

The timing engine uses the following priorities when analyzing paths and calculating slack:

- 1. False path
- 2. Max/Min delay
- 3. Multi-cycle path
- 4. Clock

When multiple constraints of different priorities are set on the same timing path, the constraint with the higher priority overrides the constraint with a lower priority. The False Path constraint has the highest priority on a path and overrides all other constraints on the same path.

If multiple constraints of the same priority apply to a path, the timing engine uses the tightest constraint. You can perform two types of timing analysis: Maximum Delay Analysis and Minimum Delay Analysis.

#### To perform the basic timing analysis:

- 1. Open the Timing Analysis View using one of the following methods:
  - In the Design Flow window, click **Verify Timing > Open Interactively** to display the SmartTime Maximum Delay Analysis View.
  - From the SmartTime Tools menu, choose Max Delay Analysis or Min Delay Analysis.
  - Click the isometry in the constraint of the second s

Note: When you open SmartTime from Libero (Verify Timing > Open Interactively), the Maximum Delay Analysis window is displayed by default.

um Delay Analysis View													
Analysis for scenario min	Fro	n -					то •						
▲ 🕅 Summary	Cu	stornize table								Apply Filter	Store Filter	Reset Fi	iter
Register to Register     X External Hold		Source Pin		Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Ho	ld (ns)	Skew (ns)		
Clock to Output Register to Asynchronous	1	Qeux[3]:CUX	Qauriji	1D	0.337	0.004	E.A.I	2.14	ŝ	0.000	3	0.033	1
External Removal Asynchronous to Register	2	Qaux[2]:CLK	Qaux[2	1D	0.338	0.305	2.453	2.14		0.000	4	0.033	
▲ SE Pin to Pin Input to Output	3	Qeux[1]:CLK	Qaux[1	D.	0.393	0.360	2.507	2.14		0.000		0.033	E
★ XX User Sets     ✓ Qauxd_filter	4	Qaux[1]:CLK	Qaux(2	1:D	0.394	0.360	2.508	2.14		0.000	9	0.034	
✓ Qaux2 filter ✓ Qaux3 filter	5	Qeux[1]:CLK	Qarox[3	I:D	0.395	0.362	2.509	2.14		0.000	1	0.033	
	6	Qaux(0):CLK	Qaux(1	iD.	0.404	0.365	2.512	2.14		0.000		0.039	
	7	Qeux[2]:CLK	Qeux[3	tD	0.434	0.402	2.549	2.14		0.000	9	0-032	
10	Nar	ne	-	Туре	Net	-	Macro	Op Delay	Total I	Fanout Edge		-	
a 6 4	1000	Summary data arrival time data required time slack						2	2.451 2.147 0.304				1
2	1	Data_arrival_time_calcula CLK CLK		Clock source				+ 0.00	0.000	,			
0.194 0.304 0.414 0.524 0.634		CLK_ibuf/U0/U_JOPAD CLK_ibuf/U0/U_JOPAD		net cell	CLK		401 18-101		0.000	2 1			

Figure 98 · Minimum Delay Analysis View

- 2. In the Domain Browser, select the clock domain. Clock domains with a vindicate that the timing requirements in these domains were met. Clock domains with an x indicate that there are violations within these domains. The Paths List displays the timing paths sorted by slack. The path with the lowest slack (biggest violation) is at the top of the list.
- 3. Select the path to view. The Path Details below the Paths List displays detailed information on how the slack was computed by detailing the arrival time and required time calculation. When a path is violated, the slack is negative and is displayed in red color.
- 4. Double-click the path to display a separate view that includes the path details and schematic view.
  - Note: In cases where the minimum pulse width of one element on the critical path limits the maximum frequency for the clock, SmartTime displays an icon for the clock name in the Summary List. Click the icon to display the name of the pin that limits the clock frequency.



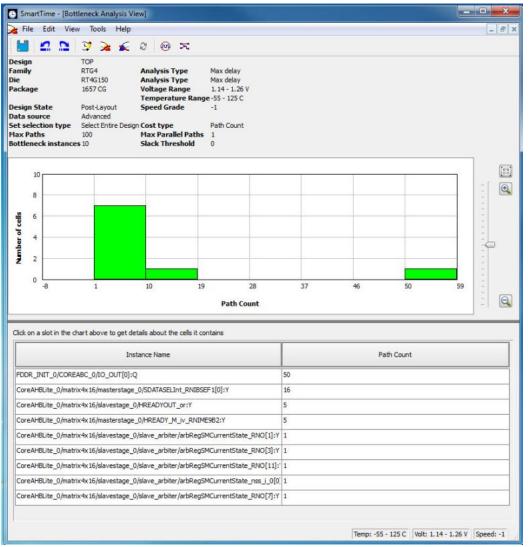
5. Repeat the above steps as required.

# Performing a Bottleneck Analysis

#### To perform a bottleneck analysis

- 1. From SmartTime's Max/Min Delay Analysis View, select **Tools > Bottleneck Analysis**. The **Timing Bottleneck Analysis Options** dialog box appears.
- 2. Select the options you wish to display for bottleneck information and click OK.

The Bottleneck Analysis View appears in a separate window (see image below).



#### Figure 99 · Bottleneck Analysis View

A bottleneck is a point in the design that contributes to multiple timing violations. The Bottleneck Analysis View contains two sections:

- Device Description
- Bottleneck Description

#### **Device Description**

The device section contains general information about the design and the parameters that define the bottleneck computation:



- Design name
- Family
- Die
- Package
- Design state
- Data source
- Set selection type
- Max paths
- Bottleneck instances
- Analysis type
- Analysis max case
- Voltage
- Temperature
- Speed grade
- Cost type
- Max parallel paths
- Slack threshold

#### **Bottleneck Description**

This section displays a graphic representation of the bottleneck analysis and lists the core of the bottleneck information for the bar selected in the chart above. If no bar is selected, the grid lists all bottleneck information.

Click the controls on the right to zoom in or out the contents in the chart.

Right-click the chart to export the chart or to copy the chart to the clipboard.

The list is divided into two columns:

- Instance name: refers to the output pin name of the instance.
- Bottleneck cost: displays the pin's cost given the chosen cost type. Pin names are listed in decreasing
  order of their cost type.

#### See Also

Timing Bottleneck Analysis Options dialog box (SmartTime)

### Managing Clock Domains

In SmartTime, timing paths are organized by clock domains. By default, SmartTime displays domains with explicit clocks. Each clock domain includes at least three path sets:

- Register to Register
- External Setup (in the Maximum Analysis View) or External Hold (in the Minimum Analysis View)
- Clock to Out

You must select a path set to display a list of paths in that specific set.

#### To manage the clock domains:

- 1. Right-click anywhere in the Domain Browser, and choose **Manage Clock Domains**. The <u>Manage</u> <u>Clock Domains</u> dialog box appears (as shown below).
- Tip: You can click the icon in the SmartTime window bar to display the Manage Clock Domains dialog box.



vailable clock domains:		Show the clock don my_clk	nains in this order:
	Add		
	Remov	/e	
	Movel	qt	
	Move Do	wn	

Figure 100 · Manage Clock Domains Dialog Box

- 2. To add a new domain, select a clock domain from the **Available clock domains** list, and click either **Add** or **New Clock** to add a non-explicit clock domain.
- 3. To remove a displayed domain, select a clock domain from the **Show the clock domain in this order** list, and click **Remove**.
- 4. To change the display order in the Domain Browser, select a clock domain from the **Show the clock** domainin this order list, and then use the **Move Up** or **Move Down** to change the order in the list.
- 5. Click **OK**. SmartTime updates the Domain Browser based on your specifications. If you have added a new clock domain, then it will include at least the three path sets as mentioned above.

#### See Also

Manage Clock Domains Dialog Box

# Managing Path Sets

You can create and manage custom path sets for timing analysis and tracking purposes. Path sets are displayed under the **Custom Path Sets** at the bottom of the Domain Browser.

#### To add a new path set:

- 1. Right-click anywhere in the Domain Browser, and choose **Add Set**. The <u>Add Path Analysis Set Dialog</u> <u>Box</u> dialog box appears (as shown below).
- Tip: You can click the icon in the SmartTime window bar to display the Add Path Analysis Set dialog box.



Add Path Analysis Set			X
Name:	Trace from: •	Source to sink	C Sink to source
Source Pins:	Sink Pins:		
DDR0/U0:CLK DDR1/U0:CLK DDREG2/INBUF_LVDS_0_inst/U0/U2_DDR1:C FIFO_inst/FIFO64K36_FULL:RCLK FIFO_inst/FIFO64K36_Q_0_inst:RCLK RAM_inst/RAM64K36_Q_0_inst:WCLK RAM_inst/RAM64K36_Q_1_inst:RCLK RAM_inst/RAM64K36_Q_1_inst:WCLK Rdf_pll0/U0:CLK Rdf_pll1/U0:CLK XCMP33/U0/U2_DDR1:CLK XCMP33/U0/U2_DDR2:CLK			
Select All	Select	All	
Filter source pins:	Filter sin	k pins:	
Pin Type: Registers by pin names	] Pin 1	ype: Register	s by pin names 💌
* Filter	*		Filter
Help	0	<	Cancel

Figure 101 · Add Path Analysis Set Dialog Box

- 2. Enter a name for the path set.
- 3. Select the source and sink pins. You can <u>use the filters</u> to control the type of pins displayed.
- 4. Click **OK**. The new path set appears under **Custom Path Sets** in the Domain Browser (as shown below).



SmartTime -	[Maximum Delay Analysis View]										- 🗆 🗙
🕒 File Edit	View Tools Help										_ 6 >
🖬 🙇 🤉	2 37 泽 🖌 8 🐵 🛪										
Maximum Delay Ar	nalysis View										
MAX Pri	alysis for scenario mary mary my_clik		m •			то •	Apply Fil	ter St	re Filter	Reset	t Filter
	Register to Register		Source Pin			Sink Pin			Slack		—
	Clock to Output					Jank Pan		(ns)	(ns)		
	legister to Asynchronous	1									
	xternal Recovery Asynchronous to Register										
	Pin to Pin										
	nput to Output										
4 2010	Jser Sets										
l r	ny_set										
		Nan	ne	Туре	Net		Macro	(	p Delay	Total	Fanol *
			Summary								
			data required time							N/C	E
			data arrival time							9.781 N/C	_
			slack Data arrival time calculation							N/C	
	This set has no path.		my_clk						0.000	0.000	
# of paths	This act has no pour.		CLK	Clock source						0.000	
2			CLK_ibuf/U0/U_IOPAD:PAD	net	CLK				0.000	0.000	
2			CLK_ibuf/U0/U_IOPAD:Y	cell			ADLIB:IOPAD_IN		2.128	2.128	
		-	CLK_ibuf_RNIVQ04:An	net	CLK_ibuf		_			2.480	-
		1	CLIVIT C DEDICOLUCIO				1010 0014		0.105	0 505	•
	slack distribution(ns)										
Ready							Temp:	0 - 85 C	blt: 1.14 -	1.26 V	Speed: STD

Figure 102 · Updated Domain Browser with User Sets

#### To remove an existing path set:

- 1. Select the path set from the User Sets in the Domain Browser.
- 2. Right-click the set to delete, and then choose Delete Set from the right-click menu.

#### To rename an existing path set:

- 1. Select the path set from User Set in the Domain Browser.
- 2. Right-click the set to rename, and then choose Rename Set from the right-click menu.
- 3. Edit the name directly in the Domain Browser.

#### See Also

Add Path Analysis Set Dialog Box Using Filters Exporting Files

### **Displaying Path List Timing Information**

The Path List in the Timing Analysis View displays the timing information required to verify the timing requirements and identify violating paths. The Path List is organized in a grid where each row represents a timing path with the corresponding timing information displayed in columns. Timing information is customizable; you can add or remove columns for each type of set.

By default, each type of set displays a subset of columns as follows:

- Register to Register: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, Minimum Period, and Skew.
- External Setup: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, and External Setup.
- Clock to Out: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, and Clock to Out.
- Input to Output: Source Pin, Sink Pin, Delay, and Slack.
- Custom Path Sets: Source Pin, Sink Pin, Delay, and Slack.

You can add the following columns for each type of set:

• Register to Register: Clock, Source Clock Edge, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Maximum Delay Constraint, and Multicycle Constraint.



- External Setup: Clock, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Input Delay Constraint, Required External Setup, Maximum Delay Constraint, and Multicycle Constraint.
- Clock to Out: Clock, Source Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Output Delay Constraint, Required Maximum Clock to Out, Maximum Delay Constraint, and Multicycle Constraint.
- Input to Output: Arrival, Required, Setup, Hold, Logic Stage Count, and Max Fanout.
- Custom Path Sets.

#### To customize the set of timing information in the Path List:

- 1. Select the set to customize.
- 2. Select the whole Paths List by clicking in the upper-left corner.
- 3. Right-click anywhere on the column headings, and then choose **Customize table** from the right-click menu. The <u>Customize Analysis View Dialog Box</u> dialog box appears (as shown below).

Customize Analysis View		
Available fields: Clock Source Clock Edge Destination Clock Edge Clock Constraint (ns) Max Delay Constraint (ns) Multicycle Constraint	Add > < Remove	Show these fields in this order: Source Pin Sink Pin Delay (ns) Slack (ns) Arrival (ns) Required (ns) Setup (ns) Minimum Period (ns) Skew (ns)
Help		Move Up Move Down OK Cancel

Figure 103 · Customize Analysis View Dialog Box

- 4. To add one or more columns, select the fields to add from the Available fields list, and click Add.
- 5. To remove one or more columns, select the fields to remove from the **Show these fields in this order** list, and click **Remove**.
- 6. Click OK to add or remove the selected columns. SmartTime updates the Timing Analysis View.

#### See Also

**Customize Analysis View** 

### **Displaying Expanded Path Timing Information**

SmartTime displays the list of paths and the path details for all parallel paths.



MAX → Strummary → Strummary	From *			То	*					
ି ଭି Summary ଭି Datasheet	,									
					,	Apply F	Filter	Store Filter	Reset Fil	lter
	Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
Register to Regi	1 U SBI/U3/rwra:CLK	U_SBI/U3/WR:D	5.658		7.916	61.571	0.668	12.690	0.019	
💛 Clock to Output	2 U_TOPM031/U_CORE/con f_2[2]:CLK	U_SBI/U4/bram_a[12]:D	48.407	70.731	50.722	121.453	0.867	49.269	-0.005	
External Recovery	3 U_T0PM031/U_C0RE/con f_2[2]:CLK		47.470	71.611	49.785	121.396	0.867	48.389	0.052	
	4 U_TOPM031/U_CORE/con f_1[3]:CLK	U_SBI/U4/bram_a[12]:D	47.412	71.726	49.727	121.453	0.867	48.274	-0.005	
× Register to Regi.	5 U_TOPM031/U_CORE/con f_2[2]:CLK		47.183	71.910	49.498	121.408	0.867	48.090	0.040	
External Setup	6 U_TOPM031/U_CORE/con f_0_0[2]:CLK	U_SBI/U4/bram_a[12]:D	47.269	71.915	49.538	121.453	0.867	48.085	-0.051	
	Details for parallel pa From: U_SBI/U3/rwra To: U_SBI/U3/wR:D			· <u>·</u> ···						
80-	Pin Name	Туре	N	et Name	Cell	Name Op	Delay (ns	) Total (ns) Fa	anout Edg	ge
	Parallel Path #1									
	data required time							61.571		_
40-	data arrival time					•		7.916		_
	slack							53.655		_
20-	Data arrival time calc	ulation								
	CLK8M						0.000			
	CLK8M	Clock source				+	0.000		1	_
40 60 80	U_IO_BUFFERS:CLK8M	net	CLK8M			+	0.000		1	_
slack distribution (ns)	U_IO_BUFFERS/CLK_BU		U_IO_BUI	FFERS/CLK		+	0.000		1521	

Figure 104 · Expanded Path View

The Path List displays all parallel paths in your design. The Path Details grid displays the path details for all parallel paths.

#### To display the Expanded Path View:

From the Path List: double-click the path, or right-click a path and select expand selected paths.

From the Expanded Path View: double-click the path, or right-click the path and select **expand path**.

Path details						Net delay 67.53%		32.479
Pin Name	Туре	Net Name	Cell Name	Op	Delay (ns)	otal (ns)	Fanout Ed	 ge
Data arrival time calculation CLK8M	1				0.000	0.000		_
CLK8M	Clock source	-		+	0.000	0.000	r	-
U IO BUFFERS:CLK8M	net	CLK8M		+	0.000	0.000	1	-
U IO BUFFERS/CLK BUF:PAD		U IO BUFFERS/CLK8M		+	0.000	0.000	r	-
U_IO_BUFFERS/CLK_BUF:GL	cell		ADLIB:GL33	+	1.175	1.175	1534 r	-
U IO BUFFERS:clk8m in	net	U IO BUFFERS/clk8m in		+	0.000	1.175	1	-
U_SBI:clk8m_in	net	clk8m in		+	0.000	1.175	1	-
U_SBI/U3:clk8m_in	net	U_SBI/clk8m_in		+	0.000	1.175	r I	-
U SBI/U3/rwra:CLK	net	U SBI/U3/clk8m in		+	1.083	2.258	r	_
III SRI/II3/nara-O	Cell	1	ADUB-DEE		0 709	2.966	A r	_
	RS/CLK_BUF	U_SBI/U3/rwra D Q CLK DFF	(	J_SE A	BI/U3/nwra 1 V INV		U_SBI/U3A -D ( ) CLK DFFL	

Figure 105 · Expanded Path View

The Expanded Path Summary provides a summary of all parallel paths for the selected path. The Path Profile chart displays the percentage of time taken by cells and nets for the selected path. If no parallel path



is selected in this view, the Path Profile shows the percentage for all paths. By default, SmartTime only shows one path for each Expanded Path. You can change this default in the <u>SmartTime Options</u> dialog box.

The Expanded Path View also includes a schematic of the path and a path profile chart for the paths selected in the Expanded Path Summary.

# **Using Filters**

You can use filters in SmartTime to limit the Path List content (that is, create a filtered list on the source and sink pin names). The filtering options appear on the top of the Timing Analysis View. You can save these filters one level below the set under which it has been created.

#### To use the filter:

- 1. Select a set in the Domain Browser to display a given number of paths, depending on your <u>SmartTime</u> <u>Options</u> settings (100 paths by default).
- 2. Enter the filter criteria in both the **From** and **To** fields and click **Apply Filter**. This limits the display to the paths that match your filter criteria.

From	U_SB*	То	u_TO*		
			Apply Filter	Store Filter	Reset Filter

Figure 106 · Maximum Delay Analysis View

3. Click **Store Filter** to save your filter criteria with a special name. The **Create Filter Set** dialog box appears (as shown below).

Create Filter Set		? ×
Name : my_filter01		
Help	OK	Cancel

Figure 107 · Create Filter Set Dialog Box

4. Enter a name for the filter, such as myfilter01, and click **OK**. Your new filter name appears below the set under which it was created.



(	MAX	Analysis for scenario Primary
[	4 🖏	Summary
		v @ my_clk
		<ul> <li>Register to Register</li> </ul>
		my_filter01
		External Setup
		Clock to Output
		Register to Asynchronous
		External Recovery
		Asynchronous to Register
	⊿	🔁 Pin to Pin
		Input to Output
	⊿	St. User Sets
		my_set

Figure 108 · my\_filter01

		From	U SB*		То	u_TO*				
		From	0_38.		10	[u_10.				
MAX						Appl	y Filter	Store Filter	Rese	t Filter
🖃 🖓 Summary										
- 🖓 Datasheet × 砢 CLK8M			Source Pin	Sink Pin	Delay	Slack,	Arrival	Required	Setup	Min
Register to Re	ai la		Jource I III		(ns)	(ns) 🦈	(ns)	(ns)	(ns)	Peri
External Setup		1 U_S	681/U1/A[15]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	43.496	75.612	45.790	121.402	0.867	
Clock to Outpu		2 11 6		U TOPM031/U CORE/evel				101.100		
Register to Async		- U_S	SBI/U1/A_0[2]:CLK	nts[15]:D	43.178	75.937	45.465	121.402	0.867	
External Recovery	y [	3 U S	BI/U1/WRITE:CLK	U_TOPM031/U_CORE/eve	42,393	76.728	44.674	121.402	0.867	
Asynchronous to	Re			nts[15]:D						
🖻 🗡 💮 PLL_CLK_IN		4 U_S	SBI/U1/A_0[8]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	42.387	76.746	44.656	121.402	0.867	
🛛 🗙 Register to Rej	gi 🛉	5		U TOPM031/U CORE/eve	42.227	76.898	44 501	121,419	0.867	
External Setup			SBI/U1/A[15]:CLK	nts[14]:D	42.227	76.838	44.521	121.419	0.867	
Clock to Output	. <b>-</b>	6 U S	BI/U1/A[15]:CLK	U_TOPM031/U_CORE/eve	42.030	77.078	44.324	121.402	0.867	
		7		nts[13]:D U TOPM031/U CORE/eve						
		1 U_9	6BI/U1/A[4]:CLK	nts[15];D	42.028	77.101	44.301	121.402	0.867	
100	II	8 11 9	BI/U1/A[13]:CLK	U_TOPM031/U_CORE/eve	41.987	77.142	44.260	121,402	0.867	
90-	_	10-0	DIVO INA[10]:CEK	nts[15]:D	41.501	11.142	44.200	121.402	0.001	
		<								>
80 -			Details for parallel p							
70-			From: U_SBI/U1/A	15]:CLK _CORE/events[15]:D						
10			10: U_10FM03170	Pin Name		T	уре	Net Name	Cell Na	0n
60-		Parallel				·	Jbc .	The traine	<u>j cen rraj</u>	001
. 50 -		Path #1								
50-			data required time							
40			data arrival time							
			slack							
30 -										
20 -			Data arrival time ca CLK8M	iculation						
20			CLK8M			Clock s	ource			+
10-			J IO BUFFERS:CLK8	M		net		CLK8M		+
			J IO BUFFERS/CLK			net		U IO BUFFER		+
	80		J IO BUFFERS/CLK			cell			ADLIB:G	· ·
40 00			J IO BUFFERS:clk8m			net		U IO BUFFER		+
slack distribution (										

Figure 109 · Updated Maximum Delay Analysis View

Repeat the above steps and cascade as many sets as you need using the filtering mechanism.



#### To remove a set created with filters:

- 1. Select the set that uses filters.
- 2. Right-click the set, and choose Delete Set from the shortcut menu.

#### To rename a set created with filters:

- 1. Select the set that uses filters.
- 2. Right-click the set, and choose Rename Set from the shortcut menu.
- 3. Edit the name directly in the Domain Browser.

#### To edit a specific filter in the set:

- 1. Select the filter to edit.
- 2. Right-click the filter, and choose Edit Set from the shortcut menu.

#### See Also

SmartTime Options Store Filter as Analysis Set Edit Set dialog box Exporting Files



# **Advanced Timing Analysis**

### **Understanding Inter-Clock Domain Analysis**

When functional paths exist across two clock domains (the register launching the data and the one capturing it are clocked by two different clock sources), you must provide accurate specification of both clocks to allow a valid inter-clock domain timing check. This is important especially when the clocks are specified with different waveforms and frequencies.

When you specify multiple clocks in your design, the first step is to consider whether the inter-clock domain paths are false or functional. If these paths are functional, then you must perform setup and hold checks between the clock domains in SmartTime. Unless specified otherwise, SmartTime considers the inter-clock domain as false, and therefore does not perform setup or hold checks between the clock domains.

If you have several clock domains that are subset of a single clock (such as if you want to measure clock tree delay from an input clock to a generated clock), you must configure Generated Clock Constraints for each of the clock domains in order for SmartTime to do execute the calculation and show timing for each of the inter-clock-domain paths.

Once you include the inter-clock domains for timing analysis, SmartTime analyzes for each inter-clock domain the relationship between all the active clock edges over a common period equal to the least common multiple of the two clock periods. The new common period represents a full repeating cycle (or pattern) of the two clock waveforms (as shown below).

For setup check, SmartTime considers the tightest relation launch-capture to ensure that the data arrives before the capture edge. The hold check verifies that a setup relationship is not overwritten by a following data launch.

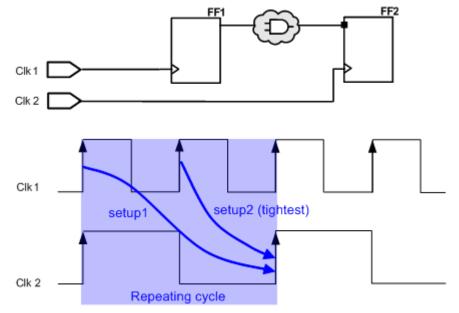


Figure 110 · Example Showing Inter-Clock Domains

#### See Also

Activating inter-clock domain analysis Deactivating a specific inter-clock domain Displaving inter-clock domain paths

# Activating Inter-Clock Domain Analysis

#### To activate the inter-clock domain checking:

- 1. In SmartTime, from the **Tools** menu choose **Options**. The <u>SmartTime Options Dialog Box</u> dialog box appears (as shown below).
- 2. In the general category, check the Include inter-clock domains in calculations for timing analysis.

SmartTime Options		? <b>×</b>
Option Categories Select a category: General Analysis Advanced	General         Operating Conditions         Perform maximum delay analysis based on         WORST         Perform minimum delay analysis based on         BEST         Clock Domains         Include inter-clock domains in calculations for timing analysis.         Include inter-clock domains in calculations for timing analysis.         Image: Second sec	case     case     Restore Defaults
Help		OK Cancel

Figure 111 · SmartTime Options Dialog Box

3. Click **OK** to save the dialog box settings.

#### See Also

Inter-Clock Domain Analysis Deactivating a Specific Inter-Clock Domain Displaying Inter-Clock Domain Paths

### **Displaying Inter-Clock Domain Paths**

Once you <u>activate the inter-clock domain checking</u> for a given clock domain CK1, SmartTime automatically detects all other domains CKn with paths ending at CK1. SmartTime creates inter-clock domain sets CKn to CK1 under the domain CK1. Each of these sets enables you to display the inter-clock domain paths between a given clock domain and CK1.

#### To display an inter-clock domain set:

- 1. Expand the receiving clock domain of the inter-clock domain in the Domain Browser to display its related sets. For the inter-clock domain CK1 to CK2, expand clock domain CK2.
- Select the inter-clock domain that you want to see expanded from these sets. Once selected, all paths between the related two domains are displayed in Paths List in the same way as any register to register set.



łaximum Delay Analysis V	iew										
Analysis for scenario	Fron	n *				To	*				
A Primary Scenario											
ର୍ଦ୍ଧି Summary 🔺								Apply Filter	Store	Filter	Reset Fil
୍ତ୍ରୀ Summary 🔺 ୍ରି Datasheet							-	<u> </u>			
⊡ × @ av1_ck		Source Pin		Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)		
Register to Regi.	1	control_word_0[0]:CLK	ufo/fo_r	:ntr[13]:D	7.793				0.381		
External Setup	2	control word 0[0]:CLK	ufp/fp_0		7.575		8.913		0.381		
Clock to Output	3	control_word_0[0]:CLK	ufp/fp_0		7.431	-1.121	8.76		0.381		
Register to Asynchrc	4	control word 0[0]:CLK		ntr[12]:D	7.220		8.55		0.357		
External Recov	5	control word 0[0]:CLK	ufp/fp (		7,194		8.53	2 7.623	0.381		
Asynchronous to Re	6	control word 0101:CLK		entr[14]:D	7,192	-0.909	8.53	7.621	0.381		
× cpu clk to av1	7	control_word_0[0]:CLK	ufp/fp_c		7.100	-0.821	8.43	3 7.617	0.381		
- × (m) cpu clk	8	control_word_0[0]:CLK	ufp/fp_c	:ntr[10]:D	7.085	-0.792	8.42	3 7.631	0.381		
× Register to Regi.	9	control_word_0[0]:CLK	ufp/stre	tch_fp[3]:D	7.082	-0.773	8.420	7.647	0.381		
× External Setup	10	control word 0101:CLK	ufn/fn_r	ntr[15]·D	6 942	-0.659	8 28	1 7.621	0 381		
Clock to Output		Details for parallel path	18								
Register to Asynchrc		From: control_word_0[0	D]:CLK								
<ul> <li>External Recov</li> </ul>		To: ufp/fp_cntr[13]:D							1 - 1 -		
Asynchronous to Re		Pin Name		Туре	<u> </u>	et Name		Cell Name	Op	elay (ns)	
av1 clk to cpu		slack									-1.51
= 🔀 Pin to Pin											
North		Data arrival time calcu	lation							0.000	
The Sate		cpu_clk		ei 1						0.000	0.00
		cpu_clk cpu_clk_pad/U0/U0:PAD		Clock source					+	0.000	0.00
	. —	cpu_cik_pad/00/00.PAD cpu_cik_pad/U0/U0:Y		net cell	cpu_clk			ADLIB:IOPAD IN		0.632	0.00
4		cpu_cik_pad/00/00.1		net	cpu_clk_pao	ULLO MET		ADLIB.IOFAD_IN	+	0.632	0.6
		cpu_cik_pad/00/01:A		cell	сри_ск_рас	JUUVINET		ADLIB:CLKIO	+	0.000	0.86
2		control word 0[0]:CLK		net	cpu clk c			ADEID.CENIO	+	0.231	1.33
		control_word_0[0];02:K		cell	cpu_cik_c			ADLIB:DFN1E10		0.489	1.82
0-		ufp/un1 fp cntr 2 i 0 a3			control word	1 0101		ADEID.DITATETC	+ 0,0	1.259	3.08
8		ufp/un1_fp_cntr_2_i0_a3				_0[0]		ADLIB:NOR2	+	0.337	3.42
° 1		ufp/un1 fp cntr 2 i 0 a3		net	ufp/un1 fp	cn tr 2 i 0		PIDEID: NOTIE	+	0.237	3.66
6		ufp/un1 fp cntr 2 i 0 a3		cell	apran_ip_	0110_0_1_0		ADLIB:NOR3A	+	0.441	4.10
		ufp/un1_fp_cntr_2_i0_a3		net	ufp/un1_fp_	cn tr. 2 i 0			+	0.729	4.83
4		ufp/un1 fp cntr 2 i 0 a3		cell	alpi all'_ip_			ADLIB:NOR3C	+	0.442	5.27
2		ufp/un1_fp_cntr_2_i_0_a3		net	ufp/un1_fp	cn tr 2 i 0			+	0.237	5.50
2		ufp/un1 fp cntr 2 i 0 a3		cell				ADLIB:NOR3C	+	0.442	5.95
		ufp/un1 fp cntr 2 i 0 o2:		net	ufp/un1_fp	cn tr 2 i 0	a3 0 10		+	0.288	6.23
0		ufp/un1 fp cntr 2 i 0 o2:		cell				ADLIB:0A1	+	0.653	6.89
		ufp/fp_cntr_6_0_a2[13]:C		net	ufp/un1_fp_	cn tr 2 i 0	o2 n		+	1.784	8.67
8		ufp/fp_cntr_6_0_a2[13]:Y		cell				ADLIB:XA1B	+	0.228	8.90
		ufp/fp_cntr[13]:D		net	ufp/fp_cntr_	6[13]			+	0.227	9.13
6		data arrival time	ĺ				i			i	9.13
4		Data required time calc									
		av1_clk		Clock Constraint						6.667	6.68
2		av1_clk		Clock source					+	0.000	6.66
		av1_clk_pad/U0/U0:PAD		net	av1_clk				+	0.000	6.66
-5 0 5 10		av1_clk_pad/U0/U0:Y		cell				ADLIB:IOPAD_IN		0.632	7.29
		av1_olk_pad/U0/U1-A		nał	aut alk nar	LULIO BUE T			4	0.000	7.29

Figure 112 · Maximum Delay Analysis View

#### See Also

Inter-Clock Domain Analysis Activating Inter-Clock Domain Analysis Deactivating a Specific Inter-Clock Domain

# Deactivating a Specific Inter-Clock Domain

To deactivate the inter-clock domain checking for the specific clock domains clk2->clk1, without disabling this option for the other clock domains:

- 1. From the Tools menu, choose Constraints Editor to open the Constraints Editor View.
- In the Constraints Browser, double-click False Path under Exceptions. The <u>Set False Path Constraint</u> dialog box appears.
- 3. Click the **Browse** button to the right of the **From** text box. The **Select Source Pins for False Path Constraint** dialog box appears.
- 4. For Specify pins, select by keyword and wildcard.
- 5. For Pin Type, select Registers by clock names from the Pin Type drop-down list.
- 6. Type the inter-clock domain name, for example Clk2, in the filter box and click Filter.
- 7. Click **OK** to begin filtering the pins by your criteria. In this example, [get\_clocks {Clk2}] appears in the **From** text box in the <u>Set False Path Constraint</u> dialog box.



- 8. Repeat steps 3 to 7 for the **To** option in the <u>Set False Path Constraint</u> dialog box, and type Clk2 in the filter box.
- 9. Click OK to validate the new false path and display it in the Paths List of the Constraints Editor.
- 10. Click the Recalculate All button 2 in the toolbar.
- 11. Select the inter-clock domain set clk2 -> clk1 in the Domain Browser (as shown below).
- 12. Verify that the set does not contain any paths.

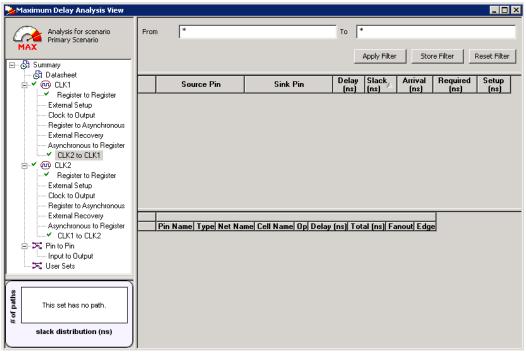


Figure 113 · Maximum Delay Analysis View

#### See Also

Inter-Clock Domain Analysis Activating Inter-Clock Domain Analysis Displaying Inter-Clock Domain Paths Select Source or Destination Pins for Constraint Dialog Box Set False Path Constraint Dialog Box

### **Timing Exceptions Overview**

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the
  optimization flow.
- Setting a maximum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

#### See Also

Specifying a Maximum Delay Constraint Specifying a Minimum Delay Constraint Specifying a Multicycle Constraint Specifying a False Path Constraint



Changing Output Port Capacitance

# Specifying a Maximum Delay Constraint

You set options in the <u>Set Maximum Delay Constraint</u> dialog box to relax or to tighten the original clock constraint requirement on specific paths.

#### To specify Max delay constraints:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set Maximum Delay Constraint</u> dialog box using one of the following methods:
  - Click the icon in the Constraints Editor.
  - From the Constraints Editor, right-click the Constraints menu and choose **Max delay**. The Set Maximum Delay Constraint dialog box appears (as shown below).

Set Maximum Delay Constraint	X
Maximum delay: ns	
From:	
Through:	
To:	
Comment:	_
Help OK Cancel	

Figure 114 · Set Maximum Delay Constraint Dialog Box

- 2. Specify the delay in the Maximum delay field.
- 3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for Max Delay Constraint dialog box (as shown below).



Select Source Pi	ins for Max Delay	Constraint		×
Specify pins	• by explicit list	🔘 by keyword and wild	lcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
∫ oaux[4]:CLK	e objects:		,	
Pin Type:	All pins	-		
*		Filter		
Help			ОК	Cancel

Figure 115 · Select Source Pins for Max Delay Constraint

- 4. Select by explicit list. (Alternatively, you can select by keyword and wildcard.)
- 5. Select the input pin(s) from the **Available Pins** list. You can also use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- 7. Click OK. The Set Maximum Delay Constraint dialog box displays the updated From pin(s) list.
- 8. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click OK.

SmartTime adds the maximum delay constraints to the Constraints List in the SmartTime Constraints Editor.

#### See Also

Timing Exceptions Overview Set Maximum Delay Constraint dialog box Specifying Maximum Delay Constraint Specifying Multicycle Constraint Specifying False Path Constraint Changing Output Port Capacitance



# Specifying a Minimum Delay Constraint

You set options in the <u>Set Minimum Delay Constraint</u> dialog box to relax or to tighten the original clock constraint requirement on specific paths.

#### To specify Min delay constraints:

- 1. Open the Set Minimum Delay Constraint dialog box using one of the following methods:
  - Click the <sup>22</sup> icon in the Constraints Editor.
  - From the Constraints Editor, right-click the Constraints Menu and choose **Min delay**. The Set Minimum Delay Constraint dialog box appears (as shown below).

Set Minimum Delay Constraint	X
Minimum delay:	
From:	
Through:	
To:	
	]
Comment:	1
Help OK Cancel	]

Figure 116 · Set Minimum Delay Constraint Dialog Box

- 2. Specify the delay in the Minimum delay field.
- 3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for Min Delay Constraint dialog box (as shown below).



Select Source Pi	ins for Min Delay	y Constraint		
Specify pins	• by explicit list	C by keyword and wild	lcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
Filter available	e objects:		,	
Pin Type:	All pins	•		
*		Filter		
Help			ОК	Cancel

Figure 117 · Select Source Pins for Min Delay Constraint

- 4. Select by explicit list. (Alternatively, you can select by keyword and wildcard.)
- 5. Select the input pin(s) from the **Available Pins** list. You can also use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- 7. Click OK. The Set Minimum Delay Constraint dialog box displays the updated From pin(s) list.
- 8. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click OK.

SmartTime adds the minimum delay constraints to the Constraints List in the SmartTime Constraints Editor.

#### See Also

Timing Exceptions Overview Set Maximum Delay Constraint dialog box Specifying Maximum Delay Constraint Specifying Multicycle Constraint Specifying False Path Constraint Changing Output Port Capacitance



# Specifying a Multicycle Constraint

You set options in the <u>Set Multicycle Constraint</u> dialog box to specify paths that take multiple clock cycles in the current design.

To specify multicycle constraints:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set Multicycle Constraint</u> dialog box using one of the following methods:
  - From the SmartTime Constraints Editor, choose Constraint > MultiCycle.
  - Click the Ricon.
  - Right-click the **Multicycle** option in the Constraint Browser and select **Add Multicycle Path Constraint**.

The Set Multicycle Constraint dialog box appears (as shown below).



et Multicycle Constraint	
Specify multiplier(s) for:  Setup Check only Setup Path Multiplier: Default setup edge	New setup
Hold edge	
Through:	····
To:	····
Comment:	<ul> <li></li> </ul>
Help OK	Cancel

Figure 118 · Set Multicycle Constraint Dialog Box

- 2. Specify the number of cycles in the Setup Path Multiplier.
- 3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for Constraint dialog box (as shown below).



Select Source Pins for Multicycle ( Specify pins :-	
Available Pins:	Assigned Pins:
FDDR_DM_RDQS FDDR_DM_RDQS[0] FDDR_DM_RDQS[1] FDDR_DQ FDDR_DQS FDDR_DQS[0] FDDR_DQS[1] FDDR_DQS_N FDDR_DQS_N[0] FDDR_DQS_N[1] FDDR_DQS_N[1] FDDR_DQS_TMATCH_0_IN	Add Add All Remove Remove All
Filter available pins :	Help
Pin Type : Input Ports	▼ OK
	Cancel

Figure 119 · Select Source Pins for Multicycle Constraint

- 4. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to the <u>Select Source or Destination Pins for Constraint Dialog Box</u>.)
- 5. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All to move theinput pin(s) move from the Available pins list to the Assigned Pins list.
- 7. Click OK.

The Set Multicycle Constraint dialog box displays the updated representation of the **From** pin(s) (as shown below).



Set Multicycle Constraint	×
Specify multiplier(s) for:  © Setup Check only © Setup and Hold Checks	
Setup Path Multiplier:	
Default setup edge Hold edge	ew setup edge
From: Aclr Clock Enable qaux[0]:CLK Clock Through:	
To:	
Comment:	
Help OK Cano	el

Figure 120 · Set Multicycle Constraint Dialog Box

- 8. Click the browse button for **Through** and **To** and add the appropriate pins. The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click **OK**. SmartTime adds the multicycle constraints to the Constraints List in the SmartTime Constraints Editor.

#### See Also

Set Multicycle Constraint Dialog Box

# Specifying a False Path Constraint

You set options in the Set False Path Constraint dialog box to define specific timing paths as false.

#### To specify False Path constraints:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set False Path Constraint</u> dialog box. You can do this by using one of the following methods:
  - From the SmartTime Constraints menu, choose False Path.
  - Click the 🙆 icon.
  - Right-click **False Path** in the Constraint Browser and choose **Add False Path Constraint**. The Set False Path Constraint dialog box appears (as shown below).

t False Path Constraint	2
From:	
1	
	×
Through:	
<	>
To:	
	~
<	>
·	
Comment:	
Help	OK Cancel

Figure 121 · Set False Path Constraint Dialog Box

2. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for False Path Constraint dialog box (as shown below).



Select Source Pi	ns for False Pat	h Constraint		
Specify pins	• by explicit list	🔿 by keyword and wild	dcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
gaux[4]:CLK ┌ Filter available	e objects:		1	
Pin Type:	All pins			
*		Filter		
,				
Help			ОК	Cancel

Figure 122 · Select Source Pins for False Path Constraint Dialog Box

- 3. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to <u>Select Source or Destination Pins for Constraint Dialog Box</u>.)
- Select the input pin(s) from the Available Pin list. You can use Filter available objects to narrow the pin list. You can select multiple ports in this window.
- 5. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- Click OK.
   The <u>Set False Path Constraint</u> dialog box displays the updated representation of the From pin(s).
- 7. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 8. Enter comments in the **Comment** section.
- 9. Click OK.

SmartTime adds the False Path constraints to the Constraints List in the SmartTime Constraints Editor.

#### See Also

Set False Path Constraint Dialog Box

### **Changing Output Port Capacitance**

Output propagation delay is affected by both the capacitive loading on the board and the I/O standard. The I/O Attribute Editor in ChipPlanner provides a mechanism for setting the expected capacitance to improve the propagation delay model. SmartTime automatically uses the modified delay model for delay calculations.



To change the output port capacitance and view the effect of this change in SmartTime Timing Analyzer, refer to the following example. The figure below shows the delay from FF3 to output port OUT2. It shows a delay of 6.603 ns based on the default loading of 35 pF.

≽ Maximum Delay An	alysis View								_ 🗆	×
Analysis for Primary Scen		From	*		То					
MAX						Apply Filter	Store	Filter F	Reset Filter	1
⊡ 🖓 Summary										-
⊡ ✓ @ CLK2			Source Pin	Sink Pin	(ns)	(ns)	Arrival (ns)	Required (ns)	Clock ta Out (ns)	1
	o Register 🛛 📔		3:CLK	OUT2	4.995		6.603		6.6	
External Set	·		39/RAMBLOCK0:CLKA	DATAOUTRAM(3)	6.300		8.121		8.13	
Clock to Out			39/RAMBLOCK0:CLKA	DATAOUTRAM(1)	6.234		8.055		8.0	
	synchronous		39/RAMBLOCK0:CLKA	DATAOUTRAM(0)	5.801		7.622		7.6	
External Rec	covery us to Register	5 \$113	39/RAMBLOCK0:CLKA	DATAOUTRAM(2)	5.658		7.479		7.4	79
⊕ ✓ @ CLK3 ⊕ ✓ @ CLK4 ⊖ ∑ Pin to Pin Input to Outy ∑ User Sets	out	Fro	tails for path m: FF3:CLK OUT2							
		FF3	Pin Name	cell	Ne	t Name	ADLIB	Name	<u>Op I</u> +	
			D_2:A	net	\$1N26		ADLIB	.0110	+	
			D_2:X	cell	\$11420		ADLIB	AND2	+	
			T2 pad/U0/U1:D	net	OUT2 c				+	
0	]		T2_pad/U0/U1:DOUT	cell			ADLIB	IOTRI OB EI		
🗧 This set has n			T2_pad/U0/U0:D	net	OUT2 pa	J/U0/NET1			+	
This set has n for any of its	paths.		12_pad/U0/U0:PAD	cell			ADLIB	IOPAD_TRI	+	
#		001	T2	net	OUT2				+	
slack distribut	ion (ns)	data	a arrival time							Ţ.
		۱'		ĩ	ï					

Figure 123 · Maximum Delay Analysis View

If your board has output capacitance of 75pf on OUT2, you must perform the following steps to update the timing number:

1. Open the I/O Attribute Editor and change the output load to 75pf.

	Port Name	Macro Cell	Pin #	Locked	Bank Name	V0 Standard	Output Drive (mA)	Slew	Resistor Pull	Skew	Output Load	Use I/O Reg
1	CLK2	ADLIB:CLKBUF	13	<b>[</b> ]	Bank1	LVTTL			None			Г
2	CLK4	ADLIB:INBUF	15		Bank1	LVTTL			None	-		Г
3	WADDR(3)	ADLIB:INBUF	85		Bank0	LVTTL			None			Г
4	DATAOUTRAM(2)	ADLIB:OUTBUF	86		Bank0	LVTTL	12	High	None	Г	35	Г
5	OUT2	ADUB:OUTBUF	16		Bank1	LVTTL	12	High	None		75	

Figure 124 · I/O Attribute Editor View

- 2. Select File > Save.
- 3. Select File > Close.
- 4. Open the SmartTime Timing Analyzer.

You can see that the Clock to Output delay changed to 7.723 ns.

# Specifying Clock Source Latency

Use clock source latency to specify the delay from the clock generation point to the clock definition point in the design.

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint.

You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

#### To specify the clock source latency:

1. Add the constraint in the <u>Editable Constraints Grid</u> or open the Set Clock Source Latency dialog box using one of the following methods:



- From the SmartTime Constraints Editor window, choose Constraints > Clock Source Latency.
- Click the icon in the Constraints Editor.
- Click Clock Source Latency in the Constraint Browser.
- Select a clock pin on which to set the source latency. You can only specify a clock source latency on a clock pin that has a clock constraint. Additionally, you may apply only one clock source latency constraint to each constrained clock pin.
- 3. Enter the Late Rise, Early Rise, Late Fall, and Early Fall values as required for your design.
  - Note: An 'early' value larger than a 'late' value can result in optimistic timing analysis.
- 4. Select the **Falling Same As Rising** check box to indicate that falling clock edges have the same latency as rising clock edges.
- 5. Select the **Early Same As Late** check box to use a single value for the clock latency, rather than a range, by clicking the checkbox.
- 6. Enter any comments to be attached to the constraint.
- 7. Click OK. The new constraint appears in the constraints list.
  - Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

### See Also

Set Clock Source Latency Dialog Box

# Specifying a False Path Constraint

You set options in the Set False Path Constraint dialog box to define specific timing paths as false.

#### To specify False Path constraints:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set False Path Constraint</u> dialog box. You can do this by using one of the following methods:
  - From the SmartTime **Constraints** menu, choose **False Path**.
  - Click the <sup>1</sup>/<sub>2</sub> icon.
  - Right-click False Path in the Constraint Browser and choose Add False Path Constraint. The Set False Path Constraint dialog box appears (as shown below).

t False Path Constraint	×
From:	
1	
<	
Through:	
<	>
To:	
<	>
Comment:	
,	
Help	OK Cancel

Figure 125 · Set False Path Constraint Dialog Box

2. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for False Path Constraint dialog box (as shown below).



Select Source Pi	ns for False Path	n Constraint		
Specify pins	• by explicit list	C by keyword and wik	dcard	
Available Pins:			Assigned Pins:	
Acir Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
∫ daux[4]:CLK	objects:		1	
Pin Type:	All pins	•		
*		Filter		
Help			ОК	Cancel

Figure 126 · Select Source Pins for False Path Constraint Dialog Box

- 3. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to <u>Select Source or Destination Pins for Constraint Dialog Box</u>.)
- 4. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 5. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- Click OK.
   The <u>Set False Path Constraint</u> dialog box displays the updated representation of the From pin(s).
- 7. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 8. Enter comments in the **Comment** section.
- 9. Click OK.

SmartTime adds the False Path constraints to the Constraints List in the SmartTime Constraints Editor.

# See Also

Set False Path Constraint Dialog Box

# Specifying Clock-to-Clock Uncertainty Constraint

Use the clock-to-clock uncertainty constraint to model tracking jitter between two clocks in your design.



#### To specify the clock-to-clock uncertainty constraint:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set Clock-to-Clock Uncertainty</u> <u>Constraint Dialog Box</u> using one of the following methods:
  - From the SmartTime Constraints Editor, choose Constraints > Clock-to-Clock Uncertainty Constraint.
- Click the icon.
- Right-click Clock-to-Clock Uncertainty Constraint in the Constraint Browser.
- 2. Specify the from and to clocks and specify the uncertainty in ns.
- 4. Enter any comments to be attached to the constraint.
- 5. Click **OK**. The new constraint appears in the constraints list.
  - Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

# See Also

Set Clock-to-Clock Uncertainty Constraint Dialog Box



# **Generating Timing Reports**

# **Types of Reports**

Using SmartTime you can generate the following types of reports:

- Timer report This report displays the timing information organized by clock domain.
- Timing Violations report This flat slack report provides information about constraint violations.
- Bottleneck report This report displays the points in the design that contribute to the most timing violations.
- Datasheet report This report describes the characteristics of the pins, I/O technologies, and timing
  properties in the design.
- Constraints Coverage report This report displays the overall coverage of the timing constraints set on the current design.
- Combinational Loop report This report displays loops found during initialization.

#### See Also

Generating a Timing Report Generating a Timing Violation Report Generating a datasheet report Generating a bottleneck report Generating a constraints coverage report Generating a Combinational Loop Report

# Generating a Timing Report

The timing report enables you to quickly determine if any timing problems exist in your design. The Maximum Delay Analysis timing report lists the following information about your design:

- Maximum delay from input I/O to output I/O
- Maximum delay from input I/O to internal registers
- Maximum delay from internal registers to output I/O
- Maximum delays for each clock network
- Maximum delays for interactions between clock networks

#### To generate a timing report:

- 1. From the SmartTime Max/Min Delay Analysis View, choose **Reports > Timer**. The <u>Timing Report</u> <u>Options Dialog Box</u> appears.
- 2. Select the options you want to include in the report, and then click OK.

The timing report appears in a separate window.

#### See Also

<u>Understanding Timing Reports</u> Timing Report Options Dialog Box

# **Understanding Timing Reports**

The timing report contains the following sections:



# Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

# Summary

The summary section reports the timing information for each clock domain.

By default, the clock domains reported are the explicit clock domains that are shown in SmartTime. You can filter the domains and get only specific sections in the report (see <u>Timing Report Options</u>).

# **Path Sections**

The paths section lists the timing information for different types of paths in the design. This section is reported by default. You can deselect this option in the <u>Timing Report Options</u> dialog box.

By default, the number of paths displayed per set is 5.

You can filter the domains using the Timing Report Options dialog box.

You can also view the stored filter sets in the generated report using the timing report options (see <u>Timing</u> <u>Report Options</u>). The filter sets are listed by name in their appropriate section, and the number of paths reported for the filter set is the same as for the main sets.

By default, the filter sets are not reported.

### **Clock domains**

The paths are organized by clock domain.

### **Register to Register set**

This set reports the paths from the registers clock pins to the registers data pins in the current clock domain.

### **External Setup set**

This set reports the paths from the top level design input ports to the registers in the current clock domain.

#### **Clock to output set**

This set reports the paths from the registers clock pins to the top level design output ports in the current clock domain.

#### **Register to Asynchronous set**

This set reports the paths from registers to asynchronous control signals (like asynchronous set/reset).

#### **External Recovery set**

This set reports the external recovery check timing for asynchronous control signals (like asynchronous set/reset).

#### Asynchronous to Register set

This set reports the paths from asynchronous control signals (like asynchronous set/reset) to registers

### Inter-clock domain

This set reports the paths from the registers clock pins of the specified clock domain to the registers data pins in the current clock domain. Inter-domain paths are not reported by default.

#### Pin to pin

This set lists input to output paths and user sets. Input to output paths are reported by default. To see the user-defined sets, use the <u>Timing Report Options</u> dialog box.



### Input to output set

This set reports the paths from the top level design input ports to top level design output ports.

### **Expanded Paths**

Expanded paths can be reported for each set. By default, the number of expanded paths to report is set to 1. You can select and change the number when you specify <u>Timing Report Options</u>.

C Timer Report		_ <b>D</b> _X
File Actions Help		
Timing Report Max Delay Ana	lysis	<b>^</b>
SmartTime Version v11.6		
Microsemi Corporation - Mic	rosemi Libero Software Release v11.6 (Version 11.6.0.16)	
Date: Thu Apr 30 15:53:18 2	015	E
Design: false path		
Family: SmartFusion2		
Die: M2S050		
Package: 484 FBGA		
Temperature Range: 0 - 85 C		
Voltage Range: 1.14 - 1.26	V	
Speed Grade: STD Design State: Post-Layout		
Data source: Production		
Min Operating Conditions: E	EST - 1.26 V - 0 C	
Max Operating Conditions: W		
Scenario for Timing Analysi	s: Primary	
SUMMARY		
Clock Domain:	my_clk	
	1.706	
Frequency (MHz):	586.166	
Required Period (ns):	10.000	
Required Frequency (MHz): External Setup (ns):	-0.025	
External Hold (ns):	0.753	
	5.117	
Max Clock-To-Out (ns):	9.781	
	Input to Output	
Min Delay (ns):	N/A	
Max Delay (ns):	N/A	
END SUMMARY		
Clock Domain my_clk		
SET Register to Register		
Path 1 From:	D2 reg:CLK	
To:	Q reg:D	
Delay (ns):	1.341	
Slack (ns):	8.294	
Arrival (ns):	5.333	
Required (ns):	13.627	
Setup (ns):	0.298	
Minimum Period (ns):	1.706	-

Figure 127 · Timing Report

### See Also

Generating timing report Timing Report Options dialog box



# **Generating a Timing Violation Report**

The timing violations report provides a flat slack report centered around constraint violations.

#### To generate a timing violation report

- 1. From the SmartTime Max/Min Delay Analysis View window, choose **Tools > Reports > Timing Violations**. The <u>Timing Violations Report Options Dialog Box</u> appears.
- 2. Select the options you want to include in the report, and then click **OK**. The timing violations report appears in a separate window.

#### See Also

Understanding Timing Violation Reports

# **Understanding Timing Violation Reports**

The timing violation report contains the following sections:

# Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

# Paths

The paths section lists the timing information for the violated paths in the design.

The number of paths displayed is controlled by two parameters:

- A maximum slack threshold to report
- A maximum number or path to report

By default, the slack threshold is 0 and the number of paths is limited. The default maximum number of paths reported is 100.

All clocks domains are mixed in this report. The paths are listed by decreasing slack.

You can also choose to expand one or more paths. By default, no paths are expanded. For details, see the timing violation report options.



<pre>File Actions Help Timing Violation Report Max Delay Analysis SmartTime Version v11.6 Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.16) Date: Thu Apr 30 16:18:45 2015 Design: false_path Family: SmartFusion2 Die: M2S050 Package: 484 FBGA Temperature Range: 0 - 85 C Voltage Range: 1.14 - 1.26 V Speed Grade: STD Design State: Post-Layout Data source: Production Min Operating Conditions: BEST - 1.26 V - 0 C Max Operating Conditions: WORST - 1.14 V - 85 C Scenario for Timing Analysis: Primary Path 1 From: D2_reg:CLK To: Q_reg:D Delay (ns): 1.341 Slack (ns): -0.373 Arrival (ns): 5.333 Required (ns): 4.960</pre>	Timing_violations Report		
SmartTime Version v11.6       Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.16)       Date: Thu Apr 30 16:18:45 2015       Design: false_path       Family: SmartFusion2       Die: M2S050       Package: 484 FBGA       Temperature Range: 0 - 85 C       Voltage Range: 1.14 - 1.26 V       Speed Grade: STD       Design State: Post-Layout       Data source: Production       Min Operating Conditions: BEST - 1.26 V - 0 C       Max Operating Conditions: WORST - 1.14 V - 85 C       Scenario for Timing Analysis: Primary       Path 1       From:     D2_reg:CLK       To:     Q_reg:D       Delay (ns):     1.341       Slack (ns):     -0.373       Arrival (ns):     5.333	File Actions Help		
Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.16) Date: Thu Apr 30 16:18:45 2015 Design: false_path Family: SmartFusion2 Die: M2S050 Package: 484 FBGA Temperature Range: 0 - 85 C Voltage Range: 1.14 - 1.26 V Speed Grade: STD Design State: Post-Layout Data source: Production Min Operating Conditions: BEST - 1.26 V - 0 C Max Operating Conditions: WORST - 1.14 V - 85 C Scenario for Timing Analysis: Primary Path 1 From: D2_reg:CLK To: Q_reg:D Delay (ns): 1.341 Slack (ns): -0.373 Arrival (ns): 5.333	Timing Violation Report Max D	elay Analysis	
Family: SmartFusion2         Die: M2S050         Package: 484 FBGA         Temperature Range: 0 - 85 C         Voltage Range: 1.14 - 1.26 V         Speed Grade: STD         Design State: Post-Layout         Data source: Production         Min Operating Conditions: BEST - 1.26 V - 0 C         Max Operating Conditions: WORST - 1.14 V - 85 C         Scenario for Timing Analysis: Primary         Path 1         From:       D2_reg:CLK         To:       Q_reg:D         Delay (ns):       1.341         Slack (ns):       -0.373         Arrival (ns):       5.333	Microsemi Corporation - Micro 11.6.0.16)		5 (Version
From:         D2_reg:CLK           To:         Q_reg:D           Delay (ns):         1.341           Slack (ns):         -0.373           Arrival (ns):         5.333	Family: SmartFusion2 Die: M2S050 Package: 484 FBGA Temperature Range: 0 - 85 C Voltage Range: 1.14 - 1.26 V Speed Grade: STD Design State: Post-Layout Data source: Production Min Operating Conditions: BES Max Operating Conditions: WOR	ST - 1.14 V - 85 C	
	From: To: Delay (ns): Slack (ns): Arrival (ns):	Q_reg:D 1.341 -0.373 5.333	

Figure 128 · Timing Violations Report

#### See Also

<u>Generating a Timing Violation Report</u> <u>Timing Violations Report Options Dialog Box</u>

# Generating a Constraints Coverage Report

The constraints coverage report contains information about the constraints in the design.

To generate a constraints coverage report, from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Constraints Coverage**. The report appears in a separate window.

#### See Also

Understanding Constraints Coverage Reports

# Understanding Constraints Coverage Reports

The constraint coverage displays the overall coverage of the timing constraints set on the current design. You can generate this report either from within Designer or within SmartTime Analyzer. The report contains three sections:

Coverage Summary

- Results by Clock Domain
- Enhancement Suggestions

Die Package Temperature Range Speed Grade Design State Analysis Min Case Analysis Max Case Scenario for Timir		false_path SmartFusion M2S050 404 FBGA 0 - 85 C 1.14 - 1.24 STD Post-Layout BEST WORST Primary	5 V		
Family Die Package Temperature Range Voltage Range Speed Grade Design State Analysis Min Case Analysis Max Case Scenario for Timir		SmartFusion M2S050 484 FBGA 0 - 85 C 1.14 - 1.20 STD Post-Layout BEST WORST	5 V		
overage Summary					
overage bananarj					
Type of check   M	let	Violated	Untested	Total	
Setup   Recovery   Output Setup   Total Setup	0 0	10 0	40 20	50 50 20	F 1
+					
Hold   Removal   Output Hold   Total Hold	10 0	0	40 20	50 20	
Total Hold	15	0	105	120	
lock domain: my_cl					
Type of check   M	let	Violated	Untested	Total	
Setup   Recovery	0	3	12 6	15	
Setup   Recovery   Output Setup   Total Setup	0 0	0	3 42	I 3 I 48	
Hold   Removal   Output Hold   Total Hold					
		0	0	3	

Figure 129 · Constraints Coverage Report

# **Coverage Summary**

The coverage summary gives statistical information on the timing constraint in the design. For each type of timing checks (Setup, Recovery, Output, Hold and Removal), it specifies how many are Met (there is a constraint and it is satisfied), Violated (there is a constraint and it is not satisfied), or Untested (no constraint was found).

# **Clock Domain**

This section provides a coverage summary for each clock domain.



# **Enhancement Suggestions**

The enhancement suggestion reports, per clock domain, a list of constraints that can be added to the design to improve the coverage. It also reports if some options impacting the coverage can be changed.

# **Detailed Stats**

This section provides detailed suggestions regarding specific clocks or I/O ports that may require to be constrained for every pin/port that requires checks.

### See Also

<u>Clock</u> <u>Input delay</u> <u>Output delay</u> <u>Setting SmartTime Options</u>

# Generating a Bottleneck Report

The bottleneck report provides a list of the bottlenecks in the design.

To generate a bottleneck report, from the,SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Bottleneck**. The report appears in a separate window.

### See Also

Understanding Bottleneck Reports Timing Bottleneck Analysis Options Dialog Box

# Understanding Bottleneck Reports - SmartFusion2, IGLOO2, RTG4

A bottleneck is a point in the design that contributes to multiple timing violations. The purpose of the bottleneck report is to provide a list of the bottlenecks in the design. You can generate this report either from SmartTime Analyzer. It contains two sections

- Device Description
- Bottleneck Analysis



File Actions Help			
Bottleneck Report Max Delay And	alysis		
SmartTime Version 11.6.0.13			
	emi Libero Software Release v11.6 (Version 11.6.0.13)		
Date: Tue Apr 21 13:18:30 2015			
Design	TOP		
Family	RTG4		
Die	RT4G150		
Package	1657 CG		
Radiation Exposure	0		
Temperature	MIL		
Voltage	MIL		
Speed Grade	-1		
Design State	Post-Layout		
Data source	Advanced		
Analysis Max Case	WORST		
Set selection type	Select Entire Design		
Cost type	Path Count		
Max Paths	100		
Max Parallel Paths	1		
Bottleneck instances	10		
Slack Threshold	0		
Scenario for Timing Analysis	Primary		
Bottleneck Analysis			
*		++	
Instance Name		Path Count	
• · · · · · · · · · · · · · · · · · · ·		**	
FDDR_INIT_0/COREABC_0/IO_OUT		1 50 1	
		16	
CoreAHBLite_0/matrix4x16/slav		15 1	
	terstage_0/HREADY_M_iv_RNIME982:Y	15	
	vestage_0/slave_arbiter/arbRegSMCurrentState_RNO[1]:Y	11 1	
	vestage 0/slave arbiter/arbRegSMCurrentState RNO[3]:Y vestage 0/slave arbiter/arbRegSMCurrentState RNO[11]:Y		
	vestage_0/slave_arbiter/arbRegSMCurrentState_RNO[11]:Y vestage 0/slave_arbiter/arbRegSMCurrentState_nss i 0[0]:Y		
	vestage_0/slave_arbiter/arbRegSMCurrentState_nss_1_0[0]:Y vestage_0/slave_arbiter/arbRegSMCurrentState_RNO[7]:Y		
[ CoreAMBLICE_U/matrix4x16/314	vestage_0/slave_arbiter/arbkegsAcurrentState_kNo[/]11	1 1	

### Figure 130 · Bottleneck Report

The bottleneck can only be computed if and only a cost type is defined. There are two options available:

- **Path count:** This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

# **Device Description**

The device section contains general information about the design, including:

- Design name
- Family
- Die
- Package
- Software version

# **Bottleneck Analysis**

This section lists the core of the bottleneck information. It is divided into two columns:

- Instance name: refers to the output pin name of the instance.
- Path Count: Displays the number of violating paths which include the instance pin.

#### See Also

<u>Generating a Bottleneck Report</u> <u>Timing Bottleneck Analysis Options Dialog Box</u>

# Generating a Datasheet Report

The datasheet reports information about the external characteristics of the design.

To generate a datasheet report, from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Datasheet**. The report appears in a separate window.

### See Also

Understanding Datasheet Reports Timing Datasheet Report Options Dialog Box

# **Understanding Datasheet Reports**

The datasheet report displays the external characteristics of the design. . You can generate this report from SmartTime Max/Min Delay Analysis View. It contains three tables:

- Pin Description
- DC Electrical Characteristics
- AC Electrical Characteristics

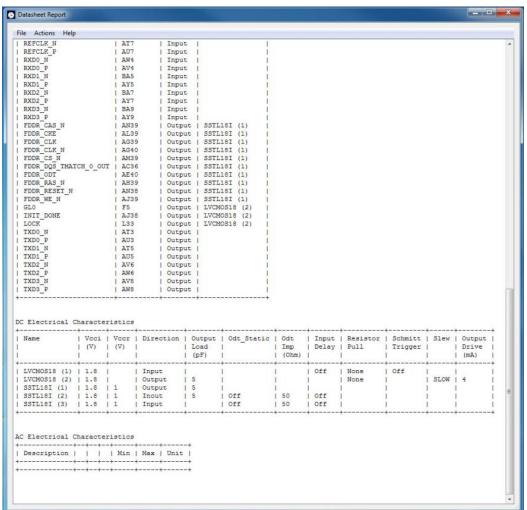


Figure 131 · Datasheet Report



# **Pin Description**

Provides the port name in the netlist, location on the package, type of port, and I/O technology assigned to it. Types can be input, output, inout, or clock. Clock ports are ports shown as "clock" in the Clock domain browser.

# **DC Electrical Characteristics**

Provides the parameters of the different I/O technologies used in the design. The number of parameters displayed depends on the family for which you have created the design.

# **AC Electrical Characteristics**

Provides the timing properties of the ports of the design. For each clock, this section includes the maximum frequency. For each input, it includes the external setup, external hold, external recovery, and external removal for every clock where it applies. For each output, it includes the clock-to-out propagation time. This section also displays the input-to-output propagation time for combinational paths.

### See Also

<u>Generating a Datasheet Report</u> <u>Timing Datasheet Report Options Dialog Box</u>

# Generating a Combinational Loop Report

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

To generate a combinational loop report, from the Maximum (or Minimum) Delay Analysis **Tools** menu, choose **Reports > Combinational Loop**. The report appears in a separate window.

To generate the combinational loop report; from the **Tools** menu, choose **Reports > Combinational Loops** 

Select either the **Plain Text** or **Comma Separated Values** option in the Combinational\_Loops Report Options dialog box and click **OK**.

The plain text report will pop up in a new window; you will be prompted to save the CSV in a directory of your choosing.

# See Also

Understanding Combinational Loop Reports

# **Understanding Combinational Loop Reports**

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.



\_ **D** \_X Combinational\_loops Report File Actions Help Combinational Loop Report SmartTime Version 11.6.0.15 Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.15) Date: Fri May 01 15:50:15 2015 Design TOP Family RTG4 Die RT4G150 Package 1657 CG Radiation Exposure Temperature Range 0 -55 - 125 C Voltage Range 1.14 - 1.26 V Speed Grade -1 Design State Post-Layout Analysis Min CaseBEST - 1.26 V - -55 CAnalysis Max CaseWORST - 1.14 V - 125 C WORST - 1.14 V - 125 C Scenario for Timing Analysis Primary No combinational loops were detected in the design.

#### Figure 132 · Combinational Loop Report

To view a graphical representation of the broken loop, open MultiView Navigator, find each pin and add them as a logical cone. For more information on how to find each pin and how to set up the logical cones, refer to <u>What is a LogicalCone</u>.

### See Also

Generating a Combinational Loop Report



# **Timing Concepts**

# Static Timing Analysis Versus Dynamic Simulation

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements. The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms.

# **Delay Models**

The first step in timing analysis is the computation of single component delays. These components could be either a combinational gate or block or a single interconnect connecting two components.

Gates that are part of the library are pre-characterized with delays under different parameters, such as inputslew rates or capacitive loads. Traditional models provide delays between each pair of I/Os of the gate and between rising and falling edges.

The accuracy with which interconnect delays are computed depends on the design phase. These can be estimated using a simple Wire Load Model (WLM) at the pre-layout phase, or a more complex Resistor and Capacitor (RC) tree solver at the post-layout phase.

# **Timing Path Types**

Path delays are computed by adding delay values across a chain of gates and interconnects. SmartTime uses this information to check for timing violations. Traditionally, timing paths are presented by static timing analysis tools in four categories or "sets":

- Paths between sequential components internal to the design. SmartTime displays this category under the Register to Register set of each displayed clock domain.
- Paths that start at input ports and end at sequential components internal to the design. SmartTime
  displays this category under the External Setup and External Hold sets of each displayed clock
  domain.
- Paths that start at sequential components internal to the design and end at output ports. SmartTime displays this category under the Clock to Out set of each displayed clock domain.
- Paths that start at input ports and end at output ports. SmartTime displays this category under the Input to Output set.

# Maximum Clock Frequency

Generally, you set clock constraints on clocks for which you have a specified requirement. The absence of violations indicates that this clock will be able to run at least at the specified frequency. However, in the absence of such requirements, you may still be interested in computing the maximum frequency of a specific clock domain.

To obtain the maximum clock frequency, a static timing analysis tool computes the minimum period for each path between two sequential elements. To compute the maximum period, the tool evaluates the maximum data path delay and the minimum skew between the two elements, as well as the setup on the receiving sequential element. It also considers the polarity of each sequential element. The maximum frequency is the



inverse of the largest value among the maximum period of all the paths in the clock domain. The path responsible for limiting the frequency of a given clock is called the critical path.

# Setup Check

The setup and hold check ensures that the design functions as specified at the required clock frequency.

Setup check specifies when data is required to be present at the input of a sequential component in order for the clock to capture this data effectively into the component. Timing analyzers evaluate the setup check as a maximum timing budget allowed between adjacent sequential elements. For more details on how setup check is processed, refer to <u>Arrival Time, Required Time, and Slack</u>.

#### See Also

Static Timing Analysis Versus Dynamic Simulation Arrival Time, Required Time, and Slack

# Arrival Time, Required Time and Slack

You can use arrival time and required time to verify timing requirements in the presence of constraints. Below is a simple example applied to verifying the clock requirement for setup between sequential elements in the design.

The arrival time represents the time at which the data arrives at the input of the receiving sequential element. In this example, the arrival time is considered from the setup launch edge at CK, taken as a time reference (instant zero). It follows the clock network along the blue line until the clock pin on FF1 (delay d1). Then it continues along the data path always following the blue line until the data pin D on FF2. Therefore,

Arrival\_Time\_{FF2:D} = d1 + d2

The required time represents when the data is required to be present at the same pin FF2:D. Assume in this example that in the presence of an FF with the same polarity, the capturing edge is simply one cycle following the launch edge. Using the period T provided to the tool through the clock constraint, the event gets propagated through the clock network along the red line until the clock pin of FF2 (delay d3). Taking into account FF2 setup (delay d4), this means that the clock constraint requires the data to be present d4 time before the capturing clock edge on FF2. Therefore, the required time is:

Required\_Time\_{F2:D} = T + d3 - d4

The slack is simply the difference between the required time and arrival time:

Slack<sub>FF2:D</sub> = Required\_Time<sub>FF2:D</sub> - Arrival\_TimeFF2:D

If the slack is negative, the path is violating the setup relationship between the two sequential elements.

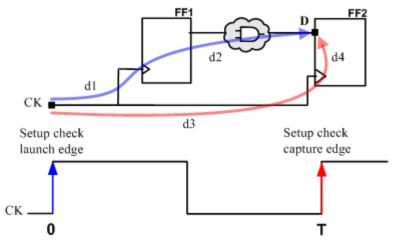


Figure 133 · Arrival Time and Required Time for Setup Check



# **Timing Exceptions Overview**

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the optimization flow.
- Setting a maximum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

### See Also

Specifying a Maximum Delay Constraint Specifying a Minimum Delay Constraint Specifying a Multicycle Constraint Specifying a False Path Constraint Changing Output Port Capacitance

# **Clock Skew**

The clock skew between two different sequential components is the difference between the insertion delays from the clock source to the clock pins of these components. SmartTime calculates the arrival time at the clock pin of each sequential component. Then it subtracts the arrival time at the receiving component from the arrival time at the launching component to obtain an accurate clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.

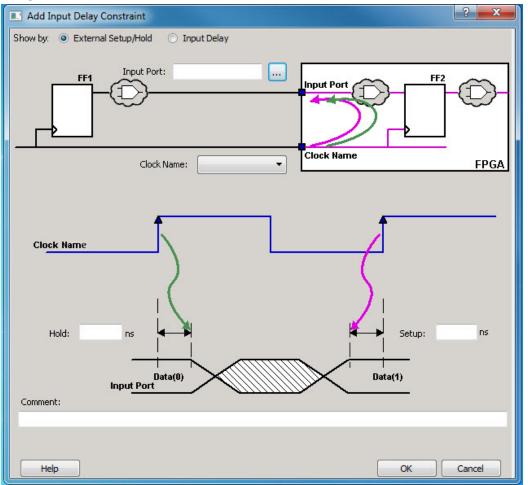
# Add Input Delay Constraint Dialog Box

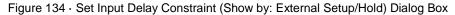
Use this dialog box to apply input delay constraints or external setup/hold constraints. This constraint defines the arrival time of an input relative to a clock.

To open the Add Input Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor Constraints menu choose **Input Delay** (**Constraints > Input Delay**).



# **External Setup/Hold**





### Input Port

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.

#### **Clock Name**

Specifies the clock reference to which the specified External Setup/Hold is related.

### **External Hold**

Specifies the external hold time requirement for the specified input ports.

## **External Setup**

Specifies the external setup time requirement for the specified input ports.

#### Comment

Enables you to provide comments for this constraint.



# Input Delay

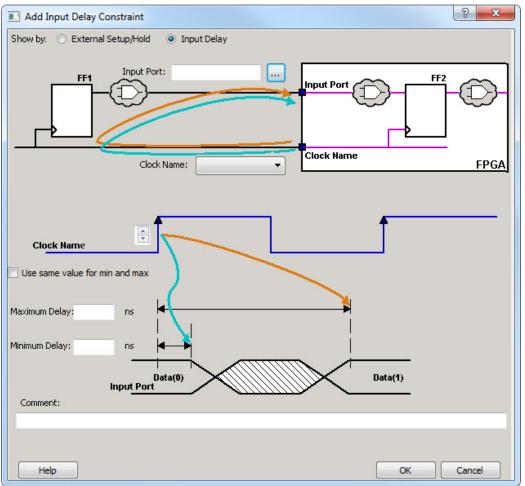


Figure 135 · Set Input Delay Constraint (Show by: Input Delay) Dialog Box

# **Input Port**

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.

### **Clock Name**

Specifies the clock reference to which the specified input delay is related.

# **Clock edge**

Indicates the launching edge of the clock (rising or falling). Use same delay for both min and max Specifies that the minimum input delay uses the same value as the maximum input delay.

### **Maximum Delay**

Specifies that the delay refers to the longest path arriving at the specified input.

# **Minimum Delay**

Specifies that the delay refers to the shortest path arriving at the specified input.

### Comment

Enables you to provide comments for this constraint.



# See Also

Specifying Input Timing Delay Constraint

# Add Output Delay Constraint Dialog Box

Use this dialog box to apply output delay constraints. This constraint defines the output delay of an output relative to a clock.

To open the Set Output Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Output Delay**.

# **Clock-to-Output**

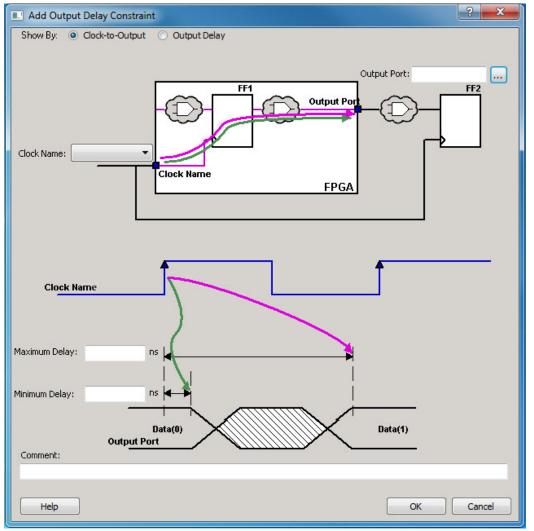


Figure 136 · Add Output Delay (Show By: Clock-to-Output) Dialog Box

# **Output Port**

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.

### **Clock Name**

Specifies the clock reference to which the specified Clock-to-Output is related.



# **Maximum Delay**

Specifies the delay for the longest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

### **Minimum Delay**

Specifies the delay for the shortest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

### Comment

Enables you to provide comments for this constraint.

# **Output Delay**

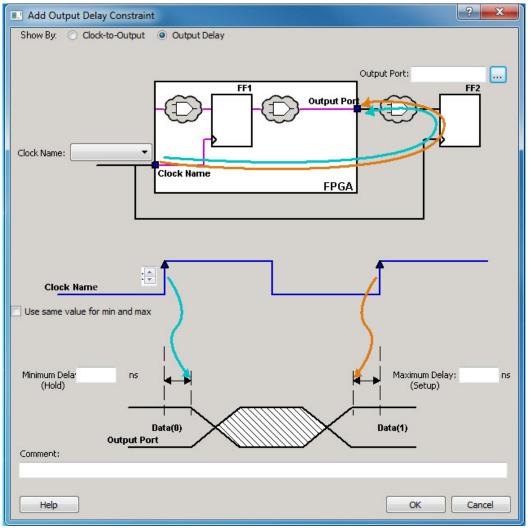


Figure 137 · Set Output Delay (Show By: Output Delay) Dialog Box

### **Output Port**

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.

### **Clock Name**

Specifies the clock reference to which the specified output delay is related.



# **Clock edge**

Indicates the launching edge of the clock (rising or falling).

### **Maximum Delay**

Specifies the delay for the longest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library setup time.

## **Minimum Delay**

Specifies the delay for the shortest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library hold time.

### Comment

Enables you to provide comments for this constraint.

### See Also

Specifying Output Timing Delay Constraint



# **Dialog Boxes**

# Add Path Analysis Set Dialog Box

Use this dialog box to specify a custom path analysis set.

Note: The Analysis menu is available only in Maximum or Minimum Delay Analysis view.

To open the Add Path Analysis Set dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, right-click a path group in the Domain Browser and select **Add Set**.

Tip: You can also click the icon in the SmartTime window bar to display the Add Path Analysis Set dialog box.

Add Path Analysis Set			×
Name:	Trace from:	Source to sir	nk C Sink to source
Source Pins: DDR0/U0:CLK DDR1/U0:CLK DDRREG2/INBUF_LVDS_0_inst/U0/U2_DDR1 FIFO_inst/FIFO64K36_FULL:RCLK FIFO_inst/FIFO64K36_Q_0_inst:RCLK RAM_inst/RAM64K36_Q_0_inst:WCLK RAM_inst/RAM64K36_Q_1_inst:RCLK RAM_inst/RAM64K36_Q_1_inst:WCLK Rdf_pll0/U0:CLK Rdf_pll1/U0:CLK	<u>^</u>	k Pins:	
XCMP33/U0/U2_DDR1:CLK XCMP33/U0/U2_DDR2:CLK			
Select All		Select All	
Filter source pins:	F	ilter sink pins:	
Pin Type: Registers by pin names	•	Pin Type:	egisters by pin names 💌
Filter		*	Filter
Help	[	ОК	Cancel

Figure 138 · Add Path Analysis Set Dialog Box

# Name

Enter the name of your path set.



# **Trace from**

Select whether you want to trace connected pins from **Source to sink** or from **Sink to source**. By default, the pins are traced Source to sink.

# **Source Pins**

Displays a list of available and valid source pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the Source Pins list.

# **Select All**

Selects all the pins in the Source Pins list to include in the path analysis set.

# **Filter Source Pins**

Enables you to specify thesource **Pin Type** and the **Filter**. The default pin type is Registers by pin name. You can specify any string value for the **Filter**. If you change the pin type, the **Source Pins** shows the updated list of available source pins.

# **Sink Pins**

Displays list of available and valid pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the **Sink Pins list.** 

# Select All

Selects all the pins in the Sink Pins list to include in the path analysis set.

# **Filter Sink Pins**

Enables you to specify the sink **Pin Type** and the **Filter**. The default pin type is Registers (by pin). You can specify any string value for the **Filter**. If you change the pin type, the **Sink Pins** shows the updated list of available sink pins.

# Analysis Set Properties Dialog Box

Use this dialog box to view information about the user created set.

To open the **Analysis Set Properties** dialog box (shown below) from the Timing Analysis View, right-click any user-created set in the Domain Browser, and choose **Properties** from the shortcut menu.

II Analysis Set Pr	operties 2 🔀
Name :	my_set
Parent set :	
From :	CoreAHBLite_0/matrix4x16/masterstage_0/SDATASELInt[0]:CLK
To :	SERDES_IF_0/SERDESIF_INST/INST_PCIE_IP:AXI_M_WREADY_HREADY
Help	OK Cancel

Figure 139 · Analysis Set Properties Dialog Box



#### Name

Specifies the name of the user-created path set.

#### **Parent Set**

Specifies the name of the parent path set to which the user-created path set belongs.

# **Creation filter**

#### From

Specifies a list of source pins in the user-created path set.

### То

Specifies a list of sink pins in the user-created path set.

### See Also

Using filters

# Edit Filter Set Dialog Box

Use this dialog box to specify a filter.

To open the **Edit Filter Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, right-click an existing filter set in the clock domain browser, and then choose **Edit Set** from the shortcut menu.

Edit Path Analysis Set	? ×
Name :- my_set1	Trace from :- () Source to sink () Sink to source
Source pins:	Sink Pins:
CFG0_GND_INST:Y CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_ SerDes_AHBBUS_0/PC
Select All	Select All
Filter source pins:	Filter sink pins:
Pin Type: All pins	Pin Type: All pins
* Filter	* Filter
Help	OK Cancel

Figure 140 · Edit Path Analysis Set Dialog Box



### Name

Specifies the name of the path you want to edit.

#### **Creation filter**

**Source Pins** - Displays a list of source pins in the user-created path set. **Sink Pins** - Displays a list of sink pins in the user-created path set.

#### See Also

Using filters

# Select Source Pins for Clock Constraint Dialog Box

Use this dialog box to find and choose the clock source from the list of available pins.

To open the **Select Source Pins for the Clock Constraint** dialog box (shown below) from the SmartTime Constraints Editor, click the **Browse** button to the right of the Clock source field in the <u>Create Clock</u> <u>Constraint</u> dialog box.

Select Source Pins for Clock Constraint	? <mark>x</mark>
Specify pins :- <ul> <li>by explicit list</li> <li>by keyword and wildcard</li> </ul>	
Available Pins: Add Add All Remove Remove All	
Filter available pins :       Pin Type :       Explicit docks       *   Filter	Help OK Cancel

Figure 141 · Select Source Pins for Clock Constraint Dialog Box

#### **Available Pins**

Displays all available pins.

#### **Filter Available Pins**

Explicit clock pins for the design is the default value. To identify any other pins in the design as clock pins, right-click the **Pin Type** pull-down menu and select one of the following:

- Explicit clocks
- Potential clocks
- Input ports
- All Pins
- All Nets
- Pins on clock network
- Nets in clock network

You can also use the Filter to filter the clock source pin name in the displayed list



### See Also

Specifying clock constraints

# Create Clock Constraint Dialog Box

Use this dialog box to enter a clock constraint setting.

It displays a typical clock waveform with its associated clock information. You can enter or modify this information, and save the final settings as long as the constraint information is consistent and defines the clock waveform completely. The tool displays errors and warnings if information is missing or incorrect.

To open the Create Clock Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Clock**.

Create Clock Constraint		8 22
Clock Name :	Clock Source :	•
Period :	ns 🔶 d	or Frequency: Mhz
	- <b>H</b>	
0.000 ns 50.0000 %		
Comment :		
Help	[	OK Cancel

Figure 142 · Create Clock Constraint Dialog Box

# **Clock Source**

Enables you to choose a pin from your design to use as the clock source.

The drop-down list is populated with all explicit clocks. You can also select the Browse button to access all potential clocks. The **Browse** button displays the <u>Select Source Pins for Clock Constraint Dialog Box</u>.

# **Clock Name**

Specifies the name of the clock constraint. This field is required for virtual clocks when no clock source is provided.

# T(zero) Label

Instant zero used as a common starting time to all clock constraints.

# Period

When you edit the period, the tool automatically updates the frequency value. The period must be a positive real number. Accuracy is up to 3 decimal places.

# Frequency

When you edit the frequency, the tool automatically updates the period value. The frequency must be a positive real number. Accuracy is up to 3 decimal places.



# **Offset (Starting Edge Selector)**

Enables you to switch between rising and falling edges and updates the clock waveform. If the current setting of starting edge is rising, you can change the starting edge from rising to falling. If the current setting of starting edge is falling, you can change the starting edge from falling to rising.

# **Duty Cycle**

This number specifies the percentage of the overall period that the clock pulse is high. The duty cycle must be a positive real number. Accuracy is up to 4 decimal places. Default value is 50%.

# Offset

The offset must be a positive real number. Accuracy is up to 2 decimal places. Default value is 0.

# Comment

Enables you to save a single line of text that describes the clock constraints purpose.

### See Also

create\_clock (SDC) Clock definition Specifying Clock Constraints

# Create Generated Clock Constraint Dialog Box

Use this dialog box to specify generated clock constraint settings.

It displays a relationship between the clock source and its reference clock. You can enter or modify this information, and save the final settings as long as the constraint information is consistent. The tool displays errors and warnings if the information is missing or incorrect.

To open the Create Generated Clock Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Generated Clock**.



Create Generated Clock Constraint
Reference Pin:
Clock Port FPGA
Generated Clock Name
The generated frequency is such as
f(clock) = f(reference) × 1 / 1 Get Pre-Computed Factor
The generated waveform is the same as 🔻 the reference waveform
Comment:
Help OK Cancel

Figure 143 · Create Generated Clock Constraint

# **Clock Pin**

Enables you to choose a pin from your design to use as a generated clock source.

The drop-down list is populated with all unconstrained explicit clocks. You can also select the Browse button to access all potential clocks and pins from the clock network. The Browse button displays the <u>Select</u> <u>Generated Clock Source</u> dialog box.

#### **Reference Pin**

Enables you to choose a pin from your design to use as a generated reference pin.

#### **Generated Clock Name**

Specifies the name of the clock constraint. This field is required for virtual clocks when no clock source is provided.

#### **Generated Frequency**

The generated frequency is a factor of reference frequency defined with a multiplication element and/or a division element.

### **Generated Waveform**

The generated waveform could be either the same as or inverted w.r.t. the reference waveform.

#### Comment

Enables you to save a single line of text that describes the generated clock constraints purpose.



# See Also

create generated clock (SDC) Specifying Generated Clock Constraints Select Generated Clock Source

# **Customize Analysis View Dialog Box**

Use this dialog box to customize the timing analysis grid.

To open the **Customize Analysis View** dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, click the **Customize table** button (circled in red in the figure below) in the Max/Min Delay Analysis View.

Delay Analysis View									
Register to Asynchronous	-	ustomize table			то	•	Apply f	Filter Store Filter	Reset Filter
External Removal Asynchronous to Register a X@ GL0		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Hold (ns)	Skew (n
× Register to Register	1	POOR_INIT_0/COREADC_0/	RTG-FODRC_0/U0/DNST_	0.764	-0.980	3.010	3.990	1.749	
Clock to Output Register to Asynchronous	2	FDOR_INIT_0/COREABC_0/	RTG4FDDRC_0/U0/INST_	0.681	-0.914	2.927	3.841	1.595	
External Removal Asynchronous to Register	3	FOOR_INET_0/COREABC_0/	RTG4PDDRC_0/U0/INST_	0.766	-0,892	3.012	3.904	1.658	
≠ √(P) GL1 *	4	FOOR_INET_0/COREABC_0/	RTG#FOORC_0/U0/INST_	0.626	-0.762	2.872	3.634	1.388	
80	5	FDOR_INET_0/COREABC_0/	RTG4FODRC_0/U0/0NST_	0.717	-0.749	2.963	3.712	1.465	
64	6	POOR_INET_0/COREABC_0/	RTG4PODRC_0/U0/INST_	0,648	-0.727	2.894	3.621	1.375	
48		•	1			·	· •		•
32		me Summary data arrival time			Туре	Net			Macro
0-0.98 -0.465 0 0.05 0.565		data required time slack Data_arrival_time_calculat							

Figure 144 · Customize Table Button

The Customize Paths	List Table I	Dialog Box appears.
		Blaidg Box appoalo.

Customize Paths List Table	2 ×
Available fields: Clock Source Clock Edge Destination Clock Edge Logic Stage Count Clock Constraint (ns) Multicycle Constraint	Add       Source Pin         Sink Pin       Delay         Delay       (ns)         Slack (ns)       Arrival (ns)         Move Up       Required (ns)         Hold (ns)       Skew (ns)
Help Restore Default	OK Cancel

Figure 145 · Customize Paths List Dialog Box

# **Available Fields**

Displays a list of all the available fields in the timing analysis grid.



# Show These Fields in This Order

Shows the list of fields you want to see in the timing analysis grid. Use **Add** or **Remove** to move selected items from **Available fields** to **Show these fields in this order** or vice versa. You can change the order in which these fields are displayed by using **Move Up** or **Move Down**.

### **Restore Defaults**

Resets all the options in the General panel to their default values.

# Manage Clock Domains Dialog Box

 $\sim$ 

Use this dialog box to specify the clock pins you want to see in the Expanded Path view.

To open the Manage Clock Domain dialog box (shown below) from the SmartTime Max/Min Delay Analysis

view, click theicon.		
Manage Clock Domains		? X
Available clock domains:	Show the clock domains in this order:	
	Add my_clk1 my_clk2	
	Remove	
	Move Up	
	Move Down	
Help New Clock	ОК	Cancel

Figure 146 · Manage Clock Domains Dialog Box

### **Available Clock Domains**

Displays alphanumerically sorted list of available clock pins. The first clock pin is selected by default.

### Show the Clock Domains in this Order

Shows the clock pins you want to see in the Expanded Path view. Use **Add** or **Remove** to move selected items from **Available clock domains** to **Show the clock domains in this order** or vice versa. You can change the order in which these clock pins are displayed by using **Move Up** or **Move Down**.

#### **New Clock**

Invokes the <u>Select Source Pins for Clock Constraint</u> dialog box. The new clock gets added at the end of the **Show the clock domains in this order** list box.

#### See Also

Managing Clock Domains



# Select Generated Clock Reference Dialog Box

Use this dialog box to find and choose the generated clock reference pin from the list of available pins.

To open the Select Generated Clock Reference dialog box (shown below) from the SmartTime Constraints Editor, open the <u>Create Generated Clock Constraint Dialog Box</u> dialog box and click the **Browse** button for the **Clock Reference**.

FDDR_ADDR		1
FDDR_ADDR[	)]	Γ
FDDR_ADDR[1	[0]	
FDDR_ADDR[1	1]	
FDDR_ADDR[1	[2]	
FDDR_ADDR[1	[3]	
FDDR_ADDR[1	[4]	
FDDR_ADDR[1	[5]	
FDDR_ADDR[1	L]	
Filter available	pins :	
Pin Type :	All Ports	•
*		Filter

Figure 147 · Select Generated Clock Reference Dialog Box

# **Filter Available Pins**

To identify any other pins in the design as the generated master pin, select **Filter available objects - Type** as **Clock Network**. You can also use the **Filter** to filter the generated reference clock pin name in the displayed list.

#### See Also

Specifying generated clock constraints

# Select Generated Clock Source Dialog Box

Use this dialog box to find and choose the generated clock source from the list of available pins.

To open the Select Generated Clock Source dialog box (shown below) from the SmartTime Constraints Editor, open the <u>Create Generated Clock Constraint</u> dialog box and click the **Browse** button for the **Clock Pin**.



Select Generat	ted Clock Source
Filter available p	ins -
Pin Type :	Explicit clocks
*	Filter
	Filter
Help	OK Cancel

Figure 148 · Select Generated Clock Source Dialog Box

# **Filter Available Pins**

Explicit clock pins for the design is the default value. To identify any other pins in the design as the generated clock source pins, from the **Pin Type** pull-down list, select **Explicit clocks**, **Potential clocks**, **All Ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. You can also use the **Filter** to filter the generated clock source pin name in the displayed list.

### See Also

Specifying generated clock constraint (SDC)

# Select Source or Destination Pins for Constraint Dialog Box

Use this dialog box to select pins or ports:

- By explicit list
- By keyword and wildcard

To open the Select Source or Destination Pins for Constraint dialog box from the SmartTime Constraints Editor, right-click the Constraint Type in the Contraint Browser to open the Add Constraint Dialog Box. From this dialog box, click the **Browse** button to open the Select Source or Destination Pins for the Constraint dialog box.

# **By Explicit List**

This is the default. This mode stores the actual pin names. The following figure shows an example dialog box for **Select Source Pins for Multicycle Constraint > by explicit list**.



Select Source Pins for Multicycle Specify pins :-		2 ×
Available Pins:	Assigned Pins:	
FDDR_DM_RDQS FDDR_DM_RDQS[0] FDDR_DM_RDQS[1] FDDR_DQ FDDR_DQS FDDR_DQS[0] FDDR_DQS[1] FDDR_DQS_N FDDR_DQS_N[0] FDDR_DQS_N[1] FDDR_DQS_TMATCH_0_IN	Add Add All Remove Remove All	
Filter available pins : Pin Type : Input Ports	Filter	Help OK Cancel

Figure 149 · Select Source Pins for Multicycle (Specify pins by explicit list) Dialog Box

### **Available Pins**

The list box displays the available valid objects. If you change the filter value, the list box shows the available objects based on the filter.

Use Add, Add All, Remove, Remove All to add or delete pins from the Assigned Pins list.

#### **Filter Available Pins**

Pin type – Specifies the filter on the available object. This can be by **Explicit clocks**, **Potential clocks**, **Input ports**, **All Pins**, **All Nets**, **Pins on clock network**,or **Nets in clock network** 

#### Filter

Specifies the filter based on which the **Available Pins** list shows the pin names. The default is \*. You can specify any string value.

### By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get\_ports, get\_pins, etc.). The following figure shows an example dialog box for **Select Source Pins for Multicycle Constraint > by keyword and wildcard**.



Resulting Pins :			
FDDR_DM_RDQS			<u>^</u>
FDDR_DM_RDQS[			=
FDDR_DM_RDQS[: FDDR_DQ	LJ		
FDDR_DQ			
FDDR_DQS[0]			
FDDR_DQS[1]			
FDDR_DQS_N			
FDDR_DQS_N[0]			
FDDR_DQS_N[1]			
FDDR_DQS_TMAT	CH_0_IN		-
FDDR_DQS_N[1] FDDR_DQS_TMAT	CH_0_IN		
ter available pins :			Help

Figure 150 · Select Source Pins for Multicycle (Specify pins by keyword and wildcard) Dialog Box

#### **Pin Type**

Specifies the filter on the available pins. This can be Registers by pin names, Registers by clock names, Input Ports, or Output Ports. The default pin type is Registers by pin names.

### Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is \*. You can specify any string value.

#### **Resulting Pins**

Displays pins from the available pins based on the filter.

# Set False Path Constraint Dialog Box

Use this dialog box to define specific timing paths as being false.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints.

To open the Set False Path Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > False Path**.

t False Path Constraint	×
From:	
<	>
Through:	
	· · · · · · · · · · · · · · · · · · ·
<	>
To:	
<	
Comment:	
	(
Help	OK Cancel

Figure 151 · Set False Path Constraint Dialog Box

## From

Specifies the starting points for false path. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

## Through

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

## То

Specifies the ending points for false path. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## Comment

Enables you to provide comments for this constraint.

### See Also

Specifying a False Path Constraint



# Set Clock Source Latency Dialog Box

Use this dialog box to define the delay between an external clock source and the definition pin of a clock within SmartTime.

To open the Set Clock Source Latency dialog box (shown below) from the Timing Analysis View, you must first <u>create a clock constraint</u>. From the **Constraints** menu, choose **Clock Source Latency**.

Set Clock Source Latency Constraint	? ×
Clock Name or Source:	•
Clock Source	
Late Rise ns	► Late Fall ns
Early Rise ns 🔶	Early Fall ns
Clock Name or Source	
Clock Edges: 🔲 Falling same as rising	Early same as late
Comment:	
Help	OK Cancel

Figure 152 · Set Clock Source Latency Dialog Box

#### **Clock Name or Source**

Displays a list of clock ports or pins that do not already have a clock source latency specified. Select the clock name or source for which you are specifying the clock source latency.

#### Late Rise

Specifies the largest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

#### **Early Rise**

Specifies the smallest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

#### Late Fall

Specifies the largest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.



### Early Fall

Specifies the smallest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

#### **Clock Edges**

Select the latency for the rising and falling edges:

Falling same as rising: Specifies that Rising and Falling clock edges have the same latency.

Early same as late : Specifies that the clock source latency should be considered as a single value, not a range from "early" to '"late".

#### Comment

Enables you to save a single line of text that describes the clock source latency.

### See Also

Specifying Clock Constraints

# Set Constraint to Disable Timing Arcs Dialog Box

Use this dialog box to specify the timing arcs being disabled to fix the combinational loops in the design. To open the Set Constraint to Disable Timing Arcs dialog box (shown below) from the Timing Analysis View, from the **Constraints** menu, choose **Disable Timing**.

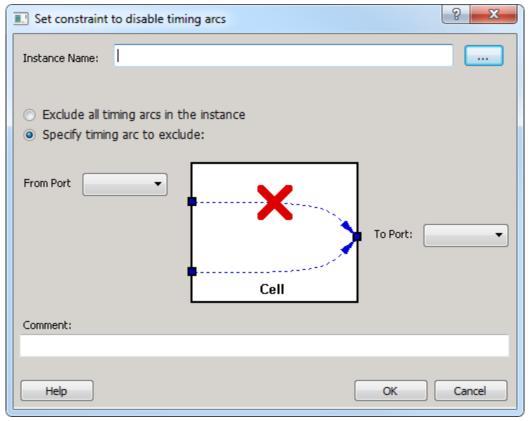


Figure 153 · Set Constraint to Disable Timing Arcs Dialog Box

#### **Instance Name**

Specifies the instance name for which the disable timing arc constraint will be created.



#### **Exclude All Timing Arcs in the Instance**

This option enables you to exclude all timing arcs in the specified instance.

#### **Specify Timing Arc to Exclude**

This option enables you to specify the timing arc to exclude. In this case, you need to specify the from and to ports:

#### From Port

Specifies the starting point for the timing arc.

To Port

Specifies the ending point for the timing arc.

#### Comment

Enables you to save a single line of text that describes the disable timing arc.

#### See Also

Specifying Disable Timing Constraint

# Set Clock-to-Clock Uncertainty Constraint Dialog Box

Use this dialog box to model tracking jitter between two clocks in your design.

To open the Set Clock-to-Clock Uncertainty Constraint dialog box (shown below), from the **Constraints** menu, choose **Clock-to-Clock Uncertainty**.



Set Clock-to-clock Uncertainty Constraint					
From Clock:	1		<b>.</b>		
Edge	C rising	C falling	⊙ both		
To Clock:	·		<b>•</b>		
Edge	C rising	C falling	• both		
Uncertainty:	ns				
Use uncertain	ty for: 🔘 setup checks	C hold checks	all checks		
Comment:					
Help			OK Cancel		

Figure 154 · Clock-to-Clock Uncertainty Constraint Dialog Box

## From Clock

Specifies clock name as the uncertainty source.

#### Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

#### **To Clock**

Specifies clock name as the uncertainty destination.

#### Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

#### Uncertainty

Enter the time in ns that represents the amount of variation between two clock edges.

### **Use Uncertainty For**

This option enables you select whether the uncertainty constraint applies to setup, hold, or all checks.

#### Comment

Enables you to save a single line of text that describes this constraint.



#### See Also

Specifying Disable Timing Constraint

# Set Input Delay Constraint Dialog Box

Use this dialog box to apply input delay constraints or external setup/hold constraints. This constraint defines the arrival time of an input relative to a clock.

To open the Set Input Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Input Delay**.

# **External Setup/Hold**

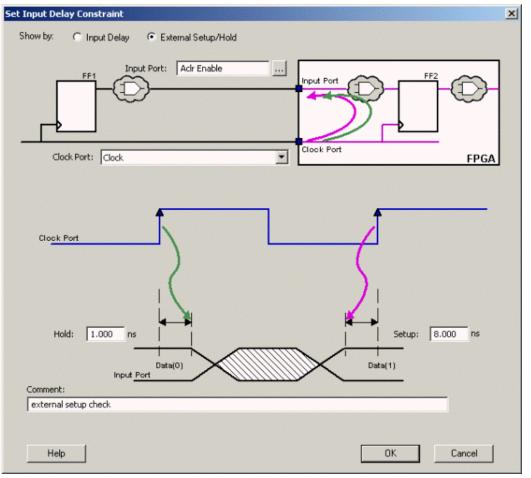


Figure 155 · Set Input Delay Constraint (Show by: External Setup/Hold) Dialog Box

## Input Port

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.

#### **Clock Port**

Specifies the clock reference to which the specified External Setup/Hold is related.

#### **External Hold**

Specifies the external hold time requirement for the specified input ports.



#### **External Setup**

Specifies the external setup time requirement for the specified input ports.

#### Comment

Enables you to provide comments for this constraint.

# Input Delay

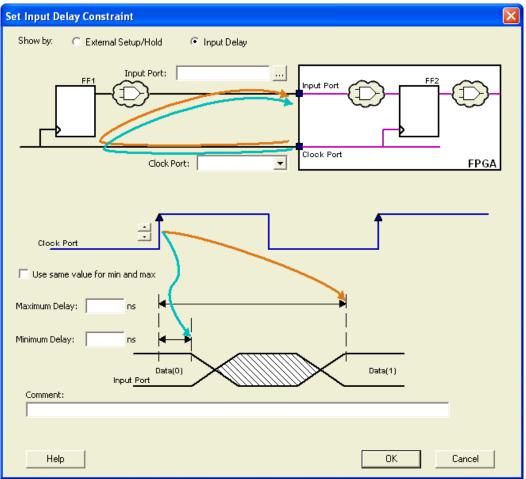


Figure 156 · Set Input Delay Constraint (Show by: Input Delay) Dialog Box

## **Input Port**

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.

#### **Clock Port**

Specifies the clock reference to which the specified input delay is related.

#### **Clock edge**

Indicates the launching edge of the clock.

#### Use max delay for both min and max

Specifies that the minimum input delay uses the same value as the maximum input delay.



#### **Maximum Delay**

Specifies that the delay refers to the longest path arriving at the specified input.

#### **Minimum Delay**

Specifies that the delay refers to the shortest path arriving at the specified input.

#### Comment

Enables you to provide comments for this constraint.

#### See Also

Specifying an Input Delay Constraint

# Set Maximum Delay Constraint Dialog Box

Use this dialog box to specify the required maximum delay for timing paths in the current design.

SmartTime automatically derives the individual maximum delay targets from clock waveforms and port input or output delays. So the maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

To open the Set Maximum Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor, click the **Constraints** menu and choose **Max Delay** (**Constraints > Max Delay**).



Set Maximum Delay Constraint	×
Maximum delay: ns	
From:	
	]
, Through:	
	]
To:	
	]
Comment:	
Help OK Cancel	]

Figure 157 · Set Maximum Delay Constraint Dialog Box

## **Maximum Delay**

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

#### From

Specifies the starting points for max delay constraint. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

#### Through

Specifies the through points for the multiple cycle constraint.



## То

Specifies the ending points for maximum delay constraint. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

#### Comment

Enables you to provide comments for this constraint.

#### See Also

Specifying a Maximum Delay Constraint

# Set Minimum Delay Constraint Dialog Box

Use this dialog box to specify the required minimum delay for timing paths in the current design.

SmartTime automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. So the minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

To open the Set Minimum Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor, click the **Constraints** menu and choose **Min Delay** (**Constraints > Min Delay**).

Set Minimum Delay (	Constraint				X
Minimum delay:	I	ns			
From:					
<				~	
Through:					
<				>	
To:					
<				~	
Comment:					
Help			ОК	Ca	ncel

Figure 158 · Set Minimum Delay Constraint Dialog Box



#### **Minimum Delay**

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

#### From

Specifies the starting points for minimum delay constraint. A valid timing starting point is a clock, a primary input, an input port, or a clock pin of a sequential cell.

#### Through

Specifies the through points for the multiple cycle constraint.

#### То

Specifies the ending points for minimum delay constraint. A valid timing ending point is a clock, a primary output, an input port, or a data pin of a sequential cell.

#### Comment

Enables you to provide comments for this constraint.

#### See Also

Specifying a Minimum Delay Constraint

# Set Multicycle Constraint Dialog Box

Use this dialog box to specify the paths that take multiple clock cycles in the current design.

Setting the multiple-cycle paths constraint overrides the single-cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks.

Note: When multiple timing constraints are set on the same timing path, the false path constraint has the highest priority and always takes precedence over multiple cycle path constraint. A specific maximum delay constraint overrides a general multicycle path constraint.

To open the Set Multicycle Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Multicycle**.



et Multicycle Constraint	
Specify multiplier(s) for: © Setup Check only © Setup and Hold Checks Setup Path Multiplier: Default setup edge	New setup
Hold edge	
Through:	
To:	× ···
Comment:	
Help OK	Cancel

Figure 159 · Set Multicycle Constraint Dialog Box

### **Setup Path Multiplier**

Specifies an integer value that represents a number of cycles the data path must have for a setup check. No hold check will be performed.

## From

Specifies the starting points for the multiple cycle constraint. A valid timing starting point is a clock, a primary input, an inout port, or the clock pin of a sequential cell.



## Through

Specifies the through points for the multiple cycle constraint.

## То

Specifies the ending points for the multiple cycle constraint. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## Comment

Enables you to provide comments for this constraint.

When you select the Setup and Hold Checks option, an additional field appears in this dialog box: **Hold Path Multiplier**.

t Multicycle Constraint
Specify multiplier(s) for: © Setup Check only © Setup and Hold Checks Setup Path Multiplier: Default setup edge New setup Hold 0
Hold Path Multiplier: 0  From:
Through:
Comment:
Help OK Cancel

Figure 160 · Set Multicycle Constraint Dialog Box with Setup and Hold Checks Selected

### **Hold Path Multiplier**

Specifies an integer value that represents a number of cycles the data path must have for a hold check, starting from one cycle before the setup check edge.

#### See Also

Specifying a Multicycle Constraint



# Set Output Delay Constraint Dialog Box

Use this dialog box to apply output delay constraints. This constraint defines the output delay of an output relative to a clock.

To open the Set Output Delay Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Output Delay**.

# **Clock-to-Output**

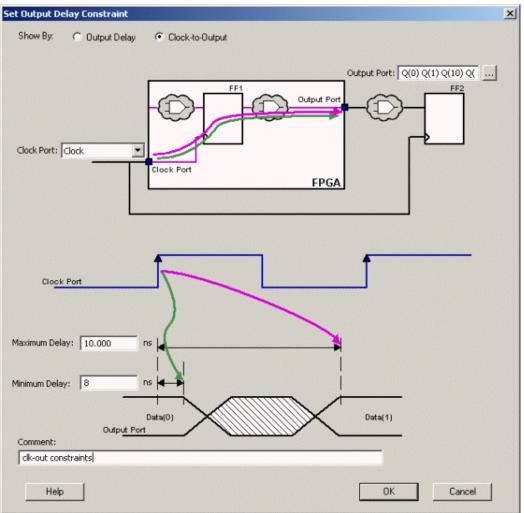


Figure 161 · Set Output Delay (Show By: Clock-to-Output) Dialog Box

## **Output Port**

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.

## **Clock Port**

Specifies the clock reference to which the specified **Clock-to-Output** is related.

#### **Clock edge**

Indicates the clock edge of the launched edge.



### **Maximum Delay**

Specifies the delay for the longest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

#### **Minimum Delay**

Specifies the delay for the shortest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

#### Comment

Enables you to provide comments for this constraint.

## **Output Delay**

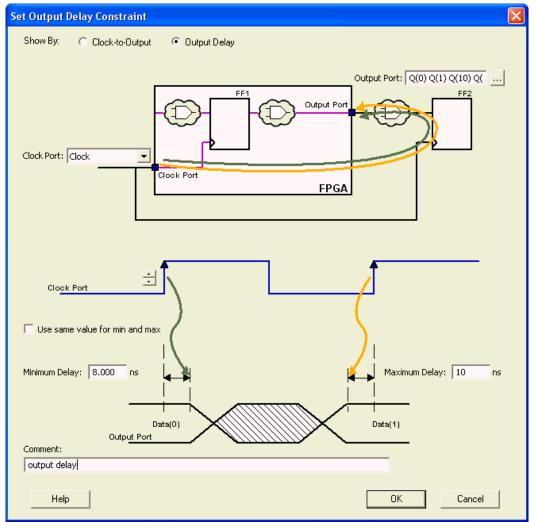


Figure 162 · Set Output Delay (Show By: Output Delay) Dialog Box

### **Output Port**

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.

#### **Clock Port**

Specifies the clock reference to which the specified output delay is related.



#### Clock edge

Indicates the launching edge of the clock.

#### **Maximum Delay**

Specifies the delay for the longest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library setup time.

#### **Minimum Delay**

Specifies the delay for the shortest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library hold time.

#### Comment

Enables you to provide comments for this constraint.

#### See Also

Specifying an Output Delay Constraint

# SmartTime Options Dialog Box - SmartFusion2, IGLOO2, RTG4

Use this dialog box to specify the SmartTime options to perform timing analysis.

This interface includes the following categories:

- General
- Analysis
- Advanced

To open the SmartTime Options dialog box (shown below) from the SmartTime tool, choose **Tools > Options**.

#### General

SmartTime Options		? ×
Option Categories Select a category: General Analysis Advanced	General Operating Conditions Perform maximum delay analysis based on WORST Perform minimum delay analysis based on BEST Clock Domains ✓ Include inter-clock domains in calculations for timing analysis. ✓ Enable recovery and removal checks.	case  case  Restore Defaults
Help		OK Cancel

Figure 163 · SmartTime Options - General Dialog Box



#### **Operating Conditions**

Allows you to perform maximum or minimum delay analysis based on the Best, Typical, or Worst case. By default, maximum delay analysis is based on WORST case and minimum delay analysis is based on BEST case.

#### **Clock Domains**

- Include inter-clock domains in calculations for timing analysis: Enables you to specify if SmartTime must use inter-clock domains in calculations for timing analysis. By default, this option is unchecked.
- Enable recovery and removal checks: Enables SmartTime to check removal and recovery time on asynchronous signals. Additional sets are created in each clock domain in Analysis View to report the corresponding paths.

#### **Restore Defaults**

Resets all the options in the General panel to their default values.

## **Analysis**

Option Categories	Analysis View	
<ul> <li>Select a category: General</li> </ul>	Display of Paths	
Analysis	Limit the number of paths shown in a path set to:	100
Advanced	<ul> <li>Filter the paths by slack value</li> <li>Slack range from:ns to:</li> <li>Show clock network details in expanded path</li> <li>Limit the number of parallel paths in expanded path to:</li> </ul>	ns
Help		Restore Defaults OK Cancel

Figure 164 · SmartTime Options - Analysis View Dialog Box

#### **Display of Paths**

Limits the number of paths shown in a path set for timing analysis. The default value is 100. You must specify a number greater than 1.

#### Filter the paths by slack value

Specifies the slack range between minimum slack and maximum slack. This option is unchecked by default.

#### Show clock network details in expanded path

Displays the clock network details as well as the data path details in the Expanded Path views.

**Limit the number of parallel paths in expanded path to**: For each expanded path, specify the maximum number of parallel paths that SmartTime displays. The default number of parallel paths is 1.

#### **Restore Defaults**

Resets all the options in the Analysis View panel to their default values.



## Advanced

SmartTime Options		? ×
Option Categories Select a category: General Analysis Advanced	Advanced Special Situtations Use loopback in bi-directional buffers(bibufs) V Break paths at asynchronous pins V Disable non-unate arcs in clock network Scenarios Use this scenario for timing analysis : Use this scenario for timing-driven place-and-route:	Primary Primary
Help		Restore Defaults OK Cancel

Figure 165 · SmartTime Options - Advanced Dialog Box

#### **Special Situations**

Enables you to specify if you need to use loopback in bi-directional buffers (bibufs) and/or break paths at asynchronous pins.

#### **Scenarios**

Enables you to select the scenario to use for timing analysis and for timing-driven place-and-route.

#### **Restore Defaults**

Resets all the options in the Analysis View panel to their default values.

# Store Filter as Analysis Set Dialog Box

Use this dialog box to specify a filter.

To open the **Store Filter as Analysis Set** dialog box (shown below) from the SmartTime Timing Analyzer, select a path and click the **Store Filter** button in the Analysis View Filter.

Store Filter	as Analysis Set		
Name:	MyFilter01		
Help		ОК	Cancel

Figure 166 · Store Filter as Analysis Set Dialog Box

### Name

Specifies the name of the filtered set.

#### See Also

Using filters



# **Timing Bottleneck Analysis Options Dialog Box**

Use this dialog box to customize the timing bottleneck report.

You can set report bottleneck options for the following categories:

- General pane
- Bottleneck pane
- Sets pane

To open the Timing Bottleneck Analysis Options dialog box (shown below) from the SmartTime tool, choose **Tools > Bottleneck Analysis**.

# **General Pane**

Timing Bottleneck Analysis Options				? ×
Option Categories Select a category: General Bottleneck Sets	General Slack Maximum slack to include	0	ns	
Help			Restore Defau	Its

Figure 167 · Timing Bottleneck Report - General Pane Dialog Box

### Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

## **Restore Defaults**

Resets all the options in the General pane to their default values.



# **Bottleneck Pane**

ption Categories	Bottleneck options	
<ul> <li>Select a category: General</li> <li>Bottleneck</li> </ul>	Cost Type:	Path Count 💌
Sets	Limit the number of paths per section to:	100
	Limit the number of parallel paths per section to:	1
	Limit the number of reported instances to:	10
		Restore Defaults

Figure 168 · Timing Bottleneck Report - Bottleneck Pane Dialog Box

## **Bottleneck Options**

**Cost Type**: Select the cost type that SmartTime will include in the bottleneck report. By default, path count is selected. You may select one of the following two items from the drop-down list:

- **Path count**: This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance. This is the default.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

**Limit the number of paths per section to**: Specify the maximum number of paths per set type that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of parallel paths per section to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the

report. Only cells that lie on these violating paths are reported. The default number of parallel paths is 1.

Limit the number of reported instances: Specify the maximum number of cells that SmartTime will include per section in the report. The default number of cells is 10.

#### **Restore Defaults**

Resets all the options in the Bottleneck panel to their default values.



## Sets Pane

Option Categories	Bottleneck options			
<ul> <li>Select a category: General Bottleneck Sets</li> </ul>	Set Selection Entire des Clock Dom Clock:		*	
	Type:			
	Use existi Name: Use Input	my_set to Output Set	•	
	Filter From:			
	То:			
			Restore Defaults	

Figure 169 · Timing Bottleneck Report - Sets Pane Dialog Box

This pane has four mutually exclusive options:

- Entire Design
- Clock Domain
- Use existing user set
- Use Input to Output Set

Entire Design: Select this option to display the bottleneck information for the entire design.

**Clock Domain**: Select this option to display the bottleneck information for the selected clock domain. You can specify the following options:

- Clock: Allows pruning based on a given clock domains. Only cells that lie on these violating paths are reported.
- Type: This option can only be used in conjunction with -clock. The acceptable values are:

Value	Description
Register to Register	Paths between registers in the design
Asynchronous to Register	Paths from asynchronous pins to registers
Register to Asynchronous	Paths from registers to asynchronous pins
External Recovery	The set of paths from inputs to asynchronous pins
External Setup	Paths from input ports to register
Clock to Output	Paths from registers to output ports

**Use existing user set**: Displays the bottleneck information for the existing user set selected. Only paths that lie within the name set are will be considered towards the bottleneck report.



Filter: Allows you to filter the bottleneck report by the following options:

• From: Reports only cells that lie on violating paths that start at locations specified by this option.

• To: Reports only cells that lie on violating paths that end at locations specified by this option.

Filter defaults to all outputs.

#### **Restore Defaults**

Resets all the options in the Paths panel to their default values.

#### See Also

**Bottleneck Analysis** 

# **Timing Datasheet Report Options Dialog Box**

Use this dialog box to select the output format for your timing datasheet report.

To open the **Timing Datasheet Report Options** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, choose **Tools > Reports > Datasheet**.

You can generate your report in one of two formats:

#### Plain Text

Select this option to save your report to disk in plain ASCII text format.

#### **Comma Separated Values**

Select this option to save your report to disk in comma-separated value format (.CSV) format, which you can import into a spreadsheet.

Option Categories	General
<ul> <li>Select a category: General</li> </ul>	Format         Image: Plain Text       Image: Comma Separated Values         Image: Edit generated XML file name
	Restore Defaults

Figure 170 · Datasheet Report Options Dialog Box

### **Restore Defaults**

Resets the option to its default value, which is Plain Text.

#### See Also

Generating a datasheet report



<u>Understanding datasheet reports</u> report (Datasheet) using SmartTime

# **Timing Report Options Dialog Box**

Use this dialog box to customize the timing report.

You can set report options for the following categories:

- <u>General</u>
- Paths
- <u>Sets</u>
- Clock Domains

To open the Timing Report Options dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports> Timer**.

## General

Option Categories	General
<ul> <li>Select a category: General Paths Sets Clock Domains</li> </ul>	Format <ul> <li>Comma Separated Values</li> <li>Edit generated XML file name</li> </ul> Summary           Include a summary of timing results in this report           Slack           Filter paths by slack threshold           Maximum slack to include
	Restore Defaults

Figure 171 · Timing Report Options - General Dialog Box

#### Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

#### Summary

Specifies whether or not the summary section will be included in the report. By default, this option is selected.

#### **Analysis**

Specifies the type of analysis to be included in the timing report. It can be either a Maximum Delay Analysis report or Minimum Delay Analysis report. By default, the Maximum Delay Analysis report is included in the timing report.



#### Slack

Specifies whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default, the paths are not filtered by slack.

#### **Restore Defaults**

Resets all the options in the General panel to their default values.

## **Paths**

Timing Report Options		×
Option Categories 	Paths         Display of paths         Include detailed path information in this report         Limit the number of reported paths per section to:         1         Limit the number of expanded paths per section to:         1         Limit the number of parallel paths in expanded path to:         1         Restore Defaults	
Help	OK	

Figure 172 · Timing Report Options - Paths Dialog Box

#### **Display of Paths**

**Include detailed path information in this report**: Check this box to include the detailed path information in the timing report.

**Limit the number of reported paths per section to**: Specify the maximum number of paths that SmartTime will include per section in the report.

**Limit the number of expanded paths per section to**: Specify the maximum number of expanded paths that SmartTime will include per section in the report.

**Limit the number of parallel paths in expanded path to**: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

#### **Restore Defaults**

Resets all the options in the Paths panel to their default values.



# Sets

Timing Report Options		X
Option Categories - Select a category: - General - Paths - Sets - Clock Domains	Sets         Display of Sets         Include user sets in this report         Include Input to Dutput sets in this report	ılts
Help	OK Cancel	

Figure 173 · Timing Report Options - Sets Dialog Box

## **Display of Sets**

Specifies whether or not the user sets will be included in the timing report.

User sets are either filters that you have created and stored on the default paths sets (Register to Register, Inputs to Register, etc.) or Pin to Pin user sets. By default, the paths for these sets are not reported. In addition, specify whether the Inputs to Output sets will be included in the report. By default, the Input to Output sets are reported.

### **Restore Defaults**

Resets both options in the Sets panel to their default values.



# **Clock Domains**

Timing Report Options		×
Option Categories 	Clock Domains Display of Clock Domains ✓ Include clock domains Limit reporting on clock domains to specified domains CLK PLL_CLK ULEDLS_BLOCK/U[1]_count[1]:G ULEDLS_BLOCK/U[2]_count[2]:G ULEDLS_BLOCK/U[2]_count[3]:G ULEDLS_BLOCK/U[5]_count[3]:G ULEDLS_BLOCK/U[5]_count[5]:C ULEDLS_BLOCK/U[5]_C UL	
	Restore Default:	s
Help	OK Cancel	

Figure 174 · Timing Report Options - Clock Domains Dialog Box

#### **Display of Clock Domains**

Lets you specify what clock domains will be included in the report. By default, the current clock domains used by the timing engine will be reported.

#### **Include Clock Domains**

Enables you to include or exclude clock domains in the report. Click the checkbox to include clock domains.

### Limit reporting on clock domains to specified domains

Lets you include one or more of the clock domain names in the box, or include additional clock domain names using **Select Domains**.

#### **Restore Defaults**

Resets all options in the Clock Domains panel to their default values.

#### See Also

<u>Generating a datasheet report</u> <u>Understanding datasheet reports</u> report (Datasheet) using SmartTime

# **Timing Violations Report Options Dialog Box**

Use this dialog box to customize the timing violation report.

You can set report violation options for the following categories:

- General
- Paths



To open the Timing Report Options dialog box (shown below) from the SmartTime tool, choose **Tools > Reports > Timing Violations**.

## General

Option Categories   Select a category:	General	
General Paths	<ul> <li>Plain Text</li> <li>Edit generated XML file name</li> </ul>	Comma Separated Values
	Slack Filter paths by slack threshold Maximum slack to include	0 ns
		Restore Defaults

Figure 175 · Timing Violations Report - General Dialog Box

## Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

#### Analysis

Lets you specify what type of analysis will be reported in the report. By default, the report includes Maximum Delay Analysis.

#### Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

#### **Restore Defaults**

Resets all the options in the General panel to their default values.



# Paths

Timing Violations Report Options		? ×
Option Categories  Select a category:	Display of paths	
General Paths	$\boxed{\ensuremath{\mathcal{V}}}$ Limit the number of reported paths	
	Limit the number of paths per section to:	100
	Limit the number of expanded paths per section to:	0
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults
Help		OK Cancel

Figure 176 · Timing Violations Report - Paths Dialog Box

### **Display of paths**

**Limit the number of reported paths**: Check this box to limit the number of paths in the report. By default, the number of paths is limited.

Limit the number of paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

**Limit the number of expanded paths per section to**: Specify the maximum number of expanded paths that SmartTime will include per section in the report. The default number of expanded paths is 0.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

#### **Restore Defaults**

Resets all the options in the Paths panel to their default values.

#### See Also

<u>Generating timing violation report</u> <u>Understanding timing violation report</u> report (Timing violations) using SmartTime



# Menus, Tools, and Shortcut Keys

# File Menu

This menu is available in both Timing Constraint Editor View and Timing Analysis View.

Command	lcon	Shortcut	Function
Commit		CTRL + S	Saves changes to the working design for this Designer session only. Note: To save changes to disk, you must also save your file in Designer.
Print Preview			Displays the active design in a Preview window
Print	9	CTRL + P	Displays the Print dialog box from which you can print your active design
Exit			Closes SmartTime

# Edit Menu

Command	lcon	Shortcut	Function
Undo	ŝ	CTRL + Z	Reverses your last action
Redo	đ	CTRL + Y	Reverses the action of your last Undo command
Cut		CTRL + X	Removes the selection from your design
Сору		CTRL + C	Copies the selection to the Clipboard
Paste	Ê	CTRL + V	Pastes the selection from the Clipboard
Modify			Displays appropriate dialog box to edit the current constraint
Delete	×	Del	Deletes the selected constraint
Select All		CTRL + A	Selects all logic in your design



# View Menu

This menu is available in both Timing Constraint Editor View and Timing Analysis View.

Command	lcon	Shortcut	Function
Recalculate All	2	F9	Recalculates all the generated values
Table: Name >			Provides option for customizing the table in the Timing Analysis View
Toolbars >			Hides or displays groups of toolbar buttons
Status Bar			Shows or hides the status bar at the bottom of the window
Scenarios			Shows or hides the scenarios panel

# View > Table

Command	lcon	Shortcut	Function
Customize Current Table			Enables you to select columns and the order of the columns for the Paths List in the Timing Analysis View

# View > Toolbars

Command	lcon	Shortcut	Function
Standard			Shows or hides the standard toolbar
Constraints			Show or hides the constraints toolbar
Analysis			Shows or hides the analysis toolbar

# **Actions Menu**

Command	lcon	Shortcut	Function
Constraints >			Provides options to create new constraints
Analysis >			Provides options to perform timing analysis



# **Actions > Constraints**

Command	lcon	Shortcut	Function
Clock	m		Displays the Create Clock Constraint dialog box
Generated Clock	HA		Displays the Create Generated Clock Constraint dialog box
Input Delay	₩ ⊠ <b>≯</b>		Displays the Set Input Delay Constraint dialog box
Output Delay	*⊠		Displays the Set Output Delay Constraint dialog box
Max Delay	$\sim$		Displays the Set Maximum Delay Constraint dialog box
Min Delay	$\sim$		Displays the Set Minimum Delay Constraint dialog box
False Path	0.		Displays the Set False Path Constraint dialog box
Multicycle	<b>M</b>		Displays the Set Mulitcycle Constraint dialog box
Latency	¶		Displays the Set Clock Source Latency dialog box
Disable Timing	5		Displays the Set Constraint to Disable Timing Arcs dialog box
Clock to Clock Uncertainty	<b>*</b>		Displays the Set Clock-to-Clock Uncertainty dialog box

# Actions > Analysis

Command	lcon	Shortcut	Function
Clock Domain	٩		Displays Manage Clock Domain dialog box
Path Set	М		Displays Add Path Analysis Set dialog box

# **Tools Menu**

Command	lcon	Shortcut	Function
Constraints Editor >			Provides options for constraints scenarios



Command	lcon	Shortcut	Function
Constraint Wizard >	9		Opens the Constraint Wizard for creating clock and I/O constraints
Timing Analyzer >			Provides options for timing analysis
Constraint Checker	<b>M</b>		Verifies if all timing constraints are valid
Reports >			Provides options to generate reports
Options			Displays the SmartTime <b>Options</b> dialog box

# Tools > Constraints Editor

Command	lcon	Shortcut	Function
1. Primary Scenario (and all other available scenarios)			Displays the primary set of timing constraints for the selected scenario
Scenarios			Opens the scenario panel, which lists all available scenarios
New scenario			Creates a new scenario

# Tools > Timing Analyzer

Command	lcon	Shortcut	Function
Maximum Delay Analysis	M		Displays the Maximum Delay Analysis View
Minimum Delay Analysis	$\mathbf{k}$		Displays the Minimum Delay Analysis View
Bottleneck Analysis			Displays the Bottleneck Analysis View

# Tools > Reports

Command	lcon	Shortcut	Function
Report Paths			Displays the <b>Timing Report Options</b> dialog box
Report Violations			Displays the <b>Timing Violations Report</b> <b>Options</b> dialog box
Report Datasheet			Displays the <b>Datasheet Report Options</b> dialog box



Command	lcon	Shortcut	Function
Report Constraints Coverage			Displays the <b>Constraints Coverage Report</b> <b>Options</b> dialog box
Report Combinational Loop			Displays the Combinational Loop report

# Window Menu

This menu is available in both Timing Constraint Editor View and Timing Analysis View.

Command	Function
New Window	Opens another window for the currently active tool <b>Note: Use these</b> windows to view different parts of the design at the same time.
Cascade	Arranges windows so you can see the title bar of each window
Tile Horizontally	Arranges windows side-by-side in a horizontal pattern
Tile Vertically	Arranges windows side-by-side in a vertical pattern
Minimize All Windows	Minimizes all active windows
Arrange Icons	Arranges minimized windows left-to-right across the bottom of the Tool window
Close All Windows	Closes all tool views

# Help Menu

Command	Function
Help Topics	Displays the first Help topic for the SmartTime tool
SmartTime User's Guide	Displays the SmartTime User's Guide
About SmartTime	Displays the current version number and copyright information for the SmartTime tool
Data Change History	Displays features and enhancements, bug fixes and known issues for the current software release that may impact timing data of the current design



# SmartTime Toolbar

The SmartTime toolbar contains commands for constraining or analyzing designs. Tool tips are available for each button.

lcon	Description
8	Commits the changes
<b>-</b>	Prints the contents of the constraints editor
<b>B</b>	Copies data to the clipboard
	Pastes data from the clipboard
	Modifies the selected object from the constraints editor
×	Deletes the selected object from the constraints editor
<u>2</u>	Undoes previous changes
2	Redoes previous changes
×	Opens the maximum delay analysis view
×	Opens the minimum delay analysis view
<b>@</b>	Opens the manage clock domains manager
X	Opens the path set manager
2	Recalculates all
37	Opens the constraints editor
m	Opens the add clock constraint dialog box
m	Opens the add generated clock constraint dialog box
<b>8</b>	Opens the set input delay clock constraint dialog box
<b>≫</b> ⊠	Opens the set output delay clock constraint dialog box
<u>m</u>	Opens the manage clock domain manager Opens the path set manager Recalculates all Opens the constraints editor Opens the add clock constraint dialog box Opens the add generated clock constraint dialog box Opens the set input delay clock constraint dialog box



lcon	Description
<u>,0</u> ,	Opens the set false path constraint dialog box
*	Opens the set maximum delay constraint dialog box
*	Opens the set minimum delay constraint dialog box
<u>M</u>	Opens the set multicycle constraint dialog box
<b>F</b>	Opens the set clock source latency dialog box
<u>100</u>	Opens the set constraint to disable timing arcs dialog box
<u></u>	Opens the set clock-to-clock uncertainty constraint dialog box
~~	Checks timing constraints
B	Opens the constraint wizard



# **Data Change History - SmartTime**

The data change history lists features, enhancements and bug fixes for the current software release that may impact timing data of the current design.

To generate a data change history, from the **Help** menu, choose **Data Change History**. This opens a data change history in text format.

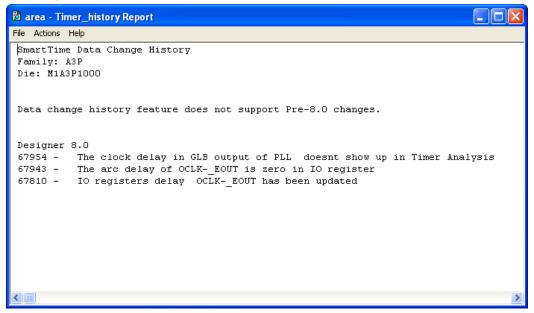


Figure 177 · SmartTime Data Change History Report



# **Tcl Commands**

## all\_inputs

Tcl command; returns an object representing all input and inout pins in the current design.

all\_inputs

### Arguments

None

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Exceptions**

You can only use this command as part of a -from, -to, or -through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path</u>, and <u>set false path</u>.

#### **Examples**

set\_max\_delay -from [all\_inputs] -to [get\_clocks ck1]

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

# all\_outputs

Tcl command; returns an object representing all output and inout pins in the current design.

all\_outputs

#### Arguments

None

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Exceptions**

You can only use this command as part of a -from, -to, or -through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path, and set false path.</u>

#### **Examples**

set\_max\_delay -from [all\_inputs] -to [all\_outputs]

#### See Also

Tcl documentation conventions



**Designer Tcl Command Reference** 

## all\_registers

Tcl command; returns an object representing register pins or cells in the current scenario based on the given parameters.

```
all_registers [-clock clock_name]
[-async_pins][-output_pins][-data_pins][-clock_pins]
```

### **Arguments**

-clock clock\_name

Specifies the name of the clock domain to which the registers belong. If no clock is specified, all registers in the design will be targeted.

-async\_pins

Lists all register pins that are async pins for the specified clock (or all registers asynchronous pins in the design).

-output\_pins

Lists all register pins that are output pins for the specified clock (or all registers output pins in the design). -data\_pins

-data\_pins

Lists all register pins that are data pins for the specified clock (or all registers data pins in the design). -clock\_pins

Lists all register pins that are data pins for the specified clock (or all registers clock pins in the design).

### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Exceptions**

You can only use this command as part of a -from, -to, or -through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path</u>, and <u>set false path</u>.

#### **Examples**

```
set_max_delay 2.000 -from { ff_m:CLK ff_s2:CLK } -to [all_registers -clock_pins -clock {
ff_m:Q }]
```

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

## check\_constraints

Tcl command; checks all timing constraints in the current scenario for validity. This command performs the same checks as when the constraint is entered through SDC or Tcl.

check\_constraints

#### **Arguments**

None



## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### **Example**

check\_constraints

# clone\_scenario (SmartFusion2, IGLOO2, and RTG4)

Tcl command; creates a new timing scenario by duplicating an existing one. You must provide a unique name (that is, it cannot already be used by another timing scenario).

clone\_scenario original new\_scenario\_name

## **Arguments**

#### original

Specifies the name of the source timing scenario to clone (copy). The source must be a valid, existing timing scenario.

new\_scenario\_name

Specifies the name of the new scenario to be created.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## Description

This command creates a timing scenario with the <u>new\_scenario\_name</u>, which includes a copy of all constraints in the original scenario. The new scenario is then added to the list of scenarios.

## Example

clone\_scenario primary my\_new\_scenario

#### See Also

<u>create\_scenario</u> <u>delete\_scenario</u> <u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

## create\_clock

Tcl command; creates a clock constraint on the specified ports/pins, or a virtual clock if no source other than a name is specified.

```
create_clock -period period_value [-name clock_name]
[-waveform> edge_list][source_objects]
```

## Arguments

#### -period period\_value

Specifies the clock period in nanoseconds. The value you specify is the minimum time over which the clock waveform repeats. The period\_value must be greater than zero.

-name clock\_name

Specifies the name of the clock constraint. You must specify either a clock name or a source.



#### -waveform edge\_list

Specifies the rise and fall times of the clock waveform in ns over a complete clock period. There must be exactly two transitions in the list, a rising transition followed by a falling transition. You can define a clock starting with a falling edge by providing an edge list where fall time is less than rise time. If you do not specify -waveform option, the tool creates a default waveform, with a rising edge at instant 0.0 ns and a falling edge at instant (period\_value/2)ns.

#### source\_objects

Specifies the source of the clock constraint. The source can be ports, pins, or nets in the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing one. You must specify either a source or a clock name.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Description

Creates a clock in the current design at the declared source and defines its period and waveform. The static timing analysis tool uses this information to propagate the waveform across the clock network to the clock pins of all sequential elements driven by this clock source.

The clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

#### **Examples**

The following example creates two clocks on ports CK1 and CK2 with a period of 6, a rising edge at 0, and a falling edge at 3:

create\_clock -name {my\_user\_clock} -period 6 CK1

create\_clock -name {my\_other\_user\_clock} -period 6 -waveform {0 3} {CK2}

The following example creates a clock on port CK3 with a period of 7, a rising edge at 2, and a falling edge at 4:

create\_clock -period 7 -waveform {2 4} [get\_ports {CK3}]

#### See Also

create\_generated\_clock <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

## create\_generated\_clock

Tcl command; creates an internally generated clock constraint on the ports/pins and defines its characteristics.

```
create_generated_clock [-name name] -source reference_pin [-divide_by divide_factor] [-
multiply_by multiply_factor] [-invert] source
```

#### Arguments

-name *name* 

Specifies the name of the clock constraint.

-source reference\_pin

Specifies the reference pin in the design from which the clock waveform is to be derived.

-divide\_by divide\_factor

Specifies the frequency division factor. For instance if the *divide\_factor* is equal to 2, the generated clock period is twice the reference clock period.



#### -multiply\_by multiply\_factor

Specifies the frequency multiplication factor. For instance if the *multiply\_factor* is equal to 2, the generated clock period is half the reference clock period.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

source

Specifies the source of the clock constraint on internal pins of the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing clock. Only one source is accepted. Wildcards are accepted as long as the resolution shows one pin.

### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Description**

Creates a generated clock in the current design at a declared source by defining its frequency with respect to the frequency at the reference pin. The static timing analysis tool uses this information to compute and propagate its waveform across the clock network to the clock pins of all sequential elements driven by this source.

The generated clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

### **Examples**

The following example creates a generated clock on pin U1/reg1:Q with a period twice as long as the period at the reference port CLK.

create\_generated\_clock -name {my\_user\_clock} -divide\_by 2 -source [get\_ports
{CLK}] U1/reg1:Q

The following example creates a generated clock at the primary output of myPLL with a period <sup>3</sup>/<sub>4</sub> of the period at the reference pin clk.

create\_generated\_clock -divide\_by 3 -multiply\_by 4 -source clk [get\_pins {myPLL:CLK1}]

#### See Also

create\_clock <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

## create\_scenario

Tcl command; creates a new timing scenario with the specified name. You must provide a unique name (that is, it cannot already be used by another timing scenario).

create\_scenario name

## Arguments

name

Specifies the name of the new timing scenario.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



## Description

A timing scenario is a set of timing constraints used with a design. Scenarios enable you to easily refine the set of timing constraints used for Timing-Driven Place-and-Route, so as to achieve timing closure more rapidly.

This command creates an empty timing scenario with the specified name and adds it to the list of scenarios.

## Example

create\_scenario scenario\_A

#### See Also

clone\_scenario Tcl Command Documentation Conventions Designer Tcl Command Reference

## expand\_path

Tcl command; displays expanded path information (path details) for paths. The paths to be expanded are identified by the parameters required to display these paths with list\_paths. For example, to expand the first path listed with list\_paths -clock {MYCLOCK} -type {register\_to\_register}, use the command expand\_path - clock {MYCLOCK} -type {register\_to\_register}. Path details contain the pin name, type, net name, cell name, operation, delay, total delay, and edge as well as the arrival time, required time, and slack. These details are the same as details available in the SmartTime Expanded Path window.

expand\_path
-index value
-set name
-clock clock name
-type set\_type
-analysis {max| min}
-format {csv | text}
-from\_clock clock name
-to\_clock clock name

## **Arguments**

#### -index value

Specify the index of the path to be expanded in the list of paths. Default is 1.

-analysis {max | min}

Specify whether the timing analysis is done is max-delay (setup check) or min-delay (hold check). Valid values: max or min.

```
-format {csv | text}
```

Specify the list format. It can be either text (default) or csv (comma separated values). The former is suited for display the latter for parsing.

-set name

Displays a list of paths from the named set. You can either use the -set option to specify a user set by its name or use both -clock and -type to specify a set.

-clock clock name

Displays the set of paths belonging to the specified clock domain. You can either use this option along with -type to specify a set or use the -set option to specify the name of the set to display.

#### -type set\_type

Specifies the type of paths in the clock domain to display in a list. You can only use this option with the - clock option. You can either use this option along with -clock to specify a set or use the -set option to specify a set name.



Value	Description
reg_to_reg	Paths between registers in the design
external_setup	Path from input ports to registers
external_hold	Path from input ports to registers
clock_to_out	Path from registers to output ports
reg_to_async	Path from registers to asynchronous pins
external_recovery	Set of paths from inputs to asynchronous pins
external_removal	Set of paths from inputs to asynchronous pins
async_to_reg	Path from asynchronous pins to registers

#### -from\_clock clock\_name

Displays a list of timing paths for an inter-clock domain set belonging to the source clock specified. You can only use this option with the -to\_clock option, not by itself.

-to\_clock clock\_name

Displays a list of timing paths for an inter-clock domain set belonging to the sink clock specified. You can only use this option with the -from\_clock option, not by itself.

-analysis *name* 

Specifies the analysis for the paths to be listed. The following table shows the acceptable values for this argument.

Value	Description
maxdelay	Maximum delay analysis
mindelay	Minimum delay analysis

#### -index list\_of\_indices

Specifies which paths to display. The index starts at 1 and defaults to 1. Only values lower than the max\_paths option will be expanded.

-format value

Specifies the file format of the output. The following table shows the acceptable values for this argument:

Value	Description	
text	ASCII text format	
csv	Comma separated value file format	

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



### **Examples**

Note: The following example returns a list of five paths:

```
puts [expand_path -clock { myclock } -type {reg_to_reg }]
puts [expand_path -clock {myclock} -type {reg_to_reg} -index { 1 2 3 } -format text]
```

See Also

list paths

## get\_cells

Tcl command; returns an object representing the cells (instances) that match those specified in the pattern argument.

get\_cells pattern

#### Arguments

pattern

Specifies the pattern to match the instances to return. For example, "get\_cells U18\*" returns all instances starting with the characters "U18", where "\*" is a wildcard that represents any character string.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Description**

This command returns a collection of instances matching the pattern you specify. You can only use this command as part of a –from, -to, or –through argument in the following Tcl commands: <u>set\_max delay</u>, <u>set\_multicycle\_path</u>, and <u>set\_false\_path</u>.

#### **Examples**

set\_max\_delay 2 -from [get\_cells {reg\*}] -to [get\_ports {out}]
set\_false\_path -through [get\_cells {Rblock/muxA}]

#### See Also

get\_clocks get\_nets get\_pins get\_ports Tcl Command Documentation Conventions Designer Tcl Command Reference

## get\_clocks

Tcl command; returns an object representing the clock(s) that match those specified in the pattern argument in the current timing scenario.

get\_clocks pattern

#### Arguments

pattern

Specifies the pattern to use to match the clocks set in SmartTime.



## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Description**

- If this command is used as a -from argument in either the set maximum (<u>set max delay</u>), or set minimum delay (<u>set min delay</u>), false path (<u>set false path</u>), and multicycle constraints (<u>set multicycle path</u>), the clock pins of all the registers related to this clock are used as path start points.
- If this command is used as a -to argument in either the set maximum (<u>set max delay</u>), or set minimum delay (<u>set min delay</u>), false path (<u>set false path</u>), and multicycle constraints (<u>set multicycle path</u>), the synchronous pins of all the registers related to this clock are used as path endpoints.

## **Example**

set\_max\_delay -from [get\_ports datal] -to \
[get\_clocks ck1]

#### See Also

<u>create\_clock</u> <u>create\_generated\_clock</u> <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

## get\_current\_scenario

Tcl command; returns the name of the current timing scenario.

get\_current\_scenario

#### **Arguments**

None

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

get\_current\_scenario

#### See Also

set\_current\_scenario Tcl documentation conventions Designer Tcl Command Reference

## get\_nets

Tcl command; returns an object representing the nets that match those specified in the pattern argument.

get\_nets pattern

## Arguments

pattern



Specifies the pattern to match the names of the nets to return. For example, "get\_nets N\_255\*" returns all nets starting with the characters "N\_255", where "\*" is a wildcard that represents any character string.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### **Description**

This command returns a collection of nets matching the pattern you specify. You can only use this command as source objects in create clock (<u>create\_clock</u>) or create generated clock (<u>create\_generated\_clock</u>) constraints and as -through arguments in the set false path, set minimum delay, set maximum delay, and set multicycle path constraints.

#### **Examples**

set\_max\_delay 2 -from [get\_ports RDATA1] -through [get\_nets {net\_chkpl net\_chkqi}]
set\_false\_path -through [get\_nets {Tblk/rm/n\*}]
create\_clock -name mainCLK -period 2.5 [get\_nets {cknet}]

#### See Also

create\_clock create\_generated\_clock set\_false\_path set\_min\_delay set\_max\_delay set\_multicycle\_path Tcl documentation conventions Designer Tcl Command Reference

## get\_pins

Tcl command; returns an object representing the pin(s) that match those specified in the pattern argument.

get\_pins pattern

## **Arguments**

#### pattern

Specifies the pattern to match the pins to return. For example, "get\_pins clock\_gen\*" returns all pins starting with the characters "clock\_gen", where "\*" is a wildcard that represents any character string.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### Example

create\_clock -period 10 [get\_pins clock\_gen/reg2:Q]

#### See Also

create\_clock
create\_generated\_clock
set\_clock\_latency
set\_false\_path
set\_min\_delay



set\_max\_delay set\_multicycle\_path Tcl documentation conventions Designer Tcl Command Reference

# get\_ports

Tcl command; returns an object representing the port(s) that match those specified in the pattern argument.

get\_portspattern

## Argument

#### pattern

Specifies the pattern to match the ports.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

### Example

create\_clock -period 10 [get\_ports CK1]

#### See Also

create\_clock set\_clock\_latency set\_input\_delay set\_output\_delay set\_min\_delay set\_max\_delay set\_false\_path set\_multicycle\_path Tcl documentation conventions Designer Tcl Command Reference

## list\_clock\_latencies

Tcl command; returns details about all of the clock latencies in the current timing constraint scenario.

list\_clock\_latencies

## **Arguments**

None

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

puts [list\_clock\_latencies]



#### See Also

set\_clock\_latency remove\_clock\_latency Tcl documentation conventions Designer Tcl Command Reference

# list\_clock\_uncertainties

Tcl command; returns details about all of the clock uncertainties in the current timing constraint scenario.

list\_clock\_uncertainties

### **Arguments**

None

### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

list\_clock\_uncertainties

#### See Also

set\_clock\_uncertainty
remove\_clock\_uncertainty
Designer Tcl Command Reference

## list\_clocks

Tcl command; returns details about all of the clock constraints in the current timing constraint scenario.

list\_clocks

## Arguments

None

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

puts [list\_clocks]

#### See Also

<u>create\_clock</u> <u>remove\_clock</u> <u>Tcl documentation conventions</u> Designer Tcl Command Reference



# list\_disable\_timings

Tcl command; returns the list of disable timing constraints for the current scenario.

list\_disable\_timings

Arguments

None

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Example

list\_disable\_timings

#### See Also

**Designer Tcl Command Reference** 

## list\_false\_paths

Tcl command; returns details about all of the false paths in the current timing constraint scenario.

list\_false\_paths

#### Arguments

None

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

puts [list\_false\_paths]

#### See Also

set\_false\_path remove\_false\_path Tcl documentation conventions Designer Tcl Command Reference

# list\_generated\_clocks

Tcl command; returns details about all of the generated clock constraints in the current timing constraint scenario.

list\_generated\_clocks

### Arguments

None

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.



## **Examples**

puts [list\_generated\_clocks]

#### See Also

create\_generated\_clock remove\_generated\_clock Tcl documentation conventions Designer Tcl Command Reference

## list\_input\_delays

Tcl command; returns details about all of the input delay constraints in the current timing constraint scenario.

list\_input\_delays

#### **Arguments**

None

### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Examples

puts [list\_input\_delays]

#### See Also

set\_input\_delay remove\_input\_delay Tcl documentation conventions Designer Tcl Command Reference

## list\_max\_delays

Tcl command; returns details about all of the maximum delay constraints in the current timing constraint scenario.

list\_max\_delays

### **Arguments**

None

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

puts [list\_max\_delays]

#### See Also

set\_max\_delay remove\_max\_delay Tcl documentation conventions Designer Tcl Command Reference



# list\_min\_delays

Tcl command; returns details about all of the minimum delay constraints in the current timing constraint scenario.

list\_min\_delays

### Arguments

None

### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

puts [list\_min\_delays]

#### See Also

set\_min\_delay remove\_min\_delay Tcl documentation conventions Designer Tcl Command Reference

## list\_multicycle\_paths

Tcl command; returns details about all of the multicycle paths in the current timing constraint scenario.

list\_multicycle\_paths

#### Arguments

None

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

puts [list\_multicycle\_paths]

#### See Also

set\_multicycle\_path
remove\_multicycle\_path
Tcl documentation conventions
Designer Tcl Command Reference



# list\_objects

Tcl command; returns a list of object matching the parameter. Objects can be nets, pins, ports, clocks or instances.

list\_objects <object>

#### **Arguments**

Any timing constraint parameter.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### Example

The following example lists all the inputs in your design:

list\_objects [all\_inputs]

You can also use wildcards to filter your list, as in the following command:

list\_objects [get\_ports a\*]

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

## list\_output\_delays

Tcl command; returns details about all of the output delay constraints in the current timing constraint scenario.

list\_output\_delays

#### Arguments

None

### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

puts [list\_output\_delays]

#### See Also

set\_output\_delay remove\_output\_delay Tcl documentation conventions Designer Tcl Command Reference

## list\_paths

Tcl command; returns a list of the *n* worst paths matching the arguments. The number of paths returned can be changed using the set\_options -limit\_max\_paths <value> command.



```
list_paths
-analysis <max | min>
-format <csv | text>
-set <name>
-clock <clock name>
-type <set_type>
-from_clock <clock name>
-to_clock <clock name>
-in_to_out
-from <port/pin pattern>
-to <port/pin pattern>
```

## Arguments

```
-analysis <max | min>
```

Specifies whether the timing analysis is done for max-delay (setup check) or min-delay (hold check). Valid values are: max or min.

```
-format < text | csv >
```

Specifies the list format. It can be either text (default) or csv (comma separated values). Text format is better for display and csv format is better for parsing.

#### -set <<u>name</u>>

Returns a list of paths from the named set. You can either use the -set option to specify a user set by its name or use both -clock and -type to specify a set.

-clock <clock name>

Returns a list of paths from the specified clock domain. This option requires the -type option.

```
-type <set_type>
```

Specifies the type of paths to be included. It can only be used along with -clock. Valid values are:

reg\_to\_reg -- Paths between registers

external\_setup -- Path from input ports to data pins of registers

external\_hold -- Path from input ports to data pins of registers

clock\_to\_out -- Path from registers to output ports

reg\_to\_async -- Path from registers to asynchronous pins of registers

external\_recovery -- Path from input ports to asynchronous pins of registers

external\_removal -- Path from input ports to asynchronous pins of registers

async\_to\_reg -- Path from asynchronous pins to registers

-from\_clock <clock name>

Used along with -to\_clock to get the list of paths of the inter-clock domain between the two clocks.

-to\_clock <*clock name*>

Used along with -from\_clock to get the list of paths of the inter-clock domain between the two clocks. -in\_to\_out

Used to get the list of path between input and output ports.

-from <port/pin pattern>

Filter the list of paths to those starting from ports or pins matching the pattern.

-to <port/pin pattern>

Filter the list of paths to those ending at ports or pins matching the pattern.

## Example

The following command displays the list of register to register paths of clock domain clk1: puts [ list\_paths -clock clk1 -type reg\_to\_reg ]



#### See Also

create\_set expand\_path set\_options

## list\_scenarios

Tcl command; returns a list of names of all of the available timing scenarios.

list\_scenarios

### Arguments

None

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

list\_scenarios

#### See Also

get\_current\_scenario Tcl documentation conventions Designer Tcl Command Reference

## read\_sdc

The read\_sdc Tcl command evaluate an SDC file, adding all constraints to the specified scenario (or the current/default one if none is specified). Existing constraints are removed if -add is not specified.

```
read_sdc
-add
-scenario scenario_name
-netlist (user | optimized)
-pin_separator (: | /)
file name
```

## Arguments

#### -add

Specifies that the constraints from the SDC file will be added on top of the existing ones, overriding them in case of a conflict. If not used, the existing constraints are removed before the SDC file is read.

#### -scenario scenario\_name

Specifies the scenario to add the constraints to. The scenario is created if none exists with this name.

```
-netlist (user | optimized)
```

Specifies whether the SDC file contains object defined at the post-synthesis netlist (user) level or physical (optimized) netlist (used for timing analysis).

-pin\_separator sep

Specify the pin separator used in the SDC file. It can be either ':' or '/'.

#### file name

Specify the SDC file name.



## Example

The following command removes all constraints from the current/default scenario and adds all constraints from design.sdc file to it: read\_sdc design.sdc

. .

See Also

write\_sdc

## remove\_all\_constraints

Tcl command; removes all timing constraints from analysis.

remove\_all\_constraints

#### **Arguments**

None

### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

### **Example**

remove\_all\_constraints

#### See Also

remove\_scenario

## remove\_clock

Tcl command; removes the specified clock constraint from the current timing scenario.

```
remove_clock -name clock_name | -id constraint_ID
```

## Arguments

-name clock\_name

Specifies the name of the clock constraint to remove from the current scenario. You must specify either a clock name or an ID.

-id constraint\_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either an ID or a clock name that exists in the current scenario.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Description**

Removes the specified clock constraint from the current scenario. If the specified name does not match a clock constraint in the current scenario, or if the specified ID does not refer to a clock constraint, this command fails.



Do not specify both the name and the ID.

#### **Exceptions**

You cannot use wildcards when specifying a clock name.

### **Examples**

The following example removes the clock constraint named "my\_user\_clock": remove\_clock -name my\_user\_clock The following example removes the clock constraint using its ID: set clockId [create\_clock -name my\_user\_clock -period 2] remove\_clock -id \$clockId

#### See Also

create\_clock Tcl Command Documentation Conventions Designer Tcl Command Reference

## remove\_clock\_latency

Tcl command; removes a clock source latency from the specified clock and from all edges of the clock.

remove\_clock\_latency {-source clock\_name\_or\_source |-id constraint\_ID}

### Arguments

#### -source clock\_name\_or\_source

Specifies either the clock name or source name of the clock constraint from which to remove the clock source latency. You must specify either a clock or source name or its constraint ID.

-id constraint\_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either a clock or source name or its constraint ID.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Description

Removes a clock source latency from the specified clock in the current scenario. If the specified source does not match a clock with a latency constraint in the current scenario, or if the specified ID does not refer to a clock with a latency constraint, this command fails. Do not specify both the source and the ID.

#### **Exceptions**

You cannot use wildcards when specifying a clock name.

#### **Examples**

The following example removes the clock source latency from the specified clock. remove\_clock\_latency -source my\_clock

#### See Also

set\_clock\_latency
Tcl Command Documentation Conventions



**Designer Tcl Command Reference** 

## remove\_clock\_uncertainty

Tcl command; removes a clock-to-clock uncertainty from the current timing scenario by specifying either its exact arguments or its ID.

```
remove_clock_uncertainty -from | -rise_from | -fall_from from_clock_list -to | -rise_to| -
fall_to to_clock_list -setup {value} -hold {value}
remove_clock_uncertainty -id constraint_ID
```

### Arguments

-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. Only one of the *-from*, *-rise\_from*, or *-fall\_from* arguments can be specified for the constraint to be valid.

#### -rise\_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. Only one of the -from, -rise\_from, or -fall\_from arguments can be specified for the constraint to be valid. -fall\_from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. Only one of the -from, -rise\_from, or -fall\_from arguments can be specified for the constraint to be valid.

#### from\_clock\_list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. Only one of the -to, -rise\_to, or -fall\_to arguments can be specified for the constraint to be valid.

-rise\_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. Only one of the -to, -rise\_to, or -fall\_to arguments can be specified for the constraint to be valid. -fall\_to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. Only one of the -to, -rise\_to, or -fall\_to arguments can be specified for the constraint to be valid.

#### $to\_clock\_list$

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-id constraint\_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either the exact parameters to set the constraint or its constraint ID.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.



## Description

Removes a clock-to-clock uncertainty from the specified clock in the current scenario. If the specified arguments do not match clocks with an uncertainty constraint in the current scenario, or if the specified ID does not refer to a clock-to-clock uncertainty constraint, this command fails.

Do not specify both the exact arguments and the ID.

### **Examples**

remove\_clock\_uncertainty -from Clk1 -to Clk2
remove\_clock\_uncertainty -from Clk1 -fall\_to { Clk2 Clk3 } -setup
remove\_clock\_uncertainty 4.3 -fall\_from { Clk1 Clk2 } -rise\_to \*
remove\_clock\_uncertainty 0.1 -rise\_from [ get\_clocks { Clk1 Clk2 } ] -fall\_to { Clk3
Clk4 } -setup
remove\_clock\_uncertainty 5 -rise\_from Clk1 -to [ get\_clocks {\*} ]
remove\_clock\_uncertainty -id \$clockId

#### See Also

remove\_clock
remove\_generated\_clock
set\_clock\_uncertainty
Designer Tcl Command Reference

## remove\_disable\_timing

Tcl command; removes a disable timing constraint by specifying its arguments, or its ID. If the arguments do not match a disable timing constraint, or if the ID does not refer to a disable timing constraint, the command fails.

remove\_disable\_timing -from value -to value name -id name

#### Arguments

#### -from from\_port

Specifies the starting port. The -from and -to arguments must either both be present or both omitted for the constraint to be valid.

#### -to to\_port

Specifies the ending port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

#### name

Specifies the cell name where the disable timing constraint will be removed. It is an error to supply both a cell name and a constraint ID, as they are mutually exclusive. No wildcards are allowed when specifying a clock name, either alone or in an accessor command1.

#### -id name

Specifies the constraint name where the disable timing constraint will be removed. It is an error to supply both a cell name and a constraint ID, as they are mutually exclusive. No wildcards are allowed when specifying a clock name, either alone or in an accessor command1.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## Example

remove\_disable\_timing -from port1 -to port2 -id new\_constraint
Designer Tcl Command Reference



# remove\_false\_path

Tcl command; removes a false path from the current timing scenario by specifying either its exact arguments or its ID.

remove\_false\_path [-from from\_list] [-to to\_list] [-through through\_list] [-id constraint\_ID]
remove\_false\_path -id constraint\_ID

#### Arguments

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through  $through\_list$ 

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint\_ID

Specifies the ID of the false path constraint to remove from the current scenario. You must specify either the exact false path to remove or the constraint ID that refers to the false path constraint to remove.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Description**

Removes a false path from the specified clock in the current scenario. If the arguments do not match a false path constraint in the current scenario, or if the specified ID does not refer to a false path constraint, this command fails.

Do not specify both the false path arguments and the constraint ID.

#### **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an Accessor command such as get\_pins or get\_ports.

#### **Examples**

The following example specifies all false paths to remove:

remove\_false\_path -through U0/U1:Y

The following example removes the false path constraint using its id:

```
set fpId [set_false_path -from [get_clocks c*] -through {topx/reg/*} -to [get_ports
out15] ]
remove_false_path -id $fpId
```

#### See Also

set\_false\_path Tcl Command Documentation Conventions Designer Tcl Command Reference



## remove\_generated\_clock

Tcl command; removes the specified generated clock constraint from the current scenario.

```
remove_generated_clock {-name clock_name | -id constraint_ID }
```

## **Arguments**

-name clock\_name

Specifies the name of the generated clock constraint to remove from the current scenario. You must specify either a clock name or an ID.

-id constraint\_ID

Specifies the ID of the generated clock constraint to remove from the current scenario. You must specify either an ID or a clock name that exists in the current scenario.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Description**

Removes the specified generated clock constraint from the current scenario. If the specified name does not match a generated clock constraint in the current scenario, or if the specified ID does not refer to a generated clock constraint, this command fails.

Do not specify both the name and the ID.

## **Exceptions**

You cannot use wildcards when specifying a generated clock name.

#### **Examples**

The following example removes the generated clock constraint named "my\_user\_clock": remove\_generated\_clock -name my\_user\_clock

#### See Also

create\_generated\_clock Tcl Command Documentation Conventions Designer Tcl Command Reference

## remove\_input\_delay

Tcl command; removes an input delay a clock on a port by specifying both the clocks and port names or the ID of the input\_delay constraint to remove.

```
remove_input_delay -clock clock_name port_pin_list
remove_input_delay -id constraint_ID
```

#### **Arguments**

#### -clock clock\_name

Specifies the clock name to which the specified input delay value is assigned. port\_pin\_list
Specifies the port names to which the specified input delay value is assigned.
-id constraint\_ID



Specifies the ID of the clock with the input\_delay value to remove from the current scenario. You must specify either both a clock name and list of port names or the input\_delay constraint ID.

### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### **Description**

Removes an input delay from the specified clocks and port in the current scenario. If the clocks and port names do not match an input delay constraint in the current scenario, or if the specified ID does not refer to an input delay constraint, this command fails.

Do not specify both the clock and port names and the constraint ID.

#### **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

#### **Examples**

The following example removes the input delay from CLK1 on port data1:

remove\_input\_delay -clock [get\_clocks CLK1] [get\_ports data1]

#### See Also

set\_input\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## remove\_max\_delay

Tcl command; removes a maximum delay constraint from the current timing scenario by specifying either its exact arguments or its ID.

```
remove_max_delay [-from from_list] [-to to_list] [-through through_list]
remove_max_delay -id constraint_ID
```

## Arguments

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass. -to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint\_ID

Specifies the ID of the maximum delay constraint to remove from the current scenario. You must specify either the exact maximum delay arguments to remove or the constraint ID that refers to the maximum delay constraint to remove.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



## **Description**

Removes a maximum delay value from the specified clock in the current scenario. If the arguments do not match a maximum delay constraint in the current scenario, or if the specified ID does not refer to a maximum delay constraint, this command fails.

Do not specify both the maximum delay arguments and the constraint ID.

### **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an Accessor command.

### **Examples**

The following example specifies a range of maximum delay constraints to remove: remove\_max\_delay -through U0/U1:Y

#### See Also

set\_max\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## remove\_min\_delay

Tcl command; removes a minimum delay constraint in the current timing scenario by specifying either its exact arguments or its ID.

```
remove_min_delay [-from from_list] [-to to_list] [-through through_list]
remove_min_delay -id constraint_ID
```

## **Arguments**

-from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

#### -to*to\_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint\_ID

Specifies the ID of the minimum delay constraint to remove from the current scenario. You must specify either the exact minimum delay arguments to remove or the constraint ID that refers to the minimum delay constraint to remove.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Description**

Removes a minimum delay value from the specified clock in the current scenario. If the arguments do not match a minimum delay constraint in the current scenario, or if the specified ID does not refer to a minimum delay constraint, this command fails.

Do not specify both the minimum delay arguments and the constraint ID.



## **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

### **Examples**

The following example specifies a range of minimum delay constraints to remove: remove\_min\_delay -through U0/U1:Y

#### See Also

set\_min\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## remove\_multicycle\_path

Tcl command; removes a multicycle path constraint in the current timing scenario by specifying either its exact arguments or its ID.

```
remove_multicycle_path [-from from_list] [-to to_list] [-through through_list]
remove multicycle_path -id constraint_ID
```

## Arguments

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to*to\_list* 

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint\_ID

Specifies the ID of the multicycle path constraint to remove from the current scenario. You must specify either the exact multicycle path arguments to remove or the constraint ID that refers to the multicycle path constraint to remove.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Description**

Removes a multicycle path from the specified clock in the current scenario. If the arguments do not match a multicycle path constraint in the current scenario, or if the specified ID does not refer to a multicycle path constraint, this command fails.

Do not specify both the multicycle path arguments and the constraint ID.

## **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

## **Examples**

The following example removes all paths between reg1 and reg2 to 3 cycles for setup check. remove\_multicycle\_path -from [get\_pins {reg1}] -to [get\_pins {reg2}]



#### See Also

set\_multicycle\_path <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

## remove\_output\_delay

Tcl command; removes an ouput delay by specifying both the clocks and port names or the ID of the output\_delay constraint to remove.

```
remove_output_delay -clock clock_name port_pin_list
remove_output_delay -id constraint_ID
```

## **Arguments**

-clock clock\_name

Specifies the clock name to which the specified output delay value is assigned.

port\_pin\_list

Specifies the port names to which the specified output delay value is assigned.

-id constraint\_ID

Specifies the ID of the clock with the output\_delay value to remove from the current scenario. You must specify either both a clock name and list of port names or the output\_delay constraint ID .

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Description**

Removes an output delay from the specified clocks and port in the current scenario. If the clocks and port names do not match an output delay constraint in the current scenario, or if the specified ID does not refer to an output delay constraint, this command fails.

Do not specify both the clock and port names and the constraint ID.

## **Exceptions**

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

## **Examples**

The following example removes the output delay from CLK1 on port out1:

remove\_output\_delay -clock [get\_clocks CLK1] [get\_ports out1]

#### See Also

set\_output\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference



## remove\_scenario

Tcl command; removes a scenario from the constraint database.

remove\_scenario <name>

### Arguments

name

Specifies the name of the scenario to delete.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### Example

The following command removes the scenario named my\_scenario: remove\_scenario my\_scenario

#### See Also

create\_scenario

## remove\_set

Tcl command; removes a set of paths from analysis. Only user-created sets can be deleted.

remove\_set -name name

## **Parameters**

-name *name* Specifies the name of the set to delete.

## **Example**

The following command removes the set named my\_set: remove\_set -name my\_set

#### See Also

create\_set

# rename\_scenario (SmartFusion2, IGLOO2, and RTG4)

Tcl command; renames an existing timing scenario to a new name. You must provide a unique name (that is, it cannot already be used by another timing scenario) for the new name.

rename\_scenario old\_name new\_name

#### **Arguments**

#### old\_name

Specifies the name of the existing timing scenario to be renamed.

new\_name

Specifies the new name for the scenario.



## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

### **Description**

This command renames an existing scenario name to a new name..

### **Example**

rename\_scenario my\_old\_scenario my\_new\_scenario

#### See Also

create\_scenario delete\_scenario Tcl documentation conventions Designer Tcl Command Reference

## save

Tcl command; saves all changes made prior to this command. This includes changes made on constraints, options and sets.

#### save

### **Arguments**

None

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Example

The following script sets the maximum number of paths reported by list\_paths to 10, reads an SDC file, and save both the option and the constraints into the design project:

```
set_options -limit_max_paths 10
read_sdc somefile.sdc
save
```

#### See Also

set\_options

## set\_clock\_latency

Tcl command; defines the delay between an external clock source and the definition pin of a clock within SmartTime.

```
set_clock_latency -source [-rise][-fall][-early][-late] delay clock
```

#### **Arguments**

-source Specifies the source latency on a clock pin, potentially only on certain edges of the clock. -rise



Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-fall

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

-late

Optional. Specifies that the latency is late bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

-early

Optional. Specifies that the latency is early bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

delay

Specifies the latency value for the constraint.

clock

Specifies the clock to which the constraint is applied. This clock must be constrained.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Description**

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint. You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

#### **Examples**

The following example sets an early clock source latency of 0.4 on the rising edge of main\_clock. It also sets a clock source latency of 1.2, for both the early and late values of the falling edge of main\_clock. The late value for the clock source latency for the falling edge of main\_clock remains undefined.

set\_clock\_latency -source -rise -early 0.4 { main\_clock }
set\_clock\_latency -source -fall 1.2 { main\_clock }

#### See Also

<u>create\_clock</u> <u>create\_generated\_clock</u> <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>



## set\_clock\_to\_output

SDC command; defines the timing budget available inside the FPGA for an output relative to a clock.

set\_clock\_to\_output delay\_value -clock clock\_ref [-max] [-min] output\_list

### Arguments

#### delay\_value

Specifies the clock to output delay in nanoseconds. This time represents the amount of time available inside the FPGA between the active clock edge and the data change at the output port.

-clock clock\_ref

Specifies the reference clock to which the specified clock to output is related. This is a mandatory argument.

-max

Specifies that *delay\_value* refers to the maximum clock to output at the specified output. If you do not specify -max or -min options, the tool assumes maximum and minimum clock to output delays to be equal.

-min

Specifies that *delay\_value* refers to the minimum clock to output at the specified output. If you do not specify -max or -min options, the tool assumes maximum and minimum clock to output delays to be equal.

#### output\_list

Provides a list of output ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## set\_clock\_uncertainty

Tcl command; specifies a clock-to-clock uncertainty between two clocks (from and to) and returns the ID of the created constraint if the command succeeded.

```
set_clock_uncertainty uncertainty -from | -rise_from | -fall_from from_clock_list -to | -
rise_to | -fall_to to_clock_list -setup {value} -hold {value}
```

#### Arguments

#### uncertainty

Specifies the time in nanoseconds that represents the amount of variation between two clock edges. -from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. Only one of the *-from*, *-rise\_from*, or *-fall\_from* arguments can be specified for the constraint to be valid.

-rise\_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. Only one of the -from, -rise\_from, or -fall\_from arguments can be specified for the constraint to be valid. -fall\_from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. Only one of the -from, -rise\_from, or -fall\_from arguments can be specified for the constraint to be valid.

#### from\_clock\_list

Specifies the list of clock names as the uncertainty source.

-to



Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. Only one of the -to, -rise\_to, or -fall\_to arguments can be specified for the constraint to be valid.

-rise\_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. Only one of the -to, -rise\_to, or -fall\_to arguments can be specified for the constraint to be valid. -fall to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. Only one of the -to,  $-rise_{to}$ , or  $-fall_{to}$  arguments can be specified for the constraint to be valid.

to\_clock\_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both <code>-setup</code> and <code>-hold</code> are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Description

The set\_clock\_uncertainty command sets the timing uncertainty between two clock waveforms or maximum clock skew. Timing between clocks have no uncertainty unless you specify it.

#### **Examples**

```
set_clock_uncertainty 10 -from Clk1 -to Clk2
set_clock_uncertainty 0 -from Clk1 -fall_to { Clk2 Clk3 } -setup
set_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
set_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3 Clk4 }
-setup
set_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
```

#### See Also

create\_clock
create\_generated\_clock
remove\_clock\_uncertainty
Designer Tcl Command Reference

## set\_current\_scenario

Tcl command; specifies the timing scenario for the Timing Analyzer to use. All commands that follow this command will apply to the specified timing scenario.

set\_current\_scenario name

#### Arguments

#### name

Specifies the name of the timing scenario to which to apply all commands from this point on.



## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

### **Description**

A timing scenario is a set of timing constraints used with a design. If the specified scenario is already the current one, this command has no effect.

After setting the current scenario, constraints can be listed, added, or removed, the checker can be invoked on the set of constraints, and so on.

This command uses the specified timing scenario to compute timing analysis.

## **Example**

set\_current\_scenario scenario\_A

#### See Also

get\_current\_scenario Tcl Command Documentation Conventions Designer Tcl Command Reference

## set\_disable\_timing

Tcl command; disables timing arcs within a cell and returns the ID of the created constraint if the command succeeded.

set\_disable\_timing -from value -to value name

## Arguments

-from from\_port

Specifies the starting port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

#### -to to\_port

Specifies the ending port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

name

Specifies the cell name where the timing arcs will be disabled.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Example

set\_disable\_timing -from A -to Y a2

#### See Also

Tcl documentation conventions Designer Tcl Command Reference



## set\_external\_check

SDC command; defines the external setup and hold delays for an input relative to a clock.

set\_external\_check delay\_value -clock clock\_ref [-setup] [-hold] [-clock\_fall] input\_list

## **Arguments**

#### delay\_value

Specifies the external setup or external hold delay in nanoseconds. This time represents the amount of time available inside the FPGA for the specified input after a clock edge.

-clock clock\_ref

Specifies the reference clock to which the specified external check is related. This is a mandatory argument.

-setup

Specifies that <u>delay\_value</u> refers to the setup check at the specified input. This is a mandatory argument if -hold is not used. You must specify either the -setup or -hold option.

-clock\_fall

Specifies that the delay is relative to the falling edge of the reference clock. The default is the rising edge. *input\_list* 

Provides a list of input ports in the current design to which *delay\_value* is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## set\_false\_path

Tcl command; identifies paths that are considered false and excluded from the timing analysis in the current timing scenario.

set\_false\_path [-from from\_list] [-through through\_list] [-to to\_list]

## **Arguments**

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Description**

The set\_false\_path command identifies specific timing paths as being false. The false timing paths are paths that do not propagate logic level changes. This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins, and the path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.



The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints. If more than one object is specified within one -through option, the path can pass through any objects.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

## Examples

The following example specifies all paths from clock pins of the registers in clock domain clk1 to data pins of a specific register in clock domain clk2 as false paths:

set\_false\_path -from [get\_clocks {clk1}] -to reg\_2:D

The following example specifies all paths through the pin U0/U1:Y to be false:

set\_false\_path -through U0/U1:Y

#### See Also

**Tcl Command Documentation Conventions Designer Tcl Command Reference** 

## set\_input\_delay

Tcl command; creates an input delay on a port list by defining the arrival time of an input relative to a clock in the current scenario.

set\_input\_delay delay\_value -clock clock\_ref [-max] [-min] [-clock\_fall] input\_list

## Arguments

#### delay\_value

Specifies the arrival time in nanoseconds that represents the amount of time for which the signal is available at the specified input after a clock edge.

-clock clock\_ref

Specifies the clock reference to which the specified input delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay\_value refers to the longest path arriving at the specified input. If you do not specify max or -min options, the tool assumes maximum and minimum input delays to be equal.

-min

Specifies that delay\_value refers to the shortest path arriving at the specified input. If you do not specify max or -min options, the tool assumes maximum and minimum input delays to be equal.

-clock\_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. input\_list

Provides a list of input ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.and IGLOOe, except ProASIC3 nano and ProASIC3L

## **Description**

The set input delay command sets input path delays on input ports relative to a clock edge. This usually represents a combinational path delay from the clock pin of a register external to the current design. For



in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds input delay to path delay for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be:

- a single port name used as source for a clock constraint
- a single pin name used as source for a clock constraint; for instance reg1:CLK. This name can be hierarchical (for instance toplevel/block1/reg2:CLK)
- an object accessor that will refer to one clock: [get\_clocks {clk}]

## **Examples**

The following example sets an input delay of 1.2ns for port data1 relative to the rising edge of CLK1: set\_input\_delay 1.2 -clock [get\_clocks CLK1] [get\_ports data1]

The following example sets a different maximum and minimum input delay for port IN1 relative to the falling edge of CLK2:

```
set_input_delay 1.0 -clock_fall -clock CLK2 -min {IN1}
set_input_delay 1.4 -clock_fall -clock CLK2 -max {IN1}
```

#### See Also

set\_output\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## set\_max\_delay

Tcl command; specifies the maximum delay for the timing paths in the current scenario.

set\_max\_delay delay\_value [-from from\_list] [-to to\_list] [-through through\_list]

## Arguments

#### delay\_value

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

#### -to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

#### -through through\_list

Specifies a list of pins, ports, cells, or nets through which the timing paths must pass.



## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## Description

This command specifies the required maximum delay for timing paths in the current design. The path length for any startpoint in from\_list to any endpoint in to\_list must be less than delay\_value.

The timing engine automatically derives the individual maximum delay targets from clock waveforms and port input or output delays.

The maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

## **Examples**

The following example sets a maximum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set\_max\_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}

The following example sets a maximum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set\_max\_delay 3.8 -to [get\_ports out\*]

## See Also

set\_min\_delay remove\_max\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## set\_min\_delay

Tcl command; specifies the minimum delay for the timing paths in the current scenario.

set\_min\_delay delay\_value [-from from\_list] [-to to\_list] [-through through\_list]

## **Arguments**

#### delay\_value

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

#### -to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-through through\_list



Specifies a list of pins, ports, cells, or nets through which the timing paths must pass.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Description**

This command specifies the required minimum delay for timing paths in the current design. The path length for any startpoint in from\_list to any endpoint in to\_list must be less than delay\_value.

The timing engine automatically derives the individual minimum delay targets from clock waveforms and port input or output delays.

The minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

## **Examples**

The following example sets a minimum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set\_min\_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}

The following example sets a minimum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set\_min\_delay 3.8 -to [get\_ports out\*]

#### See Also

set\_max\_delay remove\_min\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## set\_multicycle\_path

Tcl command; defines a path that takes multiple clock cycles in the current scenario.

```
set_multicycle_path ncycles [-setup] [-hold] [-from from_list[-through through_list[-to
to_list
```

## **Arguments**

#### ncycles

Specifies an integer value that represents a number of cycles the data path must have for setup or hold check. The value is relative to the starting point or ending point clock, before data is required at the ending point.

-setup

Optional. Applies the cycle value for the setup check only. This option does not affect the hold check. The default hold check will be applied unless you have specified another set\_multicycle\_path command for the hold value.

-hold

Optional. Applies the cycle value for the hold check only. This option does not affect the setup check.

Note: If you do not specify "-setup" or "-hold", the cycle value is applied to the setup check and the default hold check is performed (*ncycles* -1).

-from from\_list



Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins or ports through which the multiple cycle paths must pass.

-to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## Description

Setting multiple cycle paths constraint overrides the single cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks. If you change the multiplier, it affects both the setup and hold checks.

False path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

If you specify more than one object within one -through option, the path passes through any of the objects.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

## **Exceptions**

Multiple priority management is not supported in Microsemi SoC designs. All multiple cycle path constraints are handled with the same priority.

## **Examples**

The following example sets all paths between reg1 and reg2 to 3 cycles for setup check. Hold check is measured at the previous edge of the clock at reg2.

set\_multicycle\_path 3 -from [get\_pins {reg1}] -to [get\_pins {reg2}]

The following example specifies that four cycles are needed for setup check on all paths starting at the registers in the clock domain ck1. Hold check is further specified with two cycles instead of the three cycles that would have been applied otherwise.

set\_multicycle\_path 4 -setup -from [get\_clocks {ckl}]
set\_multicycle\_path 2 -hold -from [get\_clocks {ckl}]

#### See Also

remove\_multicycle\_path Tcl Command Documentation Conventions Designer Tcl Command Reference

## set\_options (SmartFusion2, IGLOO2, RTG4)

SmartTime-specific Tcl command; sets options for timing analysis. Some options will also affect timingdriven place-and-route. The same parameters can be changed in the SmartTime Options dialog box in the SmartTime GUI.

```
set_options
```

```
[-max_opcond value ]
[-min_opcond value]
[-interclockdomain_analysis value]
[-use_bibuf_loopbacks value]
```



[-enable\_recovery\_removal\_checks value] [-break\_at\_async value] [-filter\_when\_slack\_below value] [-filter\_when\_slack\_above value] [-remove\_slack\_filters] [-limit\_max\_paths value] [-expand\_clock\_network value] [-expand\_parallel\_paths value] [-analysis\_scenario value] [-tdpr\_scenario value] [-reset]

## Arguments

#### -max\_opcond value

Sets the operating condition to use for Maximum Delay Analysis. The following table shows the acceptable values for this argument. Default is *worst*.

Value	Description	
worst	Use Worst Case conditions for Maximum Delay Analysis	
typical	Use Typical conditions for Maximum Delay Analysis	
best	Use Best Case conditions for Maximum Delay Analysis	

#### -min\_opcond value

Sets the operating condition to use for Minimum Delay Analysis. The following table shows the acceptable values for this argument. Default is *best*.

Value	Description	
best	Use Best Case conditions for Minimum Delay Analysis	
typical	Use Typical conditions for Minimum Delay Analysis	
worst	Use Worst Case conditions for Minimum Delay Analysis	

-interclockdomain\_analysis value

Enables or disables inter-clock domain analysis. Default is yes.

Value	Description	
yes	Enables inter-clock domain analysis	
no	Disables inter-clock domain analysis	

-use\_bibuf\_loopbacks value

Instructs the timing analysis whether to consider loopback path in bidirectional buffers (D->Y, E->Y)as false-path {no}. Default is *yes*; i.e., loopback are false paths.

Value	Description	
yes	Enables loopback in bibufs	



Value	Description	
no Disables loopback in bibufs		

-enable\_recovery\_removal\_checks value

Enables recovery checks to be included in max-delay analysis and removal checks in min-delay analysis. Default is *yes*.

Value	Description	
yes	Enables recovery and removal checks	
no	Disables recovery and removal checks	

#### -break\_at\_async value

Specifies whether or not timing analysis is allowed to cross asynchronous pins (clear, reset of sequential elements). Default is *no*.

Value	Description	
yes	Enables breaking paths at asynchronous ports	
no	Disables breaking paths at asynchronous ports	

-filter\_when\_slack\_below value

Specifies a minimum slack value for paths reported by list\_paths. Not set by default. -filter\_when\_slack\_above value

Specifies a maximum slack value for paths reported by list\_paths. Not set by default. -remove\_slack\_filters

Removes the slack minimum and maximum set using -filter\_when\_slack\_below and filter\_when\_slack\_above.

-limit\_max\_paths value

Specifies the maximum number of paths reported by list\_paths. Default is 100. -expand\_clock\_network value

Specify whether or not clock network details are reported in expand\_path. Default is yes.

Value	Description	
yes	Enables expanded clock network information in paths	
no	Disables expanded clock network information in paths	

-expand\_parallel\_paths value

Specify the number of parallel paths {paths with the same ends} to include in expand\_path. Default is 1. -analysis\_scenario value

Specify the constraint scenario to be used for timing analysis. Default is *Primary*, the default scenario. -tdpr\_scenario value

Specify the constraint scenario to be used for timing-driven place-and-route. Default is Primary, the default scenario.



#### -reset

Reset all options to the default values, except those for analysis and TDPR scenarios, which remain unchanged.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

The following script commands the timing engine to use best operating conditions for both max-delay analysis and min-delay analysis:

set\_options -max\_opcond {best} -min\_opcond {best}

The following script changes the scenario used by timing-driven place-and-route and saves the change in the Libero project for place-and-route tools to see the change.

```
set_options -tdpr_scenario {My_TDPR_Scenario}
```

#### See Also

save

## set\_output\_delay

Tcl command; defines the output delay of an output relative to a clock in the current scenario.

set\_output\_delay [-max] [-min] delay\_value -clock clock\_ref [-clock\_fall] output\_list

## **Arguments**

#### -max

Specifies that delay\_value refers to the longest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

#### -min

Specifies that delay\_value refers to the shortest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

#### delay\_value

Specifies the amount of time before a clock edge for which the signal is required. This represents a combinational path delay to a register outside the current design plus the library setup time (for maximum output delay) or hold time (for minimum output delay).

### -clock clock\_ref

Specifies the clock reference to which the specified output delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-clock\_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge.

#### output\_list

Provides a list of output ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



## **Description**

The set\_output\_delay command sets output path delays on output ports relative to a clock edge. Output ports have no output delay unless you specify it. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds output delay to path delay for paths ending at primary outputs.

## **Examples**

The following example sets an output delay of 1.2ns for port OUT1 relative to the rising edge of CLK1:

set\_output\_delay 1.2 -clock [get\_clocks CLK1] [get\_ports OUT1]

The following example sets a different maximum and minimum output delay for port OUT1 relative to the falling edge of CLK2:

set\_output\_delay -min {OUT1} 1.0 -clock\_fall -clock CLK2
set\_output\_delay -max {OUT1} 1.4 -clock\_fall -clock CLK2

#### See Also

remove\_output\_delay set\_input\_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

## write\_sdc

Tcl command; writes timing constraints into an SDC file. If multiple constraint scenarios are defined, - scenario allows the user to specify which scenario to write. By default, the current scenario is written.

```
write_sdc
-scenario scenario name
-pin_separator (: | /)
file name
```

## **Arguments**

-scenario scenario name Specify the scenario to write. By default the current scenario is used. -pin\_separator sep Specify the pin separator used in the SDC file. It can be either ':' or '/'. file name Specify the SDC file name.

## **Example**

The following script merges two SDC files and writes the result into a third SDC file: read\_sdc first.sdc read\_sdc -add second.sdc write\_sdc merged.sdc

## See Also

read\_sdc, set\_current\_scenario VERIFYTIMING (SmartFusion2, IGLOO2, RTG4, )



# **Constraints by File Format - SDC Command Reference**

## About Synopsys Design Constraints (SDC) Files

Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi tools use a subset of the SDC format to capture supported timing constraints. Any timing constraint that you can enter using Designer tools can also be specified in an SDC file.

Use the SDC-based flow to share timing constraint information between Microsemi tools and third-party EDA tools.

Command	Action
create_clock	Creates a clock and defines its characteristics
create_generated_clock	Creates an internally generated clock and defines its characteristics
remove_clock_uncertainty	Removes a clock-to-clock uncertainty from the current timing scenario.
set_clock_latency	Defines the delay between an external clock source and the definition pin of a clock within SmartTime
<u>set_clock_uncertainty</u>	Defines the timing uncertainty between two clock waveforms or maximum skew
set_false_path	Identifies paths that are to be considered false and excluded from the timing analysis
set input delay	Defines the arrival time of an input relative to a clock
set_load	Sets the load to a specified value on a specified port
<u>set max delay</u>	Specifies the maximum delay for the timing paths
<u>set min delay</u>	Specifies the minimum delay for the timing paths
set_multicycle_path	Defines a path that takes multiple clock cycles
<u>set_output_delay</u>	Defines the output delay of an output relative to a clock

#### See Also

Constraint Entry SDC Syntax Conventions Importing Constraint Files



## SDC Syntax Conventions

The following table shows the typographical conventions that are used for the SDC command syntax.

Syntax Notation	Description
command - argument	Commands and arguments appear in Courier New typeface.
variable	Variables appear in blue, italic <i>Courier New</i> typeface. You must substitute an appropriate value for the variable.
[-argument value]	Optional arguments begin and end with a square bracket.

Note: SDC commands and arguments are case sensitive.

## Example

The following example shows syntax for the create\_clock command and a sample command:

create\_clock -period period\_value [-waveform edge\_list] source

create\_clock -period 7 -waveform {2 4}{CLK1}

## **Wildcard Characters**

You can use the following wildcard characters in names used in the SDC commands:

Wildcard	What it does	
١	Interprets the next character literally	
*	Matches any string	

Note: The matching function requires that you add a backslash (\) before each slash in the pin names in case the slash does not denote the hierarchy in your design.

## **Special Characters** ([], { }, and \)

Square brackets ([]) are part of the command syntax to access ports, pins and clocks. In cases where these netlist objects names themselves contain square brackets (for example, buses), you must either enclose the names with curly brackets ({}) or precede the open and closed square brackets ([]) characters with a backslash (\). If you do not do this, the tool displays an error message.

For example:

```
create_clock -period 3 clk\[0\]
```

set\_max\_delay 1.5 -from [get\_pins ff1\[5\]:CLK] -to [get\_clocks {clk[0]}]

Although not necessary, Microsemi recommends the use of curly brackets around the names, as shown in the following example:

set\_false\_path -from {data1} -to [get\_pins {reg1:D}]

In any case, the use of the curly bracket is mandatory when you have to provide more than one name. For example:

```
set_false_path -from {data3 data4} -to [get_pins {reg2:D reg5:D}]
```



## **Entering Arguments on Separate Lines**

If a command needs to be split on multiple lines, each line except the last must end with a backslash (\) character as shown in the following example:

```
set_multicycle_path 2 -from \
[get_pins {reg1*}] \
-to {reg2:D}
```

## See Also

About SDC Files



# **Referenced Topics**

## create\_clock

SDC command; creates a clock and defines its characteristics.

create\_clock -name name -period period\_value [-waveform edge\_list] source

## Arguments

#### -name *name*

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

-period *period\_value* 

Specifies the clock period in nanoseconds. The value you specify is the minimum time over which the clock waveform repeats. The period\_value must be greater than zero.

#### -waveform edge\_list

Specifies the rise and fall times of the clock waveform in ns over a complete clock period. There must be exactly two transitions in the list, a rising transition followed by a falling transition. You can define a clock starting with a falling edge by providing an edge list where fall time is less than rise time. If you do not specify -waveform option, the tool creates a default waveform, with a rising edge at instant 0.0 ns and ©a falling edge at instant (period\_value/2)ns.

#### source

Specifies the source of the clock constraint. The source can be ports or pins in the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing one. Only one source is accepted. Wildcards are accepted as long as the resolution shows one port or pin.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## Description

Creates a clock in the current design at the declared source and defines its period and waveform. The static timing analysis tool uses this information to propagate the waveform across the clock network to the clock pins of all sequential elements driven by this clock source.

The clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

## Exceptions

None

## Examples

The following example creates two clocks on ports CK1 and CK2 with a period of 6, a rising edge at 0, and a falling edge at 3:

create\_clock -name {my\_user\_clock} -period 6 CK1
create\_clock -name {my\_other\_user\_clock} -period 6 -waveform {0 3} {CK2}
The following example creates a clock on port CK3 with a period of 7, a rising edge at 2, and a falling
edge at 4:

```
create_clock -period 7 -waveform {2 4} [get_ports {CK3}]
```



## **Microsemi Implementation Specifics**

- The -waveform in SDC accepts waveforms with multiple edges within a period. In Microsemi design implementation, only two waveforms are accepted.
- SDC accepts defining a clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The source argument in SDC create\_clock command is optional. This is in conjunction with the -name argument in SDC to support the concept of virtual clocks. In Microsemi implementation, source is a mandatory argument as -name and virtual clocks concept is not supported.
- The -domain argument in the SDC create\_clock command is not supported.

### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Clock Definition Create Clock Create a New Clock Constraint

## create\_generated\_clock

SDC command; creates an internally generated clock and defines its characteristics.

```
create_generated_clock -name {name -source reference_pin [-divide_by divide_factor] [-
multiply_by multiply_factor] [-invert] source -pll_output pll_feedback_clock -pll_feedback
pll_feedback_input
```

## Arguments

#### -name name

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

-source reference\_pin

Specifies the reference pin in the design from which the clock waveform is to be derived.

#### -divide\_bydivide\_factor

Specifies the frequency division factor. For instance if the *divide\_factor* is equal to 2, the generated clock period is twice the reference clock period.

#### -multiply\_by multiply\_factor

Specifies the frequency multiplication factor. For instance if the *multiply\_factor* is equal to 2, the generated clock period is half the reference clock period.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

source

Specifies the source of the clock constraint on internal pins of the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing clock. Only one source is accepted. Wildcards are accepted as long as the resolution shows one pin.

-pll\_output pll\_feedback\_clock

Specifies the output pin of the PLL which is used as the external feedback clock. This pin must drive the feedback input pin of the PLL specified using the -pll\_feedback option. The PLL will align the rising edge of the reference input clock to the feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

-pll\_feedback pll\_feedback\_input



Specifies the feedback input pin of the PLL. This pin must be driven by the output pin of the PLL specified using the -pll\_output option. The PLL will align the rising edge of the reference input clock to the external feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

Creates a generated clock in the current design at a declared source by defining its frequency with respect to the frequency at the reference pin. The static timing analysis tool uses this information to compute and propagate its waveform across the clock network to the clock pins of all sequential elements driven by this source.

The generated clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

## **Examples**

The following example creates a generated clock on pin U1/reg1:Q with a period twice as long as the period at the reference port CLK.

create\_generated\_clock -name {my\_user\_clock} -divide\_by 2 -source [get\_ports {CLK}]
U1/reg1/Q

The following example creates a generated clock at the primary output of myPLL with a period <sup>3</sup>/<sub>4</sub> of the period at the reference pin clk.

create\_generated\_clock -divide\_by 3 -multiply\_by 4 -source clk [get\_pins {myPLL/CLK1}]

The following example creates a generated clock named system\_clk on the GL2 output pin of FCCC\_0 with a period equal to half the period of the source clock. The constraint also identifies GL2 output pin as the external feedback clock source and CLK2 as the feedback input pin for FCCC\_0.

```
create_generated_clock -name { system_clk } \
-multiply_by 2 \
-source { FCCC_0/CCC_INST/CLK3_PAD } \
-pll_output { FCCC_0/CCC_INST/GL2 } \
{ FCCC_0/CCC_INST/CLK2 } \
```

## **Microsemi Implementation Specifics**

- SDC accepts either –multiply\_by or –divide\_by option. In Microsemi design implementation, both are
  accepted to accurately model the PLL behavior.
- SDC accepts defining a generated clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The -duty\_cycle ,-edges and -edge\_shift options in the SDC create\_generated\_clock command are not supported in Microsemi design implementation.

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Create Generated Clock Constraint (SDC)

## remove\_clock\_uncertainty

SDC command; Removes a clock-to-clock uncertainty from the current timing scenario.



```
remove_clock_uncertainty -from | -rise_from | -fall_from from_clock_list -to | -rise_to| -
fall_to to_clock_list -setup {value} -hold {value}
remove_clock_uncertainty -id constraint_ID
```

## **Arguments**

#### -from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. You can specify only one of the *-from*, *-rise\_from*, or *-fall\_from* arguments for the constraint to be valid.

```
-rise_from
```

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. You can specify only one of the *-from*, *-rise\_from*, or *-fall\_from* arguments for the constraint to be valid. *-fall\_from* 

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. You can specify only one of the <code>-from</code>, <code>-rise\_from</code>, or <code>-fall\_from</code> arguments for the constraint to be valid.

#### from\_clock\_list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. You can specify only one of the -to, -rise\_to, or -fall\_to arguments for the constraint to be valid.

-rise\_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. You can specify only one of the -to,  $-rise_to$ , or  $-fall_to$  arguments for the constraint to be valid.

#### -fall\_to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. You can specify only one of the -to,  $-rise_to$ , or  $-fall_to$  arguments for the constraint to be valid.

#### to\_clock\_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-id constraint\_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either the exact parameters to set the constraint or its constraint ID.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## Description

Removes a clock-to-clock uncertainty from the specified clock in the current scenario. If the specified arguments do not match clocks with an uncertainty constraint in the current scenario, or if the specified ID does not refer to a clock-to-clock uncertainty constraint, this command fails.

Do not specify both the exact arguments and the ID.

## **Exceptions**

None



## **Examples**

```
remove_clock_uncertainty -from Clk1 -to Clk2
remove_clock_uncertainty -from Clk1 -fall_to { Clk2 Clk3 } -setup
remove_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
remove_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3
Clk4 } -setup
remove_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
remove_clock_uncertainty -id $clockId
```

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions set\_clock\_uncertainty

## set\_clock\_latency

SDC command; defines the delay between an external clock source and the definition pin of a clock within SmartTime.

set\_clock\_latency -source [-rise][-fall][-early][-late] delay clock

## Arguments

#### -source

Specifies a clock source latency on a clock pin.

-rise

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-fall

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

```
-invert
```

Specifies that the generated clock waveform is inverted with respect to the reference clock.

-late

Optional. Specifies that the latency is late bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

#### -early

Optional. Specifies that the latency is early bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

delay

Specifies the latency value for the constraint.

#### clock

Specifies the clock to which the constraint is applied. This clock must be constrained.



## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint. You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

## **Exceptions**

None

## **Examples**

The following example sets an early clock source latency of 0.4 on the rising edge of main\_clock. It also sets a clock source latency of 1.2, for both the early and late values of the falling edge of main\_clock. The late value for the clock source latency for the falling edge of main\_clock remains undefined.

set\_clock\_latency -source -rise -early 0.4 { main\_clock }
set\_clock\_latency -source -fall 1.2 { main\_clock }

## **Microsemi Implementation Specifics**

SDC accepts a list of clocks to -set\_clock\_latency. In Microsemi design implementation, only one clock pin can have its source latency specified per command.

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## set\_clock\_to\_output

SDC command; defines the timing budget available inside the FPGA for an output relative to a clock.

```
set_clock_to_output delay_value -clock clock_ref [-max] [-min] [-clock_fall] output_list
```

## Arguments

#### delay\_value

Specifies the clock to output delay in nanoseconds. This time represents the amount of time available inside the FPGA between the active clock edge and the data change at the output port.

#### -clock clock\_ref

Specifies the reference clock to which the specified clock to output is related. This is a mandatory argument.

-max

Specifies that delay\_value refers to the maximum clock to output at the specified output. If you do not specify –max or –min options, the tool assumes maximum and minimum clock to output delays to be equal.

-min



Specifies that delay\_value refers to the minimum clock to output at the specified output. If you do not specify -max or -min options, the tool assumes maximum and minimum clock to output delays to be equal.

-clock\_fall

Specifies that the delay is relative to the falling edge of the reference clock. The default is the rising edge. output\_list

Provides a list of output ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

The set\_clock\_to\_output command specifies the clock to output maximum and minimum delays on output ports relative to a clock edge. This usually represents a combinational path delay from a register internal to the current design to the output port. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool uses clock to output delays for paths ending at primary outputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be an object accessor that will refer to one clock. For example:

```
[get_clocks {system_clk}]
[get_clocks {sys*_clk}]
```

## **Examples**

The following example sets a maximum clock to output delay of 12 ns and a minimum clock to output delay of 6 ns for port data\_out relative to the rising edge of CLK1:

set\_clock\_to\_output 12 -clock [get\_clocks CLK1] -max [get\_ports data\_out]
set\_clock to\_output 6 -clock [get\_clocks CLK1] -min [get\_ports data\_out]

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## set\_clock\_uncertainty

SDC command; defines the timing uncertainty between two clock waveforms or maximum skew.

```
set_clock_uncertainty uncertainty (-from | -rise_from | -fall_from) from_clock_list (-to | -
rise_to | -fall_to) to_clock_list [-setup | -hold]
```

### Arguments

#### uncertainty

Specifies the time in nanoseconds that represents the amount of variation between two clock edges. The value must be a positive floating point number.

-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. You can specify only one of the -from, -rise\_from, or -fall\_from arguments for the constraint to be valid. This option is the default.

#### -rise\_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. You can specify only one of the *-from*, *-rise\_from*, or *-fall\_from* arguments for the constraint to be valid.



#### -fall\_from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. You can specify only one of the -from,  $-rise\_from$ , or  $-fall\_from$  arguments for the constraint to be valid.

from\_clock\_list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. You can specify only one of the -to, -rise\_to, or -fall\_to arguments for the constraint to be valid.

-rise\_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. You can specify only one of the -to, -rise\_to, or -fall\_to arguments for the constraint to be valid. -fall to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. You can specify only one of the -to,  $-rise_to$ , or  $-fall_to$  arguments for the constraint to be valid.

## to\_clock\_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If you do not specify either option (-setup or -hold) or if you specify both options, the uncertainty applies to both setup and hold checks.

Specifies that the uncertainty applies only to hold checks. If you do not specify either option (-setup or - hold) or if you specify both options, the uncertainty applies to both setup and hold checks.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

Clock uncertainty defines the timing between an two clock waveforms or maximum clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.

## **Exceptions**

None

## **Examples**

The following example defines two clocks and sets the uncertainty constraints, which analyzes the interclock domain between clk1 and clk2.

create\_clock -period 10 clk1 create\_generated\_clock -name clk2 -source clk1 -multiply\_by 2 sclk1 set\_clock\_uncertainty 0.4 -rise\_from clk1 -rise\_to clk2

## **Microsemi Implementation Specifics**

• SDC accepts a list of clocks to -set\_clock\_uncertainty.



## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions create\_clock (SDC) create\_generated\_clock (SDC) remove\_clock\_uncertainty

## set\_disable\_timing

SDC command; disables timing arcs within the specified cell and returns the ID of the created constraint if the command succeeded.

set\_disable\_timing [-from from\_port] [-to to\_port] cell\_name

## Arguments

-from from\_port

Specifies the starting port.

-to to\_port

Specifies the ending port.

#### cell\_name

Specifies the name of the cell in which timing arcs will be disabled.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

This command disables the timing arcs in the specified cell, and returns the ID of the created constraint if the command succeeded. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

## **Examples**

The following example disables the arc between a2:A and a2:Y.

set\_disable\_timing -from port1 -to port2 cellname

This command ensures that the arc is disabled within a cell instead of between cells.

## **Microsemi Implementation Specifics**

None

See Also Constraint Support by Family Constraint Entry Table SDC Syntax Conventions



## set\_external\_check

SDC command; defines the external setup and hold delays for an input relative to a clock.

set\_external\_check delay\_value -clock clock\_ref [-setup] [-hold] [-clock\_fall] input\_list

## Arguments

#### delay\_value

Specifies the external setup or external hold delay in nanoseconds. This time represents the amount of time available inside the FPGA for the specified input after a clock edge.

-clock clock\_ref

Specifies the reference clock to which the specified external check is related. This is a mandatory argument.

-setup

Specifies that delay\_value refers to the setup check at the specified input. This is a mandatory argument if -hold is not used. You must specify either -setup or -hold option.

-clock\_fall

Specifies that the delay is relative to the falling edge of the reference clock. The default is the rising edge. *input\_list* 

Provides a list of input ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

#### **Description**

The set\_external\_check command specifies the external setup and hold times on input ports relative to a clock edge. This usually represents a combinational path delay from the input port to the clock pin of a register internal to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool uses external setup and external hold times for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be an object accessor that will refer to one clock. For example:

```
[get_clocks {system_clk}]
[get_clocks {sys*_clk}]
```

## **Examples**

The following example sets an external setup check of 12 ns and an external hold check of 6 ns for port data\_in relative to the rising edge of CLK1:

```
set_external_check 12 -clock [get_clocks CLK1] -setup [get_ports data_in]
set_external_check 6 -clock [get_clocks CLK1] -hold [get_ports data_in]
```

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions



## set\_false\_path

SDC command; identifies paths that are considered false and excluded from the timing analysis.

set\_false\_path [-from from\_list] [-through through\_list] [-to to\_list]

## Arguments

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through\_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

The set\_false\_path command identifies specific timing paths as being false. The false timing paths are paths that do not propagate logic level changes. This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins, and the path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints. If more than one object is specified within one -through option, the path can pass through any objects.

## **Examples**

The following example specifies all paths from clock pins of the registers in clock domain clk1 to data pins of a specific register in clock domain clk2 as false paths:

set\_false\_path -from [get\_clocks {clk1}] -to reg\_2:D

The following example specifies all paths through the pin U0/U1:Y to be false: set\_false\_path -through U0/U1:Y

## **Microsemi Implementation Specifics**

SDC accepts multiple -through options in a single constraint to specify paths that traverse multiple points in the design. In Microsemi design implementation, only one -through option is accepted.

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set False Path Constraint



## set\_input\_delay

SDC command; defines the arrival time of an input relative to a clock.

set\_input\_delay delay\_value -clock clock\_ref [-max] [-min] [-clock\_fall] input\_list

## Arguments

delay\_value

Specifies the arrival time in nanoseconds that represents the amount of time for which the signal is available at the specified input after a clock edge.

-clock clock\_ref

Specifies the clock reference to which the specified input delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay\_value refers to the longest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-min

Specifies that delay\_value refers to the shortest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-clock\_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. input\_list

Provides a list of input ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion and IGLOOe, except ProASIC3 nano and ProASIC3L

## **Description**

The set\_input\_delay command sets input path delays on input ports relative to a clock edge. This usually represents a combinational path delay from the clock pin of a register external to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds input delay to path delay for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be:

- a single port name used as source for a clock constraint
- a single pin name used as source for a clock constraint; for instance reg1:CLK. This name can be hierarchical (for instance toplevel/block1/reg2:CLK)
- an object accessor that will refer to one clock: [get\_clocks {clk}]

## **Examples**

The following example sets an input delay of 1.2ns for port data1 relative to the rising edge of CLK1: set\_input\_delay 1.2 -clock [get\_clocks CLK1] [get\_ports data1]
The following example sets a different maximum and minimum input delay for port IN1 relative to the falling edge of CLK2:

```
set_input_delay 1.0 -clock_fall -clock CLK2 -min {IN1}
set_input_delay 1.4 -clock_fall -clock CLK2 -max {IN1}
```



## **Microsemi Implementation Specifics**

In SDC, the -clock is an optional argument that allows you to set input delay for combinational designs. Microsemi Implementation currently requires this argument.

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Input Delay

## set\_load

SDC command; sets the load to a specified value on a specified port.

set\_load capacitance port\_list

## Arguments

capacitance
Specifies the capacitance value that must be set on the specified ports.
port\_list
Specifies a list of ports in the current design on which the capacitance is to be set.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

The load constraint enables the Designer software to account for external capacitance at a specified port. You cannot set load constraint on the nets. When you specify this constraint on the output ports, it impacts the delay calculation on the specified ports.

## **Examples**

The following examples show how to set output capacitance on different output ports:

set\_load 35 out\_p
set\_load 40 {01 02}
set\_load 25 [get\_ports out]

## **Microsemi Implementation Specifics**

 In SDC, you can use the set\_load command to specify capacitance value on nets. Microsemi Implementation only supports output ports.

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Load on Port



## set\_max\_delay (SDC)

SDC command; specifies the maximum delay for the timing paths.

```
set_max_delay delay_value [-from from_list] [-to to_list]
```

## Arguments

#### delay\_value

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

## -to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

This command specifies the required maximum delay for timing paths in the current design. The path length for any startpoint in from\_list to any endpoint in to\_list must be less than delay\_value.

The tool automatically derives the individual maximum delay targets from clock waveforms and port input or output delays. For more information, refer to the <u>create clock</u>, <u>set input delay</u>, and <u>set output delay</u> commands.

The maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

## **Examples**

The following example sets a maximum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set\_max\_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}

The following example sets a maximum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set\_max\_delay 3.8 -to [get\_ports out\*]

## **Microsemi Implementation Specifics**

The -through option in the set\_max\_delay SDC command is not supported.

#### See Also

Constraint Support by Family



Constraint Entry Table SDC Syntax Conventions Set Max Delay

## set\_min\_delay

SDC command; specifies the minimum delay for the timing paths.

```
set_min_delay delay_value [-from from_list] [-to to_list]
```

## Arguments

#### delay\_value

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-to to\_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## Description

This command specifies the required minimum delay for timing paths in the current design. The path length for any startpoint in from\_list to any endpoint in to\_list must be less than delay\_value. The tool automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. For more information, refer to the <u>create\_clock</u>, <u>set\_input\_delay</u>, and <u>set\_output\_delay</u> commands.

The minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

## **Examples**

The following example sets a minimum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

```
set_min_delay 5 -from {ff1a:CLK ff1b:CLK} -to {ff2e:D}
```

The following example sets a minimum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

```
set_min_delay 3.8 -to [get_ports out*]
```



## **Microsemi Implementation Specifics**

The -through option in the set\_min\_delay SDC command is not supported.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

## set\_multicycle\_path

SDC command; defines a path that takes multiple clock cycles.

set\_multicycle\_path ncycles [-setup] [-hold] [-from from\_list] [-through through\_list] [-to
to\_list]

## Arguments

#### ncycles

Specifies an integer value that represents a number of cycles the data path must have for setup or hold check. The value is relative to the starting point or ending point clock, before data is required at the ending point.

-setup

Optional. Applies the cycle value for the setup check only. This option does not affect the hold check. The default hold check will be applied unless you have specified another set\_multicycle\_path command for the hold value.

-hold

Optional. Applies the cycle value for the hold check only. This option does not affect the setup check.

Note: If you do not specify "-setup" or "-hold", the cycle value is applied to the setup check and the default hold check is performed (*ncycles* -1).

#### -from from\_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

### -through through\_list

Specifies a list of pins or ports through which the multiple cycle paths must pass.

#### -to *to\_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Description**

Setting multiple cycle paths constraint overrides the single cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks. If you change the multiplier, it affects both the setup and hold checks.

False path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

If you specify more than one object within one -through option, the path passes through any of the objects.



## Examples

The following example sets all paths between reg1 and reg2 to 3 cycles for setup check. Hold check is measured at the previous edge of the clock at reg2.

set\_multicycle\_path 3 -from [get\_pins {reg1}] -to [get\_pins {reg2}]

The following example specifies that four cycles are needed for setup check on all paths starting at the registers in the clock domain ck1. Hold check is further specified with two cycles instead of the three cycles that would have been applied otherwise.

set\_multicycle\_path 4 -setup -from [get\_clocks {ckl}]
set\_multicycle\_path 2 -hold -from [get\_clocks {ckl}]

## **Microsemi Implementation Specifics**

SDC allows multiple priority management on the multiple cycle path constraint depending on the scope
of the object accessors. In Microsemi design implementation, such priority management is not
supported. All multiple cycle path constraints are handled with the same priority.

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Multicycle Path

## set\_output\_delay

SDC command; defines the output delay of an output relative to a clock.

set\_output\_delay delay\_value -clock clock\_ref [-max] [-min] [-clock\_fall] output\_list

## Arguments

delay\_value

Specifies the amount of time before a clock edge for which the signal is required. This represents a combinational path delay to a register outside the current design plus the library setup time (for maximum output delay) or hold time (for minimum output delay).

-clock clock\_ref

Specifies the clock reference to which the specified output delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay\_value refers to the longest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

-min

Specifies that delay\_value refers to the shortest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

-clock\_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. output\_list

Provides a list of output ports in the current design to which delay\_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion



## Description

The set\_output\_delay command sets output path delays on output ports relative to a clock edge. Output ports have no output delay unless you specify it. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds output delay to path delay for paths ending at primary outputs.

## **Examples**

The following example sets an output delay of 1.2ns for port OUT1 relative to the rising edge of CLK1:

set\_output\_delay 1.2 -clock [get\_clocks CLK1] [get\_ports OUT1]

The following example sets a different maximum and minimum output delay for port OUT1 relative to the falling edge of CLK2:

set\_output\_delay 1.0 -clock\_fall -clock CLK2 -min {OUT1}
set\_output\_delay 1.4 -clock\_fall -clock CLK2 -max {OUT1}

## **Microsemi Implementation Specifics**

• In SDC, the -clock is an optional argument that allows you to set the output delay for combinational designs. Microsemi Implementation currently requires this option.

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Output Delay



# **Design Object Access Commands**

Design object access commands are SDC commands. Most SDC constraint commands require one of these commands as command arguments.

Design Object	Access Command
Cell	<u>get_cells</u>
Clock	<u>get_clocks</u>
Net	get_nets
Port	<u>get_ports</u>
Pin	<u>get_pins</u>
Input ports	all_inputs
Output ports	<u>all outputs</u>
Registers	all_registers

Microsemi software supports the following SDC access commands:

## See Also

About SDC Files

## all\_inputs

Design object access command; returns all the input or inout ports of the design.

all\_inputs

## Arguments

None

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

## Example

```
set_max_delay -from [all_inputs] -to [get_clocks ck1]
```



## **Microsemi Implementation Specifics**

None

#### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## all\_outputs

Design object access command; returns all the output or inout ports of the design.

all\_outputs

## Arguments

None

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

## Example

set\_max\_delay -from [all\_inputs] -to [all\_outputs]

## **Microsemi Implementation Specifics**

None

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## all\_registers

Design object access command; returns either a collection of register cells or register pins, whichever you specify.

```
all_registers [-clock clock_name] [-cells] [-data_pins ]
[-clock_pins] [-async_pins] [-output_pins]
```

## Arguments

-clock clock\_name

Creates a collection of register cells or register pins in the specified clock domain.

-cells

Creates a collection of register cells. This is the default. This option cannot be used in combination with any other option.

-data\_pins



Creates a collection of register data pins. -clock\_pins Creates a collection of register clock pins. -async\_pins Creates a collection of register asynchronous pins. -output\_pins Creates a collection of register output pins.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## Description

This command creates either a collection of register cells (default) or register pins, whichever is specified. If you do not specify an option, this command creates a collection of register cells.

## **Exceptions**

None

## **Examples**

set\_max\_delay 2 -from [all\_registers] -to [get\_ports {out}]
set\_max\_delay 3 -to [all\_registers -async\_pins]
set\_false\_path -from [all\_registers -clock clk150]
set\_multicycle\_path -to [all\_registers -clock c\* -data\_pins
-clock\_pins]

## **Microsemi Implementation Specifics**

• None

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## get\_cells

Design object access command; returns the cells (instances) specified by the pattern argument.

get\_cells pattern

## Arguments

#### pattern

Specifies the pattern to match the instances to return. For example, "get\_cells U18\*" returns all instances starting with the characters "U18", where "\*" is a wildcard that represents any character string.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion



## Description

This command returns a collection of instances matching the pattern you specify. You can only use this command as part of a –from, -to, or –through argument for the following constraint exceptions: set\_max delay, set\_multicycle\_path, and set\_false\_path design constraints.

## **Exceptions**

None

## **Examples**

set\_max\_delay 2 -from [get\_cells {reg\*}] -to [get\_ports {out}]
set\_false\_path -through [get\_cells {Rblock/muxA}]

## **Microsemi Implementation Specifics**

None

### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## get\_clocks

Design object access command; returns the specified clock.

get\_clocks pattern

## Arguments

pattern

Specifies the pattern to match to the SmartTime on which a clock constraint has been set.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## Description

- If this command is used as a -from argument in maximum delay (set\_max\_path\_delay), false path (set false path), and multicycle constraints (set multicycle path), the clock pins of all the registers related to this clock are used as path start points.
- If this command is used as a -to argument in maximum delay (set\_max\_path\_delay), false path (set false\_path), and multicycle constraints (set multicycle\_path), the synchronous pins of all the registers related to this clock are used as path endpoints.

## **Exceptions**

None

## Example

set\_max\_delay -from [get\_ports datal] -to \
[get\_clocks ck1]



## **Microsemi Implementation Specifics**

None

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## get\_pins

Design object access command; returns the specified pins.

get\_pins pattern

## Arguments

pattern

Specifies the pattern to match the pins.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

## Example

create\_clock -period 10 [get\_pins clock\_gen/reg2:Q]

## **Microsemi Implementation Specifics**

None

### See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## get\_nets

Design object access command; returns the named nets specified by the pattern argument.

get\_nets pattern

## Arguments

#### pattern

Specifies the pattern to match the names of the nets to return. For example, "get\_nets N\_255\*" returns all nets starting with the characters "N\_255", where "\*" is a wildcard that represents any character string.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion



## Description

This command returns a collection of nets matching the pattern you specify. You can only use this command as source objects in create clock (<u>create\_clock</u>) or create generated clock (<u>create\_generated\_clock</u>) constraints and as -through arguments in set false path (<u>set\_false\_path</u>), set minimum delay (set\_min\_delay), set maximum delay (<u>set\_max\_delay</u>), and set multicycle path (<u>set\_multicycle\_path</u>) constraints.

## **Exceptions**

None

## **Examples**

set\_max\_delay 2 -from [get\_ports RDATA1] -through [get\_nets {net\_chkpl net\_chkqi}]
set\_false\_path -through [get\_nets {Tblk/rm/n\*}]
create\_clcok -name mainCLK -per 2.5 [get\_nets {cknet}]

## **Microsemi Implementation Specifics**

None

## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

## get\_ports

Design object access command; returns the specified ports.

get\_ports pattern

## Argument

#### pattern

Specifies the pattern to match the ports. This is equivalent to the macros \$in()[<pattern>] when used as – from argument and \$out()[<pattern>] when used as –to argument or \$ports()[<pattern>] when used as a – through argument.

## **Supported Families**

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

## Example

create\_clock -period 10[get\_ports CK1]

## **Microsemi Implementation Specifics**

None



## See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions



# Glossary

## arrival time

Actual time in nanoseconds at which the data arrives at a sink pin when considering the propagation delays across the path.

#### asynchronous

Two signals that are not related to each other. Signals not related to the clock are usually asynchronous.

## capture edge

The clock edge that triggers the capture of data at the end point of a path.

## clock

A periodic signal that captures data into sequential elements.

## critical path

A path with the maximum delay between a starting point and an end point. In the presence of a clock constraint, the worst critical path between registers in this clock domain is the path with the worst slack.

## dynamic timing analysis

The standard method for verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface.

## exception

See timing exception.

## explicit clock

Clock sources that can be traced back unambiguously from the clock pin of the registers they deserve, including the output of a DLL or PLL.

## filter

A set of limitations applied to object names in timing analysis to generate target specific sets.

## launch edge

The clock edge that triggers the release of data from a starting point to be captured by another clock edge at an end point.

## minimum period

Timing characteristic of a path between two registers. It indicates how fast the clock will run when this path is the most critical one. The minimum period value takes into consideration both the skew and the setup on the receiving register.

## parallel paths

Paths that run in parallel between a given source and sink pair.



## path

A sequence of elements in the design that identifies a logical flow starting at a source pin and ending at a sink pin.

## path details

An expansion of the path that shows all the nets and cells between the source pin and the sink pin.

### path set

A collection of paths.

#### paths list

Same as path set.

## post-layout

The state of the design after you run Layout. In post-layout, the placement and routing information are available for the whole design.

## potential clock

Pins or ports connected to the clock pins of sequential elements that the Static Timing Analysis (STA) tool cannot determine whether they are is enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks.

## pre-layout

The state of the design before you run Layout. In pre-layout, the placement and routing information are not available.

## recovery time

The amount of time before the active clock edge when the de-activation of asynchronous signals is not allowed.

## removal time

The amount of time after the active clock edge when the de-activation of asynchronous signals is not allowed.

### required time

The time at which the data must be at a sink pin to avoid being in violation.

## requirement

See timing requirement.

## scenario (timing constraints scenario)

Set of timing constraints defined by the user.

## setup time

The time in nanoseconds relative to a clock edge during which the data at the input to a sequential element must remain stable.



## sink pin

The pin located at the end of the timing path. This pin is usually the one where arrival time and required time are evaluated for path violation.

## skew

The difference between the clock insertion delay to the clock pin of a sink register and the insertion delay to the clock pin of a source register.

## slack

The difference between the arrival time and the required time at a specific pin, generally at the data pin of a sequential component.

## slew rate

The time needed for a signal to transition from one logic level to another.

### source pin

The pin located at the beginning of a timing path.

## **STA**

See static timing analysis.

## standard delay format (SDF)

Standard Delay Format, a standard file format used to store design data suited for back-annotation.

## static timing analysis

An efficient technique to identify timing violations in a design and to ensure that all timing requirements are met. It is well suited for traditional synchronous designs. The main advantages are that it does not require input vectors, and it exclusively covers all possible paths in the design in a relatively short run-time.

## synopsys design constraint (SDC)

A standard file format for timing constraints. Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi SoC tools use a subset of the SDC format to capture supported timing constraints. You can import or export an SDC file from the Designer software. Any timing constraint that you can enter using Designer tools, can also be specified in an SDC file.

## timing constraint

A requirement or limitation on the design to be satisfied during the design implementation.

## timing exception

An exception to a general requirement usually applied on a subset of the objects on which the requirement is applied.

## timing requirement

A constraint on the design usually determined by the specifications at the system level.



## virtual clock

A virtual clock is a clock with no source associated to it. It is used to describe clocks outside the FPGA that have an impact on the timing analysis inside the FPGA. For example, if the I/Os are synchronous to an external clock.

## WLM

Wire Load Model. A timing model used in pre-layout to estimate a net delay based on the fan-out.