ARM Cortex-M1-Enabled IGLOO Development Kit Quickstart Card

Kit Contents

Quantity	Description
1	Development board with IGLOO FPGA M1AGL1000V2-FGG484 device, including built-in FlashPro3 compatible programming circuit
2	USB A to mini-B USB cable
1	+5.0 V external power supply with international adapters
1	Quickstart card

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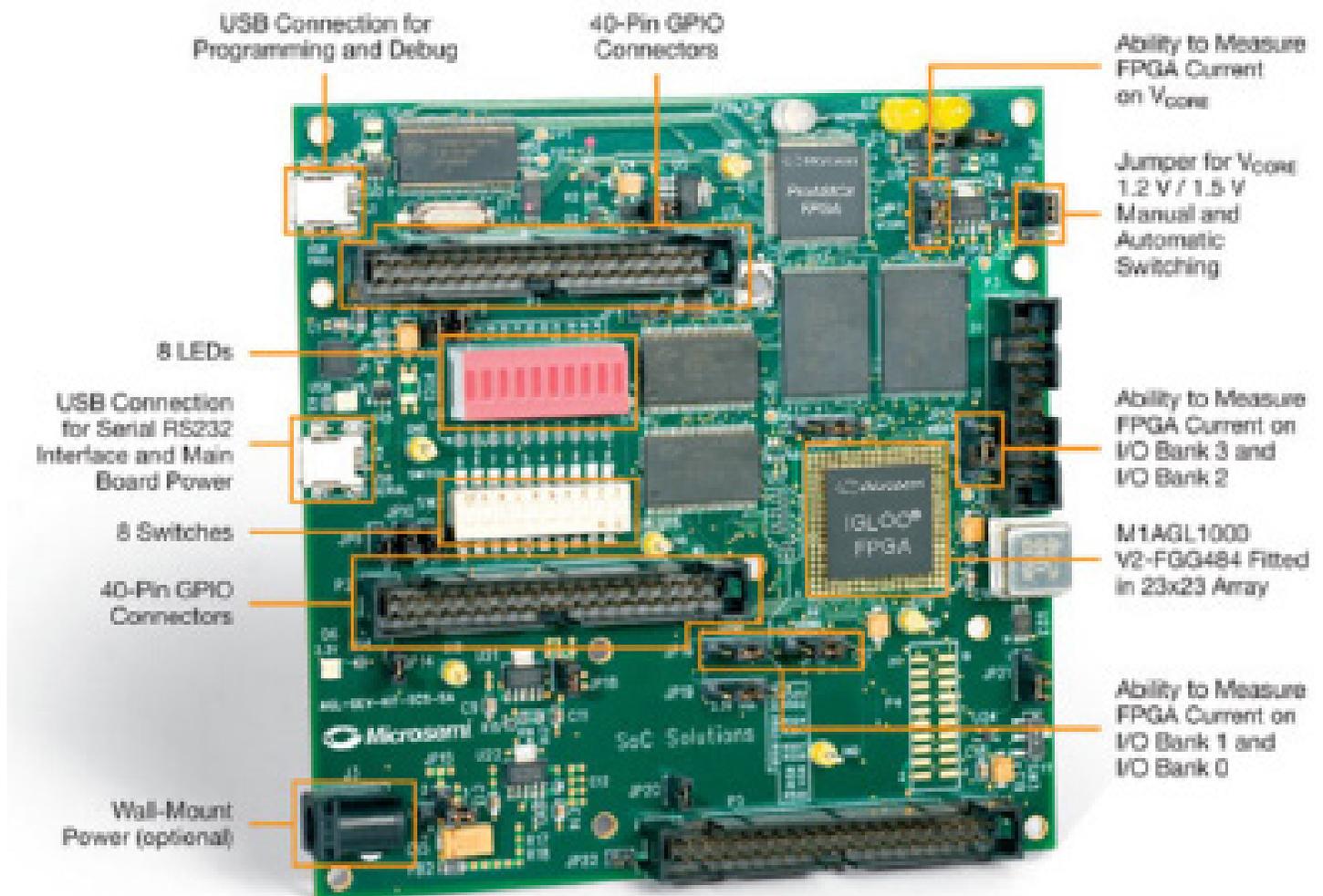
Overview

The ARM Cortex-M1-Enabled IGLOO Development Kit is an advanced microprocessor-based FPGA development and evaluation kit. The architecture provides access to a one-chip FPGA solution containing a Cortex-M1 32bit RISC processor and digital peripheral components. This Development Kit is ideal for development and verification of embedded microprocessor-based systems or subsystems, product development platforms, and algorithm development.

Hardware Features

• Microsemi M1AGL1000 IGLOO FPGA

• 1 MB SRAM

• 16 MB flash

• USB–RS232 converter chip

• GPIO connectors

• Ultra-low power with Flash*Freeze technology

• On-board FlashPro3 circuitry

• 20-Pin Cortex-M1 JTAG connector

• Socketed crystal oscillator

• Push-button power-on reset circuit

• 10 test LEDs

• 10 test switches

• Expansion connectors

Pre-Programmed Demo Design

The M1AGL Development Board is shipped with the Pre-Programmed Demo loaded in the M1AGL FPGA. Also the Traffic Light Controller embedded software image is loaded into external flash. After powering up the M1AGL Development Board for the first time, you will be able to see the Traffic Light Demo executing by observing the timed sequence of LEDs illuminating on U8. Instructions on running the demo design are available in the ARM CortexM1 Enabled IGLOO Development Kit user guide. See the Documentation Resources section for more information.

Jumper Settings

Jumper	Development Kit Function	Factory Default
JP1	Provides 3.3 V to Prog. USB interface	Installed
JP2	Provides 2.5 V to FlashPro3 FPGA	Installed
JP3	Provides 1.2 V and/or 1.5 V core voltage to IGLOO	Installed 2–3
JP4	Provides 3.3 V to FlashPro3 FPGA	Installed
JP5	Selects 1.2 V and/or 1.5 V core voltage for IGLOO FPGA	Depends on whether FPGA is V2 or V5. V2: Installed 2–3. V5: Not installed (auto switch mode)
JP6	Connects 3.3 V to pin 2 of P1 connector	Installed
JP7	Connects VIN (5 V) to pin 1 of P1 connector	Installed

Jumper	Development Kit Function	Factory Default
JP8	Connects push-button reset to P3	Not installed
JP9	Connects 3.3 V to VPUMP pin on FPGA	Installed 2–3
JP10	Connects 2.5 V to pin 2 of P2 connector	Installed
JP11	Connects RS232_TX signal from FPGA to RXD input of serial-to-USB chip	Installed
JP12	Connects RS232_RX signal from FPGA to TXD input of serial-to-USB chip	Installed
JP13	Connects 3.3 V to bank 3 of IGLOO FPGA	Installed 2–3
JP14	Connects VIN (5 V) to pin 1 of P2 connector	Installed
JP15	Provides 3.3 V to non-FlashPro3 portion of board	Installed
JP16	Connects 3.3 V to bank 0 of IGLOO FPGA	Installed 2–3
JP17	Connects 2.5 V to bank 1 of IGLOO FPGA	Installed 2–3
JP18	Connects 3.3 V to bank 2 of IGLOO FPGA	Current can be measured at this point.
JP19	Connects 3.3 V to IGLOO FPGA	Current can be measured at this point.
JP20	Supplies voltage to PLL	1–2 connects core voltage to PLL 2–3 shorts VCCPLF to GND to disable PLL and insure it does not consume power.
JP21	Selects source of Flash*Freeze pin.	1–2 connects GPIOB_0 to FF pin. 2–3 connects push-button circuit with RC and Schmitt trigger buffer.
JP22	Selects input power (5 V) to the main board logic	Factory installed between pins 1 and 4 to select power from 2.1 mm external power supply connector. Other jumper positions have been removed and are no longer supported.
JP23	Connects VIN (5 V) to pin 1 of P5 connector	Current can be measured at this point.
JP24	Connects 3.3 V to pin 2 of P5 connector	Current can be measured at this point.

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Software and Licensing

Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's low power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.

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Documentation Resources

For more information about the ARM Cortex-M1-Enabled IGLOO Development Kit, including user's guides, tutorials, and design examples, see the documentation at www.microsemi.com/products/fpga-soc/design-resources/dev-kits/igloo/cortex-m1-enabled-igloo-development-kit#documents.

Support

Technical support is available online at www.microsemi.com/soc/support and by email at soc_tech@microsemi.com

Microsemi sales offices, including representatives and distributors, are located worldwide. To find your local representative, go to www.microsemi.com/salescontacts

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