Total Ionizing Dose (TID) Radiation Testing of the Microsemi LX7730 Telemetry Controller (100krad(Si) exposure)

Test information

Location: Defense Microelectronics Activity (DMEA) Science and Engineering Gamma Irradiation Test Facility in McClellan, California
Radiation Source: Co-60
Date: 23rd January 2017
Lot #: Die1: T71899 - Die2: E30960
Date Code: 1640
Quantity tested: 4; Serial Numbers: 565, 566, 568, 569
Test Method: MIL-STD-883J, Test Method 1019.9, Condition A (Dose rate 50rad(Si)/s)
Irradiation Temperature: Room
Irradiation Bias (VCC/VDD): Static at 15V/3.3V
Annealing: Biased - Room temperature for 168 hours
Pre and Post Test facility: Microsemi AMS - San Jose

Summary

The LX7730 performance after 100krad(Si) exposure is overall very stable and comparable to pre-radiation.
A few shifts that could push some parameters outside the pre-radiation specification were observed:

- Programmable current source
  - Full scale decreases by about 5%
- Instrumentation amplifier
  - Offset variation of up to 8mV at gain=0.4, 3.55mV at gain=2 and 3mV at gain=10 were observed
  - At max VCC, offset variation of up to 7mV at gain=0.4 and 3mV at gain=2 and 10 were observed
  - At min VCC, offset variation of up to 10mV at gain=0.4, 8mV at gain=2 and 6mV at gain=10 were observed
- Adjustable threshold Bi-level MUX and DAC
  - The threshold might shift by up to 50mV and the hysteresis might decrease by up to 30% when the comparator input is biased between 0 and 5V
  - The threshold might shift by up to 10% (0.5V) and the hysteresis might decrease by up to 30% when the comparator input is biased at a negative voltage
- Fixed Threshold Bi-Level Inputs
  - The threshold might shift by up to 40mV and the hysteresis is reduced by 20%
  - The propagation delays increase by up to 60%

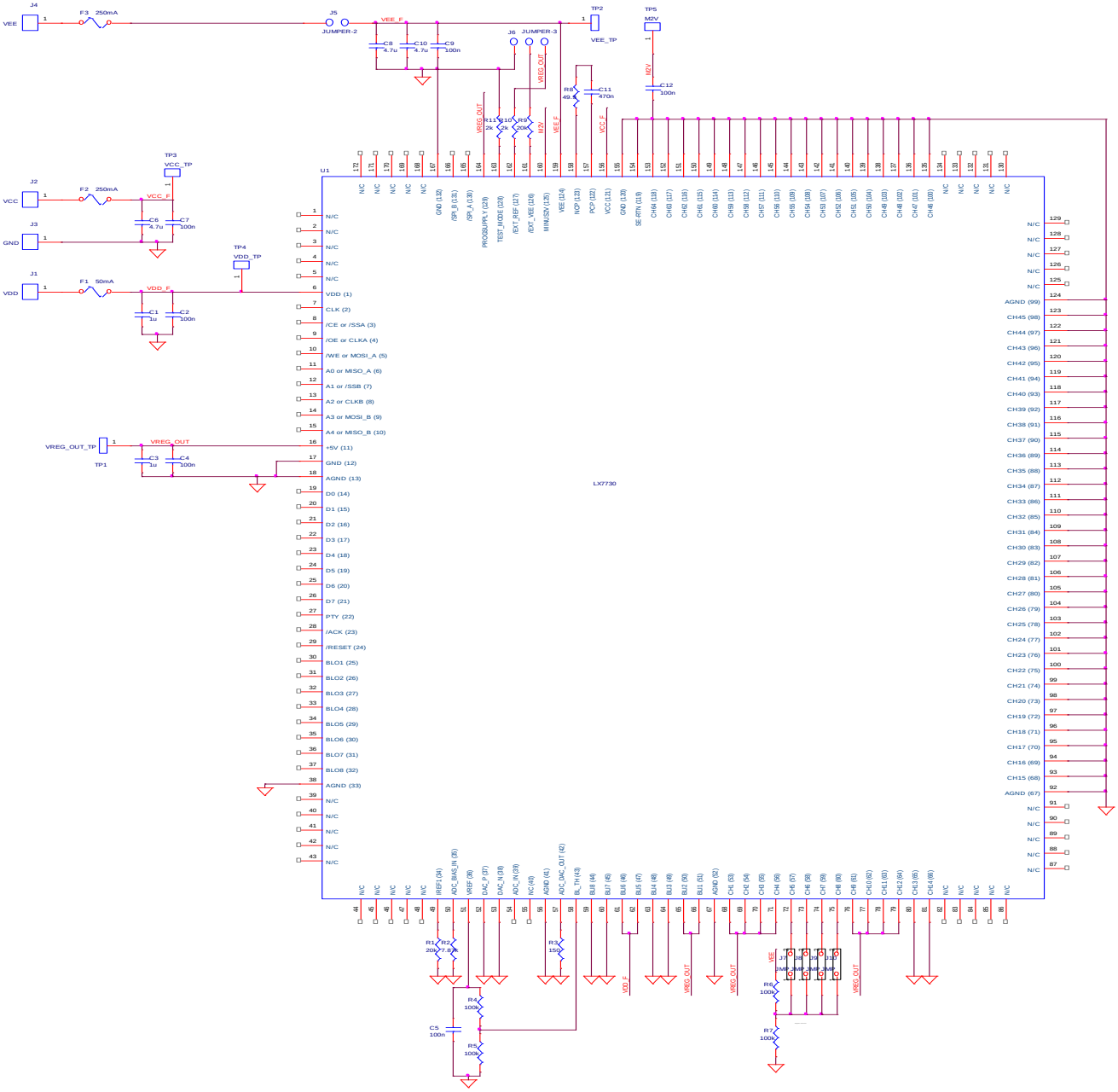
Conclusions

The test results indicate that after 100kRad exposure, the performance of the LX7730 is consistent with the pre-radiation results.

The few observed performance degradations can be mitigated at the system level as follows:

- Programmable current source full scale shift
  - Providing a method to calibrate the variation in programmable current using a precision current sense resistor on a dedicated calibration channel
- Instrumentation amplifier offset shift
  - The offset voltage can be assessed using a 100mV reference from a VREF voltage divider on a dedicated channel.
- Adjustable threshold Bi-level MUX and DAC shift
  - The threshold shift can be minimized by ensuring the comparator input is not biased with a negative voltage.

Bias circuit



Detailed Data

The pre Radiation specifications apply over the operating ambient temperature of -55C ≤ T_A ≤ 125C except where otherwise noted with the following test conditions: VCC = 15V, VDD = 3.3V; R_{IREF} = 20kΩ; $R_{ADC\_BIAS\_IN}$ = 7.87kΩ; $R_{ADC\_DAC\_OUT}$ = 158Ω; / EXT_VEE open, /EXT_REF open. CH1 and CH2 selected and CH2 grounded. CLK = 500kHz. Reg 7 =001010xx. Typical parameter refers to T_J = 25°C. Positive currents flow into the pin.

Pre and Post Irradiation measurements taken at 25C.

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Operating Current													
VCC Normal Current	38	73	84	mA	66.236	66.123	65.821	65.018	66.472	65.868	66.642	65.793	Slight decrease
VCC Standby Current	2.0	4.0	7.0	mA	4.031	4.985	4.097	4.39	4.182	4.975	4.229	4.305	Slight increase
VEE Current	-6.0	-5.0	-2.5	mA	-5.177	-4.751	-4.947	-4.491	-5.286	-4.854	-5.106	-4.673	Slight decrease
Under Voltage Detection													
VCC UVLO	9.5	10	10.5	V	9.96	9.965	9.94	10.005	9.935	9.94	9.965	9.995	Very stable
VCC UVLO Hyst	150	200	400	mV	0.195	0.190	0.205	0.200	0.200	0.200	0.200	0.200	Very stable
VEE UVLO	-7.5	-8.00	-8.20	V	-7.995	-8.045	-8.045	-8.1	-8.045	-8.09	-8	-8.055	Very stable
VEE UVLO Hyst	150	200	400	mV	0.190	0.195	0.205	0.195	0.195	0.195	0.195	0.195	Very stable
+5V UVLO	3.9	4.15	4.40	V	4.135	4.145	4.15	4.135	4.135	4.14	4.11	4.11	Very stable
+5V UVLO Hyst	0	200	400	mV	0.200	0.200	0.205	0.205	0.205	0.205	0.200	0.200	Very stable
Internally Regulated Voltages and Currents													
VCC to VEE voltage drop	1.5	2.5	3.0	V	2.718	2.62	2.648	2.649	2.741	2.657	2.714	2.61	Slight decrease
+5V voltage	4.75	5.00	5.25	V	5.052	5.051	5.079	5.075	5.047	5.045	5.073	5.073	Very stable
VREF voltage	4.95	5.00	5.05	V	5.001	5.003	4.999	5.005	5.000	5.001	5.001	5.008	Very stable
IREF pin voltage	1.568	1.60	1.632	V	1.606	1.606	1.597	1.6	1.598	1.598	1.589	1.592	Very stable
Analog MUX													
Differential Range	0		5	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Common Mode Range	-5		5	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Voltage Clamp power applied	15	16	17	V	16.009	16.013	16.008	15.923	16.004	15.998	16.006	15.987	Very stable
	-23	-17	-15	V	-20.801	-20.924	-20.728	-20.846	-20.666	-20.779	-20.722	-20.814	Very stable
Voltage Clamp (VCC=VEE=0)	15	20	23	V	20.711	20.837	20.756	20.848	20.472	20.596	20.728	20.705	Very stable
	-23	-20	-15	V	-20.713	-20.837	-20.637	-20.756	-20.581	-20.696	-20.634	-20.73	Very stable
Settling Time			10	us	2.46	3.51	2.89	3.67	2.96	4.14	2.88	3.81	50% increase
Bias Current	-200	0	200	nA	-1.586	-2.237	-2.011	-2.096	-1.86	-2.105	-1.633	-1.983	Very stable
Leakage Current	-200	0	200	nA	2.304	3.323	2.2	2.785	2.313	3.182	2.152	2.946	Very stable
Programmable Current Source													
Full scale current	1.880	1.940	2.000	mA	1.911	1.816	1.952	1.860	1.918	1.827	1.934	1.836	~4-5% Decrease
Integral nonlinearity	-7.5	0	7.5	µA	2.431	1.078	2.455	0.810	2.675	0.732	3.451	1.396	Decrease
Differential nonlinearity	-5.0	0	5.0	µA	2.279	1.591	2.077	0.890	2.266	0.674	3.628	2.482	Decrease
Full scale current	3710	3840	3950	µA	3.768	3.608	3.857	3.699	3.778	3.622	3.797	3.632	~4-5% Decrease
Integral nonlinearity	-15		15	µA	8.89	4.956	8.182	5.844	9.047	6.204	10.216	8.497	Decrease
Differential nonlinearity	-15		15	µA	7.957	4.99	8.227	4.855	7.553	5.664	7.957	9.98	Decrease
At DAC=31	290	300	310	uA	296.534	274.537	297.006	277.841	292.946	272.932	302.859	281.240	~5-6% Decrease

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Integral nonlinearity	-2.0		2.0	uA	0.537	1.564	0.395	1.376	0.334	1.804	0.341	1.586	Slight Increase
Differential nonlinearity	-2.0		2.0	uA	0.703	0.655	0.719	0.667	0.356	0.603	0.435	0.682	Stable
Instrumentation Amplifier													
Offset Voltage, Gain = 0.4	-2		25	mV	20.21	22.91	24.44	28.03	15.17	23.26	22.61	24.60	Up to 8mV increase
Offset Voltage, Gain = 2	-3		3	mV	1.27	2.22	1.21	3.78	1.16	4.61	1.83	1.72	Up to 3.5mV change
Offset Voltage, Gain = 10	-3		3	mV	-0.80	0.51	-0.68	1.91	0.60	3.64	-0.94	-1.16	Up to 3mV change
Gain Accuracy, Gain = 0.4	0.398	0.400	0.402	-	0.4004	0.4004	0.4001	0.4000	0.4001	0.4001	0.3997	0.3997	Very stable
Gain Accuracy, Gain = 2	1.992	2.000	2.004	-	1.999	1.999	1.999	1.999	1.997	1.997	1.997	1.997	Very stable
Gain Accuracy, Gain = 10	9.965	9.995	10.025	-	10.001	10.004	10.004	10.004	9.991	9.993	9.989	9.995	Very stable
400Hz 1st Pole Frequency	360	600	1000	Hz	575	575	586.089	590.625	601.714	601.714	613.433	613.433	Very stable
2kHz 1st Pole Frequency	1.4	2.8	3.8	kHz	2.133	2.133	2.172	2.172	2.234	2.234	2.273	2.258	Very stable
10kHz 1st Pole Frequency	8.8	13.5	18.2	kHz	10.5	10.5	10.539	10.539	10.578	10.578	10.617	10.617	Very stable
400Hz 2nd Pole Frequency	360	600	1000	Hz	582.183	582.183	590.625	594.531	610.156	610.156	617.339	617.339	Very stable
2kHz 2nd Pole Frequency	1.4	2.8	3.8	kHz	2.203	2.195	2.234	2.234	2.305	2.297	2.336	2.328	Very stable
10kHz 2nd Pole Frequency	8.8	13.5	18.2	kHz	10.773	10.734	10.773	10.773	10.891	10.891	10.891	10.891	Very stable
Output Step Rise Time, G=0.4	120	210	333	us	203.516	232.558	204.196	239.788	206.587	233.711	212.005	247.403	~14-16% Increase
Output Step Rise Time, G=2	31	52	87	us	52.011	55.599	51.996	56.069	50.316	53.938	50.714	55.672	~8-10% Increase
Output Step Rise Time, G=10	31	52	87	us	54.37	56.059	51.649	56.458	53.268	54.463	51.752	56.762	~8-10% Increase
Analog-to-Digital Converter (input at ADC_IN)													
Linear Range	0		2.0	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Full scale error	-2.5	0	2.5	%	-0.31	-0.19	-0.11	-0.07	-0.37	-0.33	-0.32	-0.18	Very stable
Offset Error	-10		10	mV	-3.70	-1.97	0.64	0.77	-5.36	-5.32	-3.35	-2.17	Very stable
Integral nonlinearity	-6		6	LSB	3.466	3.592	3.203	3.476	4.626	5.059	3.520	4.241	Very stable
Differential nonlinearity	-1		3	LSB	2.068	1.770	1.584	1.483	1.844	1.707	1.968	1.892	Very stable
Leakage current	-0.2	0	0.2	uA	-0.019	0.000	0.000	-0.009	-0.019	0.000	0.000	0.000	Very stable
Adjustable threshold Bi-level MUX and DAC													
Threshold DAC Max Output (If input is >=0V during TID)	4.95	5	5.05	V	4.990	5.025	4.990	5.014	4.980	5.005	4.990	5.025	Up to 50mV increase
Hysteresis DAC Max Output (If input is >=0V during TID)	**0.075**	**0.112**	**0.150**	V	0.115	0.090	0.115	0.088	0.125	0.098	0.120	0.090	Up to 30% decrease
Threshold DAC Max Output (If input is VEE/2 during TID)	4.95	5	5.05	V	4.990	4.491	4.990	4.510	4.980	4.465	4.990	4.479	~10% decrease
Hysteresis DAC Max Output (If input is VEE/2 during TID)	**0.075**	**0.112**	**0.150**	V	0.120	0.084	0.105	0.080	0.120	0.086	0.115	0.084	Up to 30% decrease
10 Bit Current DAC													
Full Scale	-2.06	-2.00	-1.94	mA	-2.002	-1.997	-2.005	-2.003	-1.981	-1.979	-2.008	-2.009	Very stable
Integral nonlinearity	-5		5	LSB	-0.616	-1.125	-0.967	-2.305	-0.646	-0.525	-0.876	-1.823	Very stable
					0.596	0.713	0.593	0.954	0.827	0.669	0.715	0.895	Very stable
Differential nonlinearity	-0.5		0.5	LSB	-0.319	-0.313	-0.325	-0.310	-0.335	-0.339	-0.321	-0.321	Very stable
					0.084	0.069	0.039	0.040	0.067	0.060	0.066	0.062	Very stable
DAC Settling Time			1	us	0.606	0.611	0.609	0.607	0.624	0.625	0.604	0.597	Very stable
Fixed Threshold Bi-Level Inputs													

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Threshold – Internal ref (Rising Voltage)	2.45	2.50	2.55	V	2.503	2.531	2.506	2.534	2.493	2.529	2.504	2.540	Up to 40mV increase
Threshold Hysteresis – Internal reference	60	120	180	mV	0.124	0.112	0.122	0.114	0.140	0.130	0.128	0.114	Up to 15% decrease
Threshold – External 2.5V (Rising Voltage)	2.45	2.50	2.55	V	2.500	2.530	2.515	2.540	2.500	2.540	2.505	2.540	Up to 40mV increase
Threshold Hysteresis – External 2.5V	60	120	180	mV	0.120	0.110	0.120	0.115	0.140	0.130	0.125	0.115	Up to 15% decrease
Voltage Clamp (power applied) – 1mA into the pin	15	20	23	V	20.639	20.720	20.585	20.641	20.472	20.583	20.507	20.592	Very stable
Voltage Clamp (power applied) – 1mA out of the pin	-23	-20	-15	V	-20.617	-20.715	-20.526	-20.636	-20.507	-20.613	-20.538	-20.613	Very stable
Voltage Clamp (power remove) – 1mA into the pin	15	20	23	V	20.543	20.639	20.427	20.536	20.385	20.506	20.417	20.509	Very stable
Voltage Clamp (power removed) – 1mA out of the pin	-23	-20	-15	V	-20.524	-20.636	-20.436	-20.556	-20.427	-20.455	-20.449	-20.534	Very stable
Bias Current at 5V	-0.2	0	1.5	uA	0.103	0.108	0.073	0.078	0.087	0.064	0.038	0.040	Very stable
Bias Current at 0V	-0.2	0	1.5	uA	0.000	-0.001	0.000	0.000	0.000	0.000	0.000	0.000	Very stable
Leakage Current at 5V (power off)	-0.2	0	1.5	uA	0.098	0.104	0.069	0.074	0.050	0.059	0.035	0.038	Very stable
Leakage Current at 0V (power off)	-0.2	0	1.5	uA	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	Very stable
Propagation Delay - High to Low transition	0.3	0.8	1.3	us	0.817	1.248	0.764	1.111	0.723	1.073	0.713	1.030	~30-60% increase
Propagation Delay - Low to High transition	0.8	2.1	3.4	us	2.234	3.014	2.549	3.394	1.898	2.423	2.201	2.900	~20-40% increase
Threshold Pin Leakage at 5V	-0.2	0	2.0	uA	0.133	0.144	0.098	0.126	0.116	0.131	0.142	0.162	Very stable
Threshold Pin Leakage at 0V	-0.2	0	2.0	uA	-0.011	-0.008	0.004	-0.004	-0.016	-0.008	-0.018	-0.006	Very stable
Logic Levels for FPGA Interface I/Os													
Input Logic Threshold at 3.3V	1.155	1.65	2.145	V	1.715	1.665	1.705	1.665	1.705	1.655	1.705	1.665	Very stable
Program pins Threshold	2.0	2.5	3.0	V	2.580	2.530	2.600	2.550	2.570	2.520	2.590	2.540	Very stable
Logic Output VOH at 100uA at 3.3V	3.0		3.3	V	3.170	3.171	3.164	3.172	3.174	3.175	3.169	3.171	Very stable
Logic Output VOL at 100uA at 3.3V	0		0.3	V	0.097	0.104	0.095	0.100	0.095	0.101	0.098	0.104	Very stable
IIH SPI_A, SPI_B (3.3V)	-2	0	2	uA	0.002	0.004	0.01	0	0.007	0.004	0.007	0.005	Very stable
IIL SPI_A, SPI_B (0V)	-10	-4	-1.5	uA	-4.15	-4.09	-4.21	-4.13	-4.37	-4.32	-4.53	-4.49	Very stable
IIH Pins 2,6,8-10,14-21, 22: I/O as input (3.3V)	1.5	4	10	uA	4.48	4.21	4.58	4.33	4.76	4.48	4.97	4.68	Very stable
IIL Pins 2,6,8-10,14-21, 22: I/O as input (0V)	-2	0	2	uA	0.035	0.008	0.036	0.016	0.038	0.02	0.033	0.017	Very stable
IIH Pins 3-5, 7 I/O as input (3.3V)	-2	0	2	uA	0.03	-0.01	0.03	-0.01	0.03	-0.01	0.03	-0.01	Very stable
IIL Pins 3-5, 7: I/O as input (0V)	-10	-4	-1.5	uA	-4.02	-4	-4.12	-4.13	-4.28	-4.28	-4.47	-4.46	Very stable
IIH /EXT_VREF or /EXT_VEE = 5V	-2	0	2	uA	0.013	0.01	-0.082	-0.045	-0.041	0.005	-0.052	-0.043	Very stable

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
IIL /EXT_VREF or /EXT_VEE = 0V	-12	-6	-1.5	uA	-6.39	-6.36	-6.54	-6.51	-6.77	-6.77	-7.07	-7.01	Very stable
IIH /RESET (5V)	1.5	4	10	uA	4.12	4.11	4.31	4.29	4.42	4.43	4.57	4.55	Very stable
IIL /RESET (0V)	-150	-66	-33	uA	-77.1	-78.5	-78.6	-79.9	-82.6	-84	-83.5	-84.3	Very stable

Parameters tested but not specified

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Instrumentation Amplifier													
Offset Voltage, Gain = 0.4 16V/3.3V	-2		32	mV	19.70	21.19	24.02	26.82	14.84	21.53	22.58	23.29	Up to 7mV increase
Offset Voltage, Gain = 0.4 11.4V/3.3V	-2		32	mV	20.45	28.54	25.04	33.47	16.50	26.77	22.71	31.96	Up to 10mV increase
Offset Voltage, Gain = 2 16V/3.3V	-3.5		4.5	mV	1.09	1.39	1.02	2.38	0.69	3.35	1.62	0.84	Up to 3mV change
Offset Voltage, Gain = 2 11.4V/3.3V	-3.5		4.5	mV	2.32	8.83	2.61	10.14	2.77	9.01	2.28	9.74	Up to 8mV change
Offset Voltage, Gain = 10 16V/3.3V	-3.5		3.5	mV	-0.96	-0.21	-0.91	1.16	0.34	2.71	-0.99	-1.68	Up to 3mV change
Offset Voltage, Gain = 10 11.4V/3.3V	-3.5		3.5	mV	-0.68	4.20	-0.24	5.44	1.29	5.95	-1.20	3.49	Up to 6mV change
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=5V	0.398		0.402	-	0.3997	0.3997	0.3994	0.3994	0.3995	0.3994	0.3990	0.3990	Very stable
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=-5V	0.398		0.402	-	0.3996	0.3996	0.3992	0.3992	0.3993	0.3993	0.3989	0.3988	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=5V	0.397		0.403	-	0.4003	0.4005	0.3999	0.4001	0.3998	0.4000	0.3996	0.3998	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=0V	0.398		0.402	-	0.4012	0.4013	0.4008	0.4010	0.4009	0.4010	0.4005	0.4006	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=-5V	0.397		0.403	-	0.4004	0.4006	0.4000	0.4002	0.3999	0.4001	0.3997	0.3999	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=5V	0.398		0.402	-	0.3995	0.3995	0.3991	0.3991	0.3992	0.3992	0.3988	0.3988	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=0V	0.398		0.402	-	0.4004	0.4003	0.4000	0.4000	0.4001	0.4000	0.3997	0.3996	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=-5V	0.398		0.402	-	0.3997	0.3997	0.3993	0.3993	0.3994	0.3993	0.3990	0.3989	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=5V	1.992		2.004	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=-5V	1.992		2.004	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=5V	1.990		2.010	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=0V	1.992		2.004	-	1.999	1.999	1.999	1.999	1.997	1.997	1.997	1.997	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=-5V	1.990		2.010	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Gain Accuracy, Gain = 2 16V/3.3V at CM=5V	1.992		2.004	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=0V	1.992		2.004	-	1.999	1.999	1.999	1.999	1.997	1.997	1.997	1.997	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=-5V	1.992		2.004	-	1.998	1.998	1.998	1.998	1.996	1.996	1.996	1.996	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=5V	9.965		10.025	-	9.993	9.998	9.997	9.999	9.983	9.986	9.982	9.987	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=-5V	9.965		10.025	-	9.994	9.996	9.996	9.997	9.982	9.985	9.982	9.991	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=5V	9.965		10.025	-	9.994	9.997	9.997	9.997	9.982	9.989	9.983	9.99	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=0V	9.965		10.025	-	10.001	10.004	10.005	10.01	9.99	9.995	9.988	9.997	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=-5V	9.965		10.025	-	9.994	9.997	9.996	10.005	9.982	9.986	9.98	10	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=5V	9.965		10.025	-	9.994	9.998	9.995	9.998	9.983	9.985	9.981	9.988	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=0V	9.965		10.025	-	10	10.006	10.003	10.008	9.989	9.993	9.99	9.994	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=-5V	9.965		10.025	-	9.994	9.996	9.995	10	9.982	9.984	9.982	9.991	Very stable
Logic Levels for FPGA Interface I/Os													
Input Logic Threshold at VDD=2.25V	0.7875	1.125	1.463	V	1.203	1.163	1.213	1.163	1.193	1.153	1.203	1.163	Very stable
Input Logic Threshold at VDD=5.5V	1.925	2.725	3.575	V	2.795	2.745	2.795	2.745	2.785	2.725	2.785	2.735	Very stable
Logic Output VOH at 100uA at VDD=2.25V	1.95		2.25	V	2.100	2.101	2.093	2.103	2.103	2.105	2.098	2.101	Very stable
Logic Output VOL at 100uA at VDD=2.25V	0		0.3	V	0.110	0.115	0.108	0.113	0.108	0.113	0.112	0.117	Very stable
Logic Output VOH at 100uA at VDD=5.5V	5.2		5.5	V	5.376	5.382	5.369	5.384	5.379	5.385	5.375	5.382	Very stable
Logic Output VOL at 100uA at VDD=5.5V	0		0.3	V	0.087	0.093	0.087	0.093	0.086	0.092	0.089	0.095	Very stable
Programmable Current Source					0.700	0.749	0.716	0.573	0.454	0.697	0.435	0.682	
Full scale current (doubWt OFF) at VCC=11.4V	1.880	1.940	2.000	mA	1.911	1.817	1.951	1.861	1.918	1.828	1.934	1.838	~4-5% Decrease
Integral nonlinearity at VCC=11.4V	-7.5	0	7.5	µA	2.447	1.159	2.573	0.842	2.636	0.745	3.550	1.490	Decrease
Differential nonlinearity at VCC=11.4V	-5.0	0	5.0	µA	2.401	1.645	2.252	0.850	2.131	0.755	3.749	2.562	Decrease
Full scale current (doubWt ON) at VCC=11.4V	3710	3840	3950	µA	3.767	3.607	3.855	3.694	3.776	3.621	3.795	3.632	~4-5% Decrease
Integral nonlinearity at VCC=11.4V	-15		15	µA	8.654	6.451	8.328	9.205	9.598	7.710	10.205	8.733	Decrease
Differential nonlinearity at VCC=11.4V	-15		15	µA	7.148	6.743	7.687	9.441	8.227	7.283	8.227	9.171	Decrease
At DAC=31 at VCC=11.4V	290	300	310	uA	296.439	274.537	296.911	277.841	292.852	272.932	302.859	281.240	~5-6% Decrease

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Integral nonlinearity at VCC=11.4V	-2.0		2.0	uA	0.579	1.660	0.428	1.483	0.329	1.907	0.309	1.688	Slight Increase
Differential nonlinearity at VCC=11.4V	-2.0		2.0	uA	0.700	0.749	0.716	0.573	0.454	0.697	0.435	0.682	Stable
Full scale current (doubWt OFF) at VCC=16V	1.880	1.940	2.000	mA	1.912	1.818	1.953	1.863	1.919	1.830	1.935	1.840	~4-5% Decrease
Integral nonlinearity at VCC=16V	-7.5	0	7.5	µA	2.455	1.096	2.470	0.732	2.620	0.695	3.539	1.473	Decrease
Differential nonlinearity at VCC=16V	-5.0	0	5.0	µA	2.387	1.672	2.117	0.782	2.185	0.769	3.776	2.657	Decrease
Full scale current (doubWt ON) at VCC=16V	3710	3840	3950	µA	3.773	3.611	3.860	3.706	3.782	3.632	3.801	3.642	~4-5% Decrease
Integral nonlinearity at VCC=16V	-15		15	µA	8.575	5.271	8.418	5.945	9.205	6.316	9.688	7.159	Decrease
Differential nonlinearity at VCC=16V	-15		15	µA	7.418	5.395	7.148	4.855	7.957	5.395	7.687	8.632	Decrease
At DAC=31 at VCC=16V	290	300	310	uA	296.534	274.537	297.006	278.030	292.946	273.026	302.953	281.523	~5-6% Decrease
Integral nonlinearity at VCC=16V	-2.0		2.0	uA	0.518	1.666	0.422	1.469	0.379	1.881	0.346	1.678	Slight Increase
Differential nonlinearity at VCC=16V	-2.0		2.0	uA	0.612	0.752	0.627	0.676	0.448	0.703	0.442	0.600	Stable
Fixed Threshold Bi-Level Inputs													
Threshold – External 0.1V (Rising Voltage) at VCC=15V	0.0	0.1	0.2	V	0.105	0.130	0.115	0.140	0.100	0.140	0.105	0.140	Up to 40mV
Threshold Hysteresis – External 0.1V at VCC=15V	60	120	180	mV	0.120	0.110	0.120	0.115	0.135	0.135	0.125	0.115	Up to 10mV decrease
Threshold – External 4.9V (Rising Voltage) at VCC=15V	4.8	4.9	5.0	V	4.900	4.940	4.910	4.945	4.900	4.945	4.905	4.945	Up to 45mV
Threshold Hysteresis – External 4.9V at VCC=15V	60	120	180	mV	0.120	0.115	0.120	0.115	0.145	0.135	0.130	0.115	Up to 15mV decrease
Threshold – Internal ref (Rising Voltage) at VCC=11.4V	2.45	2.50	2.55	V	2.504	2.532	2.506	2.535	2.493	2.530	2.507	2.540	Up to 40mV
Threshold Hysteresis – Internal reference at VCC=11.4V	60	120	180	mV	0.126	0.114	0.124	0.116	0.144	0.132	0.132	0.116	Up to 16mV decrease
Threshold – External 4.9V (Rising Voltage) at VCC=11.4V	4.8	4.9	5.0	V	4.900	4.940	4.915	4.945	4.900	4.945	4.905	4.945	Up to 45mV
Threshold Hysteresis – External 4.9V at VCC=11.4V	60	120	180	mV	0.125	0.115	0.130	0.115	0.145	0.135	0.135	0.120	Up to 15mV decrease
Adjustable threshold Bi-level MUX and DAC													
Threshold DAC Max Output (If input is >=0V during TID) at VCC=11.4V	4.95	5	5.05	V	4.990	5.013	4.990	5.012	4.980	5.014	4.990	5.019	Up to 50mV increase
Hysteresis DAC Max Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.130	0.090	0.125	0.094	0.125	0.101	0.130	0.096	~25% decrease
Threshold DAC Max Output (If input is VEE/2 during TID)	4.95	5	5.05	V	4.990	4.491	4.990	4.512	4.980	4.465	4.990	4.479	~10% decrease

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
at VCC=11.4V													
Hysteresis DAC Max Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.125	0.087	0.105	0.082	0.120	0.089	0.115	0.084	Up to 30% decrease
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=15V	-0.05	0	0.05	V	0.020	0.046	0.020	0.038	0.020	0.044	0.020	0.043	Up to 50mV increase
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=15V	0.075	0.112	0.150	V	0.125	0.093	0.120	0.096	0.130	0.101	0.125	0.096	Up to 25% decrease
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	-0.05	0	0.05	V	0.020	-0.479	0.030	-0.464	0.010	-0.508	0.030	-0.497	~0.5V decrease
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	0.075	0.112	0.150	V	0.120	0.087	0.115	0.084	0.115	0.086	0.125	0.087	Up to 30% decrease
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	-0.05	0	0.05	V	0.020	0.046	0.020	0.036	0.010	0.044	0.020	0.043	Up to 30% decrease
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.125	0.093	0.120	0.094	0.125	0.101	0.125	0.096	Up to 50mV increase
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	-0.05	0	0.05	V	0.020	-0.482	0.030	-0.464	0.010	-0.508	0.020	-0.500	Up to 25% decrease
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.120	0.084	0.115	0.082	0.120	0.086	0.115	0.084	~0.5V decrease