Total Ionizing Dose (TID) Radiation Testing of the Microsemi LX7730 Telemetry Controller (100krad(Si) exposure)

Test information
Location: Defense Microelectronics Activity (DMEA) Science and Engineering Gamma Irradiation Test Facility in McClellan, California
Radiation Source: Co-60
Date: 23rd January 2017
Lot #: Die1: T71899 - Die2: E30960
Date Code: 1640
Quantity tested: 4; Serial Numbers: 565, 566, 568, 569
Test Method: MIL-STD-883J, Test Method 1019.9, Condition A (Dose rate 50rad(Si)/s)
Irradiation Temperature: Room
Irradiation Bias (VCC/VDD): Static at 15V/3.3V
Annealing: Biased - Room temperature for 168 hours
Pre and Post Test facility: Microsemi AMS - San Jose

Summary
The LX7730 performance after 100k rad(Si) exposure is overall very stable and comparable to pre-radiation. A few shifts that could push some parameters outside the pre-radiation specification were observed:

- **Programmable current source**
  - Full scale decreases by about 5%
- **Instrumentation amplifier**
  - Offset variation of up to 8mV at gain=0.4, 3.55mV at gain=2 and 3mV at gain=10 were observed
  - At max VCC, offset variation of up to 7mV at gain=0.4 and 3mV at gain=2 and 10 were observed
  - At min VCC, offset variation of up to 10mV at gain=0.4, 8mV at gain=2 and 6mV at gain=10 were observed
- **Adjustable threshold Bi-level MUX and DAC**
  - The threshold might shift by up to 50mV and the hysteresis might decrease by up to 30% when the comparator input is biased between 0 and 5V
  - The threshold might shift by up to 10% (0.5V) and the hysteresis might decrease by up to 30% when the comparator input is biased at a negative voltage
- **Fixed Threshold Bi-Level Inputs**
  - The threshold might shift by up to 40mV and the hysteresis is reduced by 20%
  - The propagation delays increase by up to 60%

Conclusions
The test results indicate that after 100kRad exposure, the performance of the LX7730 is consistent with the pre-radiation results. The few observed performance degradations can be mitigated at the system level as follows:

- **Programmable current source full scale shift**
  - Providing a method to calibrate the variation in programmable current using a precision current sense resistor on a dedicated calibration channel
- **Instrumentation amplifier offset shift**
  - The offset voltage can be assessed using a 100mV reference from a VREF voltage divider on a dedicated channel.
- **Adjustable threshold Bi-level MUX and DAC shift**
  - The threshold shift can be minimized by ensuring the comparator input is not biased with a negative voltage.
Bias circuit
Detailed Data

The pre Radiation specifications apply over the operating ambient temperature of -55°C ≤ T_a ≤ 125°C except where otherwise noted with the following test conditions: VCC = 15V, VDD = 3.3V; R_REF = 20kΩ; R_DAC_BIAS_IN = 7.87kΩ; R_DAC_DAC_OUT = 158Ω; /EXT_VEE open, /EXT_REF open. CH1 and CH2 selected and CH2 grounded. CLK = 500kHz. Reg 7 =001010xx. Typical parameter refers to T_a = 25°C.

Positive currents flow into the pin.

Pre and Post Irradiation measurements taken at 25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Pre Radiation Specification</th>
<th>SN 565</th>
<th>SN 566</th>
<th>SN 568</th>
<th>SN 569</th>
<th>Comment</th>
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<tr>
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<td>VCC Normal Current</td>
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<td>73</td>
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<td>mA</td>
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<td>mA</td>
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<td>400</td>
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<td>mV</td>
<td>0.200</td>
<td>0.200</td>
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</table>

Internally Regulated Voltages and Currents

| Voltage to VEE voltage drop     | 1.5                         | 2.5    | 3.0    | V      | 2.718  | 2.62   | 2.648  | 2.649  | 2.741  | 2.657  | 2.714  | 2.61   | Slight decrease |
| +SV voltage                    | 4.75                        | 5.00   | 5.25   | V      | 5.052  | 5.051  | 5.078  | 5.078  | 5.047  | 5.047  | 5.079  | 5.073  | Very stable |
| VREF voltage                   | 4.95                        | 5.00   | 5.05   | V      | 5.001  | 5.003  | 4.999  | 5.005  | 5.007  | 5.001  | 5.001  | 5.008  | Very stable |
| IREF pin voltage               | 1.568                       | 1.60   | 1.632  | V      | 1.606  | 1.606  | 1.597  | 1.6    | 1.598  | 1.598  | 1.589  | 1.592  | Very stable |

Analog MUX

| Bias Current                   | -200                        | 0      | 200    | mA     | -1.586 | -2.237 | -2.011 | -2.096 | -1.86  | -2.105 | -1.633 | -1.983 | Very stable |
| Leakage Current                | -200                        | 0      | 200    | mA     | 2.304  | 3.323  | 2.2    | 2.785  | 2.313  | 3.182  | 2.152  | 2.946  | Very stable |

Programmable Current Source

| Full scale current             | 1.880                       | 1.940  | 2.000  | mA     | 1.911  | 1.816  | 1.952  | 1.860  | 1.918  | 1.827  | 1.934  | 1.836  | ~4-5% Decrease |
| Integral nonlinearity          | -7.5                        | 0      | 7.5    | µA     | 2.431  | 1.078  | 2.455  | 0.810  | 2.675  | 0.732  | 3.451  | 1.396  | Decrease |
| Differential nonlinearity      | -5.0                        | 0      | 5.0    | µA     | 2.279  | 1.591  | 2.077  | 0.890  | 2.666  | 0.674  | 3.628  | 2.482  | Decrease |
| At DAC=31                      | 290                        | 300    | 310    | uA     | 296.534| 274.537| 297.006| 277.841| 292.946| 272.932| 302.859| 281.240| ~5-6% Decrease |

~5% Increase

Very stable

% Decrease
### Instrumentation Amplifier

<table>
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<tr>
<th>Parameters</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Comment</th>
</tr>
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<tr>
<td>Integral nonlinearity</td>
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<td>2.0</td>
<td></td>
<td>uA</td>
<td>0.537</td>
<td>1.564</td>
<td>0.395</td>
<td>1.376</td>
<td>0.334</td>
<td>1.804</td>
<td>0.341</td>
<td>1.586</td>
<td>Slight Increase</td>
</tr>
<tr>
<td>Differential nonlinearity</td>
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<td></td>
<td>uA</td>
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<td>0.719</td>
<td>0.667</td>
<td>0.356</td>
<td>0.603</td>
<td>0.435</td>
<td>0.682</td>
<td>Stable</td>
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### Analog-to-Digital Converter (input at ADC_IN)

<table>
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<tr>
<th>Parameters</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
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<tr>
<td>Linear Range</td>
<td>0</td>
<td>1.2</td>
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<td>kHz</td>
<td>17.73</td>
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<td>10.539</td>
<td>10.5</td>
<td>10.539</td>
<td>10.5</td>
<td>10.539</td>
<td>Very stable</td>
</tr>
<tr>
<td>Full scale error</td>
<td>-2.5</td>
<td>0.2</td>
<td>2.5</td>
<td>%</td>
<td>-0.31</td>
<td>-0.19</td>
<td>-0.11</td>
<td>-0.07</td>
<td>-0.37</td>
<td>-0.33</td>
<td>-0.32</td>
<td>-0.18</td>
<td>Very stable</td>
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<tr>
<td>Offset Error</td>
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<td>10</td>
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<td>mV</td>
<td>-3.70</td>
<td>-1.97</td>
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<td>0.77</td>
<td>-5.36</td>
<td>-5.32</td>
<td>-3.35</td>
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<tr>
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<td>Leakage current</td>
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<td>uA</td>
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<td>-0.009</td>
<td>-0.019</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td>Very stable</td>
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### Adjustable threshold Bi-level MUX and DAC

<table>
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<th>Parameters</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Comment</th>
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<tbody>
<tr>
<td>Threshold DAC Max Output (If input is &gt;=0V during TID)</td>
<td>4.95</td>
<td>5</td>
<td>5.05</td>
<td>V</td>
<td>4.990</td>
<td>5.025</td>
<td>4.990</td>
<td>5.014</td>
<td>4.980</td>
<td>5.005</td>
<td>4.990</td>
<td>5.025</td>
<td>Up to 50mV increase</td>
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<tr>
<td>Hysteresis DAC Max Output (If input is &gt;=0V during TID)</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>%</td>
<td>0.115</td>
<td>0.090</td>
<td>0.115</td>
<td>0.088</td>
<td>0.125</td>
<td>0.098</td>
<td>0.120</td>
<td>0.090</td>
<td>Up to 30% decrease</td>
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<tr>
<td>Threshold DAC Max Output (If input is VEE/2 during TID)</td>
<td>4.95</td>
<td>5</td>
<td>5.05</td>
<td>V</td>
<td>4.990</td>
<td>4.491</td>
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<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>%</td>
<td>0.120</td>
<td>0.084</td>
<td>0.105</td>
<td>0.080</td>
<td>0.120</td>
<td>0.086</td>
<td>0.115</td>
<td>0.084</td>
<td>Up to 30% decrease</td>
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### 10 Bit Current DAC

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<th>Min</th>
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<th>Max</th>
<th>Units</th>
<th>Pre</th>
<th>Post 100k</th>
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<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
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<td>-2.003</td>
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<td>-1.979</td>
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<td>Very stable</td>
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<td>5</td>
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<td>LSB</td>
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<td>-2.305</td>
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<td>-0.876</td>
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<td>LSB</td>
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<tr>
<td>DAC Settling Time</td>
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<td>1</td>
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<td>us</td>
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<td>0.611</td>
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<td>0.607</td>
<td>0.624</td>
<td>0.625</td>
<td>0.604</td>
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**Pre Radiation Specification**

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**Hysteresis DAC Max Output (If input is >0V during TID)**

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<th>Pre</th>
<th>0.075</th>
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<tbody>
<tr>
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<td>Parameters</td>
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<td>SN 566</td>
</tr>
<tr>
<td>--------------------------------------------------------------------------</td>
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<td>--------</td>
</tr>
<tr>
<td>Threshold – Internal ref (Rising Voltage)</td>
<td>2.45</td>
<td>2.50</td>
</tr>
<tr>
<td>Threshold Hysteresis – Internal reference</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>Threshold – External 2.5V (Rising Voltage)</td>
<td>2.45</td>
<td>2.50</td>
</tr>
<tr>
<td>Threshold Hysteresis – External 2.5V</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>Voltage Clamp (power applied) – 1mA into the pin</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>Voltage Clamp (power applied) – 1mA out of the pin</td>
<td>-23</td>
<td>-20</td>
</tr>
<tr>
<td>Voltage Clamp (power remove) – 1mA into the pin</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>Voltage Clamp (power removed) – 1mA out of the pin</td>
<td>-23</td>
<td>-20</td>
</tr>
<tr>
<td>Bias Current at 5V</td>
<td>-0.2</td>
<td>0</td>
</tr>
<tr>
<td>Bias Current at 0V</td>
<td>-0.2</td>
<td>0</td>
</tr>
<tr>
<td>Leakage Current at 5V (power off)</td>
<td>-0.2</td>
<td>0</td>
</tr>
<tr>
<td>Leakage Current at 0V (power off)</td>
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<td>0</td>
</tr>
<tr>
<td>Propagation Delay - High to Low transition</td>
<td>0.3</td>
<td>0.8</td>
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<td>Propagation Delay - Low to High transition</td>
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<td>Threshold Pin Leakage at 0V</td>
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<tr>
<td>Logic Levels for FPGA Interface I/Os</td>
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<tr>
<td>Input Logic Threshold at 3.3V</td>
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<tr>
<td>Program pins Threshold</td>
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</tr>
<tr>
<td>Logic Output VDH at 100µA at 3.3V</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>Logic Output VOL at 100µA at 3.3V</td>
<td>0</td>
<td>0.3</td>
</tr>
<tr>
<td>IIH SPI_A, SPI_B (3.3V)</td>
<td>-2</td>
<td>0</td>
</tr>
<tr>
<td>IIH SPI_A, SPI_B (0V)</td>
<td>-10</td>
<td>-4</td>
</tr>
<tr>
<td>IIH Pins 2,6,8,10,14,21, 22: I/O as input (3.3V)</td>
<td>1.5</td>
<td>4</td>
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<tr>
<td>IIH Pins 2,6,8,10,14,21, 22: I/O as input (0V)</td>
<td>-2</td>
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<tr>
<td>IIH Pins 3-5, 7 I/O as input (3.3V)</td>
<td>-2</td>
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<td>IIH Pins 3-5, 7: I/O as input (0V)</td>
<td>-10</td>
<td>-4</td>
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<tr>
<td>IIH /EXT_VREF or /EXT_VEE = 5V</td>
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### Instrumentation Amplifier

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<th>SN 568</th>
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<td>Min</td>
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<td>Pre</td>
<td>Post 100k</td>
<td>Pre</td>
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<td>IIL/EXT_VREF or/EXT_VEE = 0V</td>
<td>-12</td>
<td>-6</td>
<td>-1.5</td>
<td>12.39</td>
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<td>Gain Accuracy</td>
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<td>Very stable</td>
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<td>IIL/RESET (5V)</td>
<td>1.5</td>
<td>4</td>
<td>10</td>
<td>4.12</td>
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<tr>
<td>Gain Accuracy</td>
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<td>Very stable</td>
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<td>IIL/RESET (0V)</td>
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### Pre Radiation Specification

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<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Pre</th>
<th>Post 100k</th>
<th>Comment</th>
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<tr>
<td>IIL/EXT_VREF</td>
<td>-12</td>
<td>32</td>
<td>-0.6</td>
<td>mV</td>
<td>19.70</td>
<td>21.19</td>
<td>24.02</td>
<td>26.82</td>
<td>14.84</td>
<td>21.53</td>
<td>22.58</td>
<td>23.29</td>
<td>Up to 7mV increase</td>
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<td>Offset Voltage, Gain = 0.4 16V/3.3V</td>
<td>-2</td>
<td>32</td>
<td>0</td>
<td>mV</td>
<td>20.45</td>
<td>28.54</td>
<td>25.04</td>
<td>33.47</td>
<td>16.50</td>
<td>26.77</td>
<td>22.71</td>
<td>31.96</td>
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<td>Offset Voltage, Gain = 0.4 11.4V/3.3V</td>
<td>-3.5</td>
<td>4.5</td>
<td>1.09</td>
<td>mV</td>
<td>2.32</td>
<td>8.83</td>
<td>2.61</td>
<td>10.14</td>
<td>2.77</td>
<td>9.01</td>
<td>2.28</td>
<td>9.74</td>
<td>Up to 3mV change</td>
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<td>Offset Voltage, Gain = 2 16V/3.3V</td>
<td>-3.5</td>
<td>3.5</td>
<td>-0.96</td>
<td>mV</td>
<td>-0.68</td>
<td>4.20</td>
<td>-0.24</td>
<td>5.44</td>
<td>1.29</td>
<td>5.95</td>
<td>-1.20</td>
<td>3.49</td>
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### Pre Radiation Test Limits

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<th>100kR Post</th>
<th>Pre</th>
<th>100kR Post</th>
<th>Pre</th>
<th>100kR Post</th>
<th>Pre</th>
<th>100kR Post</th>
<th>Comment</th>
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<tbody>
<tr>
<td>Gain Accuracy</td>
<td>0.398</td>
<td>0.402</td>
<td>-</td>
<td>mV</td>
<td>0.3997</td>
<td>0.3997</td>
<td>0.3994</td>
<td>0.3994</td>
<td>0.3995</td>
<td>0.3994</td>
<td>0.3990</td>
<td>0.3990</td>
<td>Very stable</td>
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### Parameters tested but not specified

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<tr>
<th>Parameters</th>
<th>SN 021</th>
<th>SN 070</th>
<th>SN 149</th>
<th>SN 276</th>
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<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Units</td>
<td>Pre</td>
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<td>Instrumentation Amplifier</td>
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<tr>
<td>Offset Voltage, Gain = 0.4 15V/3.3V at CM=5V</td>
<td>-2</td>
<td>32</td>
<td>-0.6</td>
<td>mV</td>
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<tr>
<td>Offset Voltage, Gain = 0.4 11.4V/3.3V at CM=5V</td>
<td>-3.5</td>
<td>4.5</td>
<td>1.09</td>
<td>mV</td>
</tr>
<tr>
<td>Offset Voltage, Gain = 0.4 16V/3.3V at CM=5V</td>
<td>-3.5</td>
<td>3.5</td>
<td>-0.96</td>
<td>mV</td>
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### Programmable Current Source

<table>
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<th>Parameters</th>
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<th>SN 070</th>
<th>SN 149</th>
<th>SN276</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Accuracy, Gain = 2 16V/3.3V at CM=5V</td>
<td>1.992</td>
<td>2.004</td>
<td>1.998</td>
<td>1.998</td>
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<td>Full scale current (doubWt OFF) at VCC=11.4V</td>
<td>1.880</td>
<td>1.940</td>
<td>2.000</td>
<td>mA</td>
</tr>
<tr>
<td>Integral nonlinearity at VCC=11.4V</td>
<td>-7.5</td>
<td>0</td>
<td>7.5</td>
<td>µA</td>
</tr>
<tr>
<td>Differential nonlinearity at VCC=11.4V</td>
<td>-5.0</td>
<td>0</td>
<td>5.0</td>
<td>µA</td>
</tr>
<tr>
<td>Full scale current (doubWt ON) at VCC=11.4V</td>
<td>3710</td>
<td>3840</td>
<td>3950</td>
<td>µA</td>
</tr>
<tr>
<td>Differential nonlinearity at VCC=11.4V</td>
<td>7.148</td>
<td>6.743</td>
<td>7.687</td>
<td>9.441</td>
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<tr>
<td>At DAC=31 at VCC=11.4V</td>
<td>290</td>
<td>300</td>
<td>310</td>
<td>µA</td>
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</table>

### Logic Levels for FPGA Interface I/Os

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Pre Radiation Test Limits</th>
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</thead>
<tbody>
<tr>
<td>Input Logic Threshold at VDD=2.25V</td>
<td>0.7875 1.125 1.463 V</td>
</tr>
<tr>
<td>Input Logic Threshold at VDD=5.5V</td>
<td>1.925 2.725 3.575 V</td>
</tr>
<tr>
<td>Logic Output VOL at 100uA at VDD=2.25V</td>
<td>0.110 0.115 0.108 0.113 0.108 0.113 0.112 0.117 V</td>
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<tr>
<td>Logic Output VOH at 100uA at VDD=5.5V</td>
<td>5.376 5.382 5.369 5.384 5.379 5.385 5.375 5.382 V</td>
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<tr>
<td>Logic Output VOL at 100uA at VDD=5.5V</td>
<td>0.087 0.093 0.087 0.093 0.086 0.092 0.089 0.095 V</td>
</tr>
</tbody>
</table>

### Programable Current Source

<p>| Full scale current (doubWt OFF) at VCC=11.4V                              | 1.911 1.817 1.951 1.861 1.918 1.828 1.934 1.838 mA |
| Integral nonlinearity at VCC=11.4V                                       | 2.447 1.159 2.573 0.842 2.636 0.745 3.550 1.490 µA |
| Differential nonlinearity at VCC=11.4V                                   | 2.401 1.645 2.252 0.850 2.131 0.755 3.749 2.562 µA |
| Full scale current (doubWt ON) at VCC=11.4V                              | 3.767 3.607 3.855 3.694 3.776 3.621 3.795 3.632 µA |
| At DAC=31 at VCC=11.4V                                                   | 296.439 274.537 296.911 277.841 292.852 272.932 302.859 281.240 µA |</p>
<table>
<thead>
<tr>
<th>Parameters</th>
<th>SN 021</th>
<th>SN 070</th>
<th>SN 149</th>
<th>SN276</th>
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<td>Pre Radiation Test Limits</td>
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<tr>
<td>Integral nonlinearity at VCC=11.4V</td>
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<td>Differential nonlinearity at VCC=11.4V</td>
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<td>0.700</td>
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<tr>
<td>Full scale current (doubWt OFF) at VCC=16V</td>
<td>1.880</td>
<td>1.940</td>
<td>2.000</td>
<td>mA</td>
</tr>
<tr>
<td>Integral nonlinearity at VCC=16V</td>
<td>-7.5</td>
<td>0</td>
<td>7.5</td>
<td>μA</td>
</tr>
<tr>
<td>Differential nonlinearity at VCC=16V</td>
<td>-5.0</td>
<td>0</td>
<td>5.0</td>
<td>μA</td>
</tr>
<tr>
<td>Full scale current (doubWt ON) at VCC=16V</td>
<td>3710</td>
<td>3840</td>
<td>3950</td>
<td>mA</td>
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<tr>
<td>Integral nonlinearity at VCC=16V</td>
<td>3710</td>
<td>3840</td>
<td>3950</td>
<td>mA</td>
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<tr>
<td>Pre Radiation Test Limits</td>
<td>290</td>
<td>300</td>
<td>310</td>
<td>μA</td>
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<tr>
<td>Integral nonlinearity at VCC=16V</td>
<td>290</td>
<td>300</td>
<td>310</td>
<td>μA</td>
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<tr>
<td>Differential nonlinearity at VCC=16V</td>
<td>290</td>
<td>300</td>
<td>310</td>
<td>μA</td>
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<tr>
<td><strong>Fixed Threshold Bi-Level Inputs</strong></td>
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<tr>
<td>Threshold – External 0.1V (Rising Voltage) at VCC=15V</td>
<td>0.0</td>
<td>0.1</td>
<td>0.2</td>
<td>V</td>
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<tr>
<td>Threshold Hysteresis – External 0.1V at VCC=15V</td>
<td>0.120</td>
<td>0.110</td>
<td>0.120</td>
<td>0.115</td>
</tr>
<tr>
<td>Threshold – External 4.9V (Rising Voltage) at VCC=15V</td>
<td>4.8</td>
<td>4.9</td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Threshold Hysteresis – External 4.9V at VCC=15V</td>
<td>0.120</td>
<td>0.115</td>
<td>0.120</td>
<td>0.115</td>
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<tr>
<td>Threshold – Internal ref (Rising Voltage) at VCC=11.4V</td>
<td>2.45</td>
<td>2.50</td>
<td>2.55</td>
<td>V</td>
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<tr>
<td>Threshold Hysteresis – Internal reference at VCC=11.4V</td>
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<td>0.114</td>
<td>0.124</td>
<td>0.116</td>
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<tr>
<td>Threshold – External 4.9V (Rising Voltage) at VCC=11.4V</td>
<td>4.8</td>
<td>4.9</td>
<td>5.0</td>
<td>V</td>
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<tr>
<td>Threshold Hysteresis – External 4.9V at VCC=11.4V</td>
<td>0.125</td>
<td>0.115</td>
<td>0.130</td>
<td>0.115</td>
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</table>

<p>| Adjustable threshold Bi-level MUX and DAC                                 |        |        |        |       |
| Threshold DAC Max Output (If input is &gt;=0V during TID at VCC=11.4V        | 4.95   | 5      | 5.05   | V     | 4.990 | 5.013 | 4.990 | 5.012 | 4.980 | 5.014 | 4.990 | 5.019 |
| Hysteresis DAC Max Output (If input is &gt;=0V during TID at VCC=11.4V       | 0.075  | 0.112  | 0.150  | V     | 0.130 | 0.090 | 0.125 | 0.094 | 0.125 | 0.101 | 0.130 | 0.096 |
| Threshold DAC Max Output (If input is VEE/2 during TID)                    | 4.95   | 5      | 5.05   | V     | 4.990 | 4.491 | 4.990 | 4.512 | 4.980 | 4.465 | 4.990 | 4.479 |</p>
<table>
<thead>
<tr>
<th>Parameters</th>
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<th>Max</th>
<th>Units</th>
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<td>SN276</td>
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<td>at VCC=11.4V</td>
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<tr>
<td>Hysteresis DAC Max Output (If input is VEE/2 during TID) at VCC=11.4V</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>V</td>
<td>0.125</td>
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<td>Up to 30% decrease</td>
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<tr>
<td>Threshold DAC=0 Output (If input is &gt;=0V during TID) at VCC=15V</td>
<td>-0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>0.020</td>
<td>0.046</td>
<td>0.020</td>
<td>0.038</td>
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<td>Up to 50mV increase</td>
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<tr>
<td>Hysteresis DAC=0 Output (If input is &gt;=0V during TID) at VCC=15V</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>V</td>
<td>0.125</td>
<td>0.093</td>
<td>0.120</td>
<td>0.096</td>
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<td>Up to 25% decrease</td>
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<tr>
<td>Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=15V</td>
<td>-0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>0.020</td>
<td>-0.479</td>
<td>0.030</td>
<td>-0.464</td>
<td>0.010</td>
<td>-0.508</td>
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<td>Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=15V</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>V</td>
<td>0.120</td>
<td>0.087</td>
<td>0.115</td>
<td>0.084</td>
<td>0.115</td>
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<td>Up to 30% decrease</td>
</tr>
<tr>
<td>Threshold DAC=0 Output (If input is &gt;=0V during TID) at VCC=11.4V</td>
<td>-0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
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<td>Up to 30% decrease</td>
</tr>
<tr>
<td>Hysteresis DAC=0 Output (If input is &gt;=0V during TID) at VCC=11.4V</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>V</td>
<td>0.125</td>
<td>0.093</td>
<td>0.120</td>
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<td>Up to 50mV increase</td>
</tr>
<tr>
<td>Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V</td>
<td>-0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>0.020</td>
<td>-0.482</td>
<td>0.030</td>
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<td>0.010</td>
<td>-0.508</td>
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<td></td>
<td>Up to 25% decrease</td>
</tr>
<tr>
<td>Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V</td>
<td>0.075</td>
<td>0.112</td>
<td>0.150</td>
<td>V</td>
<td>0.120</td>
<td>0.084</td>
<td>0.115</td>
<td>0.082</td>
<td>0.120</td>
<td>0.086</td>
</tr>
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<td></td>
<td></td>
<td>~0.5V decrease</td>
</tr>
</tbody>
</table>