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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 8.0

The following is a summary of the changes made in this revision.

- Updated the document for Evaluation and Splash kit.
- Updated the document for Libero SoC PolarFire v2.3.

1.2 Revision 7.0

The document was updated for Libero® SoC PolarFire v2.2.

1.3 Revision 6.0

The document was updated for Libero SoC PolarFire v2.1.

1.4 Revision 5.0

The following is a summary of the changes made in this revision.

- The document was updated to include IP core.
- Design Requirements, page 2 was edited to add CORERESET_PF details and Figure 3, page 5, JESD204B Interface Design, was updated with CORERESET_PF IP core.

1.5 Revision 4.0

The following is a summary of the changes made in this revision.

- The document is updated to include features and enhancements introduced in the Libero SoC PolarFire v2.0 release.
- Updated the GUI screens and COM port details with respect to the Libero SoC PolarFire v2.0 release.

1.6 Revision 3.0

The following is a summary of the changes made in this revision.

- The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v1.1 SP1 release.
- Information about resource utilization was updated. For more information, see Table 5, page 16.
- List of reference was added. For more information, see Appendix: References, page 29.

1.7 Revision 2.0

The following is a summary of the changes in this revision.

- The document was updated for Libero SoC PolarFire v1.1 release.
- Information about resource utilization was added.

1.8 Revision 1.0

The first publication of this document.
PolarFire FPGA JESD204B Standalone Interface

This document describes the Microsemi JESD204B standalone interface design and how to run the demo on a PolarFire Evaluation or Splash kit. The demo design features:

- CoreJESD204BTX and CoreJESD204BRX IP cores that implement the transmitter and receiver interfaces of the JESD204B standard. These IP cores are easy to integrate with the JESD204B-based data converters to develop high-bandwidth applications such as wireless infrastructure transceivers, software-defined radios, medical imaging systems, and radar and secure communications. They support link widths from x1 to x8, and link rates from 250 Mbps to 12.5 Gbps per lane using subclass 0, 1, and 2.
- PolarFire transceiver interface that can handle data rates ranging from 250 Mbps to 12.5 Gbps. It integrates several functional blocks to support multiple high-speed serial protocols within the FPGA.

The design operates in the loopback mode by sending the CoreJESD204BTX data to the CoreJESD204BRX IP core through one or more transceiver lanes, which are looped back on the board.

For Evaluation kit, two designs are provided:

- SMA-based loopback design that runs at 6.25 Gbps lane rate (with single XCVR lane for TX and RX).
- PCB-based loopback design that which runs at 5 Gbps lane rate (with two XCVR lanes, where one lane is for TX and the other for RX).

For Splash kit, PCB-based loopback design is provided that runs at runs at 5 Gbps lane rate (with single XCVR lane for TX and RX).

For more information about the JESD204B interface design implementation, and all the necessary blocks and IP cores instantiated in Libero SoC PolarFire, see Demo Design, page 3.

The JESD204B design can be programmed using any of the following options:

- **Using the stp file**: To program the device using the stp file provided along with the design files, see Programming the Device Using FlashPro, page 21.
- **Using Libero SoC PolarFire**: To program the device using Libero SoC PolarFire, see Libero Design Flow, page 14. Use this option when the demo design is modified.

### 2.1 Design Requirements

The following table lists the resources required to run the demo.

**Table 1 • Design Requirements**

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>Windows 7, 8.1, or 10</td>
</tr>
<tr>
<td>Hardware</td>
<td></td>
</tr>
<tr>
<td>PolarFire Evaluation Kit (MPF300-EVAL-KIT)</td>
<td>Rev D or later</td>
</tr>
<tr>
<td>Or</td>
<td></td>
</tr>
<tr>
<td>PolarFire Splash Kit (MPF300-Splash-KIT-ES)</td>
<td>Rev 2 or later</td>
</tr>
<tr>
<td>2 SMA-to-SMA cables (not provided with the kit)</td>
<td>Required only for Evaluation kit.</td>
</tr>
<tr>
<td>Optional: User can also test with on board loop back</td>
<td></td>
</tr>
<tr>
<td>Software</td>
<td></td>
</tr>
<tr>
<td>FlashPro</td>
<td>v2.3</td>
</tr>
<tr>
<td>Libero SoC PolarFire</td>
<td>v2.3</td>
</tr>
</tbody>
</table>
2.2 Prerequisites

Before you start:

1. Download and install Libero SoC PolarFire v2.3 on the host PC from the following location.
   https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polar-fire#downloads
   The latest versions of ModelSim and Synplify Pro are included in the Libero SoC PolarFire installation package.

   Note: A Libero Gold license is required to evaluate your designs on the MPF300 device.

2. Download the demo design files from the following location:
   For Evaluation Kit:
   http://soc.microsemi.com/download/rsc/?f=mpf_dg0755_eval_liberosocpolarfirev2p3_df
   For Splash Kit:
   http://soc.microsemi.com/download/rsc/?f=mpf_dg0755_spl_liberosocpolarfirev2p3_df

2.3 Demo Design

The PolarFire JESD204B demo design interfaces JESD204B-compliant data converters with PolarFire devices. In this design:

1. The DATA_HANDLE_0 block interfaces with the GUI. The GUI enables the selection of PRBS or waveform input.

2. The DATA_HANDLE_0 block passes the input selection to the DATA_GENERATOR_0 block, which generates and sends the corresponding input data to the CoreJESD204BTX IP core.

3. The CoreJESD204BTX IP core performs the JESD204B transmitter functions based on the configuration, and sends the data to the PF_XCVR (transceiver) IP core.

4. The encoded data is received by the CoreJESD204BRX IP core because the TX and RX lanes of the PF_XCVR block are looped back. The CoreJESD204BRX IP core performs the JESD204B receiver functions based on the configuration, and sends the data to the GUI for viewing the selected input.

5. The JESD204B GUI displays data and status received from the JESD204BRX IP.

Note: When a data error or link error is selected on the GUI, the error generator block generates that error and displays it on the GUI.
**Figure 1** • Block Diagram of SMA and PCB Loop Back (Evaluation and Splash kit)

1. On SPLASH kit, Lane 1 is used.
2. On Evaluation kit the loopback is SMA-based. On SPLASH kit, the loopback is PCB-based.

**Figure 2** • Block Diagram of PCB Loop Back (Evaluation kit)
2.3.1 Design Implementation

This section shows the Libero design implementation, describes the IPs used and their configurations, and important input/output signals.

The following figure shows the design implementation of JESD204B interface in Libero.

**Figure 3 • JESD204B Interface Design**

Note: The Evaluation and Splash kit designs are the same, except for the transceiver configuration.

As shown in the figure, the design consists of the following parts:

1. Transmit Part, page 5
2. Receive Part, page 6

2.3.1.1 Transmit Part

The following IPs form the transmit part of the design:

1. **DATA_GENERATOR**—This block implements a PRBS generator and a waveform generator. The PRBS generator generates PRBS7, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode implemented in the PRBS generator, inserts an error into the PRBS sequence. The waveform generator generates sine, sawtooth, triangle, and square waveforms. The data generator feeds the 64-bit test pattern to the JESD204BTX core, which then transmits data to the transceiver.

2. **CoreJESD204BTX**—This IP is the transmitter interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
   - Encoder: Removed
   - Data Width: 32
   - Serdes Mode: 1
   - Scrambling: Disabled
   - Device Subclass version: Disabled
   - JESD204 version: JESD204B
   - No. of Lanes: 1
   - No. of octets per frame: 2
   - No. of frames for multi-frame: 9
   - No. of multi-frames in ILA sequence: 4

The Link Configuration of CoreJESD204BTX is as follows:
   - No. of converters per device: 2
   - Converter resolution: 16
   - Total No. of bits per sample: 16
   - No. of samples per converter per frame cycle: 1
For more information about CoreJESD204BTX, see CoreJESD204BTX Handbook.

3. **ERR_GEN_0**—This block generates link errors by sending random data between CoreJESD204BTX and PF_XCVR, when the link error generation is selected on the GUI.

4. **DATA_HANDLE_0**—This block receives the input data selection and link or data error generation information from the GUI. This block also sends the data output received from the CoreJESD204BRX core and the data or link status error to the GUI for viewing.

5. **PF_XCVR**—This is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps. The following points summarize the configuration of the transceiver interface:
   - For the SMA loopback design, the transceiver block (PF_XCVR) is configured in 8b10b mode with a CDR reference clock of 156.25 MHz to support 6.25 Gbps data rate.
   - For PCB loop back demo, the transceiver block (PF_XCVR) is configured for two lanes in 8b10b mode with a CDR reference clock of 125 MHz to support 5 Gbps data rate.
   The PolarFire transmit PLL (PF_TX_PLL) is used to send the reference clock feed to the transceiver. The dedicated reference clock (PF_XCVR_REF_CLK) drives the PF_TX_PLL to generate the desired output clock for the 6.25 Gbps or 5 Gbps data rate.

   **Note:** For the Splash kit design, XCVR is configured for single lane in 8b10b mode with 5 Gbps data rate.

### 2.3.1.2 Receive Part

The following IPs form the receive part of the design:

1. **CoreJESD204BRX**—This is the receiver interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
   - Decoder: Removed
   - Data Width: 32
   - Serdes Mode: 1
   - Scrambling: disabled
   - Device Subclass Version: subclass 0
   - JESD204 version: JESD204B
   - No. of Lanes (L+1): 1
   - checksum calculation type: Octet
   - Frame Alignment Correction: Enabled
   - Link Configuration Error: Enabled
   - RAM Implementation: In FPGA Fabric
   The CoreJESD204BRX and CoreJESD204BTX IPs have the same Link configuration. For more information about CoreJESD204BRX, see CoreJESD204BRX Handbook.

2. **prbs_checker_0**—This block receives the 64-bit data from the CoreJESD204BRX IP core and checks if the received data is correct. It generates an error count and a status signal, which are sent to the GUI for status indication. The data checker only checks the PRBS sequences of the data generator.

3. **LED_DEBUG_BLK_0**—This block is used to debug the JESD204B link status and other errors. When the link is up, LEDs 4, 5, 6, 7, 8, 9 glow and LEDs 10 and 11 do not glow (with DIP 1, 2, 3, and 4 set low on the SW11 dip slide switch).

   There are two instances of PF_URAM blocks, the PF_URAM_0 block stores the JESD204B link status before sending it to the GUI. The PF_URAM_1 block stores the data received from the CoreJESD204BRX before sending the data to the GUI.

   PF_INIT_MONITOR and CoreReset_PF IPs handle the reset mechanism as summarized in the following points.
   - When the DEVICE_INIT_DONE signal from Init_monitor block goes high, the transceiver is completely configured. This signal is anded with ARST_N signal to get proper reset signal for the design.
   - CoreReset_PF synchronizes resets to the respective user-specified clock domain. This ensures that when the assertion is asynchronous, the negation is synchronous to the clock.
The following table lists the important I/O signals of the JESD204B design.

### Table 2 • I/O Signals of the JESD204B Design

<table>
<thead>
<tr>
<th>Signal Description</th>
<th>Input Signals</th>
<th>Output Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver differential inputs of the transceiver</td>
<td>LANE0_RXD_P and LANE0_RXD_N</td>
<td>LANE0_TXD_P and LANE0_TXD_N</td>
</tr>
<tr>
<td>Reset signal obtained from the SW6 push-button switch on the board</td>
<td>ARST_N</td>
<td>LED_OUT[7:0] LEDs 4, 5, 6, 7, 8, 9, 10, and 11 on the board that indicate whether link is up or down</td>
</tr>
<tr>
<td>Receiver of UART interface</td>
<td>RX</td>
<td>TX Transmitter of the UART interface</td>
</tr>
<tr>
<td>Differential reference clock obtained from the on-board 156.25 MHz oscillator</td>
<td>REF_CLK_PAD_P_0 and REF_CLK_PAD_N_0</td>
<td></td>
</tr>
<tr>
<td>Signal mapped to DIPs 1, 2, 3, 4 of SW11 dip slide switch used to debug the status and errors</td>
<td>SEL_IN[3:0]</td>
<td></td>
</tr>
</tbody>
</table>

#### 2.4 Clocking Structure

In the evaluation kit design, the on-board 156.25 MHz crystal oscillator (for SMA loopback design) and the 125 MHz crystal oscillator (for PCB loop back design) drives the XCVR reference clock, which provides clock to the DATA_GENERATOR, CoreJESD204BTX, ERR_GEN, CoreJESD204BR, LED_DEBUG, PRBS_CHECKER, USRAM 0 & 1, COREUART, and UART_IF blocks.

For the Splash kit design, the on-board 125 MHz crystal oscillator drives the XCVR reference clock. The XCVR reference clock provides clock to the DATA_GENERATOR, CoreJESD204BTX, ERR_GEN, CoreJESD204BR, LED_DEBUG, PRBS_CHECKER, USRAM 0 & 1, COREUART, and UART_IF blocks.

**Note:** If there is any change in the data rate or XCVR reference clock of the transceiver; reconfigure COREUART.
Figure 4 • Clocking Structure

The following table lists all of the clocks used in the design, their source, frequency, and purpose.

Table 3 • Clocks

<table>
<thead>
<tr>
<th>Clock Name</th>
<th>Source</th>
<th>Frequency</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAB_REF_CLOCK</td>
<td>Reference clock from the oscillator</td>
<td>156.25 MHz/125 MHz*</td>
<td>Clock for the fabric logic (UART)</td>
</tr>
<tr>
<td>REF_CLK</td>
<td>Reference clock from the oscillator</td>
<td>156.25 MHz/125 MHz*</td>
<td>CDR reference clock for the transceiver</td>
</tr>
<tr>
<td>LANE0_TX/RX_CLK_R</td>
<td>Transceiver generated TX/RX clock</td>
<td>156.25 MHz/125 MHz*</td>
<td>Clock for the transmit and receive modules in the fabric.</td>
</tr>
</tbody>
</table>

*For Evaluation kit, 156.25 MHz oscillator is used for the SMA loopback design and 125 MHz oscillator is used for the PCB loopback design. For SPLASH kit, 125 MHz oscillator is used.

1. For SMA and PCB loopback designs (Evaluation kit), the frequency is 156.25 MHz and 125 MHz respectively. For the Splash kit design the frequency is 125 MHz.

2.5 Reset Structure

The DEVICE_INIT_DONE and the ARST_N signal mapped to K22 (evaluation board) and N4 (Splash kit) initiates the reset signal (FABRIC_RESET_N) from the res_syn_0 block, which synchronizes with the TX clock of the PF_XCVR block to reset the TX modules of the design.

A two-stage synchronizer (D Flip-Flop) synchronizes the reset of the RX modules with the RX clock of PF_XCVR. Figure 5, page 9 shows the reset structure.
2.6 Simulating the PolarFire JESD204B Design

Before you start:

1. Start Libero SoC PolarFire and select Project -> Tool Profiles....
2. In the Tool Profiles window, select Synthesis and Simulation on the Tools panes and select the latest active installation directory paths for these two tools.
3. In the Project menu, click Open Project. The Open Project dialog box opens.
4. Browse the design files folder, `mpf_dg0755 EVAL LiberoProject\PF_JESD204B_SA\LiberoProject\PF_JESD204B_SA`, and select the file. Then, click Open.

The PolarFire JESD204B project opens in Libero SoC PolarFire.

Note: To simulate the Splash kit design, browse the `mpf_dg0755 SPL LiberoProject\PF_JESD204B_SA` folder.

5. Download the following IP cores from Libero SoC PolarFire -> Catalog:
   - CoreJESD204BTX
   - CoreJESD204BRX
   - PF_XCVR
   - PF_TX_PLL
   - PF_XCVR_REF_CLK
   - PF_URAM
   - COREUART
   - PF_INIT_MONITOR

A testbench is provided to simulate the JESD204B PRBS pattern and waveform selection. Figure 6, page 10 shows the interaction between testbench and the design.
The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and waveform input (sine wave, sawtooth wave, triangle wave, and square wave). It also monitors the JESD204B output status signals (SYNC_N, ALIGNED, and CGS_ERR) for the verification of JESD204B phases, and PRBS checker output status signals O_BAD and O_ERROR[4:0]. The following table lists the simulation signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Signals</strong></td>
<td></td>
</tr>
<tr>
<td>P_W_SEL</td>
<td>Input to select the PRBS pattern or waveform</td>
</tr>
<tr>
<td>WAVE_SEL[1:0]</td>
<td>Input to select the type of waveform</td>
</tr>
<tr>
<td>PRBS_SEL[1:0]</td>
<td>Input to select the type of PRBS pattern</td>
</tr>
<tr>
<td>ERR_EN</td>
<td>Input to enable error in the PRBS pattern</td>
</tr>
<tr>
<td>SYSRESET</td>
<td>Active low reset signal</td>
</tr>
<tr>
<td>SYSCLK</td>
<td>• 156.25 MHz generated clock for external loop back design</td>
</tr>
<tr>
<td></td>
<td>• 125 MHz generated clock for internal loop back design</td>
</tr>
<tr>
<td><strong>Output Signals</strong></td>
<td></td>
</tr>
<tr>
<td>TB_DATA_OUT</td>
<td>Output data from CoreJESD204BRX</td>
</tr>
<tr>
<td>TB_RX_SOMF</td>
<td>SOMF_0[3:0] signal received from the CoreJESD204BRX block</td>
</tr>
</tbody>
</table>

1. In the PCB loopback design for Evaluation kit, Lane 2 and 3 are looped back.
In the Design Flow tab, double-click Simulate under Verify Pre-Synthesized Design to simulate the design. The Simulate option is highlighted in Figure 7, page 11.

Figure 7 • Simulating the Design

When the simulation is initiated, ModelSim compiles all the design source files, runs the simulation, and configures the waveform viewer to show the simulation signals.
2.6.1 Simulation Flow

The following steps describe the JESD204B testbench simulation flow:

1. At the start, the NSYSRESET signal resets all of the components.
2. After the transceiver block is initialized, the TB_RX_READY signal is asserted high.
3. The JESD204BRX issues a synchronization request by driving the TB_SYNC_N pin low.
4. The JESD204BRX block checks the k28.5 characters transmitted by the JESD204BTX block.
5. The CGS and ILA (Initial Lane Alignment) phase starts after the TB_SYNC_N signal is asserted high.
6. The testbench checks whether the CGS_ERR signal asserts low or not, and completes the Code Group Synchronization phase.
7. The JESD204BRX link asserts the TB_SYNC_N signal to high.
8. After the successful completion of the CGS phase, the JESD204BTX block starts the ILA sequence by transmitting four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2
9. The JESD204BRX link starts receiving four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2
   The ILA phase test passes if all JESD204BRX DATA_OUT is properly received with frame alignment.
10. After successful completion of the ILA phase, the JESD204BTX block enters into the data phase.
11. In the data phase, the following data is fed to the JESD204BTX block:
    - PRBS7, PRBS15, PRBS23, and PRBS31 using the PRBS generator.
12. Sine, Square, Saw, and triangular waves are generated from the waveform generator.
13. The data checker checks the received PRBS pattern against the expected PRBS pattern.
14. The waveform output can be viewed in the Simulation window on corresponding wave selection as shown in Figure 9, page 13.
15. If no error is detected by the data checker, the testbench issues a TESTBENCH PASSED message stating that the simulation was successful. If an error is detected, the testbench issues a TESTBENCH FAILED message to indicate that the testbench has failed.

While the simulation is running, you can see the status of the test cases in the Transcript window of ModelSim, as shown in the following figure.
After simulation, the **Waveform** window displays the simulation waveforms as shown in the following figure.

**Figure 9 • Simulation Waveform Window**
This chapter describes the Libero design flow, which involves the following steps:

- Synthesize, page 14
- Place and Route, page 15
- Verify Timing, page 17
- Generate Bitstream, page 17
- Device Programming, page 17

The following figure shows these options in the Design Flow tab.

3.1 Synthesize

To synthesize the JESD204B design:

1. Double-click Synthesize from the Design Flow tab. When the synthesis is successful, a green tick mark appears as shown in the preceding figure.
2. Right-click Synthesize and select View Report to view the synthesis report and log files in the Reports tab.
3.2 Place and Route

For Evaluation kit SMA loopback design, the transceiver is placed in Quad 2, Lane 0 (as shown in Figure 11, page 15) and for the PCB loopback design, the transceiver is placed in Quad 2, Lane 2 & Lane 3 (as shown in Figure 12, page 15). For more information about the PolarFire Transceiver, see UG0677: PolarFire FPGA Transceiver User Guide.

For the Splash kit design, the transceiver is placed in Quad 1, Lane 1 as shown in Figure 13, page 16.

To place and route the JESD204B design:

1. Use I/O Editor from Libero SoC PolarFire -> Constraint Manager and place TX_PLL, XCVR_REF_CLK, and PF_XCVR as shown in Figure 11, page 15 or Figure 12, page 15.

*Figure 11 • I/O Editor XCVR View (SMA Loopback Design)*

*Figure 12 • I/O Editor XCVR View (PCB Loopback Design)*
2. Click **Save** to save the placement. The PDC file required for placing and routing the design is generated.

3. Double-click **Place and Route** from the **Design Flow** tab.
   When place and route is successful, a green tick mark appears as shown in the Figure 10, page 14.

4. Right-click **Place and Route** and select **View Report** to view the place and route report and log files in the **Reports** tab.

### 3.2.1 Resource Utilization

The following tables list the resource utilization of the JESD204B loopback design after place and route. These values may vary slightly for different Libero runs, settings, and seed values. For IP-wise utilization, see the respective handbooks.

**Table 5 • Resource Utilization (SMA Loopback Evaluation Kit)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>5437</td>
<td>299544</td>
<td>1.82</td>
</tr>
<tr>
<td>DFF</td>
<td>4768</td>
<td>299544</td>
<td>1.59</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>510</td>
<td>0.00</td>
</tr>
<tr>
<td>Logic Element</td>
<td>7488</td>
<td>299544</td>
<td>2.50</td>
</tr>
</tbody>
</table>

**Table 6 • Resource Utilization (PCB Loopback Evaluation Kit)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>5422</td>
<td>299544</td>
<td>1.81</td>
</tr>
<tr>
<td>DFF</td>
<td>4769</td>
<td>299544</td>
<td>1.59</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>510</td>
<td>0.00</td>
</tr>
<tr>
<td>Logic Element</td>
<td>7497</td>
<td>299544</td>
<td>2.50</td>
</tr>
</tbody>
</table>

**Table 7 • Resource Utilization (Splash kit)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>5406</td>
<td>299544</td>
<td>1.80</td>
</tr>
</tbody>
</table>
3.3 Verify Timing

To verify timing:

1. Double-click **Verify Timing** from the **Design Flow** tab.
   When the design successfully meets the timing requirements, a green tick mark appears as shown in **Figure 10**, page 14.
2. Right-click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

3.4 Generate Bitstream

To generate the bitstream:

1. Double-click **Generate Bitstream** from the **Design Flow** tab.
   When the bitstream is successfully generated, a green tick mark appears as shown in **Figure 10**, page 14.
2. Right-click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

3.5 Device Programming

After generating the bitstream, the PolarFire device must be programmed. To program the device, see any of the following sections based on the kit used.

- Program the Device on Evaluation kit, page 17
- Program the Device on Splash Kit, page 19

3.5.1 Programming the Device on Evaluation kit

Follow these steps to program the PolarFire device on Evaluation kit:

1. Ensure that the jumper settings on the board are same as listed in the following table.

### Table 7 • Resource Utilization (Splash kit) (continued)

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFF</td>
<td>4769</td>
<td>299544</td>
<td>1.59</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>242</td>
<td>0</td>
</tr>
<tr>
<td>Logic Element</td>
<td>7460</td>
<td>299544</td>
<td>2.49</td>
</tr>
</tbody>
</table>

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the host PC to the J5 (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.

### Table 8 • Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J18, J19, J20, J21, J22</td>
<td>Close pin 2 and 3 for programming the PolarFire FPGA through FTDI</td>
</tr>
<tr>
<td>J28</td>
<td>Close pin 1 and 2 for programming through the on-board FlashPro5</td>
</tr>
<tr>
<td>J26</td>
<td>Close pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J27</td>
<td>Close pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J4</td>
<td>Close pin 1 and 2 for manual power switching using SW3</td>
</tr>
<tr>
<td>J12</td>
<td>Close pin 3 and 4 for 2.5 V</td>
</tr>
</tbody>
</table>
5. For external loop back demo, connect **TXN** to **RXN** and **TXP** to **RXP** using the 2 SMA to SMA cables as shown in the following figure.

   The following figure shows the board setup for external loop back demo.

   **Figure 14 • Board Setup (Evaluation Kit)**

   ![Board Setup (Evaluation Kit)](image)

   When the board is powered up, power supply LEDs DS3 to DS14 glow. For more information about LEDs on the PolarFire Evaluation Board, see *UG0747: PolarFire FPGA Evaluation Kit User Guide*.

   **Note:** For PCB loop back demo, SMA cables are not required. User can skip Step 5.

6. Double-click **Run PROGRAM Action** from the **Libero > Design Flow** tab.

   Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.
When the device is successfully programmed, a green tick mark appears as shown in the following figure. See Running the Demo, page 22 to run the JESD204B standalone demo.

**Figure 15 • Programming the Device**

3.5.2 Programming the Device on Splash Kit

Follow these steps to program the PolarFire device on Splash kit:

1. Ensure that the jumper settings on the board are same as listed in the following table.

**Table 9 • Jumper Settings**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>J11</td>
<td>Jumper to select either external JTAG or on-board FTDI chip for programming the device.</td>
<td>Closed</td>
</tr>
<tr>
<td>J3</td>
<td>Jumper to select the core voltage.</td>
<td>Open</td>
</tr>
<tr>
<td>J10</td>
<td>Jumper to select either FTDI chip or external SPI Flash for programming the device.</td>
<td>Open</td>
</tr>
</tbody>
</table>

2. Connect the power supply cable to the J2 connector on the board.
3. Connect the USB cable from the host PC to the J1 (FTDI port) on the board.
4. Power on the board using the SW1 slide switch.
When the board is powered up, power supply LEDs 1 to 4 glow. For more information about LEDs on the PolarFire Splash Board, see *UG0786: PolarFire FPGA Splash Kit User Guide*.

5. Double-click **Run PROGRAM Action** from the Libero **Design Flow** tab.

Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.

When the device is successfully programmed, a green tick mark appears as shown in Figure 15, page 19.

After programming the device, see **Running the Demo**, page 22.
This chapter describes how to program the PolarFire device with the stp programming file using FlashPro. The stp file is available at the following design files folder location:

```
mpf_dg0755_eval_liberosocpolarfirev2p3_df\Programming_file
or
mpf_dg0755_spl_liberosocpolarfirev2p3_df\Programming_file
```

Follow these steps:

1. Connect the jumpers and set up the PolarFire Evaluation Kit Board as described in steps 1 to 5 of Device Programming, page 17 and shown in Figure 14, page 18.

2. On the host PC, start the FlashPro software.

3. Click New Project to create a new project. In the New Project window, do the following, and click OK:
   - Enter a project name.
   - Select Single device as the programming mode.
   - Click Configure Device.
   - Click Browse, and select the PF_JESD204B_SA.stp file from the Load Programming File window.

4. From the View Programmer pane, select the on-board FlashPro5 programmer as shown in the following figure.

5. Click Program to program the device.

   The Programmer List Window in the FlashPro, shows the Programmer Name, Programmer Type, Port, Programmer Status, and the Programmer Enabled information.

   When the device is programmed successfully, a Run Program PASSED status is displayed. The device is successfully programmed. See Running the Demo, page 22 to run the JESD204B standalone demo.
Running the Demo

This chapter describes how to install and use the JESD204B GUI to select the test patterns and monitor the loopback data. The GUI enables the selection of different PRBS test patterns as input, and displays the JESD204B status signals and PRBS status received from the board. The Waveform tab displays the output waveform samples received from the board for each waveform selected as input. The following procedure assumes that:

1. The PolarFire Evaluation or Splash board is connected
2. The PolarFire FPGA is programmed with the JESD204B design

To run the JESD204B demo:

1. Install the JESD204B_GUI application (setup.exe) from the following design files folder:
   mpf dg0755_eval_liberosocpolarfirev2p3_df\GUI
   or
   mpf dg0755_spl_liberosocpolarfirev2p3_df\GUI
2. Double-click the JESD204B_GUI application from the installation directory to start the GUI application.
3. Select the COM port number that is detected, to configure the serial port.

Note: In Device Manager on the host PC, note the COM port associated with the USB serial converter C. To determine the COM port, check the Location field in the properties of each COM port.

The following table lists the status signals displayed in the JESD204B GUI.

<table>
<thead>
<tr>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Host Connection</td>
<td>Status of the UART communication</td>
</tr>
<tr>
<td>Link Status</td>
<td>Communication link status between TX and RX</td>
</tr>
<tr>
<td>SYNC_N</td>
<td>Signal which indicates the JESD link status</td>
</tr>
<tr>
<td>ALIGNED</td>
<td>Indicates that all transceiver lanes are aligned</td>
</tr>
<tr>
<td>RX VALID</td>
<td>Indicates that the Rx data is valid. In 8b10b mode, the RX VAL is qualified, comma alignment has occurred and the CDR is locked.</td>
</tr>
<tr>
<td>PRBS status</td>
<td>Indicates the occurrence of PRBS error. If green tick mark then no PRBS error occurred</td>
</tr>
<tr>
<td>Error count</td>
<td>Number of errors that occurred during PRBS check</td>
</tr>
<tr>
<td>CGS_ERR</td>
<td>Indicates status of the code group synchronization error. If green tick mark then no CGS error occurred</td>
</tr>
<tr>
<td>NIT_ERR</td>
<td>Indicates the “not in table” error. If green tick mark then no NIT error occurred</td>
</tr>
<tr>
<td>DISP_ERR</td>
<td>Indicates the disparity error. If green tick mark then no DISP error occurred</td>
</tr>
<tr>
<td>LINK_CD_ERR</td>
<td>Indicates a link configuration data mismatch error. If green tick mark then no LINK_CD error occurred</td>
</tr>
</tbody>
</table>
4. Click Connect to connect the GUI to the board through the selected port, as shown in the following figure.

**Figure 18 • Selecting COM Port and Connecting**

<table>
<thead>
<tr>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCC_ERR</td>
<td>Indicates an “unexpected control character” error. If green tick mark then no UCC error occurred</td>
</tr>
</tbody>
</table>

After successfully connecting, the Host Connection status changes to a green tick mark as shown in the following figure.
5. Select the pattern to be transmitted using the **Input selection** drop-down and click **START**. The following figure shows the PRBS7 selection.

**Figure 19 • Host Connection Status**

**Figure 20 • PRBS7 Input Selection**

**Note:** Port numbers may vary. Select the correct port number from the list.
The selected pattern is sent over the serial transmit link. The looped back data is received by the receiver and checked for errors. The status can be monitored using the status signals on the GUI at any time as shown in the following figure.

Figure 21 • Link Status and JESD204B Status

6. Click Generate Data Error to generate error in the PRBS data and observe the error status using PRBS Status and Error Count as shown in the following figure.

Figure 22 • Generate Data Error
7. Click **Clear Error** to stop generate error in the PRBS data and observe that **PRBS Status** turns green, and the **Error Count** is zero as shown in the following figure.

*Figure 23 • Clear Data Error*

![Clear Data Error Diagram]

8. Click **Generate Link Error** to generate error between the CoreJESD204BTX and the transceiver lane and observe Link Status, SYNC_N, Aligned, RX VALID, DISP_ERR, and CGS_ERROR indicators turn red as shown in the following figure.

*Figure 24 • Generating Link Error*

![Generating Link Error Diagram]

9. Click **Clear Error** to stop generating the link error and observe the **Link Status** and JESD204B status signals change to green tick marks as shown in the following figure.
10. Select **Triangle** from the **Input Selection** drop-down to change the pattern. The selected pattern is sent over the serial transmit link and received by the CoreJESD204BRX. The status can be monitored using the status signals on the GUI.
11. Click the **Waveform** tab to view the Triangle waveform received from CoreJESD204BRX as shown in the following figure.

*Figure 26 • Triangle Waveform*

![Triangle Waveform Graph]

12. Click **Stop** to end the demo and close the GUI.
This section lists documents that provide more information about the JESD204B standard and IP cores used in the demo design.

- For information about the JESD204B interface standard, visit the JEDEC website.
- For information about PolarFire transceiver blocks, PF_TX_PLL, and PF_XCVR_REF_CLK, see UG0677: PolarFire FPGA Transceiver User Guide.
- For more information about PF_URAM(PF Micro SRAM), see UG0680: PolarFire FPGA Fabric User Guide.
- For more information about CoreJESD204BTX, see CoreJESD204BTX Handbook.
- For more information about CoreJESD204BRX, see CoreJESD204BRX Handbook.
- For more information about Libero, ModelSim, and Synplify, see the Microsemi Libero SoC PolarFire web page.