Figures

Figure 1 PCIe Demo Design Top-Level Block Diagram .................................................. 4
Figure 2 DMA0 – Example of SG DMA Operation ......................................................... 6
Figure 3 DMA1 – Example of SG DMA Operation ........................................................ 7
Figure 4 PCIe EndPoint Reference Design ................................................................. 8
Figure 5 PCIe_EP SmartDesign .................................................................................... 9
Figure 6 PCIe_TL_CLK SmartDesign ......................................................................... 10
Figure 7 CoreDMA_IO_CTRL SmartDesign ............................................................... 10
Figure 8 UART SmartDesign .................................................................................... 10
Figure 9 AXI_to_APB SmartDesign .......................................................................... 11
Figure 10 Clocking Structure .................................................................................. 12
Figure 11 Reset Structure ....................................................................................... 13
Figure 12 Simulating the Design .............................................................................. 14
Figure 13 Simulation Transcript Window .................................................................... 15
Figure 14 Simulation Waveform Window .................................................................. 15
Figure 15 Simulation Waveform Window .................................................................. 15
Figure 16 I/O Editor—XCVR View ........................................................................... 17
Figure 17 I/O Editor—DDR3 Memory View ................................................................. 17
Figure 18 I/O Editor—DDR4 Memory View (For Evaluation Kit) .............................. 17
Figure 19 Design Flow ............................................................................................. 18
Figure 20 Board Setup ............................................................................................ 19
Figure 21 Board Setup ............................................................................................ 20
Figure 22 Programming the Device ........................................................................... 20
Figure 23 Installing PCIe Demo Application ............................................................. 22
Figure 24 Successful Installation of PCIe Demo Application ......................................... 22
Figure 25 PolarFire Evaluation Kit Setup for Host PC .................................................. 23
Figure 26 PolarFire Splash Kit Setup for Host PC ....................................................... 23
Figure 27 Device Manager ........................................................................................ 24
Figure 28 Update Driver Software ........................................................................... 24
Figure 29 Browse for Driver Software ...................................................................... 24
Figure 30 Browse for Driver Software Continued ..................................................... 25
Figure 31 Windows Security ..................................................................................... 25
Figure 32 Successful Driver Installation .................................................................... 25
Figure 33 Device Manager—PCIe Device Detection .................................................. 26
Figure 34 PCIe EndPoint Demo Application ............................................................... 26
Figure 35 Device Info ............................................................................................... 27
Figure 36 Demo Controls—Continued ...................................................................... 27
Figure 37 Configuration Space .................................................................................. 28
Figure 38 PCIe BAR2 Memory Access—LSRAM ...................................................... 28
Figure 39 Continuous DMA Operations with DMA Transfer Type Selection as Both PC and LSRAM ... 29
Figure 40 Continuous DMA Memory Test—Memory Test Successful ....................... 30
Figure 41 Device Manager—UART Ports ................................................................. 31
Figure 42 UART—DMA Operations .......................................................................... 32
Figure 43 UART—Memory Test ................................................................................ 33
Figure 44 DDR4 Configurator—Evaluation Kit ........................................................... 37
Figure 45 DDR4 Configurator—Splash Kit ................................................................. 38
Figure 46 DDR4 Configurator—Memory Initialization ................................................ 39
Figure 47 DDR4 Configurator—Memory Timing ....................................................... 40
Figure 48 DDR4 Configurator—Controller ............................................................... 41
Figure 49 DDR4 Configurator—Misc ....................................................................... 41
## Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 1</td>
<td>Design Requirements</td>
<td>3</td>
</tr>
<tr>
<td>Table 2</td>
<td>Resource Utilization—Evaluation Kit</td>
<td>16</td>
</tr>
<tr>
<td>Table 3</td>
<td>Resource Utilization—Splash Kit</td>
<td>16</td>
</tr>
<tr>
<td>Table 4</td>
<td>Jumper Settings</td>
<td>19</td>
</tr>
<tr>
<td>Table 5</td>
<td>Jumper Settings</td>
<td>20</td>
</tr>
<tr>
<td>Table 6</td>
<td>PolarFire Throughput Summary—Continuous DMA Mode</td>
<td>34</td>
</tr>
<tr>
<td>Table 7</td>
<td>PolarFire Throughput Summary—SGDMA Mode</td>
<td>34</td>
</tr>
<tr>
<td>Table 8</td>
<td>PolarFire Throughput Summary—Core DMA Mode</td>
<td>34</td>
</tr>
<tr>
<td>Table 9</td>
<td>PolarFire Throughput Summary—Continuous DMA Mode</td>
<td>35</td>
</tr>
<tr>
<td>Table 10</td>
<td>PolarFire Throughput Summary—SGDMA Mode</td>
<td>35</td>
</tr>
<tr>
<td>Table 11</td>
<td>PolarFire Throughput Summary—Fabric Core DMA Mode</td>
<td>35</td>
</tr>
</tbody>
</table>
1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.0
Merged Splash kit related content and updated the document for Libero SoC PolarFire v2.3 release.

1.2 Revision 6.0
The following is a summary of the changes made in revision 6.0 of this document:
• The document was updated for Libero SoC PolarFire v2.2 release.
• Information about DDR power measurement was added. See Appendix: DDR3 and DDR4 Power Measurement, page 36.

1.3 Revision 5.0
The document was updated for Libero SoC PolarFire v2.1 release.

1.4 Revision 4.0
The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v2.0 release.

1.5 Revision 3.0
The following is a summary of the changes made in revision 3.0 of this document:
• The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v1.1 SP1 release.
• Information about setting up the device and running the demo was added, see Programming the Device Using FlashPro, page 21, and Running the Demo, page 22.
• List of reference was added. For more information, see Appendix: References, page 42.

1.6 Revision 2.0
The following is a summary of the changes in revision 2.0 of this document:
• The document was updated for Libero SoC PolarFire v1.1 release.
• Information about resource utilization was added. For more information, see Resource Utilization, page 16.

1.7 Revision 1.0
The first publication of this document.
Microsemi PolarFire® FPGAs contain fully integrated PCIe EndPoint and Root Port subsystems with optimized embedded controller blocks that use the physical layer interface (PHY) of the transceiver. Each PolarFire device includes two embedded PCIe subsystem (PCIESS) blocks that can be configured either separately, or as a pair, using the PCIESS configurator in the Libero® SoC PolarFire software.

The PCIESS is compliant with the PCI Express Base Specification, Revision 3.0 with Gen1/2 speed. It implements memory-mapped advanced microcontroller bus architecture (AMBA) advanced extensible interface 4 (AXI4) access to the PCIe space, and the PCIe access to the memory-mapped AXI4 space. For more information, see UG0685: PolarFire FPGA PCI Express User Guide.

The DDR subsystem addresses memory solution requirements for a wide range of applications with varying power consumption and efficiency levels. The subsystem can be configured to support DDR4, DDR3, DDR3L, and LPDDR3 memory devices. The subsystem is intended for accessing DDR memories for applications that require high-speed data transfers and code execution. For more information DDR memory controller, see UG0676: PolarFire FPGA DDR Memory Controller User Guide.

This document explains how to use the accompanying reference design to demonstrate the high-speed data transfer capability of the PolarFire FPGA using the hardened PCIe EndPoint, Soft DDR3, and DDR4 controller IP. The PCIe controller, built-in direct memory access (DMA) controller, and the CoreAXI4DMAController IP are used to achieve high-speed, bulk data transfers, as follows:

- The PCIe controller’s built-in DMA controller perform bulk-data transfer between contiguous/scatter gather memory locations on a host PC and contiguous memory locations of DDR3/DDR4/LSRAM.
- The CoreAXI4DMAController performs data transfers between DDR3/DDR4 memory and LSRAM using the CoreAXI4DMA controller.

The demo also shows how to use pre-synthesized design simulations using PCIe BFM script to initiate the PCIe EndPoint DMA to perform data transfers between LSRAM, DDR3, DDR4, and PCIe.

The Windows kernel mode PCIe device driver, developed using the Windows Driver Kit (WDK) platform, interacts with the PolarFire PCIe EndPoint from the host PC. A GUI application that runs on the host PC is provided to set up and initiate the DMA transactions between the host PC memory, DDR3, DDR4, and the LSRAM memories of the PolarFire Evaluation/Splash kit through the PCIe interface.

A user application interface is provided for the GUI to interact with the PCIe driver. The GUI can also initiates the DMA transactions between DDR3/DDR4 and LSRAM through UART IF. If the host PC PCIe slot is not available, the DMA between DDR3/DDR4 and LSRAM is exercised through UART IF.

The PCIe EndPoint reference design can be programmed using any of the following options:

- Using the stp file: To program the device using the stp file provided along with the design files, see Programming the Device Using FlashPro, page 21.
- Using Libero SoC PolarFire: To program the device using Libero SoC PolarFire, see Libero Design Flow, page 16. Use this option when the reference design is modified.
2.1 Design Requirements

The following table lists the hardware, software, and IP requirements for this demo design.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating system</td>
<td>64-bit Windows 7 or 10</td>
</tr>
<tr>
<td><strong>Hardware</strong></td>
<td></td>
</tr>
<tr>
<td>PolarFire Evaluation Kit (MPF300-EVAL-KIT-ES) or PolarFire Splash Kit (MPF300TS-1FCG484EES)</td>
<td>Rev C or later</td>
</tr>
<tr>
<td>– PolarFire Evaluation/Splash Board</td>
<td>Rev 2 or later</td>
</tr>
<tr>
<td>– 12 V/5 A power adapter</td>
<td></td>
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<tr>
<td>– USB 2.0 A-male to mini-B cable for UART and programming</td>
<td></td>
</tr>
<tr>
<td>PCIe Edge card ribbon cable</td>
<td></td>
</tr>
<tr>
<td>Host PC with PCIe compliant slot with x4 or higher width</td>
<td></td>
</tr>
<tr>
<td><strong>Software</strong></td>
<td></td>
</tr>
<tr>
<td>Libero SoC PolarFire</td>
<td>v2.3</td>
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<tr>
<td>ModelSim</td>
<td>10.5c Pro</td>
</tr>
<tr>
<td>Synplify Pro</td>
<td>L-2017.09M-SP1-1</td>
</tr>
</tbody>
</table>

2.2 Prerequisites

Before you start:

1. Download the design files from the following link: [http://soc.microsemi.com/download/rsc/?f=mpf_dg0756_liberosocpolarfirev2p3_df](http://soc.microsemi.com/download/rsc/?f=mpf_dg0756_liberosocpolarfirev2p3_df)
2. Download and install Libero SoC PolarFire on the host PC from the following location: [https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polarfire#downloads](https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polarfire#downloads)

The latest versions of ModelSim, Synplify Pro, and FTDI drivers are included in the Libero SoC PolarFire installation package.

2.3 Demo Design

The top-level block diagram of the PCIe EndPoint demo design is shown in Figure 1, page 4. Any external PCIe root-port or bridge can establish PCIe link with the PolarFire FPGA PCIe EndPoint and access the control registers, DDR3, DDR4, and fabric memory through BAR space using the memory write (MWr) and memory read (MRd) transaction layer packets (TLPs). The PCIe EndPoint converts these MWr and MRd TLPs into AXI4 master interface transactions and accesses the fabric memory through CoreAXI4Interconnect IP.

The PCIe Demo application on the host PC initiates the DMA transfers through the PCIe device drivers. The driver on the host PC allocates memory and initiates the DMA Engine in the PolarFire PCIe controller by accessing the PCIe DMA registers through BAR0. The PCIe controller has two independent DMA Engines:

- DMA Engine0: performs DMA from host PC memory to DDR3/DDR4/LSRAM.
- DMA Engine1: performs DMA from DDR3/DDR4/LSRAM to host PC memory.

**Note:** For SGDMA type of DMA operations, the PCIe driver finds the available memory locations and creates the buffer descriptor chain for the different memory locations. It also configures the PCIe DMA for SGDMA and the base address of the first buffer descriptor.
The PCIe demo application initiates CoreAXI4DMA controller IP to perform the DMA between DDR3 memory and LSRAM. The following are the two channels of the CoreAXI4DMA controller IP:

- **Channel0:** performs DMA from—DDR3 to DDR4, DDR3 to LSRAM, and DDR4 to LSRAM
- **Channel1:** performs DMA from—DDR4 to DDR3, LSRAM to DDR3, and LSRAM to DDR4

The host PC application initiates the CoreAXI4DMA controller IP depending on the DMA type through BAR2 when the PCIe edge connector is connected to the host PC PCIe slot. The host PC application also initiates the CoreAXI4DMA controller IP through UART IF. This option is provided to exercise the DDR throughputs when the PolarFire Evaluation/Splash kit is not connected to the host PC PCIe slot.

**Figure 1 • PCIe Demo Design Top-Level Block Diagram**
2.3.1 Design Data Flow

The demo design performs the following control plane operations:

- **LED Blink**: host PC driver performs BAR2 memory write operation (MWr) to EndPoint. The PCIe controller generates AXI write transaction on AXI_IO_CTRL logic's to blink LEDs.
- **DIP Switch Read**: host PC driver performs BAR2 memory read operation (MRd) to EndPoint. The PCIe controller generates AXI read transaction on AXI_IO_CTRL logic's to blink LEDs.
- **MSI Interrupt Count**: when on-board push button is pressed, the PCIe EndPoint generates interrupt to host PC and the host PC driver increments the corresponding interrupt counter.
- **Memory Read/Write**: host PC driver configures the ATR2 translation address to DDR3/DDR4/LSRAM base address. It performs BAR2 memory read/write transactions to DDR3/DDR4/LSRAM memories.

The demo design supports three types of DMA operations.

- Continuous DMA operations
- SDGMA Operations
- Core DMA Operations

2.3.1.1 Continuous DMA Operations

The PCIe DMA0/DMA1 controllers perform DMA between continuous memory locations when SGDMA mode is disabled. The following sections explain the data flow of DMA0 and DMA1.

2.3.1.1.1 DMA0 – Host PC Memory to DDR3/DDR4/LSRAM

PCle DMA Engine0 performs continuous DMA from host PC memory to DDR3/DDR4/LSRAM memories as described in the following steps:

1. PolarFire_PCIE_GUI application sets up the DMA controller through the PCIe link. This includes DMA source and destination, address, and size.
2. DMA controller initiates a read transaction to the PCIe core.
3. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the host PC.
4. The host PC returns a completion (CplD) TLP to the PCIe link.
5. This returned data is written to the DDR3/DDR4/LSRAM memories using PCIe AXI master interface.
6. The DMA controller repeats this process (from step 2 to 5) until the DMA size of data transfer is completed.
7. The DMA controller sends the MSI0 interrupt to the host PC, the driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire_PCIE_GUI application.

2.3.1.1.2 DMA1 – DDR3/DDR4/LSRAM to Host PC Memory

PCle DMA Engine1 performs continuous DMA from DDR3/DDR4/LSRAM memories to host PC memory as described in the following steps:

1. PolarFire_PCIE_GUI application sets up the DMA controller through the PCIe link. This includes DMA source and destination, address, and size.
2. DMA controller initiates an AXI burst read transaction to read the data from DDR3/DDR4/LSRAM memories.
3. The DMA controller initiates write transaction to PCIe core with the read data. The PCIe core sends a memory write (MWr) TLP to the host PC.
4. The DMA controller repeats this process (steps 2 and 3) until the DMA size of data transfer is completed.
5. The DMA controller sends the MSI1 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire_PCIE_GUI application.
2.3.1.2 SGDMA Operations

The PCIe DMA0/DMA1 performs DMA between scattered host PC memory locations and continuous memories of PolarFire when SGDMA mode is enabled.

2.3.1.2.1 Host PC Memory to DDR3/DDR4

PCIe DMA Engine0 performs DMA from host PC memory to DDR3/DDR4 memories as shown in the following figure.

The following steps describe the SGDMA operation of PCIe DMA0:

1. PolarFire_PCIe_GUI application requests the PCIe driver for SG DMA. The driver on the host PC allocates the available memory location and creates the buffer descriptors with the scattered memory location addresses and location size.
2. The destination DDR3/DDR4 memory is treated as the continuous memory. The driver configures the PCIe DMA0 with the first buffer descriptor address and initiates the DMA.
3. DMA controller initiates read transaction to the PCIe core with the buffer descriptor address.
4. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the host PC. The host PC returns a completion (CplD) TLP to the PCIe link.
5. The DMA controller extracts these buffer descriptors and initiates the read transaction to PCIe core with the host PC memory location address in the descriptor.
6. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the host PC. The host PC returns a completion (CplD) TLP to the PCIe link.
7. This return data is written to the DDR3/DDR4 memories using PCIe AXI master interface.
8. The DMA controller repeats this process (from step 3 to 7) until the DMA size of data transfer is completed.
9. The DMA controller sends the MSI0 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire_PCIe_GUI application.

*Figure 2* • DMA0 – Example of SG DMA Operation
2.3.1.2.2 DDR3/DDR4 to Host PC Memory:

PCIe DMA Engine1 performs DMA from DDR3/DDR4 memories to host PC memory as shown in the following figure.

The following steps describe the SGDMA operation of PCIe DMA1:

1. PolarFire_PCIe_GUI application requests the PCIe driver for SG DMA. The driver on the host PC allocates the available memory locations and creates the buffer descriptors with the scattered memory location addresses and location size.
2. The source DDR3/DDR4 memory is treated as the continuous memory. Single buffer descriptor is created in LSRAM with the base address of DDR3/DDR4 memory. The LSRAM base address is provided to DMA controller for source descriptor address.
3. The driver configures the PCIe DMA1 with the first host PC destination buffer descriptor address and initiates the DMA.
4. DMA controller initiates read transaction to the PCIe core with the buffer descriptor address.
5. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the host PC. The host PC returns a completion (CplD) TLP to the PCIe link.
6. The DMA controller extracts these buffer descriptors and initiates an AXI burst read transaction to read the data from DDR3/DDR4 memories.
7. With this read data, DMA controller initiates the write transaction to PCIe core with the host PC memory location address in the descriptor.
8. The PCIe core sends the memory write (MWr) transaction layer packets (TLP) to the host PC.
9. The DMA controller repeats this process (from step 4 to 8) until the DMA size of data transfer is completed.
10. The DMA controller sends the MSI1 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire_PCIe_GUI application.

Figure 3 • DMA1 – Example of SG DMA Operation
2.3.2 Design Implementation

The following figure shows the Libero SoC PolarFire software top-level design implementation of the PCIe EndPoint reference design.

**Figure 4 • PCIe EndPoint Reference Design**

The top-level design includes the following SmartDesign components, memory controller subsystems, and AXI4Interconnect IP:

- PCIe EP subsystem
- CoreDMA and UART subsystem
- AXItoAPB
- DDR3 subsystem
- DDR4 subsystem
- AXI LSRAM
- AXI4Interconnect IP
2.3.2.1 PCIe EP Subsystem

The PCIe_EP SmartDesign implements PCIe EndPoint and its clocking scheme as shown in the following figure. It also includes the sw_debounce module, which is used to suppress bounces from on-board push buttons and to generate a pulse to the PCIe controller interrupt line. The rst_controller logic is used to reset the PCIe EndPoint when host PC generates the EndPoint reset through PCIe PERSTn side band signal. The rst_controller.v fabric logic monitors the PERSTn signal of PCIe Edge card. It performs the assertion and de-assertion of PCIe and PCS soft resets on raising edge of PERSTn signal. It uses the dynamic reconfiguration interface (DRI) to access the PCIe and PCS soft reset registers. For more information about DRI, see *UG0677: PolarFire FPGA Transceiver User Guide*.

The PCIE core is configured as an EndPoint with maximum link speed and maximum link width—Gen2 (5.0 Gbps) link speed and x4 link width. The **Simulation Level** in the configurator is set to **BFM** to simulate the design using PCIe BFM script. The PCIe fabric interface is always the same regardless of the link width or lane rate. APB interface is enabled to access the PCIe DMA and Address translation registers.

The following two BARs are configured in 64-bit:

- **BAR0**: accesses the PCIe DMA, address translation, and interrupt registers through the PCIe controller’s APB interface. The address translation register associated with BAR0 is configured to translate the BAR0 address to the PCIe APB IF base address (0x0300_0000).
- **BAR2**: accesses the fabric control registers and AXI LSRAM, DDR3, and DDR4 memories. By default, the address translation register associated with BAR2 is configured to access the fabric control registers (0x1000_0000). To access the LSRAM, DDR3, and DDR4 memories, the driver on the host PC configures the BAR2 address translation register (TRSL_ADDR) to LSRAM (0x3000_0000)/DDR3 (0x2000_0000)/ DDR4 (0x4000_0000) memory base address using the PCIe APB IF through BAR0.

**Figure 5** • PCIe_EP SmartDesign

The PCIe_TL_CLK SmartDesign implements PCIe TL CLK for PolarFire devices as shown in Figure 6, page 10. PCIe TL CLK needs to be connected to CLK_125MHZ of Tx PLL. In PolarFire devices, TL CLK is available only after PCIe initialization. The 80 MHz clock is derived from the on-chip 160 MHz oscillator to drive the TL CLK during PCIe initialization. The NGMUX is used to switch this clock to the required CLK_125MHz after PCIe initialization. The BANK 0, BANK 1, and BANK 7 calibration status signals of PF Initialization Monitor IP is used to generate CALIB_DONE signal, which is used for DDR3/DDR4 reset.
2.3.2.2 CoreDMA and UART Subsystem

The CoreDMA_IO_CTRL SmartDesign implements fabric registers, CoreDMA4DMA IP initialization, and UART_SD as shown in the following figure.

axi4dma_init logic initiates the CoreDMA through AXI4Lite interface to perform the DMA as per commands from GUI. axi_io_ctrl block receives commands from PCIe BAR space and controls the IOs or axi4dma_init logic.

The CoreAXI4DMAController IP is configured for 64-bit AXI4 data width, and to generate interrupts for descriptor0 and descriptor1. Descriptor0 is used for—DDR3 to DDR4, DDR3 to LSRAM, and DDR4 to LSRAM DMA and descriptor1 is used for—DDR4 to DDR3, LSRAM to DDR3, and LSRAM to DDR4 DMA.

The UART_SD SmartDesign implements logic required to communicate with UART IF as shown in the following figure. cmd_ctrlr block receives commands from UART and triggers the logic to perform CoreDMA/DDR memory initialization. pattern_gen_checker block initializes the DDR memory with the specified pattern and compares against specified pattern.
2.3.2.3 Memory Controller Subsystem

2.3.2.3.1 DDR3

The DDR3 subsystem is configured to access the 16-bit DDR3 memory through an AXI4 interface. The “PolarFire evaluation kit DDR3 memory” preset is applied to configure all of the memory initialization and timing parameters in the DDR3 configurator.

Note: DDR3 is applicable only for Evaluation kit demo design.

2.3.2.3.2 DDR4

The DDR4 subsystem is configured to access the 16-bit DDR4 memory through an AXI4 64-bit interface. The DDR4 memory initialization and timing parameters are configured as per the DDR4 memory on PolarFire Evaluation/Splash kit. For more information about DDR4 subsystem configuration, see Appendix: DDR4 Configuration, page 37.

Note: The PolarFire Evaluation/Splash kit supports 32-bit DDR4 memory. This demo design uses only 16-bit DDR4 memory to meet the 200 MHz fabric logic Place and Route timing.

2.3.2.3.3 AXI LSRAM

The AXI LSRAM in the design is configured for 4KB. This 4KB is over written if more than 4KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

2.3.2.4 AXI to APB SmartDesign

The AXI_to_APB SmartDesign implements AXI to APB using different IP cores as shown in the following figure. AXI to APB IF is to access the PCIe control registers through the PCIe APB IF from the BAR0 space.

Figure 9 • AXI_to_APB SmartDesign

2.3.2.5 CoreAXI4Interconnect IP

The CoreAXI4Interconnect IP is configured for the following master and slave ports:

- Master0: PCIe
- Master1: CoreAXI4DMAController IP
- Master2: Pattern generator and checker logic (pattern_gen_checker block)
- Slave0: AXItoAPB bridge (0x0000_0000 to 0xFFFF_FFFF)
- Slave1: AXI Slave Fabric Registers (0x1000_0000 to 0x1FFF_FFFF)
- Slave2: DDR3 Subsystem (0x2000_0000 to 0x2FFF_FFFF) (Not enabled for Splash kit)
- Slave3: AXI4 LSRAM (0x3000_0000 to 0x3FFF_FFFF)
- Slave4: DDR4 Subsystem (0x4000_0000 to 0x4FFF_FFFF)

Slave0 is configured to convert AXI4 transactions to AXI3 transactions.
### 2.4 Clocking Structure

The following figure shows the clocking structure of PCIe EndPoint reference design.

- **Clock Domain 1**: generates PCIe TL_CLK. At power-up, it uses 80 MHz clock and switches to 125 MHz after completion of PCIe initialization.
- **Clock Domain 2**: generates CDR reference and XCVR clocks for PCIe.
- **Clock Domain 3**: generates 50 MHz clock for PCIe APB, DDR4 PLL reference, and CCC reference clocks. DDR4 subsystem generates a 200 MHz (166.66 MHz for Splash kit) clock for fabric AXI interface logic. DDR3 subsystem generates 166.66 MHz clock and is connected to AXI interconnect slave2 CDC interface.

*Figure 10* • Clocking Structure

---

*: DDR3 is applicable only for Evaluation demo design.

**: On Splash kit, 166.66 MHz is used.
2.5 Reset Structure

The CoreReset_PF synchronizes the external USER_RESETN (SW6 on PolarFire Evaluation kit and SW2 on PolarFire Splash kit) to DDR4 system clock (200 MHz) and generates the FABRIC_RESET_N, which drives the fabric AXI interface logic. CoreReset_PF uses the DEVICE_INIT_DONE signal, which is asserted when the device initialization is complete. For more information about device initialization, see UG0725: PolarFire FPGA Device Power-Up and Resets User Guide.

For more information on CoreReset_PF IP core, see CoreReset_PF handbook from the Libero catalog.

The DDR3/DDR4 subsystem does not require a synchronization reset as it has the reset synchronization logic. The following figure shows the reset structure in the reference design.

![Figure 11 • Reset Structure](image)

*NOTE: On Splash Kit, 166.66 MHz is used.

2.6 Throughput Measurement

The fabric logic uses 32-bit counters to count the number of clock cycles in each DMA transfer. The host PC application starts these counters while initiating the DMA transfers, and the fabric logic stops these counters at the end of the DMA transfer. The DMA Engine interrupts the host PC at the end of the DMA transfer and the host PC application reads the counters to calculate throughput as follows:

Throughput = Transfer Size (Byte) × Clock Frequency/Number of clock cycles taken for a transfer

The throughput includes all of the overhead of the AXI, PCIe, and DMA controller transactions.

2.7 Simulating the Design

Before you start:

1. Start Libero SoC PolarFire, and in the Project menu, click Open Project.
3. Open the Design Hierarchy window and double-click the PCIe_EP_Demo component.
   The SmartDesign page opens on the right pane and displays the high-level design. You can view the design blocks and IP cores instantiated for the PCIe EndPoint interface design.
4. Download the PF_XCVR_REF_CLK, PF_TX_PLL, PF_CCC, PF_PCIE, CoreAXI4Interconnect, CoreAXI4DMAController, DDR3, DDR4, CoreAHBLite, CoreAPB, CoreAXItoAHBL, CoreAHBLtoAPB, CoreUART, and PolarFire SRAM IP cores under Libero SoC PolarFire > Catalog.
The PCIe BFM performs 1 KB DMA operations between PCIe and DDR3, DDR4 and LSRAM memories by initiating AXI burst transactions. The PCIe BFM simulation model replaces the entire PCIe EndPoint interface with a simple BFM that can send write transactions and read transactions over the AXI interface. These transactions are driven by a script file (.bfm) and allow easy simulation of the FPGA design connected to a PCIe interface. For more information about BFM commands, see UG0685: PolarFire FPGA PCI Express User Guide. The micron DDR3 and DDR4 memory models are instantiated in the testbench for simulating DDR3 and DDR4 memory controllers.

**Note:** In the Design Flow tab, system verilog is selected, as the memory models from Micron are in the system verilog.

In the Project settings > Design Flow tab, double-click Simulate under Verify Pre-Synthesized Design to simulate the design, as shown in the following figure. The ModelSim tool takes about 10 to 15 minutes to complete the simulation.

**2.7.1 Simulation Flow**

The following steps describe the PCIe BFM simulation flow:

1. At the start, the NSYSREST signal, reset all the components.
2. DDR3 and DDR4 memory controllers initializes the DDR3/DDR4 memories and release the CTRLR READY.
3. The PCIe BFM starts executing the BFM script PCIex4_PCIex4_0_PF_PCIE_PCIE_1_user.bfm.
4. The PCIe EndPoint AXI4 master interface initiates write and read burst transactions to SRAM_AXI_0, DDR3, DDR4 through CoreAXI4Interconnect as per the .bfm script.
5. After 18 µs, the simulation completes. PCIE1 BFM Simulation Complete – 282 Instructions – NO ERRORS message is displayed for Evaluation kit, as shown in Figure 13, page 15.
6. After 13 µs, the simulation completes. PCIE1 BFM Simulation Complete – 272 Instructions – NO ERRORS message is displayed for Splash kit.

The ModelSim transcript window displays the BFM commands execution messages, as shown in the following figure. For more information about BFM commands, see the SmartFusion2 FPGA Microcontroller Subsystem BFM Simulation User Guide.
The following figure shows the actual waveform window showing the sequence of data being written and read using the BFM.
3 Libero Design Flow

The Libero design flow involves the following steps:

- Synthesize
- Place and route
- Verify timing
- Design and Memory Initialization
- Generate Bitstream
- Run PROGRAM Action

3.1 Synthesize

Go to the Design Flow window and double-click Synthesize.

When the synthesis is successful, a green tick mark appears as shown in Figure 19, page 18.

3.1.1 Resource Utilization

The following table lists the resource utilization of the PCIe Endpoint design for Evaluation kit. These values may vary slightly for different Libero runs, settings, and seed values.

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>43486</td>
<td>299544</td>
<td>14.52</td>
</tr>
<tr>
<td>DFF</td>
<td>33781</td>
<td>299544</td>
<td>11.28</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>1536</td>
<td>0.00</td>
</tr>
<tr>
<td>User I/O</td>
<td>131</td>
<td>512</td>
<td>25.59</td>
</tr>
<tr>
<td>– Single-ended I/O</td>
<td>119</td>
<td>512</td>
<td>23.24</td>
</tr>
<tr>
<td>– Differential I/O Pairs</td>
<td>6</td>
<td>256</td>
<td>2.34</td>
</tr>
</tbody>
</table>

The following table lists the resource utilization of the PCIe Endpoint design for Splash kit. These values may vary slightly for different Libero runs, settings, and seed values.

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>29663</td>
<td>299544</td>
<td>9.90</td>
</tr>
<tr>
<td>DFF</td>
<td>22232</td>
<td>299544</td>
<td>7.42</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>732</td>
<td>0.00</td>
</tr>
<tr>
<td>User I/O</td>
<td>76</td>
<td>244</td>
<td>31.15</td>
</tr>
<tr>
<td>– Single-ended I/O</td>
<td>70</td>
<td>244</td>
<td>28.69</td>
</tr>
<tr>
<td>– Differential I/O Pairs</td>
<td>3</td>
<td>122</td>
<td>2.46</td>
</tr>
</tbody>
</table>
3.2  Place and Route

To place and route the design, the TX_PLL, XCVR_REF_CLK, DDR3, DDR4, and CCC need to be constrained using the I/O Editor as shown in the following figures.

*Figure 16 • I/O Editor—XCVR View*

*Figure 17 • I/O Editor—DDR3 Memory View*

*Figure 18 • I/O Editor—DDR4 Memory View (For Evaluation Kit)*
Go to the Design Flow window and double-click Place and Route. When place and route is successful, a green tick mark appears as shown in Figure 19, page 18.

### 3.3 Verify Timing

Go to the Design Flow window and double-click Verify Timing. When the design successfully meets the timing requirements, a green tick mark appears as shown in the following figure.

*Figure 19 • Design Flow*

### 3.4 Generate Bitstream

To generate the bitstream:

1. Double-click Generate Bitstream from the Design Flow tab. When the bitstream is successfully generated, a green tick mark appears as shown in Figure 22, page 20.
2. Right-click Generate Bitstream and select View Report to view the corresponding log file in the Reports tab.
3.5 Run PROGRAM Action for Evaluation Kit

After generating the bitstream, the PolarFire device must be programmed. Follow these steps to program the PolarFire device:

1. Ensure that the jumper settings on the board are the same as those listed in the following table.

   **Table 4 • Jumper Settings**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J18, J19, J20, J21, J22</td>
<td>Short pin 2 and 3 for programming the PolarFire FPGA through FTDI</td>
</tr>
<tr>
<td>J28</td>
<td>Short pin 1 and 2 for programming through the on-board FlashPro5</td>
</tr>
<tr>
<td>J26</td>
<td>Short pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J27</td>
<td>Short pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J4</td>
<td>Short pin 1 and 2 for manual power switching using SW3</td>
</tr>
<tr>
<td>J12</td>
<td>Short pin 3 and 4 for 2.5 V</td>
</tr>
</tbody>
</table>

2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the Host PC to **J5** (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.

**Figure 20 • Board Setup**

5. Double-click **Run PROGRAM Action** from the **Libero > Design Flow** tab.
3.6 Run PROGRAM Action for Splash Kit

After generating the bitstream, the PolarFire device must be programmed. Follow these steps to program the PolarFire device:

1. Ensure that the jumper settings on the board are the same as those listed in the following table.

Table 5 • Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5, J6, J7, J8, J9</td>
<td>Short pin 2 and 3 for programming the PolarFire FPGA through FTDI</td>
</tr>
<tr>
<td>J11</td>
<td>Short pin 1 and 2 for programming through the FTDI chip</td>
</tr>
<tr>
<td>J10</td>
<td>Short pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J4</td>
<td>Short pin 1 and 2 for manual power switching using SW1</td>
</tr>
<tr>
<td>J3</td>
<td>Open pin 1 and 2 for 1.0 V</td>
</tr>
</tbody>
</table>

2. Connect the power supply cable to the J2 connector on the board.
3. Connect the USB cable from the Host PC to J1 (FTDI port) on the board.
4. Power on the board using the SW1 slide switch.

Figure 21 • Board Setup


When the device is programmed successfully, a green tick mark appears as shown in the following figure. See Running the Demo, page 22 to run the PCIe EndPoint demo.

Figure 22 • Programming the Device
This section describes how to program the PolarFire device with the .stp programming file using FlashPro. The .stp file is available at the following design files folder location:

```
mpf_dg0756_liberosocpolarfirev2p3_df\ProgrammingFile
```

To program the PolarFire device using FlashPro, complete the following steps:

1. Ensure that the jumper settings on the board are the same as listed in Table 4, page 19 (for eval) and Table 5, page 20 (for splash).

   **Note:** The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the **J9** connector on the Evaluation board or **J2** connector on the Splash board.

3. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the Evaluation board or **J1** (FTDI port) on the Splash board.

4. Power on the board using the **SW3** slide switch on the Evaluation board or **SW1** slide switch on the Evaluation board.

5. On the host PC, launch the FlashPro software.

6. Click **New Project** to create a new project.

   In the New Project window, enter a project name.

7. Click **Browse** and navigate to the location where you want to save the project.

8. Select **Single device** as the programming mode and click **OK** to save the project.

9. Click **Configure Device**.

10. Click **Browse**, and navigate to the location where the PCIe_EP_Demo_EvalKit.stp or PCIe_EP_Demo_SplashKit.stp file is located and select the file. The default location is:

    `<download_folder>\mpf_dg0756_liberosocpolarfirev2p3_df\ProgrammingFile`

11. Click **Open**. The required programming file is selected and ready to be programmed in the device.

12. Click **PROGRAM** to program the device.

   When the device is programmed successfully, a Run **PASSED** status is displayed. See Running the Demo, page 22 to run the PCIe EndPoint demo.
Running the Demo

This section describes how to install and use the PCIe Demo application. The PolarFire PCIe demo application is a simple graphic user interface (GUI) that runs on the host PC to communicate with the PolarFire PCIe EndPoint device. It provides PCIe link status, driver information, and demo controls. The PolarFire PCIe demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made.

This section also describes how to connect the kit to the Host PC PCIe Slot. If the host PC PCIe slot is not available, the DMA between DDR3/DDR4 and LSRAM can be exercised through UART IF.

5.1 Installing PCIe Demo Application

To install the PolarFire PCIe Demo application:

1. Install the GUI_Installer (setup.exe) from the following design files folder:
   mpf_dg0756_liberoscopolarfirev2p3_df\GUI_Installer
2. Double-click the setup.exe in the provided GUI installation (GUI_Installer\setup.exe).
3. Apply default options as shown in the following figure.

   Figure 23 • Installing PCIe Demo Application

   ![Installing PCIe Demo Application](image)

4. Click **Next** to start the installation.
5. Click **Finish** to complete the installation.

   Figure 24 • Successful Installation of PCIe Demo Application

   ![Successful Installation of PCIe Demo Application](image)
5.2 Running the Demo Through PCIe

This section shows how to connect the board to host PC PCIe slot, installing the PCIe drivers and running the demo application.

5.2.1 Connecting the Board to the Host PC PCIe Slot

1. After successful programming, power OFF the PolarFire Evaluation/Splash board and shut down the host PC.
2. Connect the CON3 - PCIe Edge connector of the PolarFire Evaluation/Splash board to the host PC’s PCIe slot through the PCI Edge card ribbon cable.
   - This demo is designed to work with any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot, the demo switches to Gen 1 mode.

   **Note:** Power OFF the host PC while inserting the PCIe Edge connector. If it is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode may fail. The device detection and selection depend on the host PC PCIe configuration.

   **Note:** After connecting the board to the host PC, the host PC may power on without manually switching on the PC.

   The following figure shows the board setup for the host PC in which PolarFire Evaluation Kit is connected to the host PC PCIe slot.

   ![Figure 25 • PolarFire Evaluation Kit Setup for Host PC](image)

3. Power on the power supply switch SW3.

   The following figure shows the board setup for the host PC in which PolarFire Splash Kit is connected to the host PC PCIe slot.

   ![Figure 26 • PolarFire Splash Kit Setup for Host PC](image)

4. Power on the power supply switch SW1.
5. Power on the host PC and check the **Device Manager** of the Host PC for the PCIe Device.
   The following figure shows the example **Device Manager** window.

![Device Manager](image)

**Note:** If the device is still not detected, check if the BIOS version in the host PC is the latest, and if PCI is enabled in the host PC BIOS.

### 5.2.2 Driver Installation

Perform the following steps to install the PCIe drivers on the host PC:

1. Right-click **PCI Device** in the **Device Manager** and select **Update Driver Software...** as shown in the following figure. To install the drivers, administrative rights are required.

![Update Driver Software](image)

**Note:** Uninstall the existing Microsemi PolarFire drivers on the host PC before proceeding to next step.

2. In the **Update Driver Software - PCIe Device** window, select **Browse my computer for driver software** as shown in the following figure.

![Browse for Driver Software](image)
3. Browse the drivers folder: `mpf_dg0756_liberoscopolarfirev2p3_df\PCIe_Drivers\Win_64bit_PCIe_Driver` and click **Next** as shown in the following figure.

*Figure 30 • Browse for Driver Software Continued*

![Browse for driver software on your computer](image1)

4. The **Windows Security** dialog box is displayed. Click **Install** as shown in the following figure. After successful driver installation, a message appears. See *Figure 32*, page 25.

*Figure 31 • Windows Security*

![Would you like to install this device software?](image2)

*Figure 32 • Successful Driver Installation*
5.2.3 Running the PCIe Demo Application

The following steps describe how to run the demo design:

1. Click to expand the PolarFire PCIe device in the host PC Device Manager as shown in the following figure.

   **Figure 33 • Device Manager—PCIe Device Detection**

   ![Device Manager Screen](image)

   **Note:** If a warning message is displayed for PolarFire PCIe driver while accessing, uninstall and re-install the driver.

2. Go to All Programs > PolarFire_PCIE_GUI > PolarFire_PCIE_GUI. The PolarFire PCIe Demo window is displayed as shown in the following figure.

   **Figure 34 • PCIe EndPoint Demo Application**

   ![Demo Application Screen](image)
3. Click **Connect**. The application detects and displays the information related to the connected kit such as Device Vendor ID, Device Type, Driver Version, Driver Time Stamp, Demo Type, Supported Link Width, Negotiated Link Width, Supported Speed, Negotiated Speed, Number of Bars, and BAR Address as shown in the following figure.

*Figure 35 • Device Info*

![Device Info Figure](image)

4. Click the **Demo Controls** tab to display the **LED Controls**, **DIP Switch Status**, and **Interrupt Counters**.

5. Click **Start LED ON/OFF Walk**, **Enable DIP SW Session**, and **Enable Interrupt Session** to view the controlling LEDs (observe LED4 to LED11 on the PolarFire Evaluation Kit and LED1 to LED8 on the PolarFire Splash Kit), getting the DIP switch (ON/OFF the DIP1 to DIP4 on the PolarFire Evaluation/Splash Kit) status, and monitoring the interrupts (press SW7 to SW10 on the PolarFire Evaluation Kit and SW3 to SW6 on the PolarFire Splash Kit to generate interrupt) simultaneously as shown in the following figure.

*Figure 36 • Demo Controls—Continued*

![Demo Controls Figure](image)
6. Click the **Config Space** tab to view the details about the PCIe configuration space as shown in the following figure.

*Figure 37 • Configuration Space*

![Configuration Space Diagram]

7. Click the **PCIe Read/Write** tab to perform read and write operations to DDR/LSRAM using BAR2 space.

8. Select LSRAM/DDR3/DDR4 and then click **Read** to read the 4 KB memory mapped to BAR2 space for DDR and LSRAM as shown in the following figure.

*Note:* PCIe BAR2-DDR3 is applicable only for Evaluation Kit.

*Figure 38 • PCIe BAR2 Memory Access—LSRAM*

![PCIe BAR2 Memory Access Diagram]

9. Click the **DMA Operations** tab for different DMA operations such as DDR and LSRAM.

*Note:* DDR3 DMA options are not applicable for Splash kit demo.
5.2.3.1 Continuous DMA—Operations

The following instructions describe running DMA operations between PC and DDR3, PC and DDR4, PC and LSRAM:

1. Select one of the following options from the DMA Transfer Type Selection drop-down list:
   - **PC->DDR3**—to transfer the data from host PC to PolarFire DDR3 memory
   - **DDR3->PC**—to transfer the data from PolarFire DDR3 memory to host PC
   - **Both PC<>DDR3**—to transfer the data from host PC to and from PolarFire DDR3 memory
   - **PC->DDR4**—to transfer the data from host PC to PolarFire DDR4 memory
   - **DDR4->PC**—to transfer the data from PolarFire DDR4 memory to host PC
   - **Both PC<>DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory
   - **PC->LSRAM**—to transfer the data from host PC to PolarFire LSRAM memory
   - **LSRAM->PC**—to transfer the data from PolarFire LSRAM memory to host PC
   - **Both PC<>LSRAM**—to transfer the data from host PC to and from PolarFire LSRAM memory

2. Select **Transfer Size** (4KB to 64KB) from the drop-down list. Maximum contiguous DMA size is 64KB because the host PC may not have contiguous memory of more than 64 KB. For DMA operations that require more than 64 KB, use SGDMA.

3. Enter the **Loop Count** in the box.

4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps.

   **Note:** The AXI LSRAM in the design is configured for 4KB. This 4KB is over written if more than 4KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

The following figure shows the throughput and average throughput in MBps.

*Figure 39 • Continuous DMA Operations with DMA Transfer Type Selection as Both PC and LSRAM*
5.2.3.2 Continuous DMA—Memory Test

The following instructions describe running Memory Test between PC and DDR3/DDR4/LSRAM:

1. Select one of the following options from the Test Selection drop-down list:
   - **PC->DDR3**—to transfer the data from host PC to and from PolarFire DDR3 memory
   - **PC->DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory
   - **PC->LSRAM**—to transfer the data from host PC to and from PolarFire LSRAM memory

2. Select Transfer Size (4KB to 64KB) from the drop-down list.

3. Select Pattern Selection from the drop-down list—Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's.

4. Click **Start**. GUI performs the following task:
   - The host PC creates a buffer and initializes the memory
   - Initiates the PC to DDR DMA
   - Erases the PC buffer
   - Initializes the DDR to PC DMA
   - Compares the memory against expected memory

**Memory Test Successful** window appears, as shown in the following figure.

*Figure 40* • Continuous DMA Memory Test—Memory Test Successful

Note: If memory test fails, the GUI displays the first failed memory location.

Note: Change the **Offset Address** and click **View Memory** to read the RAM memory content.

5.2.3.3 SGDMA—Operations

The following instructions describe running SGDMA operations between PC and DDR3, PC and DDR4:

1. Select one of the following options from the DMA Transfer Type Selection drop-down list:
   - **PC -> DDR3**—to transfer the data from host PC to PolarFire DDR3 memory
   - **DDR3 -> PC**—to transfer the data from PolarFire DDR3 memory to host PC
   - **Both PC <-> DDR3**—to transfer the data from host PC to and from PolarFire DDR3 memory
   - **PC -> DDR4**—to transfer the data from host PC to PolarFire DDR4 memory
   - **DDR4 -> PC**—to transfer the data from PolarFire DDR4 memory to host PC
   - **Both PC <-> DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory

2. Select Transfer Size (4KB to 64KB) from the drop-down list.
Running the Demo

3. Enter the Loop Count in the box. The Buffer Descriptors show the number of descriptors created by the host driver for each SGDMA operation.
4. Click Start Transfer. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps.

5.2.3.4 SGDMA—Memory Test
The following instructions describe running Memory Test between PC and DDR3/DDR4/LSRAM:

1. Select one of the following options from the Test Selection drop-down list:
   - PC<->DDR3—to transfer the data from host PC to and from PolarFire DDR3 memory
   - PC<->DDR4—to transfer the data from host PC to and from PolarFire DDR4 memory
2. Select Transfer Size (4KB to 1MB) from the drop-down list.
3. Select Pattern Selection from the drop-down list—Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A’s, and Fill with all 5’s.
4. Click Start. GUI performs the following task:
   - The host PC creates a buffer and initializes the memory
   - Initiates the PC to DDR DMA
   - Erases the PC buffer
   - Initializes the DDR to PC DMA
   - Compares the memory against expected memory

Memory Test Successful window appears.

5. Click OK.

5.2.3.5 Core DMA—Operations
The following instructions describe running DMA operations between LSRAM and DDR3, LSRAM and DDR4, DDR3 and DDR4:

1. Select one of the following options from the DMA Transfer Type Selection drop-down list:
   - LSRAM -> DDR3—to transfer the data from LSRAM to PolarFire DDR3 memory
   - DDR3-> LSRAM—to transfer the data from PolarFire DDR3 memory to LSRAM
   - Both LSRAM <->DDR3—to transfer the data from LSRAM to and from PolarFire DDR3 memory
   - LSRAM -> DDR4—to transfer the data from LSRAM to PolarFire DDR4 memory
   - DDR4-> LSRAM—to transfer the data from PolarFire DDR4 memory to LSRAM
   - Both LSRAM <->DDR4—to transfer the data from LSRAM to and from PolarFire DDR4 memory
   - DDR4 -> DDR3—to transfer the data from DDR4 to DDR3 memory
   - DDR3 -> DDR4—to transfer the data from DDR3 to DDR4 memory
   - Both DDR4 <-> DDR3—to transfer the data from DDR4 to and from DDR3 memory
2. Select Transfer Size (4KB to 1MB) from the drop-down list.
3. Enter the Loop Count in the box.
4. Click Start Transfer. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps.

Note: The AXI LSRAM in the design is configured for 4KB. This 4KB is over written if more than 4KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

5. Click Exit to quit the demo.

5.3 Running the Demo Through UART
The following steps describes how to run a demo using UART if the host PC PCIe slot is not available:
Check the Device Manager of the host PC for UART ports.
The following figure shows the example UART ports in the Device Manager window.

Figure 41 • Device Manager—UART Ports
The following steps describe how to run the reference design using UART IF:

1. Go to All Programs > PolarFire_PCIe_GUI > PolarFire_PCIe_GUI. The PolarFire PCIe Demo window is displayed.
2. Select UART radio button and click Connect.

The GUI application scans for UART port and after successful connection, displays the DMA Operations UART tab as shown in Figure 42, page 32.

### 5.3.1 UART—DMA Operations

The following instructions describe the different ways to read data through LSRAM and DDR:

1. Select one of the following options from the **Continuous DMA Transfer Type Selection** drop-down list:
   - DDR3 -> LSRAM: to transfer the data from DDR3 to PolarFire LSRAM memory.
   - LSRAM -> DDR3: to transfer the data from PolarFire LSRAM memory to DDR3.
   - Both DDR3 <-> LSRAM: to transfer the data from DDR3 to and from PolarFire LSRAM memory.
   - LSRAM -> DDR4: to transfer the data from LSRAM to PolarFire DDR4 memory.
   - DDR4 -> LSRAM: to transfer the data from PolarFire DDR4 memory to LSRAM.
   - Both LSRAM <-> DDR4: to transfer the data from LSRAM to and from PolarFire DDR4 memory.
   - DDR4 -> DDR3: to transfer the data from DDR4 to DDR3 memory.
   - DDR3 -> DDR4: to transfer the data from DDR3 to DDR4 memory.
   - Both DDR4 <-> DDR3: to transfer the data from DDR4 to and from DDR3 memory.
   - Both DDR3 <-> DDR4: to transfer the data from DDR3 to and from DDR4 memory.

2. Select **Transfer Size** (4KB to 512KB) from the drop-down lists.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows DMA throughput and average throughput from the DDR memory to the LSRAM.

**Figure 42 • UART—DMA Operations**

**Note:** The AXI LSRAM in the design is configured for 4KB. This 4KB is over written if more than 4KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.
5.3.1.1 UART—Memory Test

The following instructions describe running Memory Test between PC and DDR3/DDR4/LSRAM:

1. Select Transfer Size (4KB to 1MB) from the drop-down list.
2. Select Pattern Selection from the drop-down list—Increment, Decrement, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's. For successful Memory test operation, the Patter Type for Mem Init and Patter Type for Mem Test should be same.
3. Click Memory Test.
   - GUI sends command to fabric logic to initiate the LSRAM/DDR3/DDR4 memory
   - GUI sends command to fabric logic to read and compare LSRAM/DDR3/DDR4 memory

The following figure shows UART—Memory Test tab.

Figure 43 • UART—Memory Test

Note: Change the Offset Address and click View Memory to read the RAM memory content.

4. Click View Memory. It shows 1KB of RAM memory content.
5. Click OK.
6. Click Exit to quit the demo.
### 5.4 Throughput Summary of Evaluation Kit

The following tables list the throughput values observed.

#### Table 6 • PolarFire Throughput Summary—Continuous DMA Mode

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC to LSRAM</td>
<td>64 K</td>
<td>1090</td>
<td>1078</td>
</tr>
<tr>
<td>LSRAM to PC</td>
<td></td>
<td>1129</td>
<td>1127</td>
</tr>
<tr>
<td>Both PC to and from LSRAM</td>
<td></td>
<td>1088/1106</td>
<td>1065/1105</td>
</tr>
<tr>
<td>PC to DDR4</td>
<td>64 K</td>
<td>1062</td>
<td>1050</td>
</tr>
<tr>
<td>DDR4 to PC</td>
<td></td>
<td>524(^1)</td>
<td>523</td>
</tr>
<tr>
<td>Both PC to and from DDR4</td>
<td></td>
<td>1062/523</td>
<td>1044/523</td>
</tr>
<tr>
<td>PC to DDR3</td>
<td>64 K</td>
<td>495</td>
<td>494</td>
</tr>
<tr>
<td>DDR3 to PC</td>
<td></td>
<td>326(^1)</td>
<td>326</td>
</tr>
<tr>
<td>Both PC to and from DDR3</td>
<td></td>
<td>495/327</td>
<td>494/327</td>
</tr>
</tbody>
</table>

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4's maximum of 256 beat), which causes low read performance of DDR3/DDR4.

#### Table 7 • PolarFire Throughput Summary—SGDMA Mode

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC to DDR4</td>
<td>1 MB</td>
<td>1013</td>
<td>1012</td>
</tr>
<tr>
<td>DDR4 to PC</td>
<td></td>
<td>524(^1)</td>
<td>524</td>
</tr>
<tr>
<td>Both PC to and from DDR4</td>
<td></td>
<td>1010/524</td>
<td>1010/524</td>
</tr>
<tr>
<td>PC to DDR3</td>
<td>1 MB</td>
<td>500</td>
<td>498</td>
</tr>
<tr>
<td>DDR3 to PC</td>
<td></td>
<td>328(^1)</td>
<td>327</td>
</tr>
<tr>
<td>Both PC to and from DDR3</td>
<td></td>
<td>500/328</td>
<td>498/327</td>
</tr>
</tbody>
</table>

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4's maximum of 256 beat), which causes low read performance of DDR3/DDR4.

#### Table 8 • PolarFire Throughput Summary—Core DMA Mode

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSRAM to DDR4</td>
<td>1 MB</td>
<td>1475</td>
<td>1475</td>
</tr>
<tr>
<td>DDR4 to LSRAM</td>
<td></td>
<td>1205</td>
<td>1205</td>
</tr>
<tr>
<td>Both LSRAM to and from DDR4</td>
<td></td>
<td>1475/1205</td>
<td>1475/1205</td>
</tr>
<tr>
<td>LSRAM to DDR3</td>
<td>1 MB</td>
<td>611</td>
<td>611</td>
</tr>
<tr>
<td>DDR3 to LSRAM</td>
<td></td>
<td>562</td>
<td>562</td>
</tr>
<tr>
<td>Both LSRAM to and from DDR3</td>
<td></td>
<td>611/562</td>
<td>611/562</td>
</tr>
<tr>
<td>DDR4 to DDR3</td>
<td>1 MB</td>
<td>611</td>
<td>611</td>
</tr>
<tr>
<td>DDR3 to DDR4</td>
<td></td>
<td>562</td>
<td>562</td>
</tr>
<tr>
<td>Both DDR4 to and from DDR3</td>
<td></td>
<td>611/562</td>
<td>611/562</td>
</tr>
</tbody>
</table>

**Note:** DDR3 throughput is less due to AXI interconnect CDC path limitation.
### 5.5 Throughput Summary of Splash Kit

The following table lists the throughput values observed.

**Table 9 • PolarFire Throughput Summary—Continuous DMA Mode**

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC to LSRAM</td>
<td>64 K</td>
<td>1068</td>
<td>1075</td>
</tr>
<tr>
<td>LSRAM to PC</td>
<td></td>
<td>959</td>
<td>960</td>
</tr>
<tr>
<td>Both PC to and from LSRAM</td>
<td></td>
<td>1065/959</td>
<td>1046/959</td>
</tr>
<tr>
<td>PC to DDR4</td>
<td>64 K</td>
<td>1057</td>
<td>1057</td>
</tr>
<tr>
<td>DDR4 to PC</td>
<td></td>
<td>439²</td>
<td>439</td>
</tr>
<tr>
<td>Both PC to and from DDR4</td>
<td></td>
<td>1064/439</td>
<td>1046/440</td>
</tr>
</tbody>
</table>

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4’s maximum of 256 beat), which causes low read performance of DDR4.

**Table 10 • PolarFire Throughput Summary—SGDMA Mode**

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC to DDR4</td>
<td>1 MB</td>
<td>996</td>
<td>998</td>
</tr>
<tr>
<td>DDR4 to PC</td>
<td></td>
<td>440²</td>
<td>440</td>
</tr>
<tr>
<td>Both PC to and from DDR4</td>
<td></td>
<td>1006/440</td>
<td>997/440</td>
</tr>
</tbody>
</table>

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4’s maximum of 256 beat), which causes low read performance of DDR4.

**Table 11 • PolarFire Throughput Summary—Fabric Core DMA Mode**

<table>
<thead>
<tr>
<th>DMA Transfer Type</th>
<th>DMA Size</th>
<th>Throughput (MBps)</th>
<th>Average Throughput (MBps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR4 to LSRAM</td>
<td>1 MB</td>
<td>1044</td>
<td>1043</td>
</tr>
<tr>
<td>LSRAM to DDR4</td>
<td></td>
<td>1220</td>
<td>1220</td>
</tr>
<tr>
<td>Both LSRAM to and from DDR4</td>
<td></td>
<td>1042/1220</td>
<td>1042/1220</td>
</tr>
</tbody>
</table>
6 Appendix: DDR3 and DDR4 Power Measurement

6.1 DDR3

The PolarFire Evaluation Kit board has a current sense resistor (R118) for 1.5 V power rail. Measure the voltage across the R118 using test points TP134 and TP135 and use the following equations to get the DDR3 power. This measurement includes PolarFire DDR3 IO power consumption and actual Micron DDR3 memory power consumption.

\[
\text{Current (mA)} = \frac{\text{MeasureVoltage (mV)}}{R} \\
\text{Power (mW)} = \text{Current} \times \text{Voltage}
\]

While running the demo, the measured voltage across R118 is 6.3 mV and resistor value is 0.01 Ω.

Current (mA) = 6.3 / 0.01 = 630 mA
Power = 630 \times 1.5 = 945 mw

6.2 DDR4

The PolarFire Evaluation Kit board has a current sense resistor (R222) for 1.2 V power rail. Measure the voltage across the R222 using test points TP132 and TP133 and use the following equations to get the DDR4 power. This measurement includes PolarFire DDR4 IO power consumption and actual Micron DDR4 memory power consumption.

\[
\text{Current (mA)} = \frac{\text{MeasureVoltage (mV)}}{R} \\
\text{Power (mW)} = \text{Current} \times \text{Voltage}
\]

While running the demo, the measured voltage across R222 is 2.4 mV and resistor value is 0.01 Ω.

Current (mA) = 2.4 / 0.01 = 240 mA
Power = 240 \times 1.2 = 288 mw
Appendix: DDR4 Configuration

The DDR4 subsystem is configured to access the 16-bit DDR4 memory through an AXI4 64-bit interface. The DDR4 memory initialization and timing parameters are configured as per the DDR4 memory on PolarFire Evaluation kit. The following figures show general configuration settings for the DDR4 memory.

Note: The PolarFire Evaluation kit supports 32-bit DDR4 memory. This demo design uses only 16-bit DDR4 memory to meet the 200 MHz fabric logic Place and Route timing.

Figure 44 • DDR4 Configurator—Evaluation Kit
Figure 45 • DDR4 Configurator—Splash Kit
The following figure shows initialization configuration settings for the DDR4 memory.

*Figure 46 • DDR4 Configurator—Memory Initialization*
The following figure shows timing configuration settings for the DDR4 memory.

**Figure 47 • DDR4 Configurator—Memory Timing**

<table>
<thead>
<tr>
<th>Timing parameters dependent on speed bin</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRAS (ns)</td>
</tr>
<tr>
<td>tRC (ns)</td>
</tr>
<tr>
<td>tRP (ns)</td>
</tr>
<tr>
<td>tRCD (ns)</td>
</tr>
<tr>
<td>tRRD (ns)</td>
</tr>
<tr>
<td>tCCDL (cycles)</td>
</tr>
<tr>
<td>tCCDS (cycles)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing parameters dependent on operating condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>tREFI (ns)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing parameters dependent on speed bin and page size</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRP (ns)</td>
</tr>
<tr>
<td>tFAW (ns)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing parameters dependent on speed bin and clock frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRTR_L (cycles)</td>
</tr>
<tr>
<td>tRTR_S (cycles)</td>
</tr>
<tr>
<td>tRRD_L (cycles)</td>
</tr>
<tr>
<td>tRRD_S (cycles)</td>
</tr>
<tr>
<td>tRTP (ns)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Other Timing parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>tUQxN (cycles)</td>
</tr>
<tr>
<td>tUQ Calibration Type</td>
</tr>
<tr>
<td>tUQxCE (cycles)</td>
</tr>
<tr>
<td>tUQpower (cycles)</td>
</tr>
<tr>
<td>Enable User tQ Calibration Controls</td>
</tr>
<tr>
<td>Automatic tQ Calibration Period (us)</td>
</tr>
</tbody>
</table>
The following figure shows controller configuration settings for the DDR4 memory.

**Figure 48 • DDR4 Configurator—Controller**

The following figure shows miscellaneous configuration settings for the DDR4 memory.

**Figure 49 • DDR4 Configurator—Misc**
Appendix: References

This section lists documents that provide more information about the PCIe EndPoint and IP cores used in the reference design.

- For more information about PolarFire transceiver blocks, PF_TX_PLL, and PF_XCVR_REF_CLK, see UG0677: PolarFire FPGA Transceiver User Guide.
- For more information about PF_PCIE, see UG0685: PolarFire FPGA PCI Express User Guide.
- For more information about PF_CCC, see UG0684: PolarFire FPGA Clocking Resources User Guide.
- For more information about DDR3/DDR4 memory, see UG0676: PolarFire FPGA DDR Memory Controller User Guide.
- For more information about Libero, ModelSim, and Synplify, see the Microsemi Libero SoC PolarFire web page.
- For more information about PolarFire FPGA Evaluation Kit, see UG0747: PolarFire FPGA Evaluation Kit User Guide.
- For more information about PolarFire FPGA Splash Kit, see UG0786: PolarFire FPGA Splash Kit User Guide.
- For more information about CoreAHBLite, see CoreAHBLite Handbook.
- For more information about CoreAHBtoAPB3, see CoreAHBtoAPB3 Handbook.
- For more information about CoreUART, see CoreUART Handbook.