UG0752
User Guide
PolarFire FPGA Power Estimator

a Microchip company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Features were updated to show the most recent version of the Power Estimator.

1.2 Revision 3.0

Features were updated to show the most recent version of the Power Estimator.

1.3 Revision 2.0

Features were updated to show the most recent version of the Power Estimator.

1.4 Revision 1.0

Revision 1.0 is the first publication of this document.

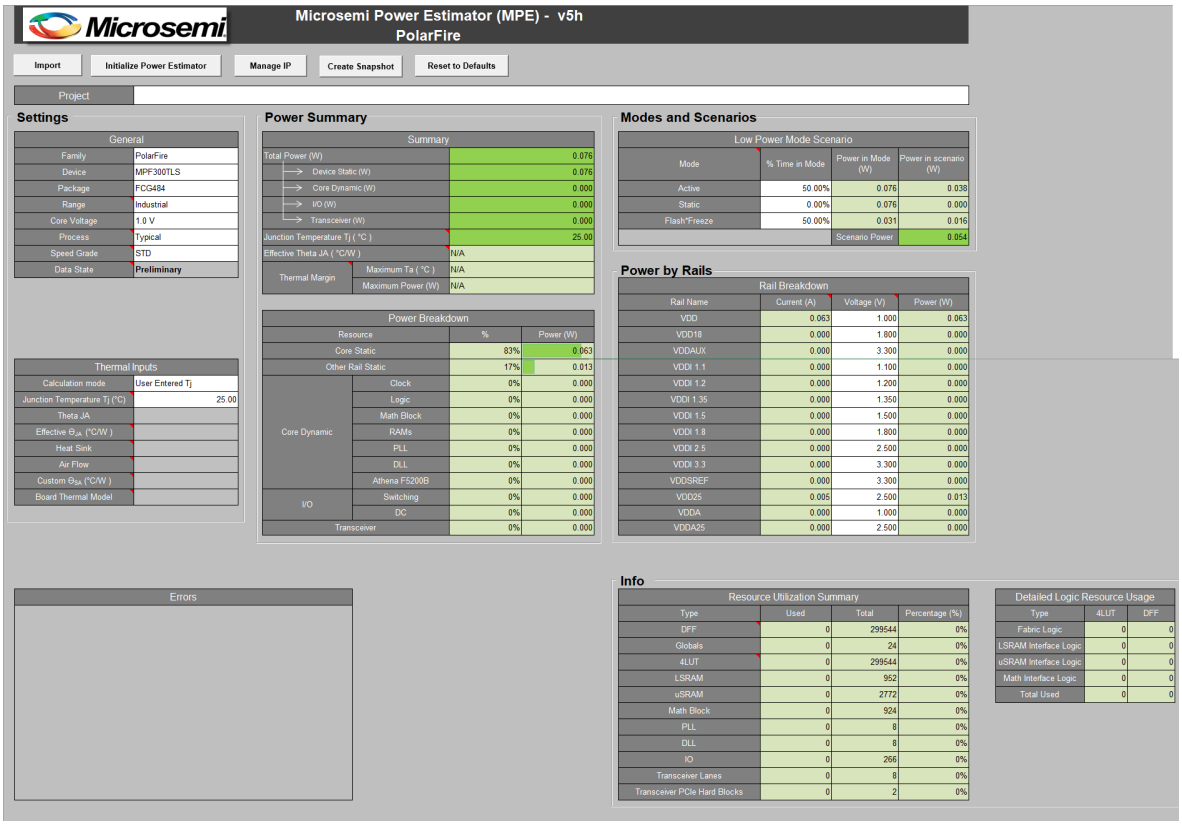
2 Introduction

Early power estimation helps designers define the design architecture within the power budget by applying suitable power saving strategies. It also helps board designers make informed decisions about the power supplies and heat sink to be used for the application. Microsemi Power Estimator (MPE) PolarFire® is a spreadsheet-based tool that enables designers to estimate the power consumption of PolarFire FPGAs from design concept to design implementation. It provides thermal analysis, as well as information about the contribution of various factors in the total power consumption of an FPGA. Operating frequencies, device resources, clock resources, toggle rates, and other parameters are first entered into the Power Estimator. These parameters are then combined with pre-determined power models based on simulation and characterized device data to estimate power consumption. The following are the key features of the Power Estimator:

- Simple GUI elements integrated into a worksheet for quick power estimation
- Power estimation during active, standby, and Flash*Freeze power modes
- Power estimation using scenarios
- Separate worksheets with power estimation for specific device features
- Calculation of junction temperature based on user-specified thermal inputs
- Ability to create snapshots for future reference and data backup

The accuracy of power estimation depends on the settings and data entered in the tool, so it is important to enter realistic data. Also, the Power Estimator results are an early estimation of power consumption rather than measured data. Actual power consumption depends on the actual RTL design, place-and-route, and operating conditions. It is recommended to use the Power Estimator for early-stage power estimation and use the SmartPower for Libero® SoC tool for accurate and detailed power estimation for designs after place-and-route. For more information about SmartPower for Libero SoC, see *SmartPower for Libero SoC PolarFire Software*.

Figure 1 • **Microsemi Power Estimator PolarFire**



3 Getting Started with Power Estimator

This section describes the system requirements for using the Power Estimator, the process to download the Power Estimator, and input requirements to maximize the accuracy of Power Estimator results.

3.1 System Requirements

The following are the minimum software requirements for using the Power Estimator:

- Microsoft Excel 2003, 2007, 2010, or 2013
- A Windows operating system that supports the above versions of Microsoft Excel

Note: OpenOffice spreadsheets and Google Sheets are not supported.

3.2 Downloading Power Estimator and Enabling Macros

The latest version of the Power Estimator is available for download on the Microsemi *Power Estimators and Calculators* web page.

The Power Estimator workbook has several built-in macros. By default, the macro security level in Microsoft Excel is set to *high*, which automatically disables macros. To allow macro execution (required for the Power Estimator to function properly), open the Power Estimator workbook and perform the following steps.

In Microsoft Excel 2010 and 2013:

1. Click **File** > **Options**.
2. Click **Trust Center** in the left pane, and then click **Trust Center Settings**.
3. Click **Macro Settings** in the left pane, and select **Enable all macros**.
4. Click **OK.**

In Microsoft Excel 2007:

1. Click the Office button, and click **Excel Options**.
2. Click **Trust Center** in the left pane, and then click **Trust Center Settings**.
3. Click **Macro Settings** in the left pane, and select **Enable all macros**.
4. Click **OK.**

In Microsoft Excel 2003:

1. Click **Tools** > **Macro** > **Security**.
2. Click **Security Level**, and select **Medium**.
3. Click **OK.**

After performing these steps, close the Power Estimator workbook and reopen it. In the security notification that appears at the top, click **Enable this content** or **Enable Macros** (as applicable) to start using the workbook.

3.3 Input Requirements

The power consumption of an FPGA depends largely on the number of logic elements in the FPGA fabric. The following details must be as close as possible to the actual design for reasonably accurate power estimation:

- Device, package, and operating conditions
- Number of flip-flops, LUTs, LSRAM blocks, µSRAM blocks, math blocks, and I/Os
- High-speed serial (HSS) interface and double data rate (DDR) interface details
- System clock and clock domain information
- Logic and I/O toggle rates
- Enable and write rates of the RAM

4 Using the Power Estimator Workbook

This section describes how to provide inputs for power estimation and view the power estimation results for the FPGA as a whole, as well as for individual features of the FPGA. It also provides a recommended flow for using the Power Estimator.

4.1 Power Estimator User Interface

The Power Estimator workbook has a Summary worksheet, which provides an at-a-glance view of the power estimation, and feature-specific worksheets that provide more detailed information about specific design resources. All the cells in the workbook are color coded to indicate their edit ability and the type of data they contain.The toolbar available in the Summary worksheet of the Power Estimator has simple GUI buttons to import and reset data, initialize power estimation, capture snapshots of Power Estimator data, and manage design IP.

4.1.1 Color Coding

In order to input the data required for power estimation and interpret the results of the Power Estimator, it is important to understand the color codes used in the Power Estimator workbook. The workbook has several worksheets, and the cells in each worksheet are color coded to simplify data entry and review. The following table shows the color codes used in the workbook.

Table 1 • **Power Estimator Color Codes**

Cell Color	Description
White	Editable field where data can be entered. Editable fields in the Settings section are mandatory.
Gray	Non-editable, description field.
Light Gray	Field not applicable because of selections made in other, related fields.
Green	Read-only, computed, summary value.
Light green	Read-only, computed, individual value.
Red	Input error. Details of the error can be found in the Errors section of the Summary worksheet.

4.1.2 Power Estimator Worksheets

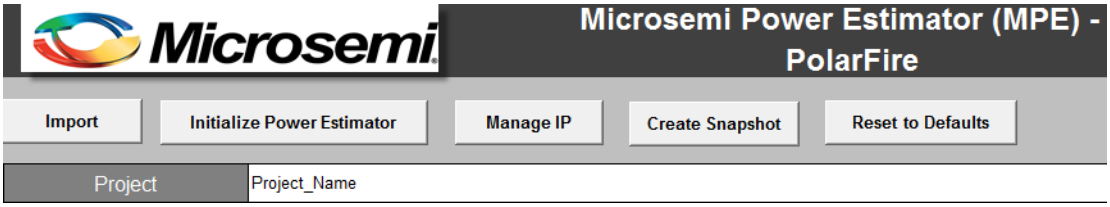
The following worksheets are available in the Power Estimator workbook:

- **Summary:** This is the first worksheet in the workbook. It allows you to input the device settings, modes and scenarios, and power rail details. It displays total power, as well as power breakdown by rails and resources. It also displays any errors that may exist in the data entered in any of the worksheets.
- **Snapshot:** This worksheet displays power consumption data captured at various points in time for future reference. A maximum of 10 snapshots can be saved. For more information, see Create Snapshot, **page 11**.
- **Feature-specific worksheets:** These worksheets contain power and utilization data for specific device features such as clocks, logic, LSRAM, µSRAM, transceivers, I/Os, PLLs and DLLs, and security blocks.
- **User:** This is a blank worksheet where any calculations can be performed and notes entered.
- **Release:** This worksheet contains release notes for all the versions of the Power Estimator, starting with the most current release.

4.1.3 MPE Toolbar

The MPE toolbar at the top of the Summary worksheet provides options for quick import and entry of resource and IP data and allows you to optionally enter a project name.

Figure 2 • **MPE Toolbar**

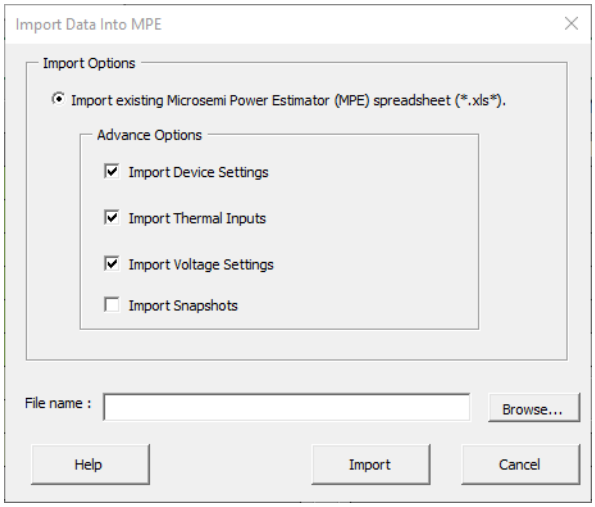


The following sections describe each of the MPE toolbar buttons.

4.1.3.1 Import

The Import button opens the Importing Data Into MPE wizard, which allows you to select an existing Power Estimator worksheet and import data from it. You can either choose to import all data or import specific data using the check box available under Advance Options, as shown in the following figure.

Figure 3 • **Import Data Into MPE Wizard**



4.1.3.2 Initialize Power Estimator

The Initialize Power Estimator button opens the Initialize Power Estimator wizard where basic design data such as system clock frequency, number of design resources, I/O technology, and toggle rate can be entered for quick and easy power estimation. For more information, see Initializing Power Estimation, page 16.

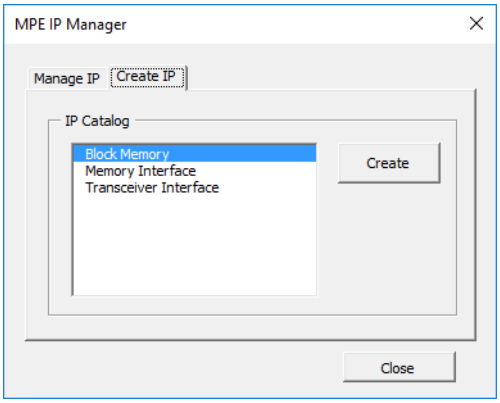
4.1.3.3 Manage IP

The Manage IP button opens the MPE IP Manager wizard, which allows you to add and delete any IP used in the design to the Power Estimator input data. Based on the details entered, values are automatically populated in the various feature-specific tabs, and the Power Estimator results are updated to include the resources consumed by the IP. The IP Manager wizard consists of the following two tabs:

- **Create IP:** creates memory and transceiver interface IP
- **Manage IP:** deletes previously created IP

The following figure shows the MPE IP Manager wizard.

Figure 4 • **MPE IP Manager Wizard**



Using the Create IP tab, you can create three types of IP: memory interface, transceiver interface, and block memory configuration (as shown in the preceding figure). The following figures show the MPE Memory Interface Configuration, MPE Transceiver Interface Configuration, and MPE block memory configuration windows that open when you select **Memory Interface**, **Transceiver Interface**, and **Block Memory** configuration respectively, in the IP catalog and click **Create**.

Figure 5 • **MPE Memory Interface Configuration Wizard**

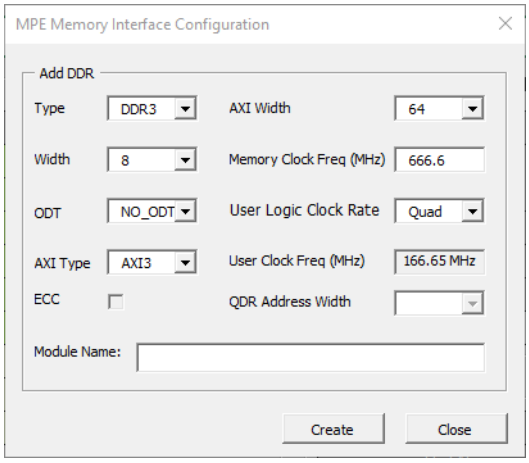


Figure 6 • **MPE Transceiver Interface Configuration Wizard**

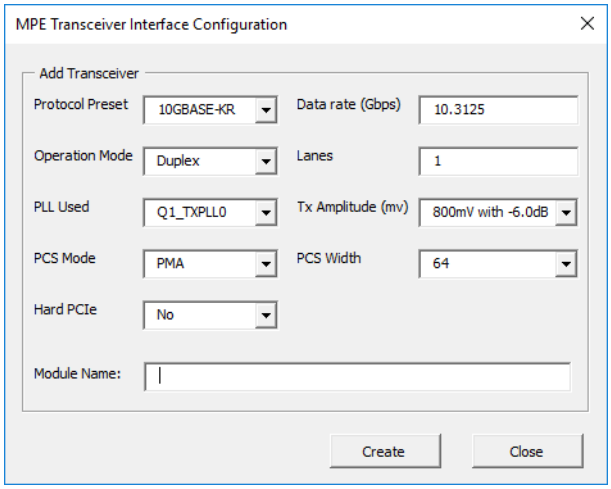


Figure 7 • **MPE Block Memory Configuration—LSRAM**

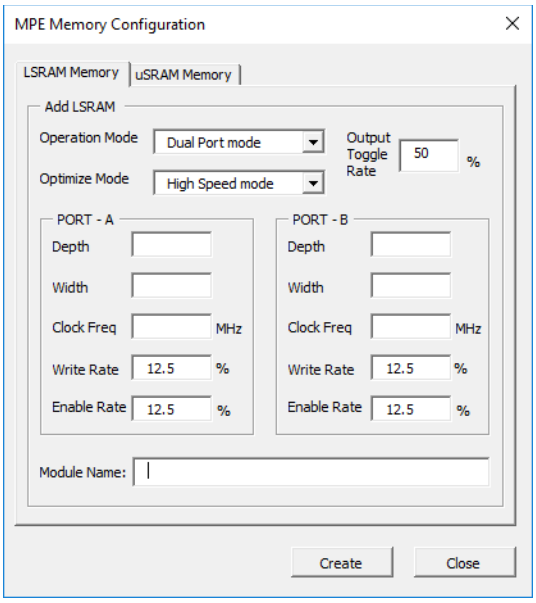
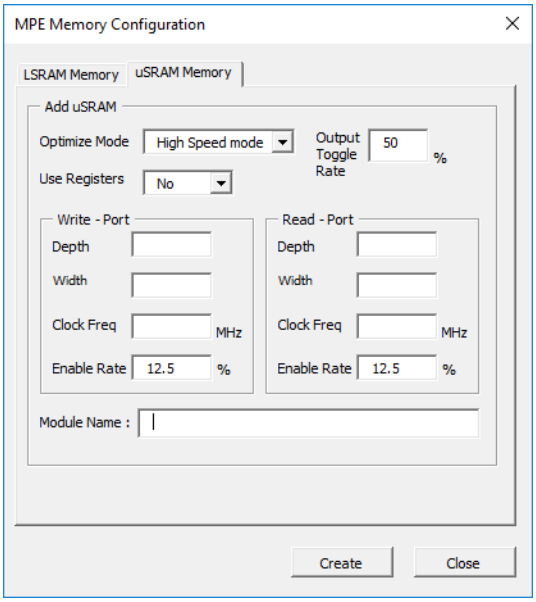


Figure 8 • **MPE Block Memory Configuration—µSRAM**



The following table lists the parameters required for creating an IP using the MPE IP Manager.

Table 2 • **Parameters Required for Creating IP**

IP	Parameter	Description
Memory Interface	Type	DDR memory type. Available options are DDR3, LPDDR3, QDR, and DDR4.
	Width	Memory interface width. Available options are 8, 16, 32, and 64 bits for DDR3 and DDR4; 16 and 32 bits for LPDDR3; 9, 18, and 36 bits for QDR.
	ODT	Input on-die termination (ODT) impedance in ohms.
	AXI Type	AXI interface type. Available options are AXI3 and AXI4.
	ECC	Enable correction code (ECC) status. Select or deselect the checkbox to indicate whether ECC is enabled.
	AXI Width	AXI interface width. Automatically selected based on the memory width.
	Memory Clock Freq (MHz)	Memory clock frequency.
	User Logic Clock Rate	User logic clock rate.The Quad option is automatically selected.
	User Clock Freq (MHz)	User clock frequency. Automatically populated based on other memory parameters.
	Module Name	Name of the memory interface module.
QDR address width	Width	Address width of QDR memory. Available options are 18, 19, 20, and 21

Table 2 • **Parameters Required for Creating IP** ***(continued)***

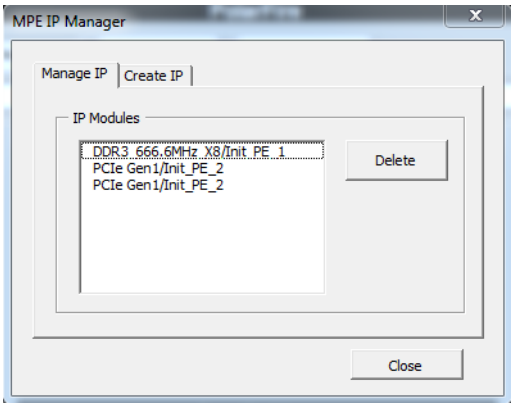
IP	Parameter	Description
Transceiver Interface	Protocol Preset	Protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
	Operation Mode	Hardware configuration mode used for the transceiver block. Available options are duplex, transmitter, and receiver.
	PLL Used	PLL that provides the clock for the transceiver block.
	PCS Mode	PCS interface mode that connects the transceiver PMA to the FPGA fabric, and provides data, control, and status signaling to the fabric IP. Available options are: – PMA – 8b/10b – PIPE – 64b/66b – 64b/67b
	Hard PCIe	Hard PCIe usage status. Choose **Yes** if hard PCIe is used for the transceiver block. Choose **No** if soft PCIe is used. Applies to PCIe Gen1 and Gen2 protocols only.
	Data Rate (Gbps)	Rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps.
	Lanes	Number of transceiver lanes in the transceiver block.
	Tx Amplitude (mV)	Transmit (TX) driver's differential swing amplitude.
	PCS Width	PCS width. Automatically selected based on the PCS mode (protocol preset). If the protocol supports multiple widths, the desired width can be manually selected.
	Module Name	Name of the transceiver interface module.

Table 2 • **Parameters Required for Creating IP** ***(continued)***

IP	Parameter	Description
Block memory configuration: LSRAM	Operation mode	Select the operating mode of LSRAM—Dual Port mode or Two Port mode.
	Optimize mode	Select the optimize mode of LSRAM—Low power or High speed.
	Output toggle rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
	Depth	Enter the depth of LSRAM required
	Width	Enter the width of LSRAM required
	Clock frequency	Enter the clock frequency for A and B ports of the block memory.
	Write rate	Enter the percentage of time for A and B ports, which are used for write operations. It implies that the time not used for write operations is used for read operations.
	Enable rate	Enter the average percentage of time for ports A and B are enabled.
	Module name	Name of the block memory
Block memory configuration: USRAM	Optimize mode	Select the optimize mode of USRAM—Low power or High speed.
	Output toggle rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
	Use registers	Choose **Yes** if you want to implement µSRAMS as registers. Else choose **No**.
	Depth	Enter the depth of µSRAM required
	Width	Enter the width of µSRAM required
	Clock frequency	Enter the clock frequency for read and write ports
	Enable rate	Enter the percentage of time, the write and read ports are enabled.
	Module name	Name of the block memory

After the IP is created, the IP module is listed on the Manage IP tab, as shown in the following figure.

Figure 9 • **MPE IP Manager IP Modules List**



To delete an IP, select the IP, and click **Delete**.

4.1.3.4 Create Snapshot

The Create Snapshot button captures a snapshot of the current power estimation data and saves it for future reference. The saved data appears in the Snapshot worksheet as shown in the following figure. A maximum of 10 snapshots can be saved in the Power Estimator. If this number is exceeded, a message is displayed asking you to delete a worksheet before saving another snapshot.

Figure 10 • **Snapshot Worksheet**

Create Snapshot		Restore	delete	Restore	delete	Restore	delete
Snapshot Name		Snapshot 1		Snapshot 2		Snapshot 3	
Summary							
Total Power (W)		2.742		2.264		2.226	
→ Device Static (W)		0.578		0.105		0.066	
→ Core Dynamic (W)		1.450		1.445		1.445	
→ IO (W)		0.268		0.268		0.268	
→ Transceiver (W)		0.447		0.447		0.447	
Junction Temperature Tj (°C)		80.17		34.91		10.00	
Effective Theta JA (°C/W)		11.00		11.00		N/A	
Thermal Margin	Maximum Ta (°C)	66.10		71.25		N/A	
	Maximum Power (W)	4.55		8.18		N/A	
General							
Family		PolarFire		PolarFire		PolarFire	
Device		MPF500T		MPF200T		MPF300TS	
Package		FULLPKG		FULLPKG		FCG1152	
Range		Extended		Extended		Industrial	
Thermal Inputs							
Calculation mode		Estimated Tj		Estimated Tj		User Entered Tj	
Junction/Ambient Temperature		50		10		10	
Theta JA		Custom Theta JA		Custom Theta JA		N/A	
Effective ΘJA		11		11		N/A	
Power Breakdown		%	Power (W)	%	Power (W)	%	Power (W)
Device Static		20%	0.562	4%	0.091	2%	0.053
Other Rail Static		1%	0.016	1%	0.013	1%	0.013
Core Dynamic	Clock	15%	0.410	18%	0.405	18%	0.405
	Logic	22%	0.597	26%	0.597	27%	0.597
	Math Block	6%	0.161	7%	0.161	7%	0.161
	RAMs	10%	0.276	12%	0.276	12%	0.276
	PLL	0%	0.007	0%	0.007	0%	0.007
	DLL	0%	0.000	0%	0.000	0%	0.000
	Athena F5200B	0%	0.000	0%	0.000	0%	0.000
IO	Switching	3%	0.078	3%	0.078	4%	0.078
	DC	7%	0.189	8%	0.189	9%	0.189
Transceiver		16%	0.447	20%	0.447	20%	0.447

To delete a snapshot that is no longer required, click the Delete button corresponding to the snapshot you want to delete. To restore the current Power Estimator data to that associated with a specific snapshot, click the Restore button corresponding to the snapshot.

4.1.3.5 Reset to Defaults

The Reset to Defaults button opens a window with the following options to reset the data in the Power Estimator workbook to default values:

- **Reset Data:** Resets the data in feature-specific worksheets only.
- **Reset all settings:** Resets the data in the Summary worksheet and the feature-specific worksheets.
- **Reset all settings and snapshots:** Resets all the data in the workbook including the Summary and Snapshot worksheets.

Note: You can also reset existing data (from feature-specific worksheets only) using the Initialize Power Estimator wizard. For more information, see Initializing Power Estimation, page 16.

4.2 Recommended Flow

The following is the sequence of steps recommended for estimating power using the Power Estimator:

1. **Settings:** Select the basic settings, that is, the device, package, temperature grade, operating conditions, and thermal inputs. For more information, see Configuring Basic Settings, page 12.
2. **Modes and scenarios (optional):** Enter the percentage of the device operational time in various modes, for example, 50% in active mode and 50% in Flash*Freeze mode. For more information, see Selecting Modes and Scenarios, page 15.
3. **Initialization:** Click the Initialize Power Estimator button in the MPE toolbar, and enter design-specific data to initialize power estimation. For more information, see Initializing Power Estimation, page 16.
4. **Power Estimation Results:** View the values populated in the Summary worksheet and the feature-specific worksheets. For more information, see Viewing and Analyzing Power Estimator Results, page 25.

Note: If the design uses multiple modules, after selecting parameters in the Initiate Power Estimation wizard, enter the details of additional modules in the appropriate feature-specific worksheets for accurate power estimation. For more information, see Entering Feature-Specific Data, page 18.

4.3 Providing Inputs for Power Estimation

This section describes how to provide general and thermal inputs, select modes and scenarios, and initialize power estimation.

4.3.1 Configuring Basic Settings

The first step for estimating power is to enter the design settings in the Summary worksheet of the Power Estimator workbook. The settings are classified into general settings and thermal inputs. The following table describes each of the settings.

Table 3 • **General Settings and Thermal Inputs**

Setting	Description
General Settings	
Family	Device family. This is automatically selected as PolarFire.
Device	Device part number. Available options are MPF100T, MPF100TS, MPF100TL, MPF100TLS. MPF200T, MPF200TS, MPF200TL, MPF200TLS, MPF300T, MPF300TS, MPF300TL, MPF300TLS, MPF300XT, MPF500T, MPF500TS, MPF500TL, and MPF500TLS.
Package	Device package. Available options vary per device.
Range	Product grade. Select **Industrial** for industrial applications (-40° C to 100° C temperature range) and **Extended** for other applications (0° C to 100° C temperature range).
Core Voltage	Core voltage used for the design. PolarFire devices support 1.0 V and 1.05 V core voltage.

Table 3 • **General Settings and Thermal Inputs *(continued)***

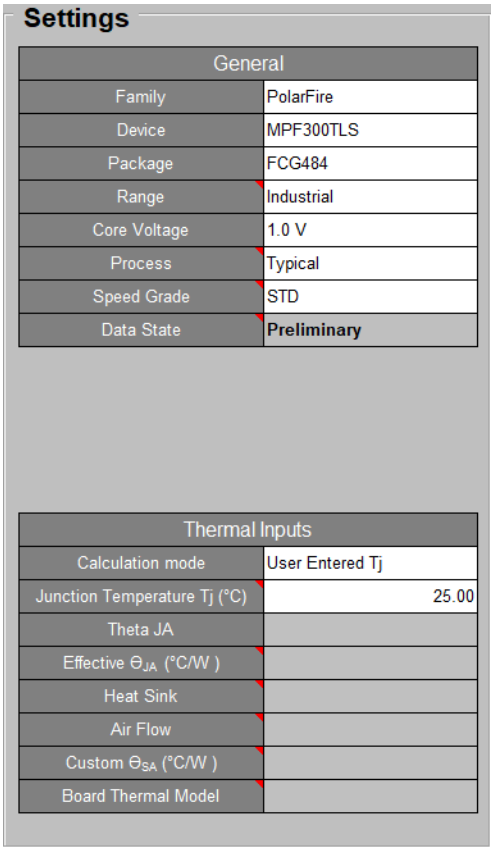
Setting	Description
Process	Manufacturing process variations for the design. Available options are: **Typical:** uses the average power dissipation factor of the resources used in the design. **Maximum:** uses the highest power dissipation factor from the resources used in the design.
Speed Grade	Speed grade used in the design. Available options are: STD and -1. The speed grade has a significant impact on the quiescent current for some devices. Specifying a speed grade helps estimate quiescent current more accurately.
Data State	Readiness level of the data entered as inputs. Available options are: **Advance:** Initial, estimated data based on simulation, other products, and speed grades. Cannot be used for production. **Preliminary:** Data based on simulation and/or initial characterization. Information is likely to be correct, but changes are possible. **Production:** Data considered to be final. In this data state, we recommend using SmartPower for Libero SoC instead of Power Estimator.
Thermal Inputs	
Calculation mode	The method of calculation of junction temperature. Available options are: **User Entered Tj:** allows the user to specify the junction temperature. **Estimated Tj:** calculates junction temperature based on user-specified thermal inputs that are enabled when this option is selected.
Junction Temperature Tj (°C)	User-specified junction temperature of the device. Applicable only if User Entered Tj is selected as the calculation mode.
Ambient Temperature Ta (°C)	Temperature of the air surrounding the device. Applicable only if Estimated Tj is selected as the calculation mode. Calculates junction temperature based on power dissipation and either thermal resistance or effective θJA, depending on the option selected for Theta JA.
Theta JA	Applicable only if Estimated Tj is selected as the calculation mode. Available options are: **Custom Theta JA:** allows a custom effective Theta Ja to be entered. **Estimated Theta JA** (for future release)**:** enables the Heat Sink, Air Flow, Custom θ SA (°C/W), and Board Thermal Model fields and estimates the effective Theta JA based on the values entered.
Effective θJA (°C/W)	Effective thermal resistance calculated based on user-specified device, package, air flow, heat sink, and board model inputs, and pre-determined characterization and simulation data. Applicable only if Estimated Tj is selected as the calculation mode. In conditions not covered by the available options or where extensive thermal remodeling is done, a custom value can be entered by selecting Custom Theta JA in the Theta JA field.
Heat Sink	Heat sink selection from standard profiles based on device package and air flow. To enter a custom value, select the Custom option.

Table 3 • **General Settings and Thermal Inputs *(continued)***

Setting	Description
Air Flow (for future release)	Ambient air flow in meters per second (m/s), which, when increased, reduces the junction temperature, and when reduced, increases the junction temperature. Applicable only if both Estimated TJ and Estimated Theta JA are selected. Available options are Still Air (meaning no air flow), 1.0 m/s, and 2.5 m/s.
Custom θSA (°C/W) (for future release)	User-specified heat sink-to-ambient thermal resistance. Applicable only if both Estimated TJ and Estimated Theta JA are selected. To enter a custom value, select the Custom option in the Heat Sink field.
Board Thermal Model (for future release)	The thermal model of the board. Applicable only if both Estimated TJ and Estimated Theta JA are selected. Available options are: **None:** assumes that no heat is dissipated through the board. **JEDEC (2s2p):** assumes that the board has characteristics of the JEDEC 2s2p test board specified in the JESD51-9 standard.

The following figure shows the General Settings and Thermal Inputs sections of the Power Estimator.

Figure 11 • **General Settings and Thermal Inputs**



4.3.2 Selecting Modes and Scenarios

The Power Estimator allows you to optionally specify the percentage of time the device spends in active, static, and Flash*Freeze modes, and uses this information to calculate the power consumption in the specified scenario.

Based on the values entered in the % Time in Mode column, the following values are calculated for each mode:

- **Power in Mode (W):** Shows the power consumed in the mode assuming 100% of the time was spent in the same mode.
- **Power in Scenario (W):** Shows the power consumed in the mode taking into account the percentage of time specified for that mode.

Note: If the percentage across modes exceeds 100, an error is displayed.

The following figure shows the Modes and Scenarios section of the Power Estimator.

Figure 12 • **Modes and Scenarios**

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (W)	Power in scenario (W)
Active	50.00%	0.081	0.040
Static	25.00%	0.068	0.017
Flash*Freeze	25.00%	0.031	0.008
		Scenario Power	0.065

4.3.3 Entering Rail Voltages

Depending on the device, package, and design resources used, the Power Estimator automatically populates the voltages for applicable power supplies in the Power by Rail section of the Summary worksheet. You can manually change the voltage values (within acceptable ranges) to calculate power supply at different voltages. Based on the voltage entered for each supply, the current requirement (Current (A)) and the estimated power consumption (Power (W)) of the supply are automatically calculated, as shown in the following figure.

Figure 13 • **Power by Rail Section**

Power by Rails

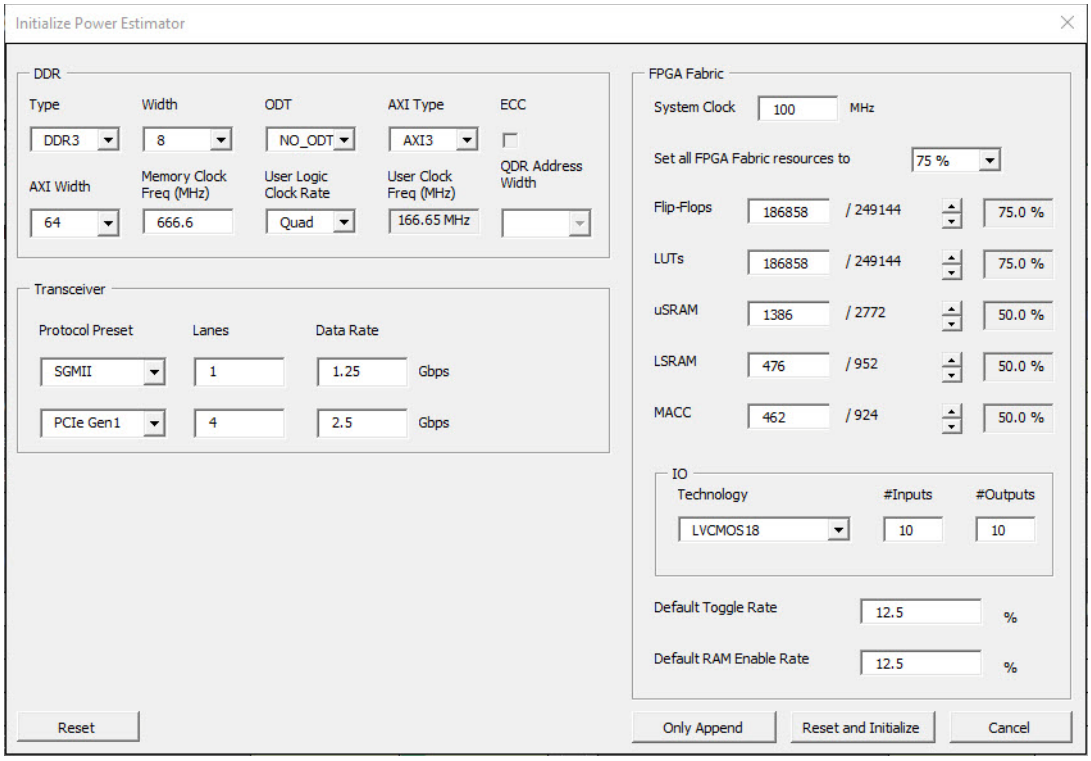
Rail Breakdown			
Rail Name	Current (A)	Voltage (V)	Power (W)
VDD	0.070	1.000	0.070
VDD18	0.000	1.800	0.000
VDDAUX	0.000	3.300	0.000
VDDI 1.1	0.000	1.100	0.000
VDDI 1.2	0.000	1.200	0.000
VDDI 1.35	0.000	1.350	0.000
VDDI 1.5	0.000	1.575	0.000
VDDI 1.8	0.000	1.800	0.000
VDDI 2.5	0.000	2.500	0.000
VDDI 3.3	0.000	3.300	0.000
VDDSREF	0.000	3.300	0.000
VDD25	0.005	2.500	0.013
VDDA	0.000	1.000	0.000
VDDA25	0.000	2.500	0.000

4.3.4 Initializing Power Estimation

After entering the settings, click the Initialize Power Estimator button on the MPE toolbar, and enter applicable design-specific values in the Initialize Power Estimator wizard. Based on the inputs provided in the wizard, design data is automatically populated in the feature-specific worksheets (such as Clock, Logic, and LSRAM) of the Power Estimator workbook. Entries thus populated can be edited from the feature-specific worksheets to provide more accurate inputs for power estimation, including module names and additional rows of data that were not entered when initiating power estimation. For more information, see Entering Feature-Specific Data, page 18.

The following figure shows the Initialize Power Estimator wizard.

Figure 14 • **Initialize Power Estimator Wizard**



The following table lists the parameters available in the Initialize Power Estimator wizard.

Table 4 • **Initialize Power Estimator Wizard Fields**

Parameter	Sub-Parameter	Action
DDR	Type	Choose the DDR memory type. Available options are DDR3 and DDR4.
	Width	Choose the memory interface width.
	ODT	Specify the input on-die termination impedance in ohms.
	AXI Type	Choose the AXI interface type. Available options are AXI3 and AXI4.
	ECC	Check to enable correction code. Available only for 32- and 64-bit memory interface width.
	AXI Width	Choose the AXI interface width.
	Memory Clock Freq (MHz)	Enter the memory clock frequency.
	User Logic Clock Rate	The user logic clock rate type is automatically selected as **Quad**.
	User Clock Freq (MHz)	The user clock frequency is automatically populated based on other memory parameters.
QDR	QDR address width	Address width of QDR memory. Available options are 18, 19, 20, and 21
Transceiver	Protocol Preset	Choose a protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
	Lanes	Enter the number of transceiver lanes in the block.
	Data Rate	Enter the rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps.

Table 4 • **Initialize Power Estimator Wizard Fields *(continued)***

Parameter	Sub-Parameter	Action
FPGA Fabric	System Clock	Enter the fabric clock frequency. Default value: 100 MHz Valid range: 0 to 400 MHz
	Set all FPGA Fabric resources to	Use this list to choose a single design utilization percentage for all fabric resources. Available values are 25%, 50%, 75%, and 100%. If necessary, the utilization of individual resources can be edited using the up and down arrows provided for each resource.
	Flip-flops	Enter the number of flip-flops used in the design, or choose the percentage of overall design resources used by flip-flips.
	LUTs	Enter the number of LUTs used in the design, or choose the percentage of overall design resources used by LUTs.
	µSRAM	Enter the number of µSRAM blocks used in the design, or choose the percentage of overall design resources used by µSRAM blocks.
	LSRAM	Enter the number of LSRAM blocks used in the design, or choose the percentage of overall design resources used by LSRAM blocks.
	MACC	Enter the number of math blocks used in the design, or choose the percentage of overall design resources used by math blocks.
IO	Technology	Select the I/O standard used in the design from the list of available standards.
	Inputs	Enter the number of inputs in the design.
	Outputs	Enter the number of outputs in the design.
Default Toggle Rate		Enter a default toggle rate for the design resources.
Default RAM Enable Rate		Enter a default RAM enable rate for µSRAM and LSRAM.

After entering the data, to append the data to existing data in the various worksheets of the Power Estimator workbook, click **Only Append**. To clear the existing resource data and replace it with fresh data entered in the wizard, click **Reset and Initialize**.

4.3.5 Entering Feature-Specific Data

The Initiate Power Estimator wizard is designed to collect basic design data required for power estimation. To add module names and additional rows of data that are not supported by the Initialize Power Estimator wizard, use the worksheet specific to each device feature. The following sections provide information about each feature-specific worksheet in the Power Estimator workbook.

4.3.5.1 Clocks

Details of clocks used in the design are entered in the Clock worksheet. PolarFire devices support various clock networks such as global clock networks, bank clock networks, input/output regional clock networks (ICLK), and local regional clock networks (LCLK). Each row in the Clock worksheet is associated with a separate clock domain. Based on the values entered, the power consumption of each clock domain is populated in the Power (W) column.

The following table lists the parameters required for each clock domain in the Clock worksheet.

Table 5 • **Clock Worksheet Parameters**

Parameter	Action
Name	Enter the name of the clock domain.
Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks: 0 to 1250 MHz.
Clock Type	Choose the clock type: Global, Regional (ICLK), Regional (LCLK), or Bank Clock.
Fanout	Enter the number of registers and other synchronous elements (LSRAM, µSRAM, math blocks and I/Os) clocked in the design. Not applicable to bank clocks.
Clock Buffer Enable Rate	Enter the average percentage of time the entire clock tree is active for the clock domain. A 100% clock buffer enable rate means that the clock tree is toggled at the clock frequency.

For more information about the clocking resources in PolarFire FPGAs, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

4.3.5.2 Logic

Each row in the Logic worksheet represents a separate logic module. Based on the values entered, the power consumption of the logic in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the Logic worksheet.

Table 6 • **Logic Worksheet Parameters**

Parameter	Action
Name	Enter the name of the logic module.
Clock Frequency (MHz)	Enter the clock domain frequency. Valid ranges are: For global clocks, ICLK, and LCLK: 0 to 550 MHz. For bank clocks, 0 to 1250 MHz.
Number of DFF	Enter the number of D-flip-flops (sequential modules) used in the module.
Number of 4LUT	Enter the number of 4-input LUTs used in the module.
Design Complexity	Enter the average fanout of nets driven by the registers and LUTs in the module.
Toggle Rate	Enter the toggle rate for the registers and LUTs in the module.

For more information about PolarFire FPGA fabric logic, see *UG0680: PolarFire FPGA Fabric User Guide*.

LSRAM

Each row in the LSRAM worksheet represents a separate logic module. Based on the values entered, the power consumption of LSRAM blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the LSRAM worksheet.

Table 7 • **LSRAM Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the LSRAM block(s).
Number of LSRAM blocks	Enter the number of LSRAM blocks used in the module.
Width	Enter the data width of each RAM port. Available options are 1, 2, 5, 10, 20, 32, and 40. For mixed-width RAMs, use a larger port width for a conservative estimate.
Clock Frequency (MHz)	Enter the clock frequency for ports A and B of the module in the column corresponding to each port. The maximum frequency supported is 450 MHz.
Write Rate	Enter the percentage of time ports; A and B are used for write operations in the column corresponding to each port. It is implied that the time that is not used for write operations is used for read operations.
Read Rate (1 - Write Rate)	Enter the percentage of time; ports A and B are used for read operations in the column corresponding to each port.
Write Mode	Different write modes—simple write, read before write, and write feed through
Enable Rate	Enter the average percentage of time ports A and B are enabled in the column corresponding to each port.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
Pipeline enable	Register pipeline can be enabled or disabled
ECC enable	ECC can be enabled or disabled

For more information about LSRAM support in PolarFire devices, see *UG0680: PolarFire FPGA Fabric User Guide*.

µSRAM

Each row in the µSRAM worksheet represents a separate logic module. Based on the values entered, the power consumption of µSRAM blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the µSRAM worksheet.

Table 8 • **µSRAM Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the µSRAM block(s).
Number of µSRAM blocks	Enter the number of µSRAM blocks used in the module.
Width	Enter the data width of each RAM port. The number can be any positive integer up to 12. For mixed-width RAMs, use a larger port width for a conservative estimate.

Table 8 • **µSRAM Worksheet Parameters *(continued)***

Parameter	Action
Use Registers	Select **Yes** or **No**, respectively, to enable and disable the use of registers.
Write Clock Frequency	Enter the clock frequency of the write port of the µSRAM blocks in the module.
Read Clock Frequency	Enter the clock frequency of the read port of the µSRAM blocks in the module.
Enable Rate	Enter the percentage of time the write and read ports are enabled in the column corresponding to each port.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.

For more information about µSRAM support in PolarFire devices, see *UG0680: PolarFire FPGA Fabric User Guide*.

4.3.5.3 Math Blocks

Details of math blocks used in the design are entered in the Math Block worksheet. Each row in this worksheet represents a separate logic module. Based on the values entered, the power consumption of math blocks in each module is populated in the Power (W) column.

The following table lists the parameters required for each module in the Math Block worksheet.

Table 9 • **Math Block Worksheet Parameters**

Parameter	Action
Name	Enter the name of the module containing the math block(s).
Clock Frequency (MHz)	Enter the clock domain frequency. Maximum frequency supported is 450 MHz.
Number of Math Blocks	Enter the number of math blocks used in the module.
Output Toggle Rate	Enter the average percentage of time the clock enable is active regardless of the activity on RAM data and address inputs.
Mode	Provide the mode of operation for the math block. The following modes are supported: – Normal-Multiplier – Normal-Multiplier-Accumulator – SIMD – DOTP
Pre Adder	Can be enabled or disabled
Pipelined input	Input data pipelining can be enabled or disabled
Pipelined output	Output data pipelining can be enabled or disabled

For more information about math blocks in PolarFire devices, see *UG0680: PolarFire FPGA Fabric User Guide*.

4.3.5.4 I/Os

Details of I/O blocks used in the design are entered in the IO worksheet. Each row in the IO worksheet represents a separate I/O bus or module. Based on the values entered for each module, power consumption of the VDD, VDD18, VDDAUX, and VDDI supplies, along with the total power consumption across supplies, is automatically populated.

The following table lists the parameters required for each module in the IO worksheet.

Table 10 • **IO Worksheet Parameters**

Parameter	Action
Name	Enter the name of the I/O bus or module.
Bank Type	Choose the bank type: HSIO, GPIO, or XCVR_REFCLK.
I/O standard	Choose the I/O standard from the list of available standards.
Input Pins[1]	Enter the number of input pins or input differential pairs used in the module.
Output Pins[1]	Enter the number of output pins or output differential pairs used in the module.
Bidir Pins[1]	Enter the number of bidirectional pins or bidirectional differential pairs used in the module.
Schmitt Trigger	Can be enabled or disabled for inputs pin or bidirectional pin
ODT	Select the input on-die termination (ODT) impedance in ohms. Available options are 60, 120, and NO_ODT.
Output Drive (mA) / Drive Impedance (Ω)	This setting is used for outputs or bidirectional IOs.
Slew Calibration	This setting is used for outputs and bidirectional IOs.
Output Load (pF)	Enter the capacitance of the board and the external components.
IOG Mode	If I/O gearing is not used, choose **Unused**. If it is used, choose from the list of available modes.
Clock (MHz)	Enter the clock domain frequency. Maximum frequency supported is 800 MHz.
Data Rate	Select the data rate for the I/Os in the module. For I/Os used as clocks, choose **Clock**. For others, choose **SDR** (single data rate) or **DDR** (double data rate).
Toggle Rate	Enter the toggle rate of the I/Os in the module.
Output Enable	Enter the percentage of time outputs are enabled in the module. For bidirectional I/Os, the input path is assumed to be active when outputs are disabled.

1. Differential pairs must be considered as a single pin.

For more information about I/O support in PolarFire FPGAs, see *UG0686: PolarFire PGA User I/O User Guide*.

4.3.5.5 Transceivers

Details of transceiver blocks used in the design are entered in the Transceiver worksheet. Because the PLLs in PolarFire FPGAs can drive up to four lanes, each row in the worksheet may represent either a single-lane or a multi-lane transceiver block. The number of lanes used must be specified for each block.

The following table lists the parameters required for each transceiver block in the Transceiver worksheet.

Table 11 • **Transceiver Worksheet Parameters**

Parameter	Action
Name	Enter the name of the transceiver block.
Protocol Preset	Choose a protocol to interface the fabric with the transceiver. Based on the selection, other fields such as PLL used, data rate, CTLE drive, PCS mode, PCS width, and hard PCIe are automatically populated (they can be manually changed by selecting from the available options, if necessary). Available options are: – PCIe Gen1 – PCIe Gen2 – 10GBase-KR – SGMII
Number of Lanes	Enter the number of transceiver lanes in the block.
Operational Mode	Choose the hardware configuration mode used for the transceiver block: Duplex, Transmitter, or Receiver.
Data Rate (Gbps)	Specify the rate of operation of the transceiver. Supported range is 0.5 Gbps to 12.7 Gbps.
PLL Used	Choose the PLL that provides the clock for the transceiver block. Q#_TXPLL0 and Q#_TXPLL1 can be used by a pair of adjacent transmit lanes with the adjacent transceiver quad lane blocks either above, below, or both above and below the PLL. Q#_TXPLL_SSC is used within the quad only.
DFE Enable	Choose **Yes** if differential feedback equalization (DFE), used in conjunction with CTLE to equalize channel response, is enabled for the transceiver block. Choose **No** if DFE is not enabled.
Eye Monitor Enable	Choose **Yes** if eye monitor (an on-device circuitry to visualize post-equalization signal quality in the receive (RX) path) is enabled for the transceiver block. Choose **No** if eye monitor is not enabled.
CTLE	Specify the number of CTLE drives. CTLE equalizes low-pass channel response and compensates high frequency losses in the channel, improving the quality of received signals. Available mapping factors are 0, 1, 2, and 3.
TX Amplitude (mV)	Enter the transmit (TX) driver's differential swing amplitude.
Mode	Choose the PCS interface mode that connects the transceiver PMA to the FPGA fabric and provides data, control, and status signaling to the fabric IP. Available options are: – PMA – 8b/10b – PIPE – 64b/66b – 64b/67b

Table 11 • **Transceiver Worksheet Parameters *(continued)***

Parameter	Action
Width	Choose the FPGA fabric interface width. Available options vary based on the protocol selected.
Hard PCIe	Choose **Yes** if hard PCIe is used for the transceiver block. Choose **No** if soft PCIe is used. Applies to PCIe Gen1 and Gen2 protocols only.

For more information about transceiver support in PolarFire FPGAs, see *UG0677: PolarFire FPGA Transceiver User Guide*.

4.3.5.6 PLLs and DLLs

PolarFire devices have two PLLs and two DLLs in each corner of the FPGA fabric to provide flexible clocking schemes for the logic implemented in the fabric. Details of the PLLs used in the fabric are entered in the PLL Power section and those of the DLLs are entered in the DLL Power section of the PLL & DLL worksheet. The following table lists the parameters required for each PLL or DLL in this worksheet.

Table 12 • **PLL & DLL Worksheet Parameters**

Parameter	Action
Name	Enter the name of the PLL or DLL module.
Reference Clock Frequency (MHz)	Enter the reference clock frequency for the PLL or DLL module.
Output0 Frequency (MHz)	Enter the frequency of output 0.
Output1 Frequency (MHz)[1]	Enter the frequency of output 1.
Output2 Frequency (MHz)[1]	Enter the frequency of output 2.
Output3 Frequency (MHz)[1]	Enter the frequency of output 3.
Mode[1]	Choose the PLL mode as low power or low jitter.

1. This parameter is applicable to PLLs only, and, therefore, does not appear in the DLL Power section.

For more information about PLLs and DLLs in PolarFire FPGAs, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

4.3.5.7 Security

PolarFire FPGAs support data security using an Athena TeraFire F5200B DPA-resistant cryptoprocessor. Details of this cryptoprocessor are entered in the **User Crypto** worksheet.

The following table lists the parameters required in the **User Crypto** worksheet.

Table 13 • **User Crypto Worksheet Parameters**

Parameter	Action
Clock Frequency (MHz)	Enter the clock domain frequency. Maximum value is 250 MHz.
Toggle Rate	Enter the toggle rate of the user crypto block.

For more information about the security features of PolarFire FPGAs, see *UG0753: PolarFire FPGA Security User Guide*.

4.4 Viewing and Analyzing Power Estimator Results

This section explains how to view and analyze the results of Power Estimator to optimize power for PolarFire FPGAs.

4.4.1 Viewing Power Estimation Data

Based on the data provided in the Initialize Power Estimator wizard and the feature-specific worksheets, power consumption is estimated and the results displayed in all the tabs. The following table lists the various power estimation views generated in the Power Estimator.

Table 14 • **Power Estimator Views**

View	Description	Worksheet and Section
Power by type	Provides device static and core dynamic power details	Summary worksheet – Power Summary section
Power by resource	Provides a consolidated view of power used by each device feature, such as clock, logic, and I/Os	Summary worksheet – Power Breakdown section
Power based on modes and scenarios	Provides power consumption based on the percentage of time spent in various operational modes	Summary worksheet – Modes and Scenarios section
Power by rail	Provides power breakdown for each voltage rail	Summary worksheet – Power by Rail section
Resource utilization	Provides the utilization rate for each device feature	Summary worksheet – Resource Utilization section Feature-specific worksheet – Utilization section
Power by hard block	Provides the power breakdown for transceiver hard blocks	Transceiver worksheet – Power (W) by Hard Block section

4.4.2 Analyzing Power Estimation Data

Proper analysis of the Power Estimator results can help balance your power and performance goals. Actions that can be taken based on the results vary based on the application's requirements and cost considerations. The following are the examples of design changes that can be made based on the Power Estimator results:

- Thermal inputs significantly affect the total power. If the total power exceeds the power margin, reduce the ambient temperature by installing a suitable heat sink, ensuring proper air flow, and using other cooling devices. You can check the total power at different ambient temperatures and heat sink/air flow settings using the Power Estimator.
- Choose a device suitable for the design based on the power margin and resource utilization. For example:
  - If the power exceeds marginal value and there are unused logic elements (that is, the resource utilization is significantly less than 100%), change the device to one that uses less logic elements.
  - If the resource utilization exceeds 100%, it means the device selected does not support the number of resources used in the design. In this case, choose a device with more logic elements to meet the design requirements.
- Choose the appropriate speed grade for the design based on your power and performance goals. A higher speed grade improves performance but leads to higher static power. To prevent unnecessary power costs, avoid using a speed grade higher than necessary for optimal performance of the application.

5 Appendix: Additional Documentation

This document assumes that the reader has a good understanding of the PolarFire device, is experienced in digital and analog board design, and knowledgeable in the electrical characteristics of systems. Background information on the key theories and concepts of FPGA design is available in *High Speed Digital Design: A Handbook of Black Magic*[1] and other industry literature. The following documents provide additional information about the PolarFire FPGA architecture and help use the Power Estimator effectively:

- *PO0137: PolarFire FPGA Product Overview*
- *DS0141: PolarFire FPGA Datasheet*
- *UG0726: PolarFire FPGA Board Design User Guide*
- *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*
- *UG0680: PolarFire FPGA Fabric User Guide*
- *UG0714: PolarFire FPGA Programming User Guide*
- *UG0684: PolarFire FPGA Clocking Resources User Guide*
- *UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide*
- *UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide*
- *UG0748: PolarFire FPGA Low Power User Guide*
- *UG0676: PolarFire FPGA DDR Memory Controller User Guide*
- *UG0743: PolarFire FPGA Debugging User Guide*
- *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*
- *UG0677: PolarFire FPGA Transceiver User Guide*
- *UG0685: PolarFire FPGA PCI Express User Guide*
- *UG0753: PolarFire FPGA Security User Guide*
- *UG0686: PolarFire FPGA User I/O User Guide*

1.Johnson, Howard, and Martin Graham, High Speed Digital Design: A Handbook of Black Magic. Prentice Hall PTR, 1993. ISBN-10 0133957241 or ISBN-13: 978-0133957242