UG0722
User Guide
PolarFire FPGA Packaging and Pin Descriptions

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Information about DDR lane for I/O CDR (SGMII interface) was added. See Table 4, page 8.
- Information about Package marking was added. See Package Marking, page 22
- Information about thermal resistances of PolarFire Package device was added. See Thermal Specifications, page 21.
- Information about packing and shipping was added. See Packing and Shipping, page 22.
- Added Table 3, page 8, Table 5, page 8, and Table 20, page 21.

1.2 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated Figure 5, page 5 and Figure 6, page 6.
- Information about unused condition of pins were updated. For more information, see Table 10, page 11, Table 14, page 14, Table 15, page 15, Table 16, page 15, Table 17, page 15, and Table 18, page 16.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 PolarFire FPGA Packaging and Pin Descriptions

This guide provides pin and packaging information (such as bank assignments and mechanical information) for PolarFire™ FPGAs.

PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see *UG0686: PolarFire FPGA User I/O User Guide*.

2.1 Packaging Overview

PolarFire FPGAs are available in multiple packages. Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. HSIO and GPIO banks have a maximum supply voltage of 1.8 V and 3.3 V, respectively.

The following table lists the PolarFire FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

Table 1 • **PolarFire FPGA Device and Package Combinations**

Device	I/O Type	Packages						
		FCG1152	FCG784	FCG484	FCVG484	FCSG536	FCSG325	FCSG325
	Pitch (mm)	1.0	1.0	1.0	0.8	0.5	0.5	0.5
	Size (mm)	35 × 35	29 × 29	23 × 23	19 × 19	16 × 16	11 × 11	11 × 14.5
MPF100	HSIO			96	120		84	
	GPIO			148	164		86	
	Total I/O			244	284		170	
	XCVR Lanes			8	4		4	
MPF200	HSIO		132	96	120	120		84
	GPIO		232	148	164	180		86
	Total I/O		364	244	284	300		170
	XCVR Lanes		16	8	4	4		4
MPF300	HSIO	276	156	96	120	120		
	GPIO	236	232	148	164	180		
	Total I/O	512	388	244	284	300		
	XCVR Lanes	16	16	8	4	4		
MPF500	HSIO	324	156					
	GPIO	260	232					
	Total I/O	584	388					
	XCVR Lanes	24	16					

2.2 Bank Locations

PolarFire FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the MPF100, MPF200, MPF300, and MPF500 devices with available package combinations.

Figure 1 • **PolarFire MPF500-FCG1152 I/O Bank Locations**

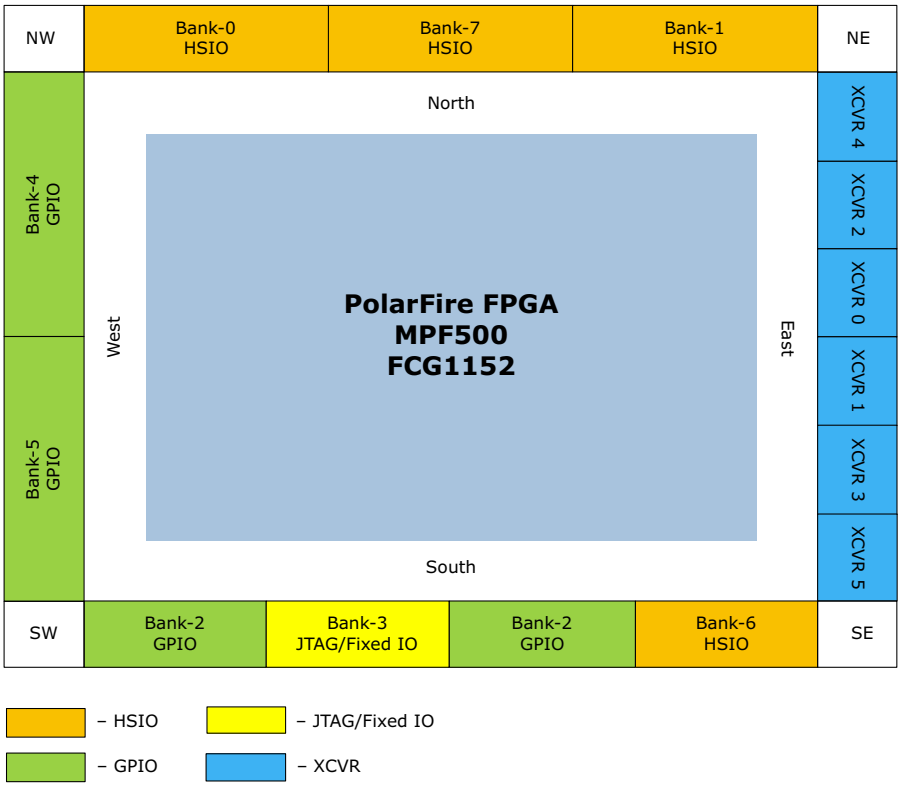


Figure 2 • **PolarFire MPF300-FCG1152 I/O Bank Locations**

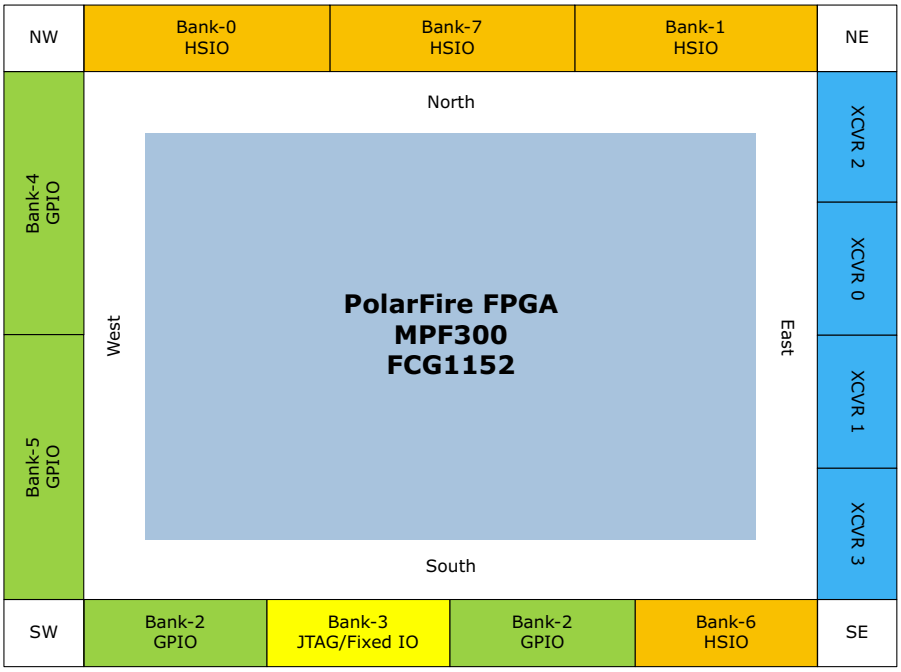


Figure 3 • **PolarFire MPF500/MPF300-FCG784 I/O Bank Locations**

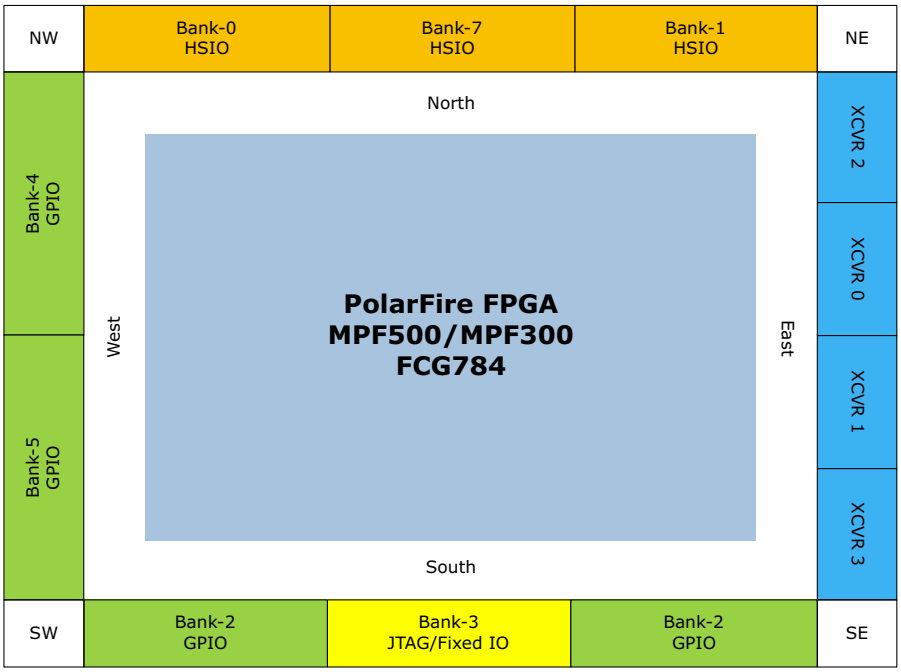


Figure 4 • **PolarFire MPF200-FCG784 I/O Bank Locations**

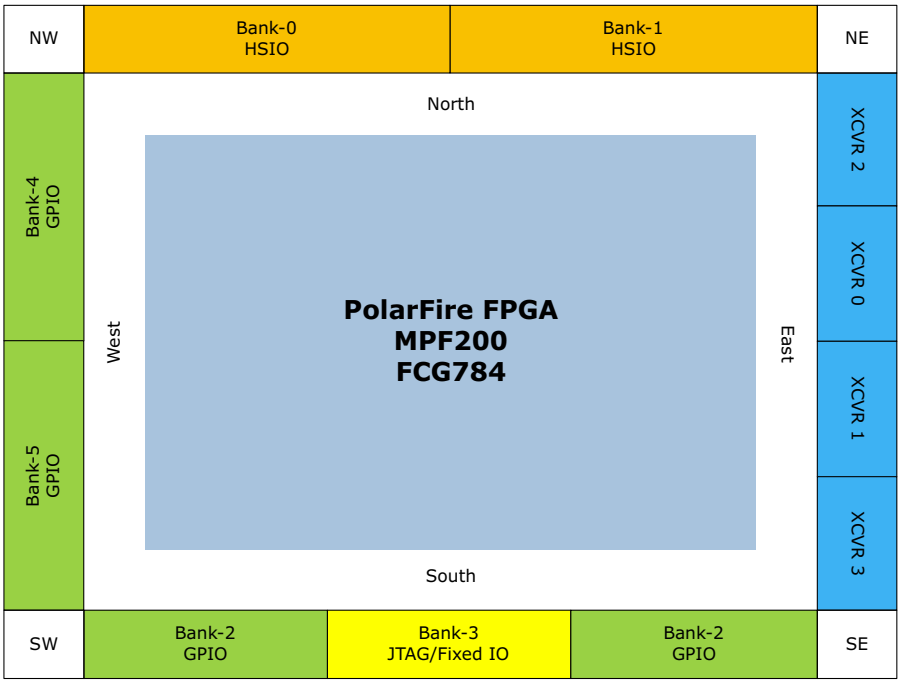
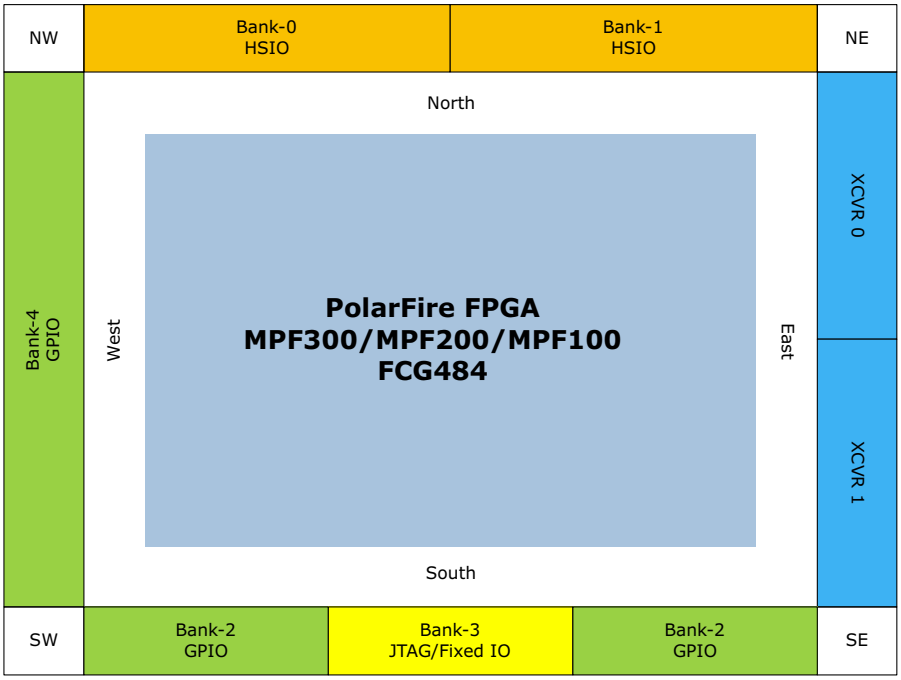
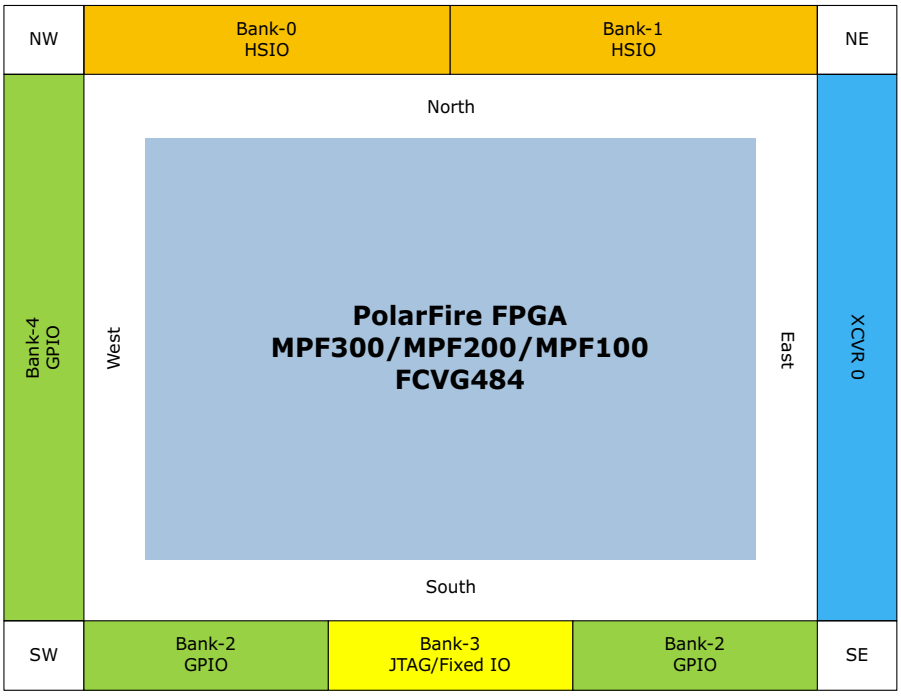


Figure 5 • **PolarFire MPF300/MPF200/MPF100-FCG484 I/O Bank Locations**



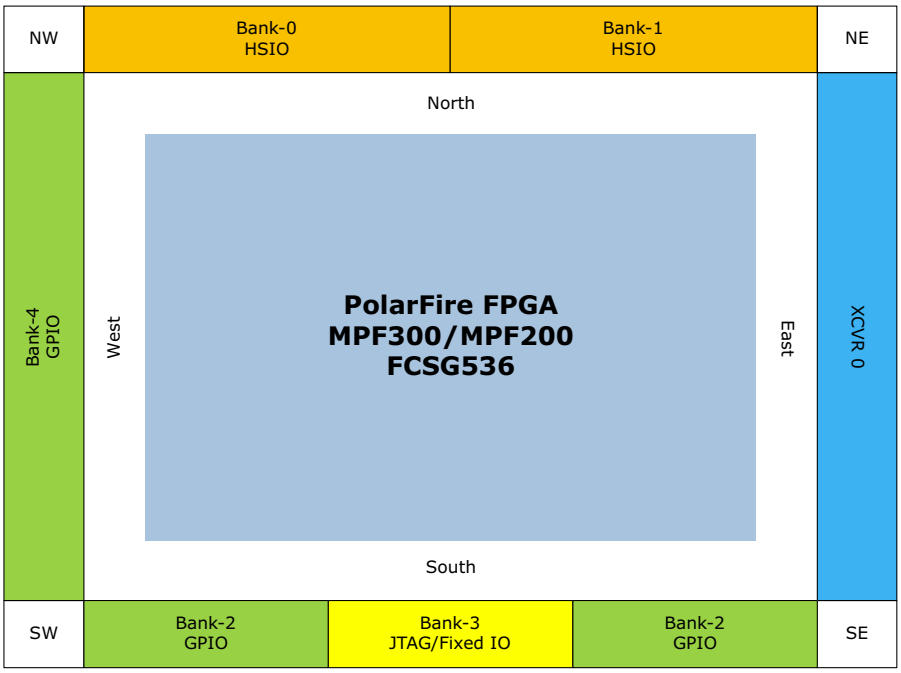
Note: Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 6 • **PolarFire MPF300/MPF200/MPF100-FCVG484 I/O Bank Locations**



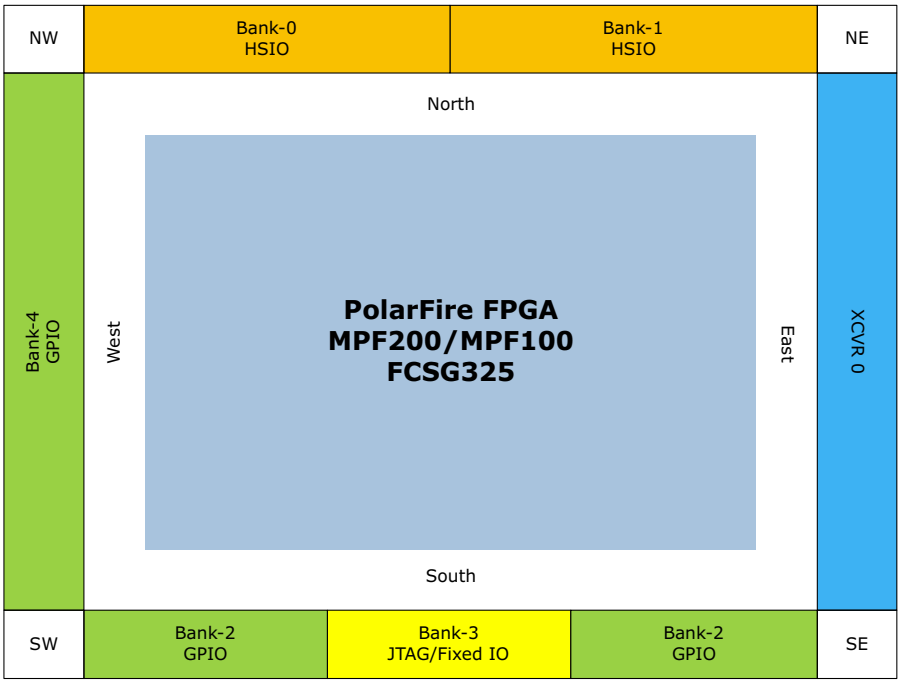
Note: Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 7 • **PolarFire MPF300/MPF200-FCSG536 I/O Bank Locations**



Note: Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 8 • **PolarFire MPF200/MPF100-FCSG325 I/O Bank Locations**



Note: In the MPF200 device, Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

The following table lists the organization of the I/O banks in PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe is supported only in XCVR0.

Table 2 • **Organization of I/O Banks**

	FCG1152		**FCG784**		**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
Bank Number	**MPF500**	**MPF300**	**MPF500 MPF300**	**MPF200**	**MPF300 MPF200 MPF100**	**MPF300 MPF200 MPF100**	**MPF300 MPF200**	**MPF200 MPF100**
Bank 0	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 1	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 2	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 3	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O
Bank 4	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 5	GPIO	GPIO	GPIO	GPIO				
Bank 6	HSIO	HSIO						
Bank 7	HSIO	HSIO	HSIO					
XCVR 0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
XCVR 1	Yes	Yes	Yes	Yes	Yes			
XCVR 2	Yes	Yes	Yes	Yes				
XCVR 3	Yes	Yes	Yes	Yes				
XCVR 4	Yes							
XCVR 5	Yes							

The following table lists the number of I/Os per bank for each package combination.

Table 3 • **Number of I/Os per Bank for Each Package Combination**

Package	Device	Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7	XCVRs
FCG1152	MPF300	72	60	96	Dedicated I/Os	92	48	72	72	16
FCG784	MPF300	72	60	96	Dedicated I/Os	92	44	NA	24	16
FCG484	MPF300	48	48	84	Dedicated I/Os	64	NA	NA	NA	8
FCVG484	MPF300	60	60	96	Dedicated I/Os	68	NA	NA	NA	4
FCSG536	MPF300	60	60	96	Dedicated I/Os	84	NA	NA	NA	4

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane. For more information about DDR lanes for each package in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*.

Table 4 • **PolarFire DDR Lane Information for I/O CDR (SGMII interface)**

Device	Package	DDR Lanes		
MPF300	FCG1152	DDR_S_0 to DDR_S_13	DDR_N_0 to DDR_N_16	DDR_W_0 to DDR_W_11
	FCG784	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_16	DDR_W_0 to DDR_W_11
	FCG484	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0, DDR_W_4,DDR_W_5 and DDR_W_9 to DDR_W_11
	FCVG484	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0, DDR_W_4,DDR_W_5 and DDR_W_9 to DDR_W_11
	FCSG536	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0 and DDR_W_4 to DDR_W_11

The following table lists the XCVR channels for PolarFire device/package.

Table 5 • **Serial Transceiver Channels**

Device	FCG1152	FCG784	FCG484	FCVG484	FCSG536	FCSG325
MPF500T	24	16				
MPF300T	16	16	8	4	4	
MPF200T		16	8	4	4	4
MPF100T			8	4		4

2.3 Pin Descriptions

PolarFire devices have user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

2.3.1 User I/O

PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating supplies ranging from 1.2 V to 3.3 V. GPIO supports multiple standards, including 3.3 V with an integrated clock data recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each PolarFire FPGA user I/O uses a IOxyBz naming convention, where:

- **IO** = the type of I/O.
- **x** = the I/O pair number in bank z.
- **y** = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- **B** = bank (see note in Supported I/O Features, page 9).
- **z** = bank number.

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

2.3.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

Table 6 • **Supported I/O Features**

I/O Feature	HSIO	GPIO	Additional Information
Programmable on/off clamp		Yes	
Hot-plug		Yes	
Cold sparing	Yes	Yes	
True differential output driver		Yes	
Programmable on/off 100 Ω differential termination		Yes	
PVT-compensated output drive	Yes	Yes	
Programmable slew control		Yes	
PVT compensated slew control	Yes		
Programmable input hysteresis	Yes	Yes	
Mobile industry processor interface (MIPI) (input)		Yes	High-speed and low-power.
MIPI (output)		Yes	High-speed.

Note: Bank 5 VDDI power pins are connected to Bank 4 VDDI power pins within package substrates (FCG484, FCVG484, FCS536, and FCSG325) for pin migration compatibility.

2.3.1.2 Supported I/O Standards

PolarFire FPGA user I/O are configured to different I/O standards as listed in the following table.

Table 7 • **Supported I/O Standards**

Type	I/O Standard	Voltage	Reference Voltage	Single-Ended	Differential	HSIO	GPIO
Single-ended Standards	PCI33	3.3 V		Yes			Yes
	LVTTL33	3.3 V		Yes			Yes
	LVCMOS33	3.3 V		Yes			Yes
	LVCMOS25	2.5 V		Yes			Yes
	LVCMOS18	1.8 V		Yes		Yes	Yes
	LVCMOS15	1.5 V		Yes		Yes	Yes
	LVCMOS12	1.2 V		Yes		Yes	Yes
	LVSTL11	1.1 V		Yes		Yes	
Reference Standards	SSTL25	2.5 V	1.25 V	Yes	Yes		Yes
	SSTL18	1.8 V	1.0 V	Yes	Yes	Yes	Yes
	HSUL18	1.8 V	1.0 V	Yes	Yes	Yes	Yes
	SSTL15	1.5 V	0.75 V	Yes	Yes	Yes	Yes
	HSTL15	1.5 V	0.75 V	Yes	Yes	Yes	Yes
	SSTL135	1.35 V	0.67 V	Yes	Yes	Yes	
	HSTL135	1.35 V	0.67 V	Yes	Yes	Yes	
	HSUL12	1.2 V	0.6 V	Yes	Yes	Yes	
	HSTL12	1.2 V	0.6 V	Yes	Yes	Yes	
	POD12	1.2 V	0.6 V	Yes	Yes	Yes	
Differential Standards	SLVS25	2.5 V			Yes	Yes	Yes
	HCSL (input only)	1.8 V/2.5 V /3.3 V			Yes	Yes	Yes
	SLVSE	1.5 V			Yes	Yes	Yes
	PPDS25	2.5 V			Yes		Yes
	BUSLVDSE	2.5 V			Yes		Yes
	MLVDSE	2.5 V			Yes		Yes
	BUSLVDS	2.5 V/3.3 V			Yes		Yes
	MLVDS	2.5 V/3.3 V			Yes		Yes
	LVPECL	3.3 V			Yes		Yes
	LVDS	2.5 V/3.3 V			Yes		Yes
	RSDS (output only)	2.5 V/3.3 V			Yes		Yes
	MINILVDS (output only)	2.5 V			Yes		Yes
	MIPI	MIPI Specification			Yes		Yes

2.3.1.3 Mixed Mode Operation

I/O standard LVCMOS receivers are designed to support mixed modes of operation. The following tables provide details on the mixed LVCMOS receiver modes. The transmit mode is always defined by the VDDI bank voltage. If the VDDI bank is 3.3 V, then the output voltage drives to 3.3 V. Thus, the only output standard supported is LVCMOS33.

Table 8 • **Mixed LVCMOS Receiver Modes for GPIO**

VDDI	LVCMOS33	LVCMOS25	LVCMOS18	LVCMOS15	LVCMOS12
3.3 V	Yes	Yes	Yes	No	Yes
2.5 V	Yes	Yes	Yes	Yes	Yes
1.8 V	Yes	Yes	Yes	Yes	Yes
1.5 V	Yes	Yes	Yes	Yes	Yes
1.2 V	Yes	Yes	No	Yes	Yes

Table 9 • **Mixed LVCMOS Receiver Modes for HSIO**

VDDI	LVCMOS18	LVCMOS15	LVCMOS12
1.8 V	Yes	Yes	Yes
1.5 V	Yes	Yes	Yes
1.2 V	No	Yes	Yes

2.3.1.4 Internal Clamp Diode Control Circuitry

Internal clamp diode control circuitry is present for both HSIO and GPIO. The option to switch the diode on or off is only available for GPIO. For HSIO, the internal clamp diode is always on by default. If the signaling levels of the receiver are greater than the VDDIx of the bank, the clamp diode must be disabled to support hot-plug insertion and mixed mode support. GPIO (except PCI standard) supports hot-plug insertion, which disables the clamp diode from pad to VDDIx.

2.3.2 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For more information on power sequence, see *UG0726: PolarFire FPGA Board Design User Guide*.

Table 10 • **Supply Pins**

Name	Description	Operating Voltage	Unused Condition
XCVR_VREF[1]	Voltage reference for transceiver.	0.9 V/1.25 V	Connect to VSS through a 10 KΩ resistor.
VDD_XCVR_CLK	Power for transceiver reference clock input buffers.	2.5 V/3.3 V	2.5 V/3.3 V or connect to VSS through a 10 KΩ resistor, see *UG0677: PolarFire FPGA Transceiver User Guide*.
VDDA25[2]	Transceiver PLL power	2.5 V	2.5 V or connect to VSS through 10k resistor.
VDDA[2]	Power for transceiver Tx and Rx lanes 0, 1, 2, 3.	1.0 V/1.05 V	1.0 V/1.05 V or connect to VSS through 10k resistor.
VSS	Core digital ground.		Must connect to the ground.
VDD	Device core digital supply.	1.0 V/1.05 V	Must connect to the core supply.

Table 10 • **Supply Pins *(continued)***

Name	Description	Operating Voltage	Unused Condition
VDDIx (JTAG Banks)	Supply for I/O circuits in a bank.	1.8 V/2.5 V/3.3 V	1.8 V/2.5 V/ 3.3 V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V or connect to VSS through a 10 KΩ resistor.
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V	1.2 V/1.5 V/ 1.8 V or connect to VSS through a 10 KΩ resistor.
VDD25	Power for corner PLLs and PNVM.	2.5 V	Must connect to 2.5 V.
VDD18	Power for programming and HSIO receiver.	1.8 V	Must connect to 1.8 V.
VDDAUXx	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5 V or 3.3 V and must be always equal to or higher than VDDIx.	Greater than or equal to VDDI	2.5 V/3.3 V or connect to VSS through a 10 KΩ resistor.

1. SSTL25 (stub series terminated logic) I/O standard for 1.25 V VREF, SSTL18 I/O standard for 0.9 V, and HSUL18 I/O standard for 0.9 V.
2. Special attention needed for noise isolation.

2.3.2.1 Packaging Decoupling Capacitors

PolarFire 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed (1.6 Gbps) I/O operation.

For small, low-profile CSP packages (0.5 mm ball pitch, 15 mm × 15 mm and smaller), package decoupling capacitors are not available.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

Table 11 • **Packaging Decoupling Capacitors**

Power Supply	0.8 mm Pitch		1 mm Pitch	
	Number of Capacitors	Value	Caps available	Value
VDDI0			1	1 µF/4 V/0306
VDDI1			1	1 µF/4 V/0306
VDDI2			1	1 µF/6.3 V/0306
VDDI4			1	1 µF/6.3 V/0306
VDDI5			1	1 µF/6.3 V/0306
VDDI6[1]			1	1 µF/4 V/0306
VDDI7[1]			1	1 µF/4 V/0306
VDD			1	2.2 µF/4 V/0508
VDD18			2	1 µF/4 V/0306
VDDA	2	10 nF/ 10 V/0201	2	10 nF/ 10 V/0201

1. 0.8 mm pitch PolarFire packages do not support VDDI6 and VDDI7.

2.3.3 Memory Interface

Valid locations for DDR memory interfaces are shown in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*. By using the Libero® System-on-Chip (SoC) PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information on the memory interface, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

The following table lists the reference receiver modes of I/O standards.

Table 12 • **Reference Receiver Modes**

I/O Standard	V_{DDIx}	V_{REF}	On-die Termination (ODT) (in Ω)	Bank Type	Speed (Mbps)	Application
SSTL18	1.8 V	0.9 V	40/50/60/80/120/240	GPIO, HSIO	800 1066	RLDRAM2
SSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	1066 1333	DDR3
SSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1333	DDR3L
HSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	900 1100	QDRII+
HSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1066	RLDRAM3
HSUL12	1.2 V	0.6 V	60/120/40	HSIO	1066 1333	LPDDR2, LPDDR3
HSTL12	1.2 V	0.6 V	60/120/240	HSIO	1266	QDRII+
POD	1.2 V	0.6 V	20/30/40/60/120	HSIO	1600	DDR4

2.3.4 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR, DDR2, DDR3, and DDR4 memories. It supports 8-, 16-, and 32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC PolarFire software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information on DDR signals, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide.*

2.3.5 Clocking Pins

CCC blocks, located at each corner of the PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information on clocking pins, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. See Table 10, page 11 for more information on CCC pin voltage.

Table 13 • **Clocking Pins**

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of PolarFire device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

2.3.6 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the PolarFire controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up.

Table 14 • **JTAG Pins**

Name	Direction	Weak Pull-up	Description	Unused Condition
TMS	Input	15 KΩ to VJTAG	JTAG test mode select (TMS).	DNC
TDI	Input	15 KΩ to VJTAG	JTAG data input pin. In ATPG/test mode, when using a 4-bit TDI bus, this I/O is used as TDI[0].	DNC
TDO	Output		JTAG data out.	DNC
TCK	Input		JTAG clock.	Must connect to VSS through 10 KΩ resistor.
TRSTB	Input	15 KΩ to VJTAG	JTAG reset (asserted low).	Must connect to VDDI3 through 1 KΩ resistor per pin, not to be shared with any other pins.

Table 15 • **Device Reset Pins**

Name	Direction	Weak Pull-up	Description	Unused Condition
DEVRST_N	Input	22 KΩ	Device reset (asserted low).	Must connect to VDDI3 through 1 KΩ resistor per pin, not to be shared with any other pins.

Table 16 • **SPI Interface Pins**

Name	Direction	Description	Unused Condition
SCK	Bi-directional	SPI clock.	Must connect to VSS through 10 KΩ resistor.
SS	Bi-directional	SPI slave select.	Must connect to VSS through 10 KΩ resistor.
SDI	Input	SDI input for the shared SPI interface.	Must connect to VDDI3 through 10 KΩ resistor.
SDO	Output	SDO output for the shared SPI interface.	DNC
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.	Must connect to VSS through 10 KΩ resistor.
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller. 0: SPI slave interface 1: SPI master interface	Must connect to VSS through 10 KΩ resistor.

Table 17 • **Probe and Other Pins**

Name	Direction	Description	Unused Condition
LPRB_A			Libero-defined DNC.
LPRB_B			Libero-defined DNC.
FF_EXIT_N	Input	External trigger to wake up from flash freeze.	Libero-defined DNC.

2.3.7 XCVR Interface

The transceiver I/O available in the PolarFire devices are dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

Table 18 • **XCVR Interface Pins**

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P XCVR_xy_REFCLK_N	Input	Differential serial reference clock xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	DNC.
XCVR_x_TXy_P XCVR_x_TXy_N	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC.
XCVR_x_RXy_P XCVR_x_RXy_N	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC, see *UG0677: PolarFire FPGA Transceiver User Guide*

2.4 Pin Compatibility Between Devices

To be updated

2.5 Package Pinouts

The following table lists packaging pinouts of PolarFire devices. Detailed PPATs are available for download and they contain revision history, device specification, power supplies, pinouts, and BGA graphic. For more information about PPATs, see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*.

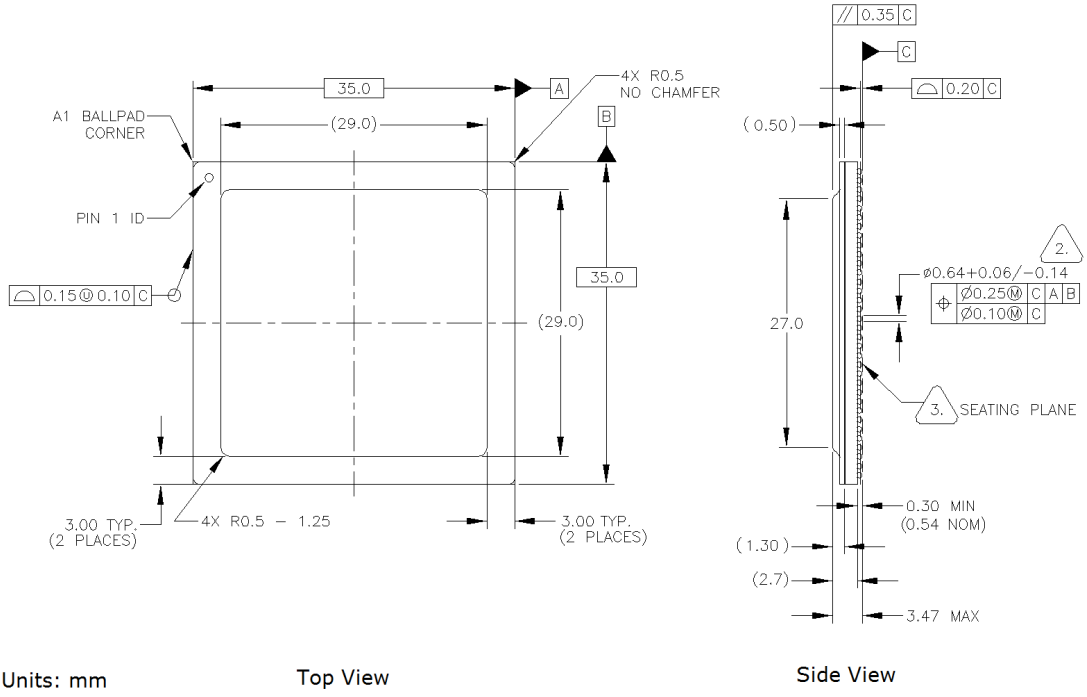
Table 19 • **Package Pin Outs**

	Packages					
Device	**FCG1152**	**FCG784**	**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
MPF500	MPF500-FCG1152	MPF500-FCG784				
MPF300	MPF300-FCG1152	MPF300-FCG784	MPF300-FCG484	MPF300-FCVG484	MPF300-FCSG536	
MPF200		MPF200-FCG784	MPF200-FCG484	MPF200-FCVG484	MPF200-FCSG536	MPF200-FCSG325
MPF100			MPF100-FCG484	MPF100-FCVG484		MPF100-FCSG325

2.6 Mechanical Drawings

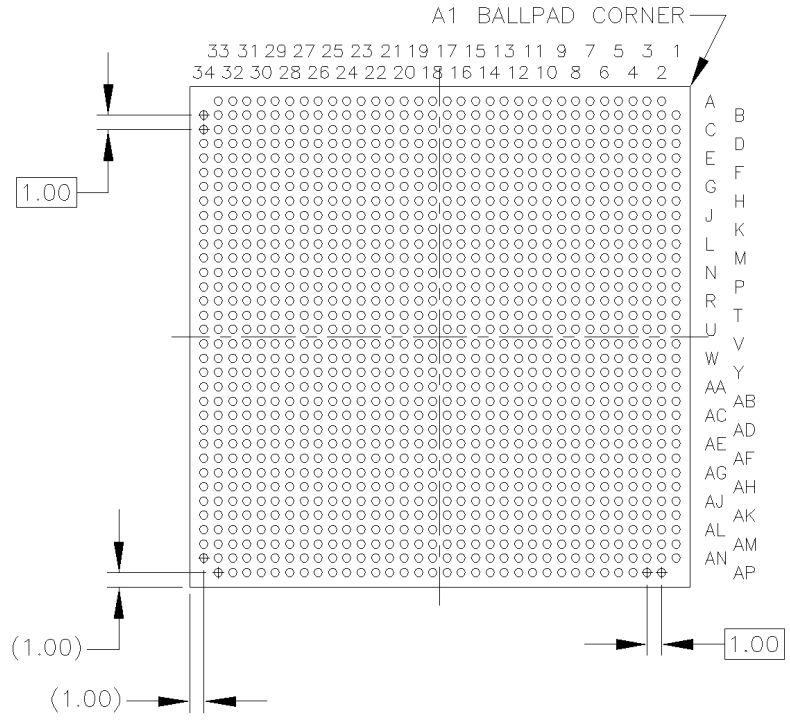
The following illustrations show the top, bottom, and side views and dimensions for the PolarFire FPGAs.

Figure 9 • **FCG1152 Package Top-View and Side-View**



Units: mm Top View Side View

Figure 10 • **FCG1152 Package Bottom-View**



Units: mm Bottom View – 1152 Solder Balls

Figure 11 • **FCG784 Package Top-View and Side-View**

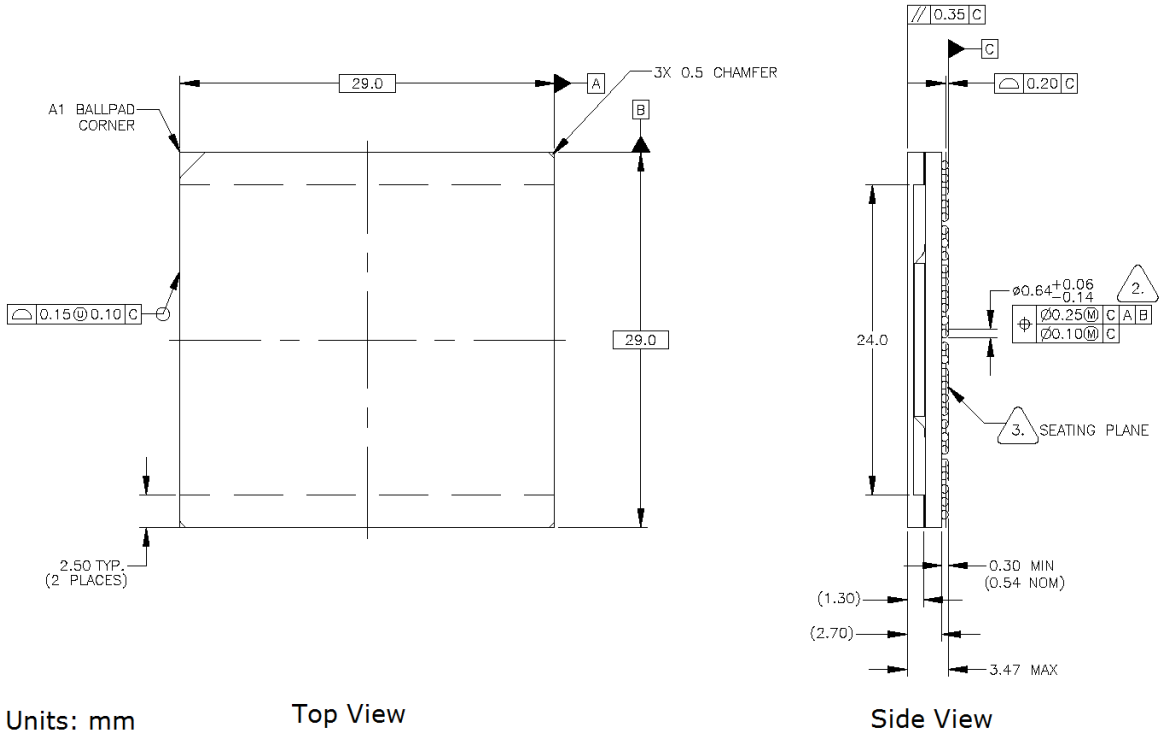


Figure 12 • **FCG784 Package Bottom-View**

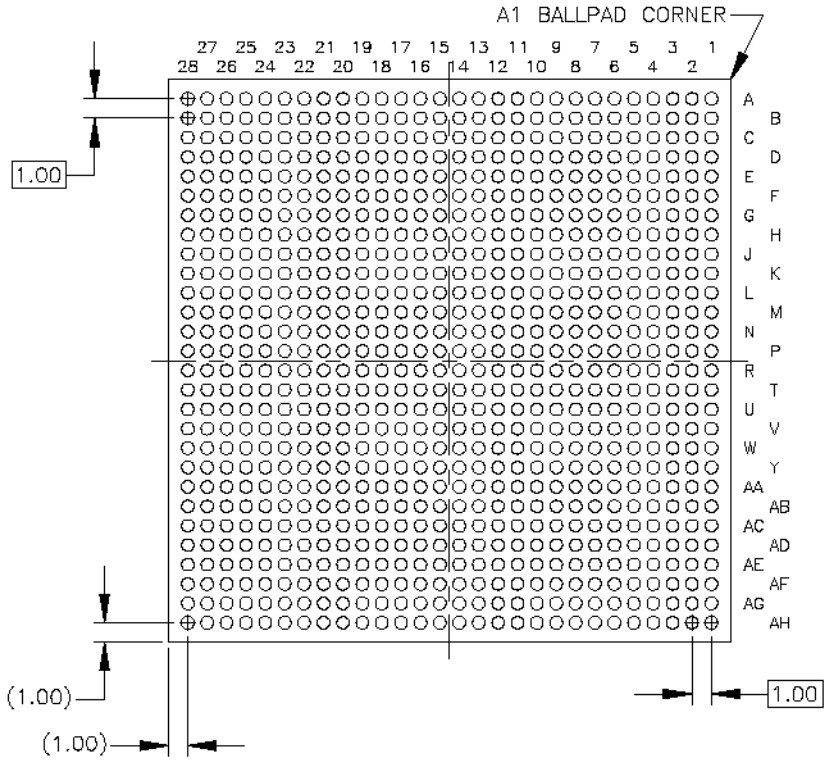


Figure 13 • **FCG484 Package Top-View and Side-View**

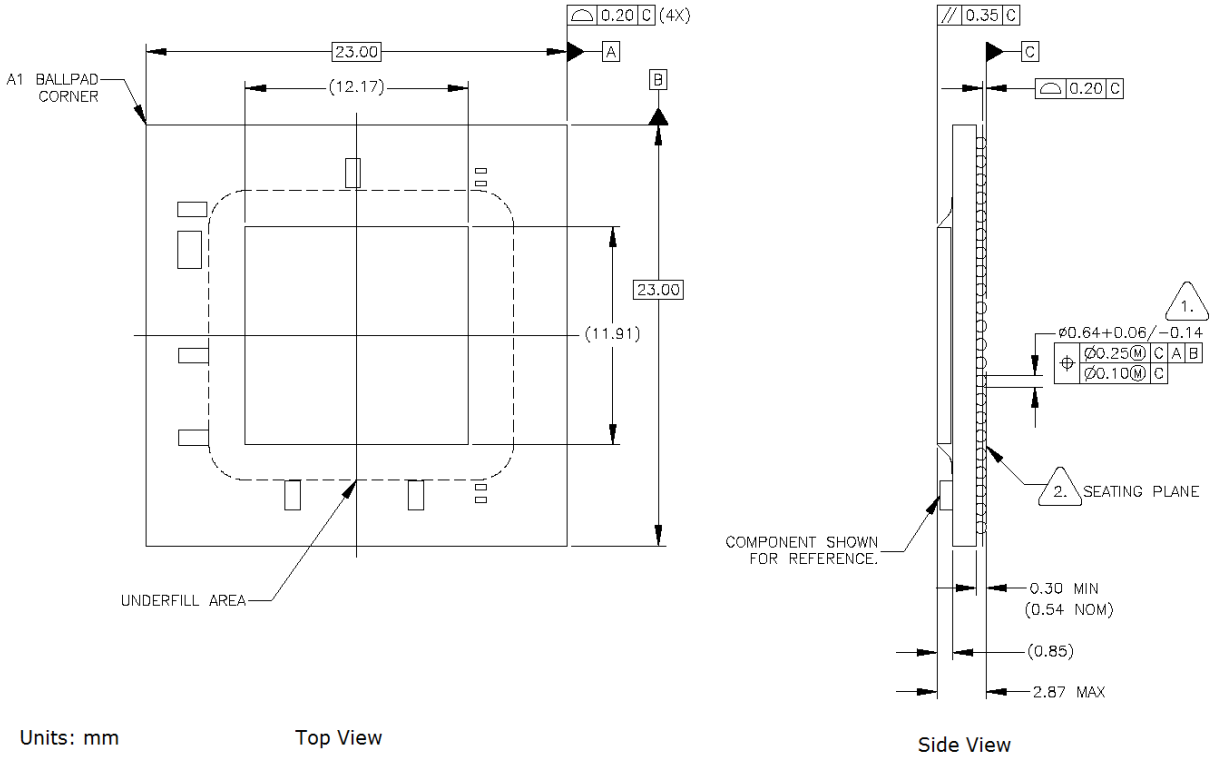


Figure 14 • **FCG484 Package Bottom-View**

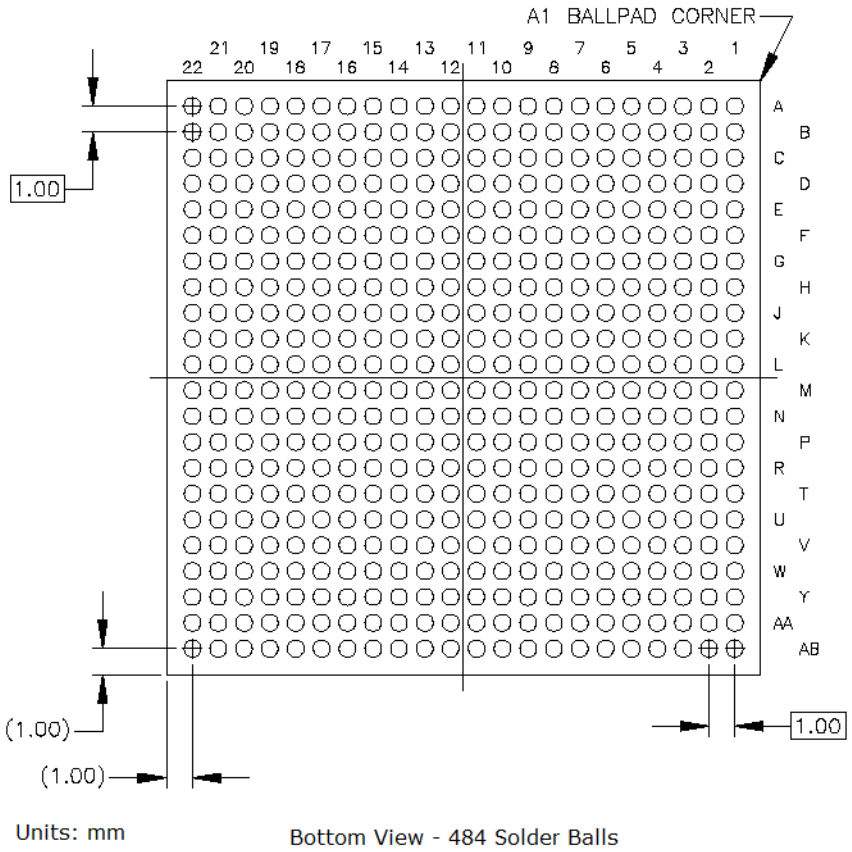


Figure 15 • **FCVG484 Package Top-View and Side-View**

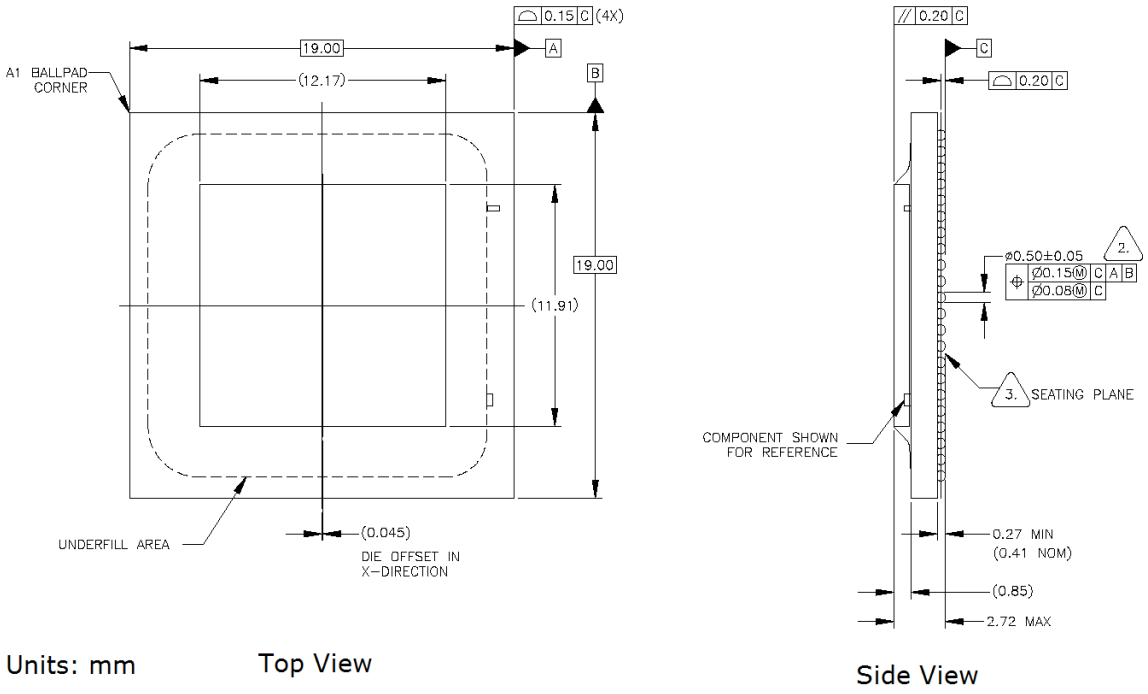
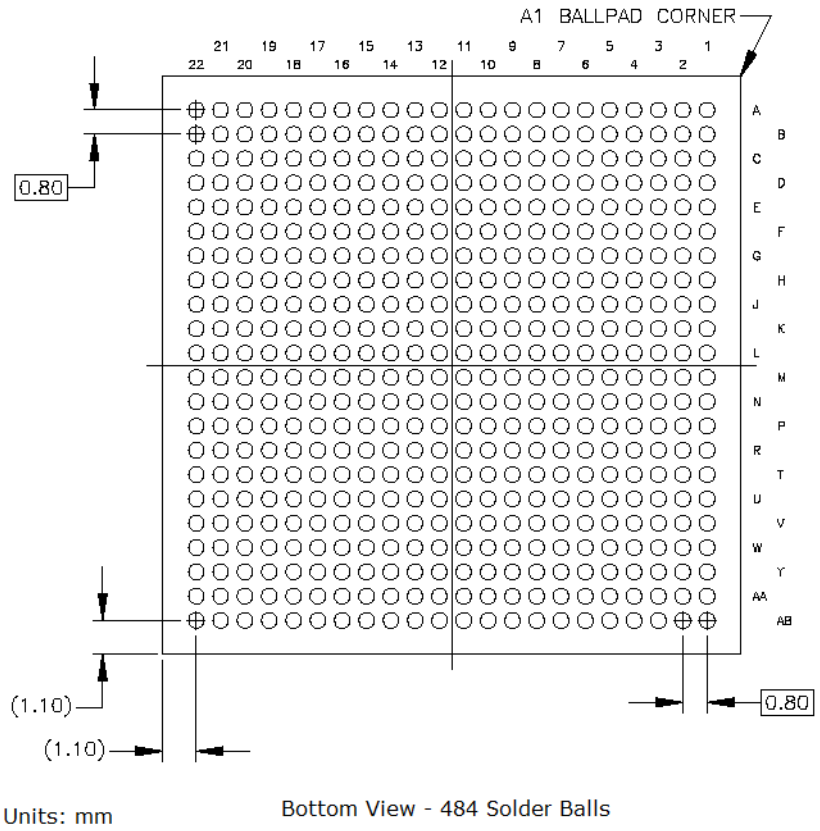


Figure 16 • **FCVG484 Package Bottom-View**



The following table lists the PolarFire FPGAs Package description and specification.

Table 20 • **PolarFire FPGAs Package Information**

		Package Specifications			
Package	**Description**	**Package type**	**Pitch (mm)**	**Size (mm)**	**Maximum I/Os**
FCG1152	Flip-chip with heat spreader	BGA	1	35 × 35	512
FCG784	Flip-chip with heat spreader	BGA	1	29 × 29	388
FCG484	Flip-chip	BGA	1	23 × 23	244
FCVG484	Flip-chip	BGA	0.8	19 × 19	284
FCSG536	Flip-chip	BGA	0.5	16 × 16	300
FCSG325	Flip-chip	BGA	0.5	11 × 11, 11 × 14.5	170

2.7 Thermal Specifications

The following table lists the thermal resistances of PolarFire FPGA package devices.

Table 21 • **PolarFire Package Thermal Resistances**

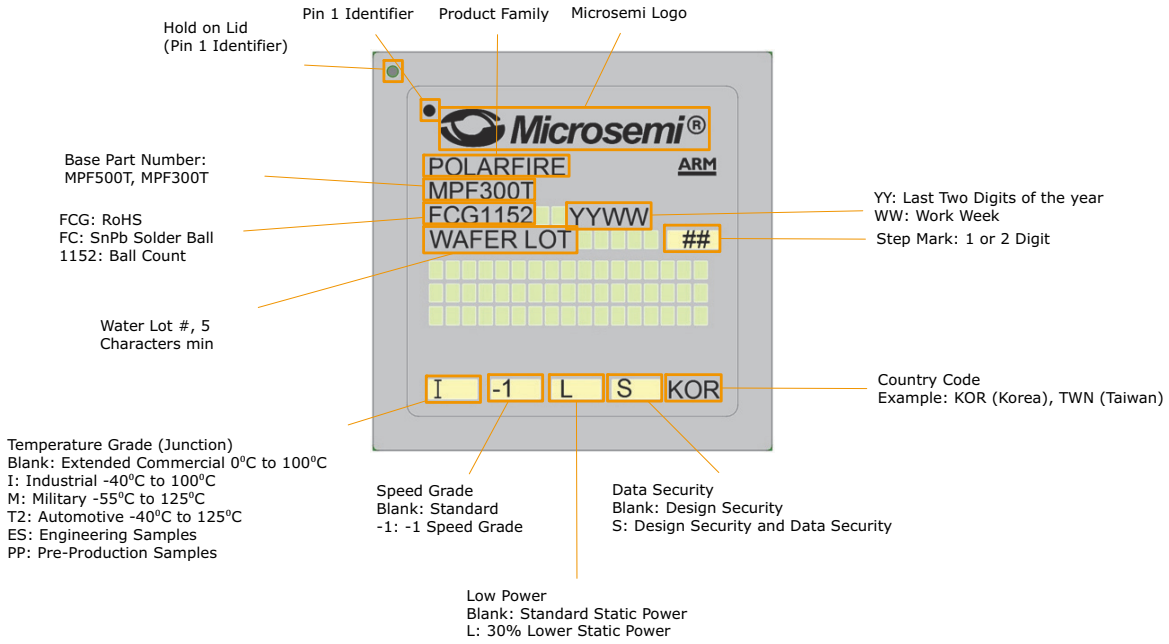
Package	**Environment**	**Theta-JA**	**Theta-JB**	**Theta-JC**	**Psi-JB**	**Psi-JT**
MPF300-FCG1152	Still air	8.00	2.09	0.429	1.96	0.290
	1.0 m/s	6.04			2.92	0.288
	2.5 m/s	5.21			2.79	0.290
MPF300-FCG484	Still air	14.98	7.80	0.047	6.24	0.011
	1.0 m/s	11.58			5.69	0.015
	2.5 m/s	10.26			5.47	0.016
MPF300-FCSG536	Still air	14.17	3.46	1.749	3.57	0.054
	1.0 m/s	11.49			6.73	0.113
	2.5 m/s	10.40			6.47	0.159

Note: Junction temperature is measured using Psi-JT = (Tj - Tc)/P and board temperature is measured using Psi-JB = (Tj - Tb)/P.

2.8 Package Marking

Microsemi normally marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microsemi's PolarFire FPGA device.

Figure 17 • **Detailed Marking for Each Character Code**



2.9 Packing and Shipping

The PolarFire series devices are packed in trays, which are used to pack most of the Microsemi surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 22 • **Standard Device Counts per Tray and Carton**

Package	Maximum Number of Devices Per Tray	Maximum Number Trays Per Stack	Maximum Number of Units per Inner Carton
FCG1152	24	5	120
FCG484	60	5	300
FCVG484	84	5	420
FCSG536	90	5	450
FCSG325	176	5	880