UG0722
User Guide
PolarFire FPGA Packaging and Pin Descriptions

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 5.0

Information about I/O bank locations was updated. See Figure 1, page 3, Figure 2, page 4, Figure 3, page 4, Figure 4, page 5, Figure 5, page 5, Figure 6, page 6, Figure 7, page 6, and Figure 8, page 7.

1.2 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Information about shield output pin was updated. See Table 14, page 14.
- Information about VDDIx (JTAG bank) and VDD_XCVR_CLK operating voltage was updated. See Table 7, page 10.
- Information about auxiliary supply for I/O circuits was updated. See Table 7, page 10.
- Information about Thermal resistance was updated. See Thermal Specifications, page 22.
- Information about PCB design rules was added. See Recommended PCB Design Rules for BGA Packages, page 27.
- Information about heat sink guidelines was added. See Thermal Management, page 24.
- FCSG325 and FCSG536 mechanical drawings were added. See Figure 17, page 19, Figure 18, page 19, Figure 19, page 20, Figure 20, page 20, Figure 21, page 21, and Figure 22, page 21.

1.3 Revision 3.0

The following is a summary of the changes made in revision 3.0 of this document.

- Information about DDR lane for I/O CDR (SGMII interface) was added. See Table 4, page 8.
- Information about Package marking was added. See Package Marking, page 23
- Information about thermal resistances of PolarFire Package device was added. See Thermal Specifications, page 22.
- Information about packing and shipping was added. See Packing and Shipping, page 24.
- Table 3, page 8, Table 5, page 8, and Table 17, page 22 were added.

1.4 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Figure 5, page 5 and Figure 6, page 6 were updated.
- Information about unused condition of pins was updated. See Table 7, page 10, Table 11, page 13, Table 12, page 13, Table 13, page 13, Table 14, page 14, and Table 15, page 14.

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

2 PolarFire FPGA Packaging and Pin Descriptions

This guide provides pin and packaging information (such as bank assignments and mechanical information) for PolarFire® FPGAs.

PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see *UG0686: PolarFire FPGA User I/O User Guide*.

2.1 Packaging Overview

PolarFire FPGAs are available in multiple packages. Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. HSIO and GPIO banks have a maximum supply voltage of 1.8 V and 3.3 V, respectively.

The following table lists the PolarFire FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

Table 1 • **PolarFire FPGA Product Family[1]**

Features		MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4 LUT + DFF)	109	192	300	481
	Math Blocks (18 × 18 MACC)	336	588	924	1480
	LSRAM Blocks (20 kbit)	352	616	952	1520
	µSRAM Blocks (64 × 12)	1008	1764	2772	4440
	Total RAM (Mbits)	7.6	13.3	20.6	33
	µPROM (Kbits 9-bit bus)	297	297	459	513
	User DLLs/PLLs	8	8	8	8
High-Speed I/O	250 Mbps to 12.7 Gbps Transceiver Lanes	8	16	16	24
	PCIe Gen2 End Points/Root Ports	2	2	2	2
Total I/Os	Total User I/Os	284	368	512	584

Table 1 • **PolarFire FPGA Product Family[1] *(continued)***

Features		MPF100	MPF200	MPF300	MPF500
Packaging	Type/Size/Pitch	Total User I/O (HSIO/GPIO)/Transceivers			
	FCSG325 (11 mm × 11 mm, 11 mm × 14.5 mm, 0.5 mm)	170(84/86)/4	170(84/86)/4		
	FCSG536 (16 mm × 16 mm, 0.5 mm)		300(120/180)/4	300(120/180)/4	
	FCVG484 (19 mm × 19 mm, 0.8 mm)	284(120/164)/4	284(120/164)/4	284(120/164)/4	
	FCG484 (23 mm × 23 mm, 1.0 mm)	244(96/148)/8	244(96/148)/8	244(96/148)/8	
	FCG784 (29 mm × 29 mm, 1.0 mm)		364(132/232)/16	388(156/232)/16	388(156/232)/16
	FCG1152 (35 mm × 35 mm, 1.0 mm)			512(276/236)/16	584(324/260)/24

1. Devices in the same package are pin compatible.

2.2 Bank Locations

PolarFire FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the MPF100, MPF200, MPF300, and MPF500 devices with available package combinations.

Figure 1 • **PolarFire MPF500-FCG1152 I/O Bank Locations**

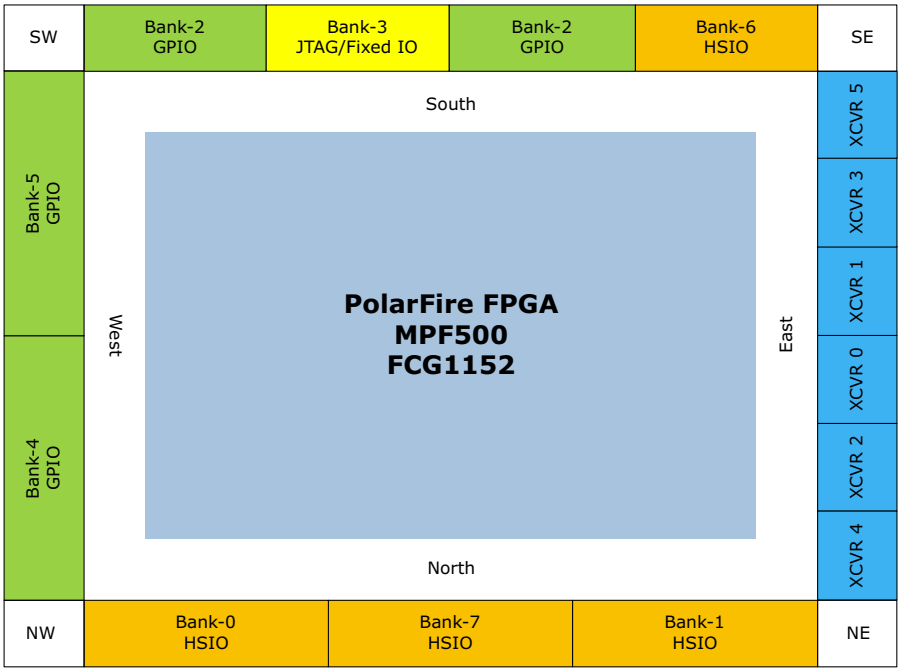


Figure 2 • **PolarFire MPF300-FCG1152 I/O Bank Locations**

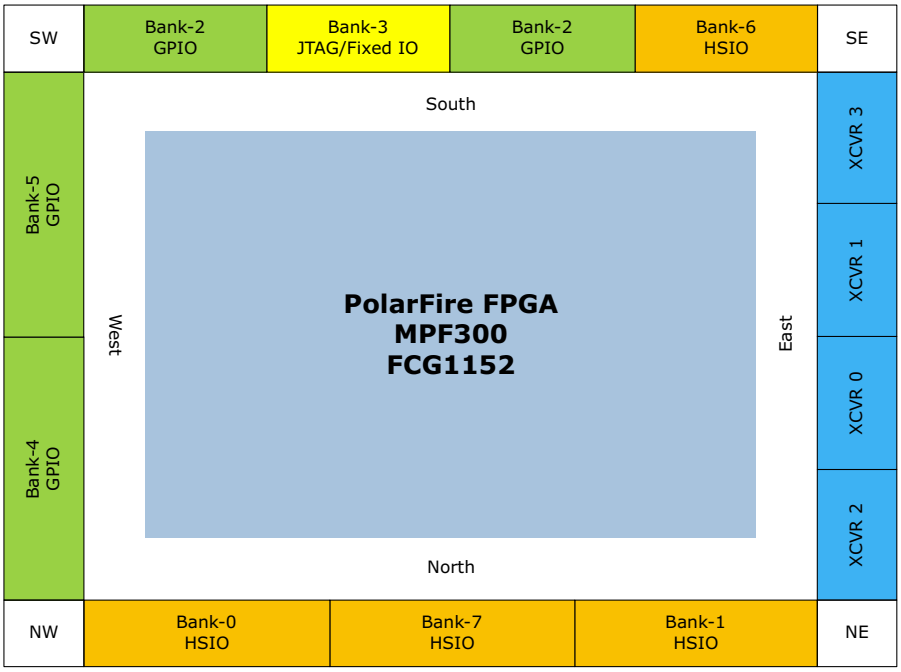


Figure 3 • **PolarFire MPF500/MPF300-FCG784 I/O Bank Locations**

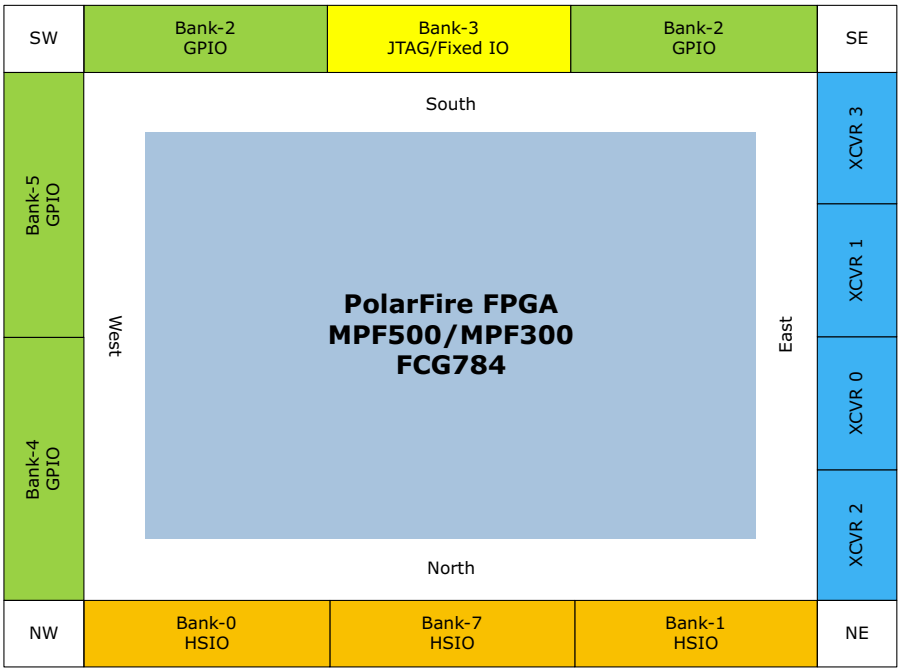


Figure 4 • **PolarFire MPF200-FCG784 I/O Bank Locations**

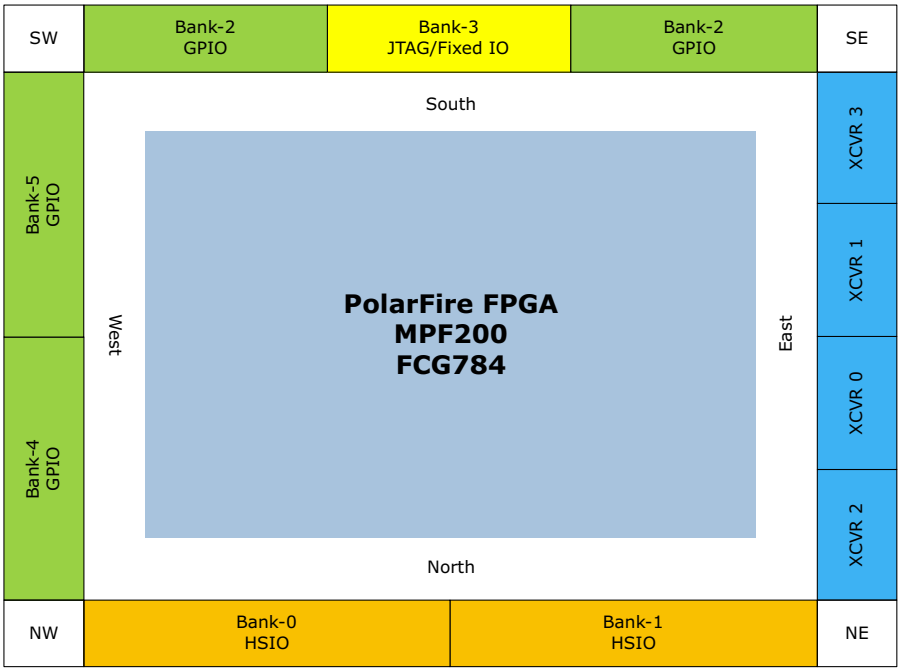
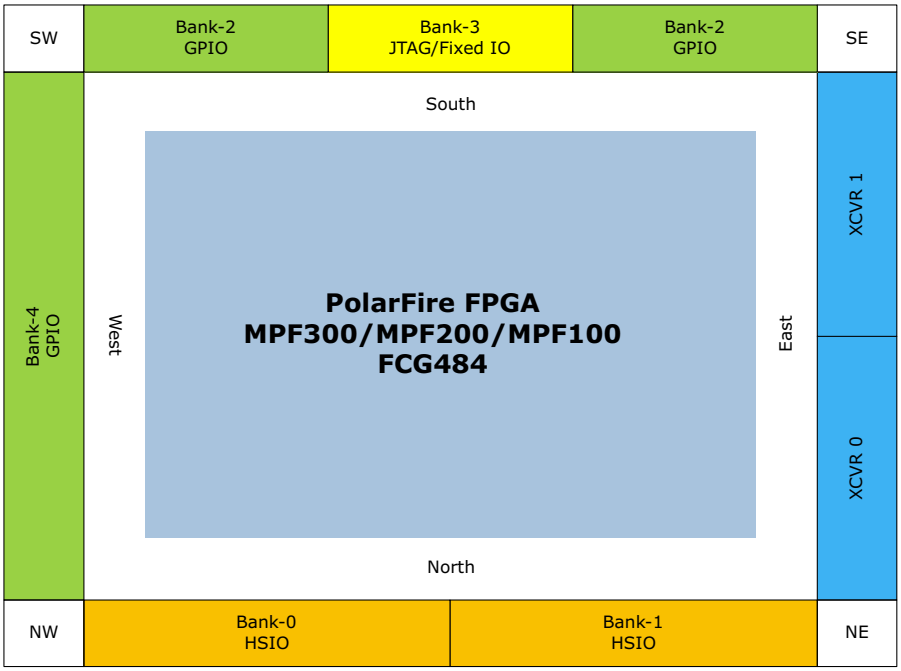
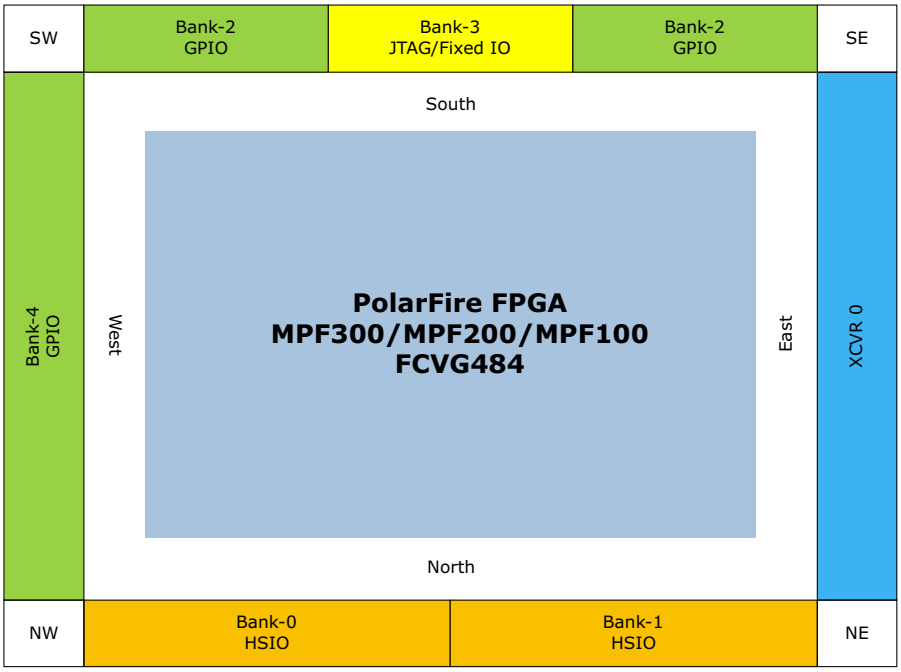


Figure 5 • **PolarFire MPF300/MPF200/MPF100-FCG484 I/O Bank Locations**



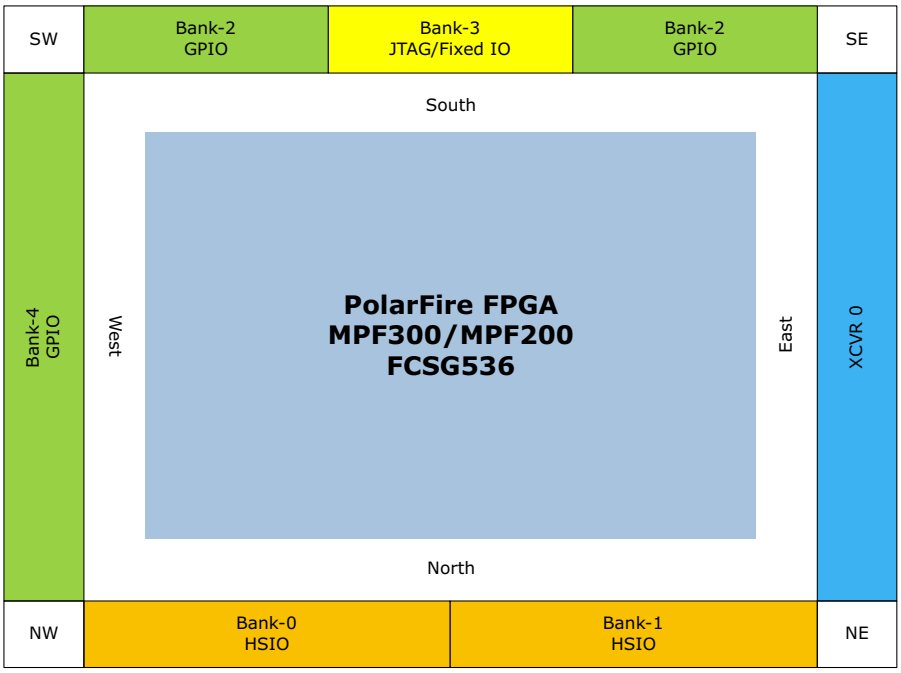
Note: In MPF300 and MPF200 devices, Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 6 • **PolarFire MPF300/MPF200/MPF100-FCVG484 I/O Bank Locations**



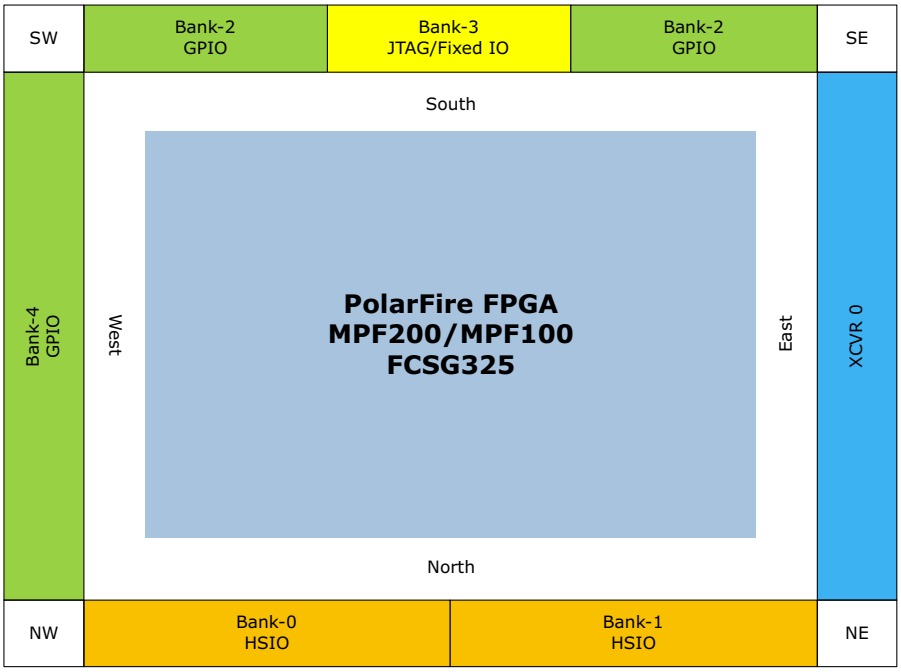
Note: In MPF300 and MPF200 devices, Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 7 • **PolarFire MPF300/MPF200-FCSG536 I/O Bank Locations**



Note: Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

Figure 8 • **PolarFire MPF200/MPF100-FCSG325 I/O Bank Locations**



Note: In the MPF200 device, Bank 5 VDDI is connected to Bank 4 VDDI in the package substrate for pin migration compatibility.

The following table lists the organization of the I/O banks in PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe is supported only in XCVR0.

Table 2 • **Organization of I/O Banks**

	FCG1152		**FCG784**		**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
Bank Number	**MPF500**	**MPF300**	**MPF500 MPF300**	**MPF200**	**MPF300 MPF200 MPF100**	**MPF300 MPF200 MPF100**	**MPF300 MPF200**	**MPF200 MPF100**
Bank 0	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 1	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 2	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 3	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O
Bank 4	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 5	GPIO	GPIO	GPIO	GPIO				
Bank 6	HSIO	HSIO						
Bank 7	HSIO	HSIO	HSIO					
XCVR 0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
XCVR 1	Yes	Yes	Yes	Yes	Yes			
XCVR 2	Yes	Yes	Yes	Yes				
XCVR 3	Yes	Yes	Yes	Yes				
XCVR 4	Yes							
XCVR 5	Yes							

The following table lists the number of I/Os per bank for each package combination.

Table 3 • **Number of I/Os per Bank for Each Package Combination**

Package	Device	Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7	XCVRs
FCG1152	MPF300	72	60	96	Dedicated I/Os	92	48	72	72	16
FCG784	MPF300	72	60	96	Dedicated I/Os	92	44	NA	24	16
FCG484	MPF300	48	48	84	Dedicated I/Os	64	NA	NA	NA	8
FCVG484	MPF300	60	60	96	Dedicated I/Os	68	NA	NA	NA	4
FCSG536	MPF300	60	60	96	Dedicated I/Os	84	NA	NA	NA	4

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane. For more information about DDR lanes for each package in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*.

Table 4 • **PolarFire DDR Lane Information for I/O CDR (SGMII interface)**

Device	Package	DDR Lanes		
MPF300	FCG1152	DDR_S_0 to DDR_S_13	DDR_N_0 to DDR_N_16	DDR_W_0 to DDR_W_11
	FCG784	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_16	DDR_W_0 to DDR_W_11
	FCG484	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0, DDR_W_4,DDR_W_5 and DDR_W_9 to DDR_W_11
	FCVG484	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0, DDR_W_4,DDR_W_5 and DDR_W_9 to DDR_W_11
	FCSG536	DDR_S_0 to DDR_S_7	DDR_N_0 to DDR_N_4 and DDR_N_12 to DDR_N_16	DDR_W_0 and DDR_W_4 to DDR_W_11

The following table lists the XCVR channels for PolarFire device/package.

Table 5 • **Serial Transceiver Channels**

Device	FCG1152	FCG784	FCG484	FCVG484	FCSG536	FCSG325
MPF500	24	16				
MPF300	16	16	8	4	4	
MPF200		16	8	4	4	4
MPF100			8	4		4

2.3 Evaluation Packages

The package status designation is based on a released package design. Package status with this designation are considered stable. Dedicated and power/ground pins are fixed, however, some pins (generic FPGA I/O) and mechanical specifications might change prior to production release. Boards should not be developed using Evaluation packages (for example, FCSG325_Eval).

2.4 Pin Descriptions

PolarFire devices have user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

2.4.1 User I/O

PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating supplies ranging from 1.2 V to 3.3 V. GPIO supports multiple standards, including 3.3 V with an integrated clock data recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each PolarFire FPGA user I/O uses a IOxyBz naming convention, where:

- **IO** = the type of I/O.
- **x** = the I/O pair number in bank z.
- **y** = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- **B** = bank (see note in Supported I/O Features, page 9).
- **z** = bank number.

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

2.4.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

Table 6 • **Supported I/O Features**

I/O Feature	HSIO	GPIO	Additional Information
Programmable on/off clamp		Yes	
Hot-plug		Yes	
Cold sparing	Yes	Yes	
True differential output driver		Yes	
Programmable on/off 100 Ω differential termination		Yes	
PVT-compensated output drive	Yes	Yes	
Programmable slew control		Yes	
PVT compensated slew control	Yes		
Programmable input hysteresis	Yes	Yes	
Mobile industry processor interface (MIPI) (input)		Yes	High-speed and low-power.
MIPI (output)		Yes	High-speed.

Note: Bank 5 VDDI power pins are connected to Bank 4 VDDI power pins within package substrates (FCG484, FCVG484, FCS536, and FCSG325) for pin migration compatibility.

2.4.2 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For more information on power sequence, see *UG0726: PolarFire FPGA Board Design User Guide*.

Table 7 • **Supply Pins**

Name	Description	Operating Voltage	Unused Condition
XCVR_VREF[1]	Voltage reference for transceiver.	0.9 V/1.25 V	Connect to VSS through a 10 KΩ resistor.
VDD_XCVR_CLK[2]	Power for transceiver reference clock input buffers.	2.5 V/3.3 V	2.5 V/3.3 V or connect to VSS through a 10 KΩ resistor, see *UG0677: PolarFire FPGA Transceiver User Guide*.
VDDA25[3]	Transceiver PLL power	2.5 V	2.5 V or connect to VSS through 10k resistor.
VDDA[3]	Power for transceiver Tx and Rx lanes 0, 1, 2, 3.	1.0 V/1.05 V	1.0 V/1.05 V or connect to VSS through 10k resistor.
VSS	Core digital ground.		Must connect to the ground.
VDD	Device core digital supply.	1.0 V/1.05 V	Must connect to the core supply.
VDDIx (JTAG Bank)[2]	Supply for I/O circuits in a bank.	1.8 V/2.5 V/3.3 V	1.8 V/2.5 V/ 3.3 V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V or connect to VSS through a 10 KΩ resistor.
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V	1.2 V/1.5 V/ 1.8 V or connect to VSS through a 10 KΩ resistor.
VDD25	Power for corner PLLs and PNVM.	2.5 V	Must connect to 2.5 V.
VDD18	Power for programming and HSIO receiver.	1.8 V	Must connect to 1.8 V.
VDDAUXx	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5 V or 3.3 V and must be always equal to or higher than VDDIx of GPIO banks.	Greater than or equal to VDDI	2.5 V/3.3 V or connect to VSS through a 10 KΩ resistor.

1. SSTL25 (stub series terminated logic) I/O standard for 1.25 V VREF, SSTL18 I/O standard for 0.9 V, and HSUL18 I/O standard for 0.9 V.
2. The VDDIx (JTAG bank) and VDD_XCVR_CLK operating voltage should not be more than 2.5 V. Future releases would support an operating voltage, ranging from 2.5 V to 3.3 V.
3. Special attention needed for noise isolation.

2.4.2.1 Packaging Decoupling Capacitors

PolarFire 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed I/O operation.

Small, low-profile CSP packages (0.5 mm ball pitch, 16 mm × 16 mm and smaller) do not have package decoupling capacitors.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

Table 8 • **Packaging Decoupling Capacitors**

Power Supply	0.8 mm Pitch		1 mm Pitch	
	Number of Capacitors	Value	Caps available	Value
VDDI0			1	1 µF/4 V
VDDI1			1	1 µF/4 V
VDDI2			1	1 µF/6.3 V
VDDI4			1	1 µF/6.3 V
VDDI5			1	1 µF/6.3 V
VDDI6[1]			1	1 µF/4 V
VDDI7[1]			1	1 µF/4 V
VDD			1	2.2 µF/4 V
VDD18			2	1 µF/4 V
VDDA	2	4.7nF /6.3 V 1.0nF/16.0 V	4	4.7nF/6.3 V 2.2 nF/6.3 V 1.5 nF/6.3 V 1.0 nF/16.0 V

1. 0.8 mm pitch PolarFire packages do not support VDDI6 and VDDI7.

2.4.3 Memory Interface

Valid locations for DDR memory interfaces are shown in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*. By using the Libero® SoC PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information on the memory interface, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

The following table lists the reference receiver modes of I/O standards.

Table 9 • **Reference Receiver Modes**

I/O Standard	V_{DDIx}	V_{REF}	On-die Termination (ODT) (in Ω)	Bank Type	Speed (Mbps)	Application
SSTL18	1.8 V	0.9 V	40/50/60/80/120/240	GPIO, HSIO	800 1066	RLDRAM2
SSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	1066 1333	DDR3
SSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1333	DDR3L
HSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	900 1100	QDRII+
HSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1066	RLDRAM3
HSUL12	1.2 V	0.6 V	60/120/40	HSIO	1066 1333	LPDDR2, LPDDR3
HSTL12	1.2 V	0.6 V	60/120/240	HSIO	1266	QDRII+
POD	1.2 V	0.6 V	20/30/40/60/120	HSIO	1600	DDR4

2.4.4 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR, DDR2, DDR3, and DDR4 memories. It supports 8-, 16-, and 32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC PolarFire software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information on DDR signals, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide.*

2.4.5 Clocking Pins

CCC blocks, located at each corner of the PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information on clocking pins, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. See Table 7, page 10 for more information on CCC pin voltage.

Table 10 • **Clocking Pins**

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of PolarFire device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

2.4.6 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the PolarFire controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up.

Table 11 • **JTAG Pins**

Name	Direction	Weak Pull-up	Description	Unused Condition
TMS	Input	15 KΩ to VJTAG	JTAG test mode select (TMS).	DNC
TDI	Input	15 KΩ to VJTAG	JTAG data input pin. In ATPG/test mode, when using a 4-bit TDI bus, this I/O is used as TDI[0].	DNC
TDO	Output		JTAG data out.	DNC
TCK	Input		JTAG clock.	Must connect to VSS through 10 KΩ resistor.
TRSTB	Input	15 KΩ to VJTAG	JTAG reset (asserted low).	Must connect to VDDI3 through 1 KΩ resistor per pin, not to be shared with any other pins.

Table 12 • **Device Reset Pins**

Name	Direction	Weak Pull-up	Description	Unused Condition
DEVRST_N	Input	22 KΩ	Device reset (asserted low).	Must connect to VDDI3 through 1 KΩ resistor per pin, not to be shared with any other pins.

Table 13 • **SPI Interface Pins**

Name	Direction	Description	Unused Condition
SCK	Bi-directional	SPI clock.	Must connect to VSS through 10 KΩ resistor.
SS	Bi-directional	SPI slave select.	Must connect to VSS through 10 KΩ resistor.
SDI	Input	SDI input for the shared SPI interface.	Must connect to VDDI3 through 10 KΩ resistor.
SDO	Output	SDO output for the shared SPI interface.	DNC
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.	Must connect to VSS through 10 KΩ resistor.
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller. 0: SPI slave interface 1: SPI master interface	Must connect to VSS through 10 KΩ resistor.

Table 14 • **Probe and Other Pins**

Name	Direction	Description	Unused Condition
LPRB_A	Output	Live Probe signal A	Libero-defined DNC.
LPRB_B	Output	Live Probe signal B	Libero-defined DNC.
FF_EXIT_N	Input	External trigger to wake up from flash freeze.	Libero-defined DNC.
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.	Only when DDR controller is in use.

2.4.7 XCVR Interface

The transceiver I/O available in the PolarFire devices are dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

Table 15 • **XCVR Interface Pins**

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P XCVR_xy_REFCLK_N	Input	Differential serial reference clock xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	DNC.
XCVR_x_TXy_P XCVR_x_TXy_N	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC.
XCVR_x_RXy_P XCVR_x_RXy_N	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC, see *UG0677: PolarFire FPGA Transceiver User Guide*

2.5 Pin Compatibility Between Devices

To be updated

2.6 Package Pin-outs

The following table lists packaging pin-outs of PolarFire devices. Detailed PPATs are available for download and they contain revision history, device specification, power supplies, pin-outs, and BGA graphic. For more information about PPATs, see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#documentation/packaging*.

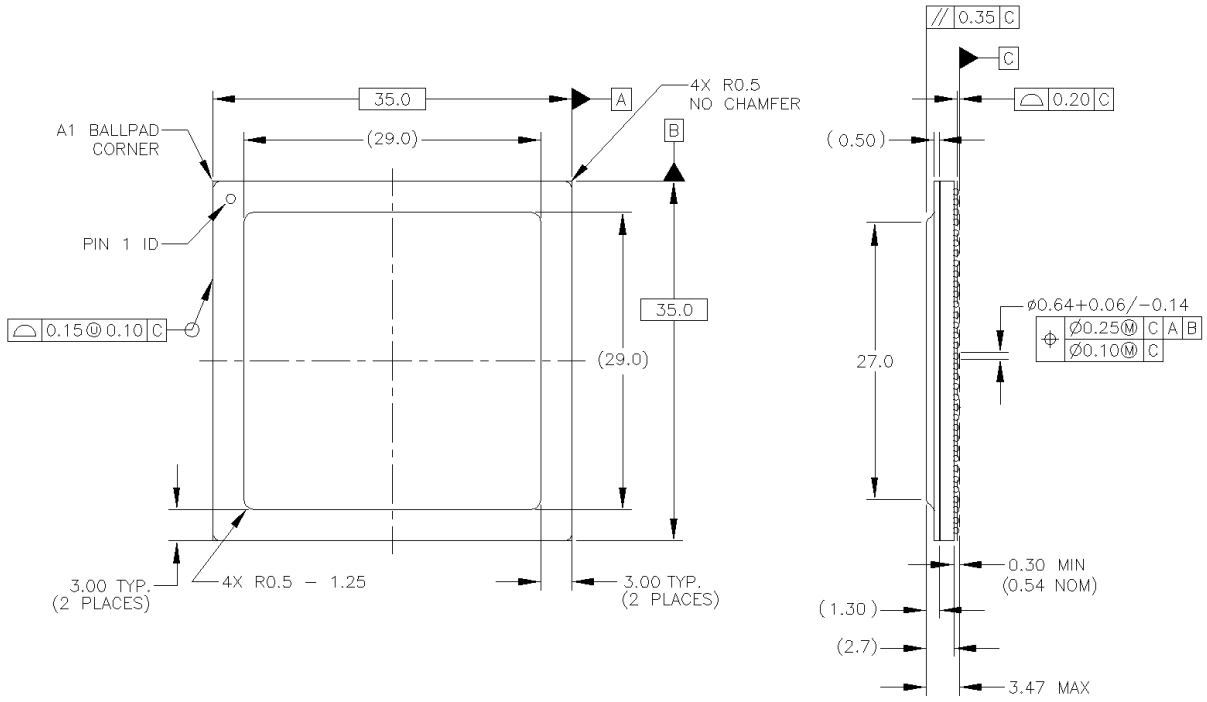
Table 16 • **Package Pin Outs**

	Packages					
Device	**FCG1152**	**FCG784**	**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
MPF500	Yes	Yes				
MPF300	Yes	Yes	Yes	Yes	Yes	
MPF200		Yes	Yes	Yes	Yes	Yes
MPF100			Yes	Yes		Yes

2.7 Mechanical Drawings

The following illustrations show the top, bottom, and side views and dimensions for the PolarFire FPGAs.

Figure 9 • **FCG1152 Package Top-View and Side-View**



Units: mm

Figure 10 • **FCG1152 Package Bottom-View**

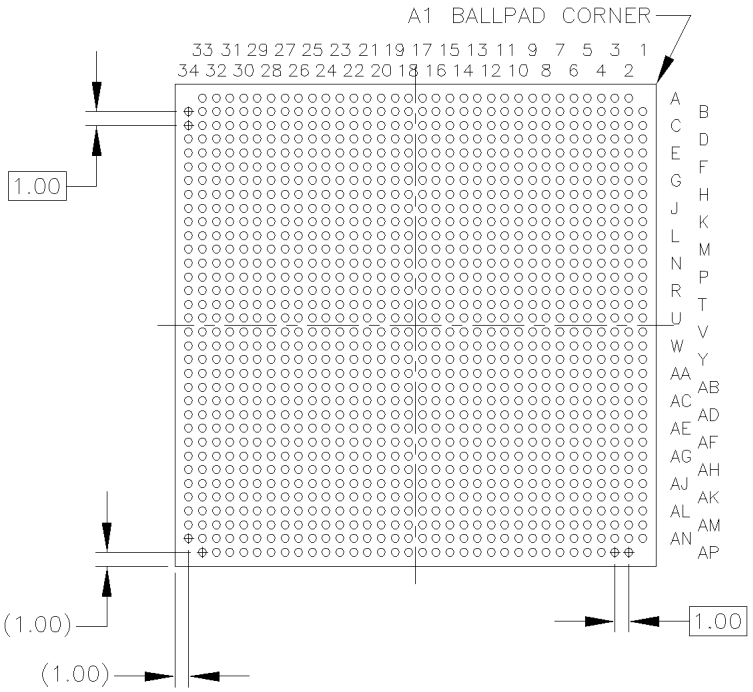
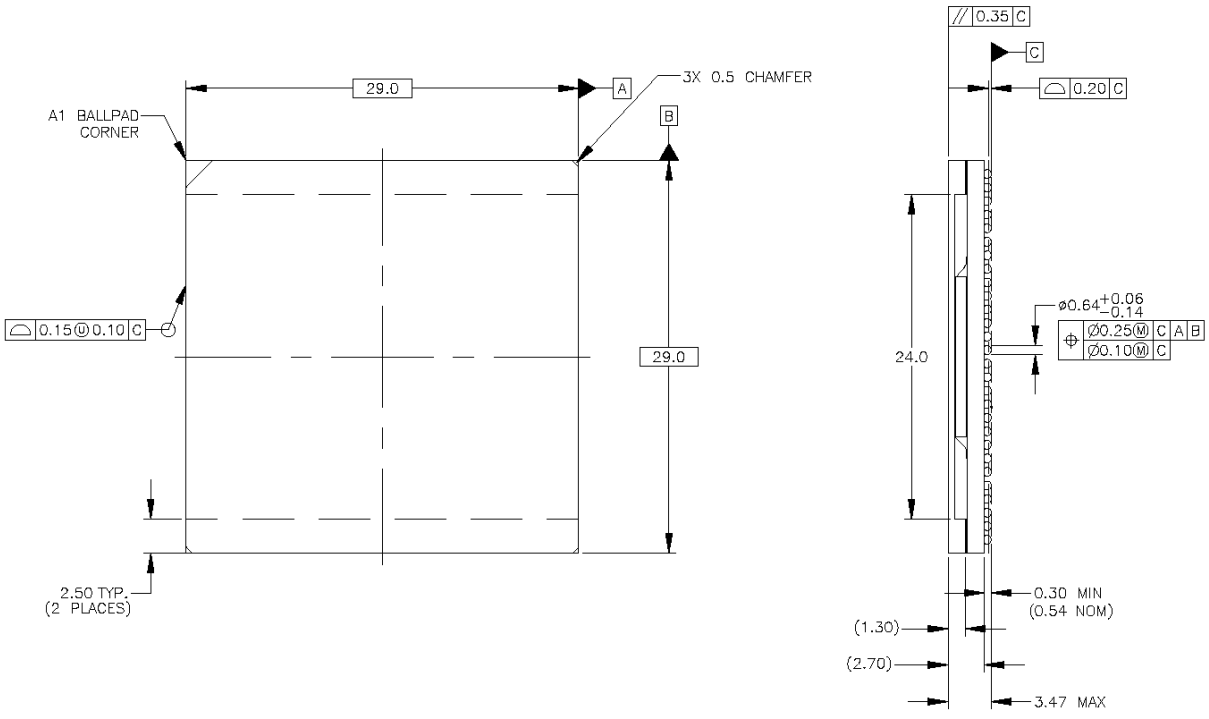


Figure 11 • **FCG784 Package Top-View and Side-View**



Units: mm

Figure 12 • **FCG784 Package Bottom-View**

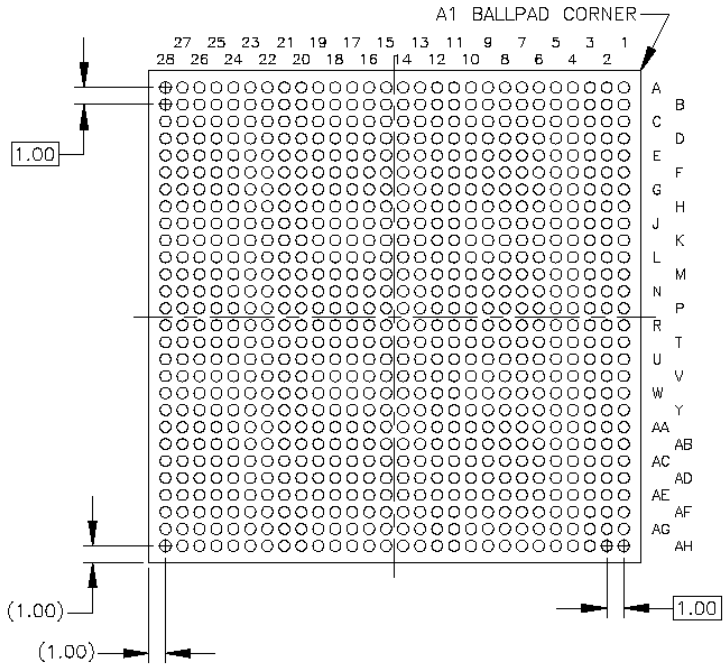
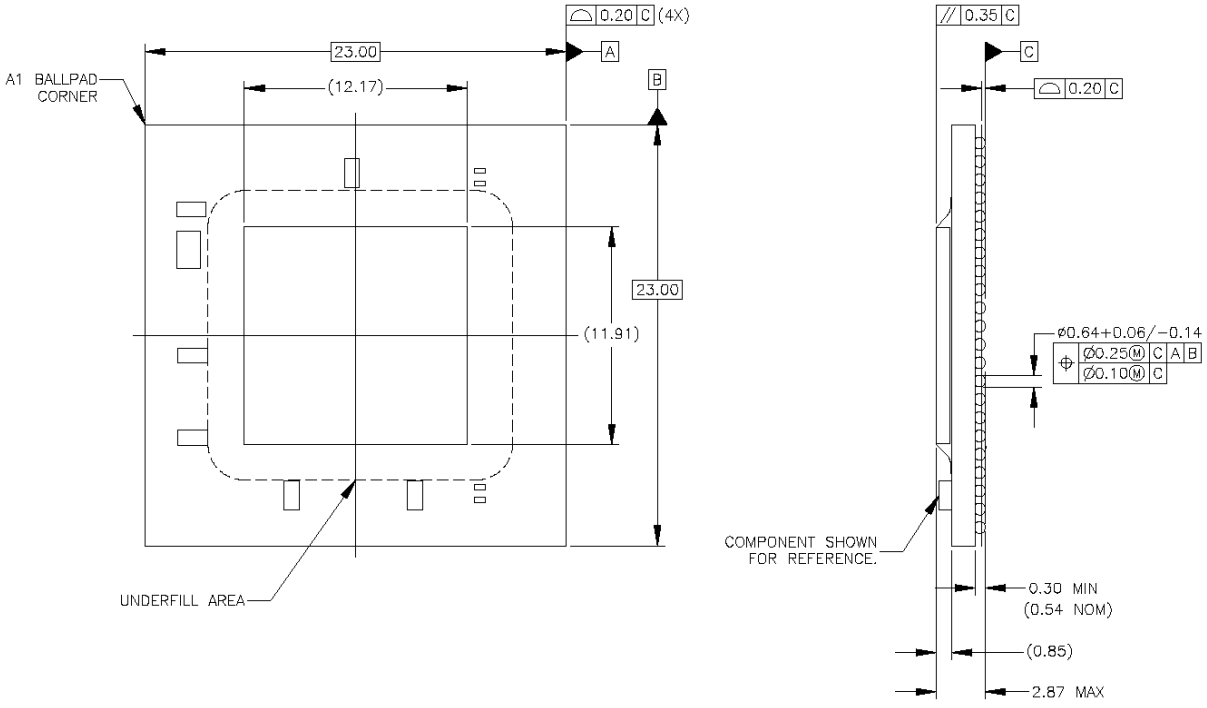


Figure 13 • **MPF300-FCG484 Package Top-View and Side-View**



Units: mm

Figure 14 • **MPF300-FCG484 Package Bottom-View**

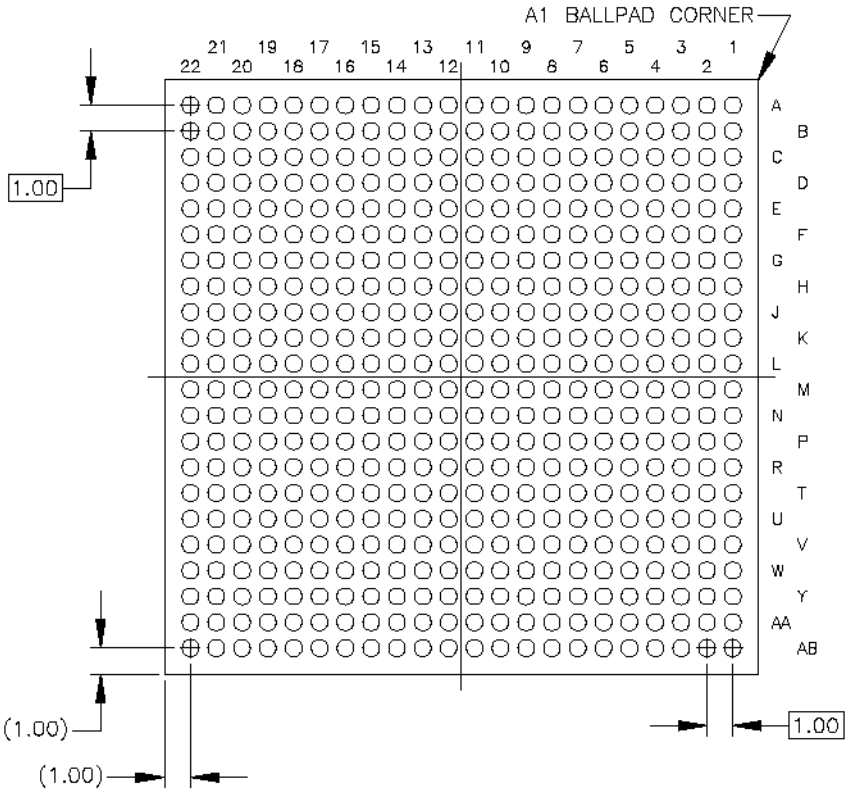
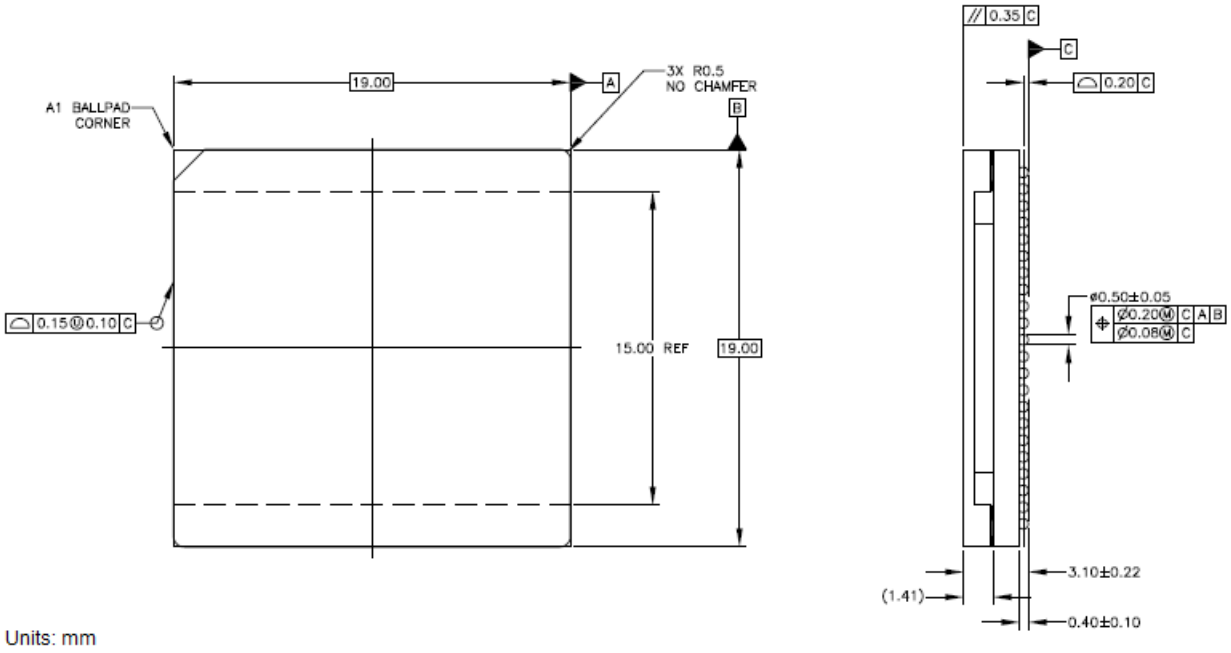


Figure 15 • **FCVG484 Package Top-View and Side-View**



Units: mm

Figure 16 • **FCVG484 Package Bottom-View**

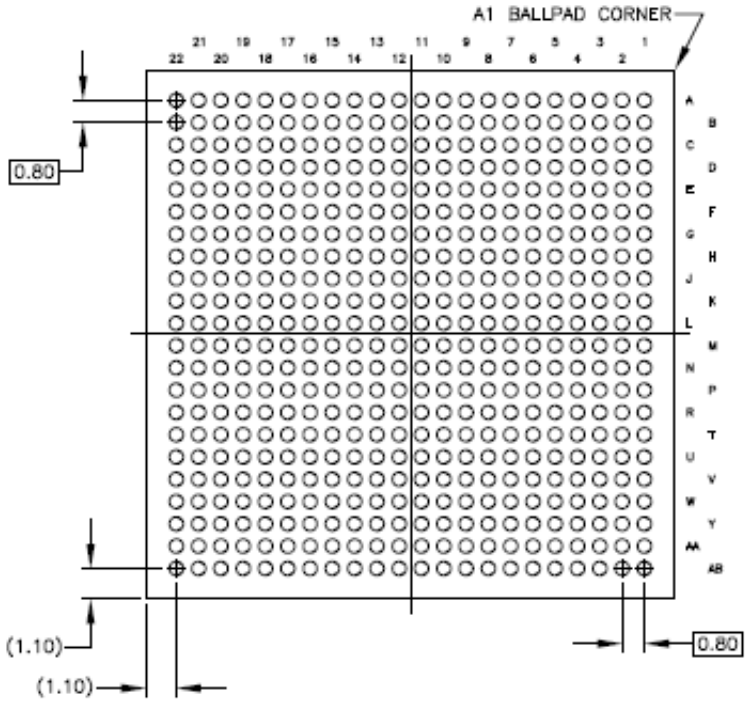


Figure 17 • **FCSG536 Package Top-View and Side-View**

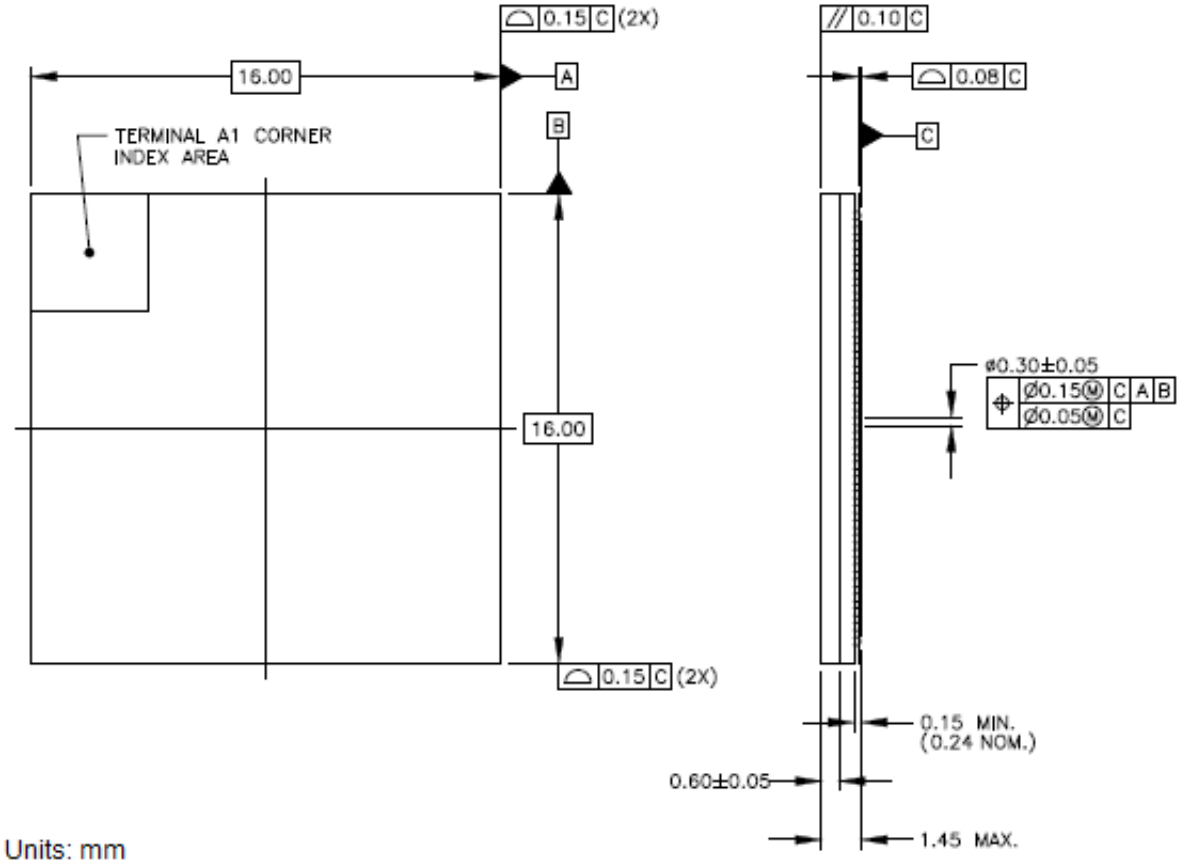


Figure 18 • **FCSG536 Package Bottom-View**

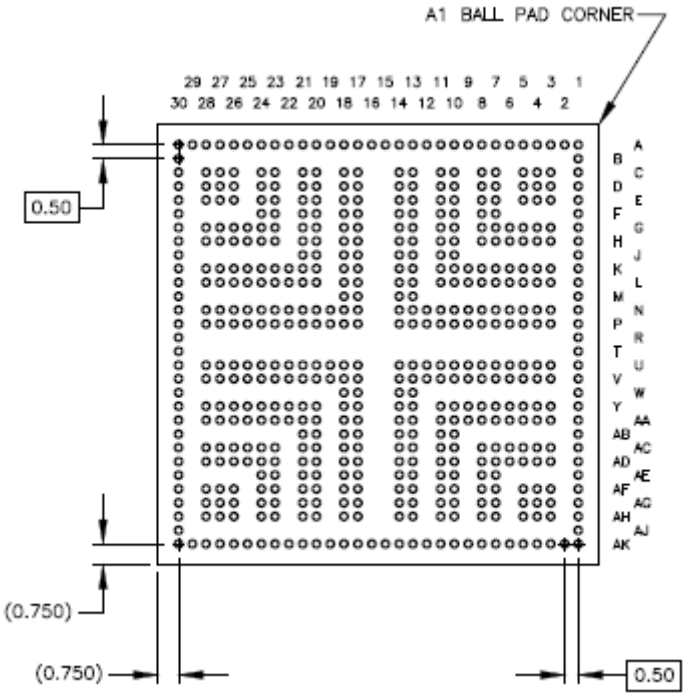


Figure 19 • **MPF200-FCSG325 Package Top-View and Side-View**

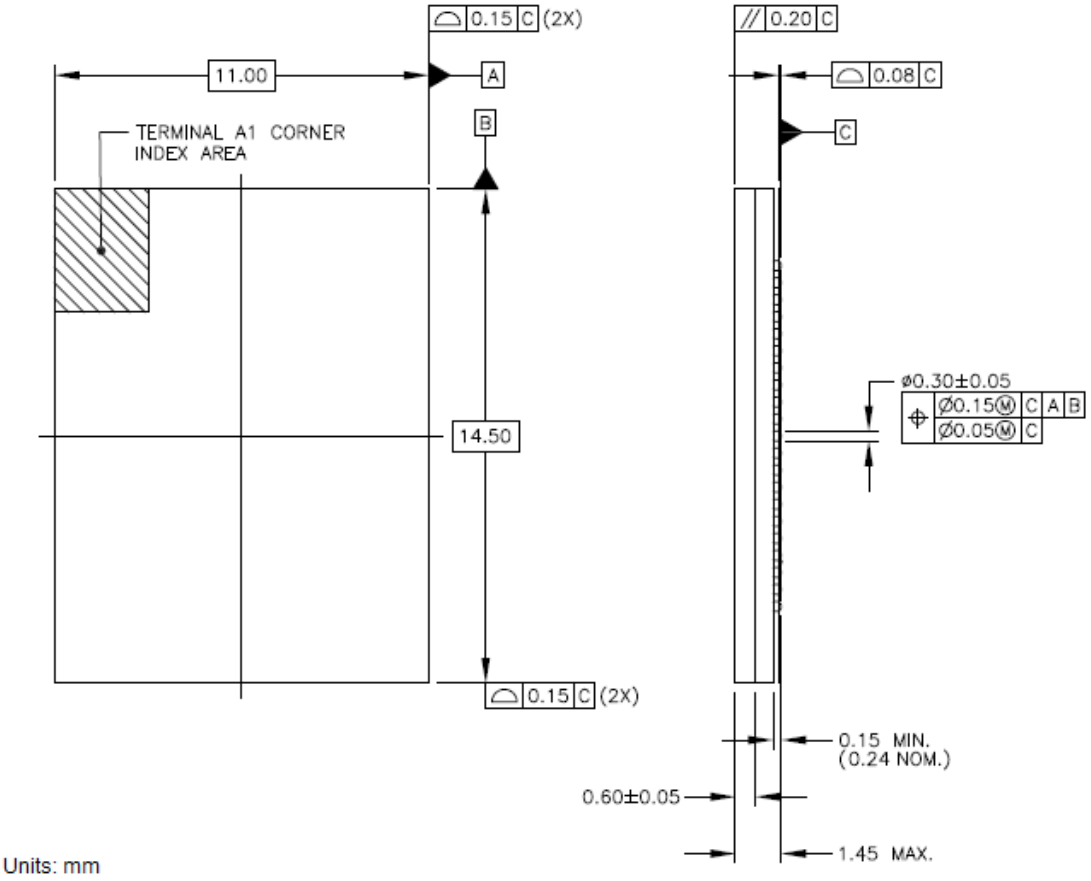


Figure 20 • **MPF200-FCSG325 Package Bottom-View**

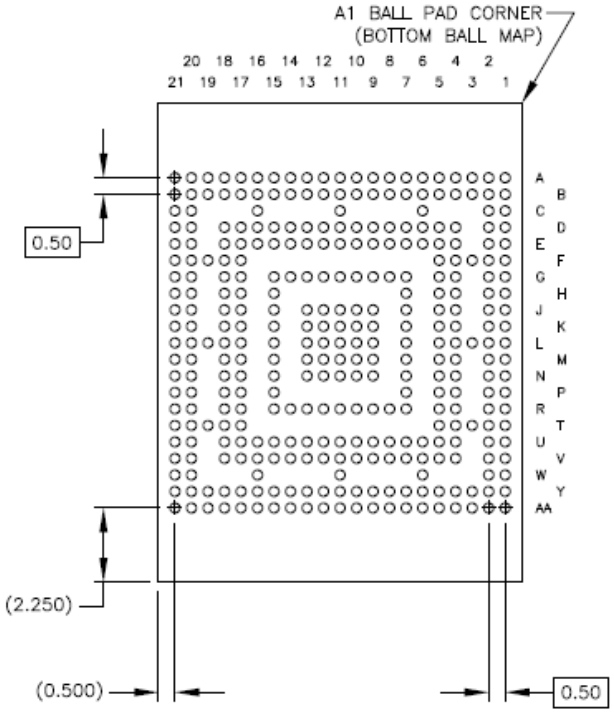


Figure 21 • **MPF100-FCSG325 Package Top-View and Side-View**

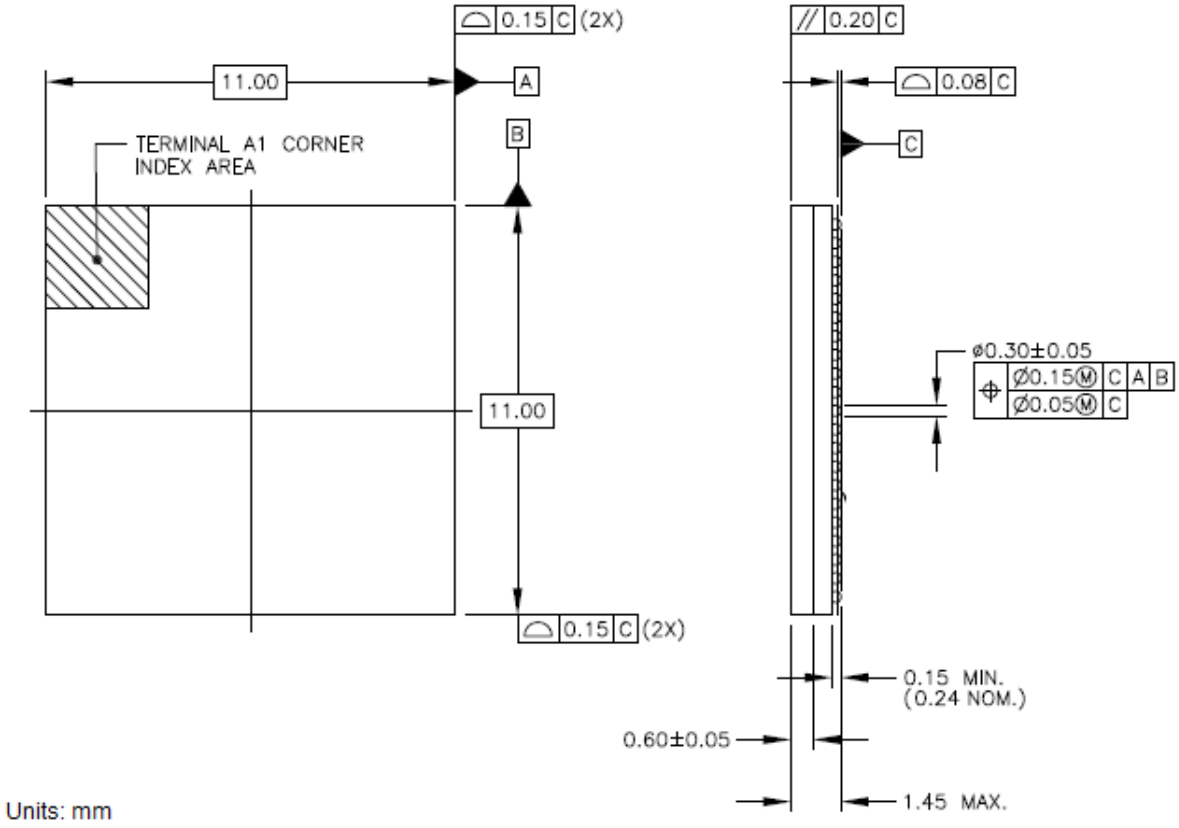
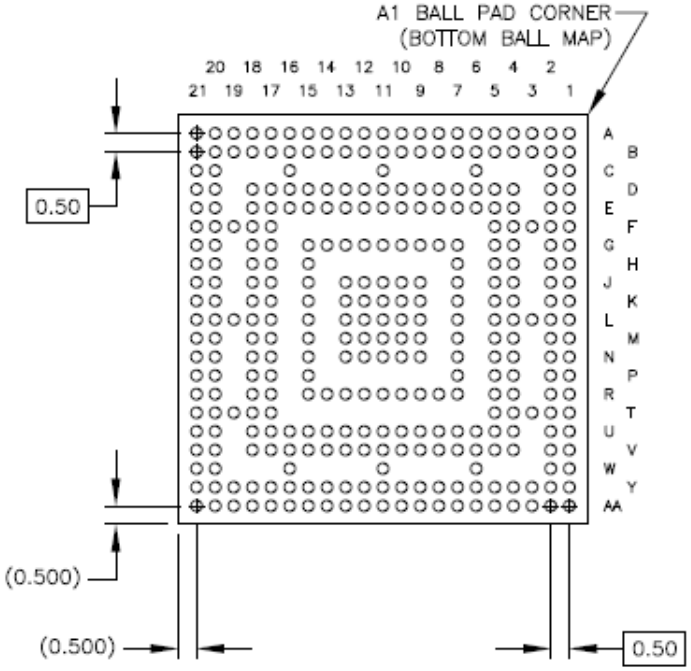


Figure 22 • **MPF100-FCSG325 Package Bottom-View**



The following table lists the PolarFire FPGAs Package description and specification.

Table 17 • **PolarFire FPGAs Package Information**

		Package Specifications			
Package	**Description**	**Package type**	**Pitch (mm)**	**Size (mm)**	**Maximum I/Os**
FCG1152	Flip-chip with lid	BGA	1	35 × 35	512
FCG784	Flip-chip with lid	BGA	1	29 × 29	388
FCG484	Flip-chip	BGA	1	23 × 23	244
FCVG484	Flip-chip with lid	BGA	0.8	19 × 19	284
FCSG536	Flip-chip	CSP	0.5	16 × 16	300
FCSG325	Flip-chip	CSP	0.5	11 × 11, 11 × 14.5	170

2.8 Thermal Specifications

The following table lists the thermal resistances of PolarFire FPGA package devices.

Table 18 • **PolarFire Package Thermal Resistance**

Package	**Environment**	**Theta-JA**	**Theta-JB**	**Theta-JC**	**Psi-JB**	**Psi-JT**	**Unit**
MPF500-FCG1152	Still Air	7.76	1.88	0.293	1.71	0.182	C/W
	1.0 m/s	5.81			2.69	0.185	
	2.5 m/s	4.98			2.57	0.187	
MPF300-FCG1152	Still Air	8.00	2.09	0.429	1.96	0.290	C/W
	1.0 m/s	6.04			2.92	0.288	
	2.5 m/s	5.21			2.79	0.290	
MPF500-FCG784	Still Air	9.31	2.72	0.199	2.23	0.081	C/W
	1.0 m/s	7.19			2.23	0.095	
	2.5 m/s	6.35			2.18	0.101	
MPF300-FCG784	Still Air	9.51	2.95	0.254	2.46	0.114	C/W
	1.0 m/s	7.36			2.43	0.126	
	2.5 m/s	6.51			2.37	0.132	
MPF200-FCG784	Still Air	9.68	3.10	0.345	2.65	0.156	C/W
	1.0 m/s	7.51			2.58	0.171	
	2.5 m/s	6.66			2.52	0.180	
MPF300-FCG484	Still Air	12.40	5.09	0.047	4.16	0.010	C/W
	1.0 m/s	9.88			5.64	0.015	
	2.5 m/s	8.70			5.32	0.016	
MPF300-FCG484 (M Temp)	Still Air	11.74	4.69	0.476	3.68	0.170	C/W
	1.0 m/s	8.92			4.85	0.192	
	2.5 m/s	7.56			4.44	0.207	
MPF200-FCG484	Still Air	12.80	5.56	0.062	4.58	0.014	C/W
	1.0 m/s	10.29			6.05	0.018	
	2.5 m/s	9.12			5.73	0.020	

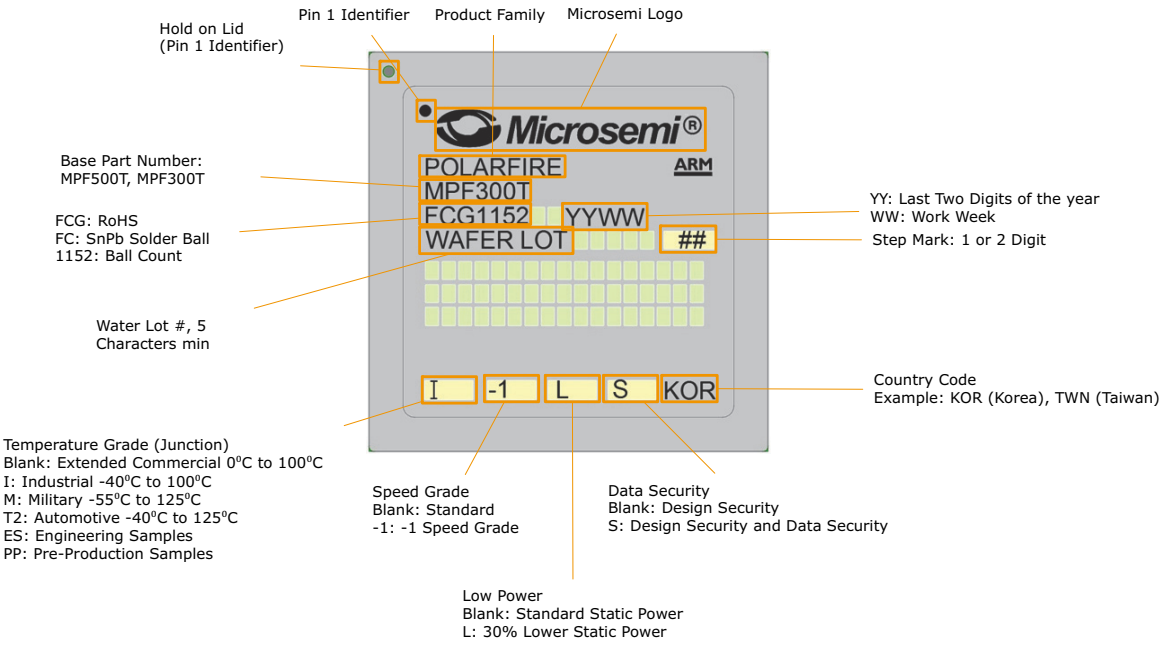
Table 18 • **PolarFire Package Thermal Resistance *(continued)***

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
MPF100-FCG484	Still Air	13.52	6.37	0.979	5.30	0.021	C/W
	1.0 m/s	11.02			6.76	0.022	
	2.5 m/s	9.86			6.46	0.024	
MPF300-FCVG484	Still Air	13.19	4.51	0.251	3.66	0.100	C/W
	1.0 m/s	11.11			3.96	0.110	
	2.5 m/s	9.88			3.81	0.116	
MPF200-FCVG484	Still Air	13.39	4.75	0.341	3.9	0.144	C/W
	1.0 m/s	11.30			4.18	0.157	
	2.5 m/s	10.06			4.02	0.166	
MPF100-FCVG484	Still Air	13.67	5.02	0.509	4.17	0.247	C/W
	1.0 m/s	11.58			4.45	0.264	
	2.5 m/s	10.34			4.29	0.274	
MPF300-FCSG536	Still Air	14.17	3.46	1.749	3.57	0.054	C/W
	1.0 m/s	11.49			6.73	0.113	
	2.5 m/s	10.40			6.47	0.159	
MPF200-FCSG536	Still Air	14.90	4.45	2.123	4.10	0.059	C/W
	1.0 m/s	12.32			7.53	0.119	
	2.5 m/s	11.19			7.23	0.187	

2.9 Package Marking

Microsemi normally marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microsemi's PolarFire FPGA device.

Figure 23 • **Detailed Marking for Each Character Code**



2.10 Packing and Shipping

The PolarFire series devices are packed in trays, which are used to pack most of the Microsemi surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 19 • **Standard Device Counts per Tray and Carton**

Package	Maximum Number of Devices Per Tray	Maximum Number Trays Per Stack	Maximum Number of Units per Inner Carton
FCG1152	24	5	120
FCG484	60	5	300
FCVG484	84	5	420
FCSG536	90	5	450
FCSG325	176	5	880

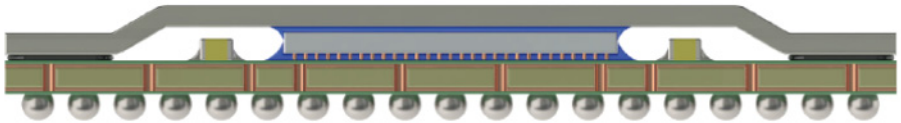
2.11 Thermal Management

Microsemi PolarFire FPGAs are offered in lidded flip-chip BGA (FCBGA) format. Lidded FCBGA features a controlled bond-line thermal interface material (TIM) thickness that reduces the thermal resistance (Theta-JC) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the printed circuit board.

Optimized package electrical performance with multiple power and ground planes to take care of signal return paths, and dense core via under the die to improve power delivery adds benefit in dissipating heat through the bottom of the package and to the board.

PolarFire FPGAs in FCG484 are also available in bare die FCBGA. Bare die flip-chip BGA produces the lowest possible thermal resistance (Theta-JC) between the junction and any externally applied thermal solution.

Figure 24 • **Heat Spreader with Thermal Interface Material**



2.11.1 System Level Heat Sink Solutions

The use of external heat sinks, component placement in the PCB, and air flow in the system depends on the physical and mechanical limitations of the system. A system level thermal design engineer must understand these limitations and device capabilities to effectively manage the complete thermal strategy.

2.12 Thermal Interface Material

When using external heat sinks, a suitable thermal interface material must be considered to effectively transfer the heat from the component to the heat sink, and eventually to the environment.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. Microsemi recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

For lidded flip-chip BGAs, the lid contacts the external heat sink while bare die flip-chip BGAs, the surface of the silicon contacts the external heat sink. The surface areas of lidded flip-chip BGAs and bare die flip-chip BGAs are different. The system level thermal design engineer must choose the appropriate TIM to be used.

Thermal interface material is required because the surfaces of both the PolarFire package and heat sinks base are not smooth. The surface roughness reduces the effective contact area between the package and the heat sinks base. The insulating air gaps created by voids between contacting surfaces are too large. The thermal interface materials fills these gaps and allows an effective conductive transfer of heat from the package to the external heat sink.

Selection of the appropriate thermal interface material is critical to ensure the lowest thermal contact resistance. One must consider the thermal conductivity of the TIM—flatness of the surface contact areas, the applied pressure on the thermal interface material and the total thermal contact area. In addition to thermal performance, TIMs are selected based on the ease of use in assembly and long term reliability.

2.12.1 Heat Sink Attachments

There are six main methods for heat sink attachment. The following table lists their advantages and disadvantages.

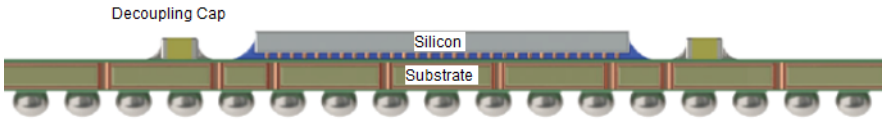
- Thermal tape
- Thermally conductive adhesive
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs
- Thermal compound (also called as thermal gel, thermal grease, thermal paste, heat-sink paste or heat-sink compound)

2.13 Heat Sink Guidelines for Bare-die Flip-Chip Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

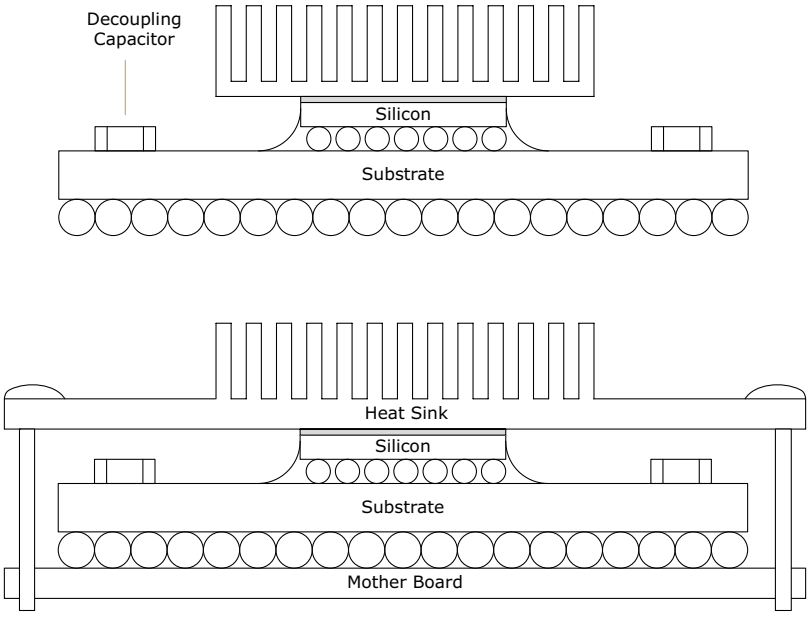
When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered. This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors. When attaching the heat sink to the bare-die flip-chip BGA, ensure that the TIM thickness and the force applied during heat sink placement are even.

Figure 25 • **Cross Section of Bare-die Flip-chip BGA**



Care must be taken while attaching a heat sink to the bare-die package after the component is placed onto the PCBs.

Figure 26 • **Recommended Application of Heat Sink**



2.14 Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

2.15 Recommended PCB Design Rules for BGA Packages

Microsemi provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in Table 20, page 27. For Microsemi BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter) as shown in the following figure.

The space between the NSMD pad and the solder mask; the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Figure 27 • **Ball and Via Dimensions**

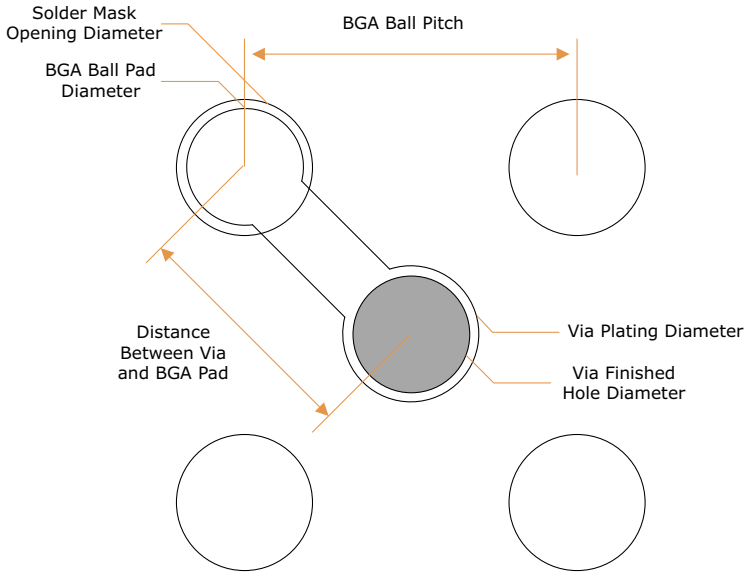


Table 20 • **Recommended PCB Design Rules**

	0.5 mm Pitch	0.8 mm Pitch	1.0 mm Pitch
Design Rule for Packages	**FCSG**	**FCVG**	**FCG**
BGA Ball Pad Diameter	0.27 mm	0.4 mm	0.51 mm
Solder mask opening diameter	0.3 mm	0.43 mm	0.54 mm
BGA Ball pitch	0.5 mm (19.7 mils)	0.8 mm (31.5 mils)	1.00 mm (39.37 mils)
Line width between via and solder land	0.13 mm	0.13 mm	0.15 mm
Distance between via and solder Land	0.35 mm	0.56 mm	0.7 mm
Via Finished hole diameter	0.1 mm	0.33 mm	0.33 mm
Via Plating Diameter	0.25 mm	0.48 mm	0.48 mm

Note: For more information about package fanout, see *AC462: PolarFire FPGA Package Fanout Application Note*.

2.16 Moisture Sensitive Level

The following table lists Microsemi PolarFire packages moisture sensitive levels (MSL).

Table 21 • **Moisture Sensitive Levels**

Package	MSL
FCG1152	4
FCG784	4
FCG484	4
FCVG484	4
FCSG536	3
FCSG325	3