UG0726
User Guide
PolarFire FPGA Board Design

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 7.0

The following is a summary of the changes made in this revision:

- Added MIPI Hardware Design Guidelines, page 20.
- Added reset guidelines in Reset, page 16.
- Added power-supply decoupling capacitors for the following device packages:
  - MPF200T-FCG484 (0.8 mm), see Table 7, page 8.
  - MPF200T-FCSG536 (0.5 mm), see Table 8, page 8.
  - MPF200T-FCG325 (0.5 mm), see Table 9, page 9.
  - MPF100T-FCG325 (0.5 mm), see Table 10, page 9.
  - MPF100T-FCG484 (0.8 mm), see Table 11, page 10.

1.2 Revision 6.0

The following is a summary of the changes made in revision 6.0 of this document:

- Reference Voltage (V_{REFx})information updated in Power Supplies, page 4.
- Added basic information about Pin Assignment Tables, page 14.
- Power-Supply Decoupling Capacitors—MPF300T - FCG1152/FCG784/FCG484 updated in Table 3, page 6.
- Power-Supply Decoupling Capacitors—MPF500T - FCG1152/FCG784 (1mm), Power-Supply Decoupling Capacitors—MPF200T - FCG784/FCG484 (1mm), and MPF100T - FCG484 (1mm) added in Table 2, page 5, Table 6, page 7, and Table 12, page 10 respectively.
- Added MIPI Hardware Design Guidelines, page 20.
- Added Reset, page 16.

1.3 Revision 5.0

The following is a summary of the changes made in revision 5.0 of this document:

- Details of power supply decoupling capacitors for MPF300-FCG1152, MPF300-FCG484, MPF300-FCG784, MPF300-FCVG484, and MPF300-FCSG536 devices were updated. For more information, see Table 3, page 6, Table 4, page 6, and Table 5, page 7.
- XCVR_REF and VDD_XCVR_CLK supply pins details were added. For more information, see Power Supplies, page 4).
- Information about VDDIx and VDDAUXx power supplies was updated. For more information, see Unused Power Supply, page 12.
- A note about the power supply constraint of VDDI3 and VDD_XCVR_CLK pins was added. For more information, see Power Supplies, page 4.
- Details of decoupling capacitors in PolarFire devices were added. For more information, see Table 13, page 11.
- Additional information about VDDIx, VDDAUXx, and VDD_XCVR_CLK pins was added. For more information, see Unused Power Supply, page 12.
- The design checklist for XCVR pins was updated. For more information, see Table 19, page 23.
- Information about VREF was added to core power supply operation details. For more information, see Power Supplies, page 4.
- Information about cold sparing was updated. For more information, see Cold Sparing, page 14.
- JTAG pin details were updated. For more information, see Table 16, page 17.
- The SPI master mode programming connectivity diagram was updated. For more information, see Figure 7, page 18.
- Information about device reset was updated. For more information, see Reset, page 16.
- DDR3 and DDR4 placement and routing guidelines were removed. These guidelines are available in *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

1.4 Revision 4.0

Revision 4.0 was published in September 2017. The sections *Termination Schemes* and *PCB Capacitor Placement and Mounting Techniques* were removed from this document.

1.5 Revision 3.0

Following is a summary of changes made in revision 3.0 of this document:

- Added the Board Design Checklist chapter. For more information, see Board Design Checklist, page 23.
- Added the Special Pins, page 19 section in the PolarFire FPGA Board Design, page 3 chapter.
- Updated the Power-up sequence for core supplies. For more information, see Power Supplies, page 4 and Power-Supply Topology, page 11.
- Removed a note related to XCVR_TX and RX signals under the Unused Power Supply, page 12 section.
- Updated the VDDI pin name from VDDIx to VDDI3 in the Device Programming section. For more information, see Device Programming, page 17.

1.6 Revision 2.0

Following was a summary of changes made in revision 2.0 of this document:

- Values in the Power-Supply Decoupling Capacitors—MPF300-FCG484 table were updated.
- Values and parameters were updated in the SPI Master Mode Programming Pins table. For more information, see Table 17, page 18.
- Updated Figure 2. For more information, see Figure 2, page 12.

1.7 Revision 1.0

The first publication of this document.

2 PolarFire FPGA Board Design

Good board design practices are required to achieve expected performance from both PCBs and PolarFire® devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This document is intended for readers who are familiar with the PolarFire device, experienced in digital board design, and know about the electrical characteristics of systems. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of PolarFire FPGAs.

2.1 Designing the Board

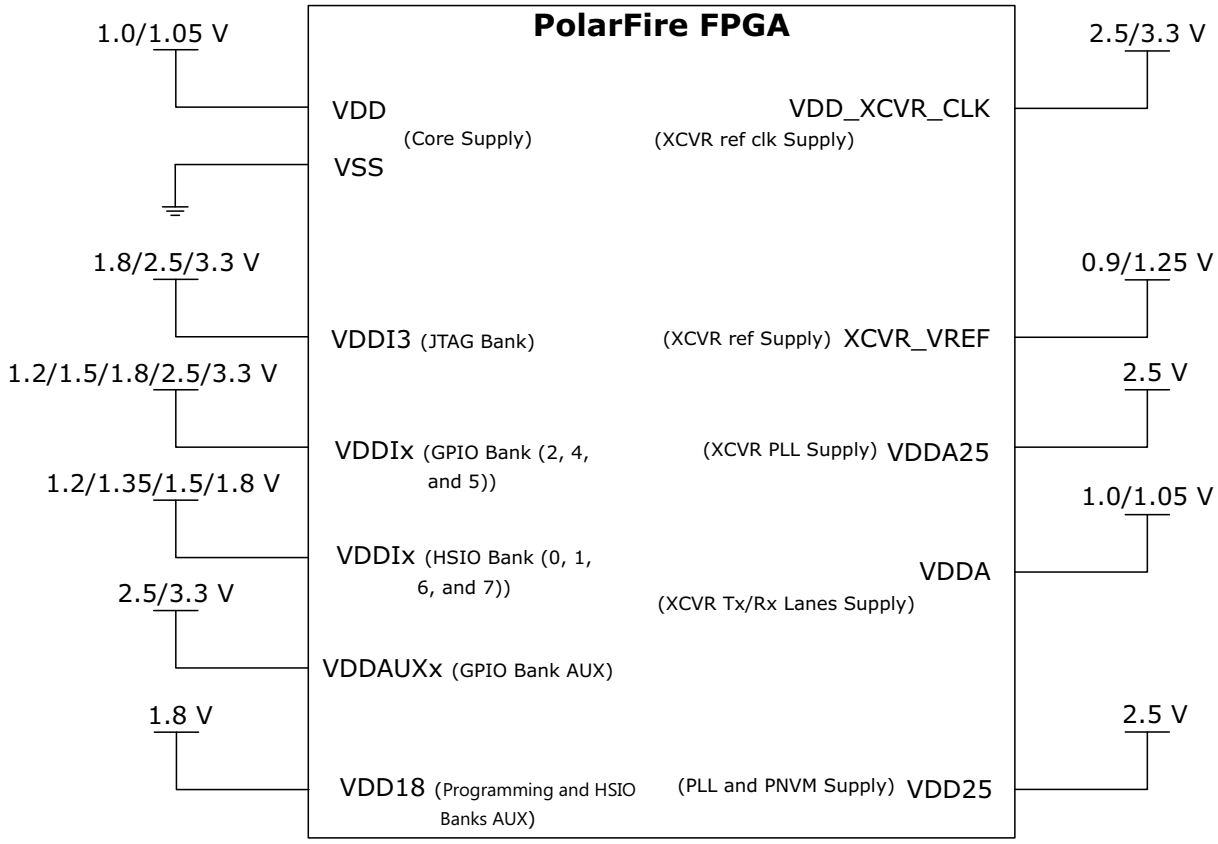
PolarFire FPGAs are flash-based FPGAs that support various high-speed memory interfaces such as DDR3/DDR4, lowest power 12.7 Gbps transceiver (XCVR), built-in low-power dual PCIe Gen2, and fabric I/O such as high-speed I/O (HSIO) and general-purpose I/O (GPIO).

Subsequent sections discuss the following:

2.2 Power Supplies

The following illustration shows the typical power supply requirements for PolarFire devices, and the recommended connections of power rails when every part of the device is used in a system. For information on decoupling capacitors associated with individual power supplies, see PolarFire Decoupling Capacitors, page 5.

Figure 1 • **Power Supplies**



For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the *DS0141: PolarFire FPGA Datasheet*.

The following table lists the various power supplies required for PolarFire FPGAs.

Table 1 • **Supply Pins**

Name	Description
XCVR_VREF	Voltage reference for transceivers
VDD_XCVR_CLK	Power to input buffers for the transceiver reference clock
VDDA25	Power to the transceiver PLL
VDDA	Power to the transceiver TX and RX lanes
VSS	Core digital ground
VDD	Device core digital supply
VDDI3 (JTAG Bank)	Power to JTAG bank pins

Table 1 • **Supply Pins *(continued)***

Name	Description
VDDIx (GPIO Banks)	Power to GPIO bank pins
VDDIx (HSIO Banks)	Power to HSIO bank pins
VDD25	Power to corner PLLs and PNVM
VDD18	Power to programming and HSIO auxiliary supply
VDDAUXx	Power to GPIO auxiliary supply

- V_{REFx}—is the reference voltage for DDR3 and DDR4 signals. VREF voltages can be generated internally and externally.
  - Internal VREF - not subjected to PCB and package inductance and capacitance loss. These changes provide the highest performance and can be programmed as required by DDR controller.
  - External VREF—is fixed and cannot be programed as required. The PCB and package inductance and capacitance impact the V_{REF} performance.

For the GPIO bank, if VDDIx is 2.5 V or 3.3 V, the respective VDDAUXx supply must be tied to the VDDIx supply. If VDDIx for a given GPIO bank is less than or equal to 2.5 V, the respective VDDAUXx supply of the I/O bank must be powered at 2.5 V nominal.

Note: All the other supplies can be powered up in any sequence. The on-chip power-on reset circuitry requires the V_{DD}, V_{DD18}, and V_{DD25} supplies to ramp monotonically from 0 V to the minimum recommended operating voltage.

For a detailed pin description, see *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*.

2.2.1 PolarFire Decoupling Capacitors

The following table lists the requirement of all decoupling capacitors for the MPF300-FCG1152 device.

Table 2 • **Power-Supply Decoupling Capacitors—MPF500T - FCG1152/FCG784 (1mm)**

	Ceramic							Tantalum
Pin Name	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}			4					3
V_{DD18}			2				2	
V_{DD25}			5			1		
V_{DDA}	3	1	6				2	
V_{DDA25}			4				1	
V_{DDIO3}			2			1		
V_{DDAUXx}[1]			2				1	
GPIO Bank[2]			2				1	
HSIO Bank[3]			2				1	
VDD_XCVR_CLK			2			1		
XCVR_VREF			2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF300T-FCG1152/784/484 (1 mm).

Table 3 • **Power-Supply Decoupling Capacitors—MPF300T - FCG1152/FCG784/FCG484 (1 mm)**

	Ceramic							Tantalum
Pin Name	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}			4					2
V_{DD18}			2				2	
V_{DD25}			5				1	
V_{DDA}	3	1	6				1	
V_{DDA25}			4				1	
V_{DDAUXx}[1]			5				1	
V_{DDIO3}			2			1		
GPIO Bank[2]			2				1	
HSIO Bank[3]			2				1	
VDD_XCVR_CLK			2			1		
XCVR_VREF			2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF300-FCVG484 (0.8mm) device.

Table 4 • **Power-Supply Decoupling Capacitors—MPF300T - FCVG484 (0.8mm)**

	Ceramic								Tantalum
Pin Name	**1 nF**	**2.2 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}				4	1				2
V_{DD18}				2				2	
V_{DD25}				5			1		
V_{DDA}		2	2	1				1	
V_{DDA25}	1			1				1	
V_{DDAUXx}[1]				2				1	
V_{DDIO3}				2			1		
GPIO Bank[2]				2				1	
HSIO Bank[3]				2				1	
VDD_XCVR_CLK				2			1		
XCVR_VREF				2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF300-FCSG536 (0.5mm) device.

Table 5 • **Power-Supply Decoupling Capacitors—MPF300T - FCSG536 (0.5mm)**

	Ceramic								Tantalum
Pin Name	**1 nF**	**2.2 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}				4	1				2
V_{DD18}			1	2				2	
V_{DD25}				5			1		
V_{DDA}	2	3	1	1				1	
V_{DDA25}	1			1				1	
V_{DDAUXx}[1]				2				1	
V_{DDIO3}				2			1		
GPIO Bank[2]				2				1	
HSIO Bank[3]				2				1	
VDD_XCVR_CLK				2			1		
XCVR_VREF				2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

Table 6 • **Power-Supply Decoupling Capacitors—MPF200T - FCG784/FCG484 (1mm)**

	Ceramic							Tantalum
Pin Name	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}		2	2					2
V_{DD18}			2				2	
V_{DD25}			5			1		
V_{DDA}	3	1	6				1	
V_{DDA25}			4				1	
V_{DDIO3}			2			1		
V_{DDAUXx}[1]			2				1	
GPIO Bank[2]			2				1	
HSIO Bank[3]			2				1	
VDD_XCVR_CLK			2			1		
XCVR_VREF			2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF200T-FCG484 (0.8 mm) device.

Table 7 • **Power-Supply Decoupling Capacitors—MPF200T - FCVG484 (0.8 mm)**

Pin Name	Ceramic									Tantalum
	1 nF	2.2 nF	4.7 nF	10 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
V_{DD}					4	1				2
V_{DD18}					2				2	
V_{DD25}					5			1		
V_{DDA}		2		2	1				1	
V_{DDA25}	1				1				1	
V_{DDIO3}					2			1		
VDDAUXx[1]					2				1	
GPIO Bank[2]					2				1	
HSIO Bank[3]					2				1	
VDD_XCVR_CLK					2			1		
XCVR_VREF					2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF200T-FCSG536 (0.5 mm) device.

Table 8 • **Power-Supply Decoupling Capacitors—MPF200T - FCSG536 (0.5 mm)**

Pin Name	Ceramic									Tantalum
	1 nF	2.2 nF	4.7 nF	10 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
V_{DD}					4	1				2
V_{DD18}					2				2	
V_{DD25}					5			1		
V_{DDA}	2	3		1	1				1	
V_{DDA25}	1				1				1	
V_{DDIO3}					2			1		
VDDAUXx[1]					2				1	
GPIO Bank[2]					2				1	
HSIO Bank[3]					2				1	
VDD_XCVR_CLK					2			1		
XCVR_VREF					2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF200T-FCG325 (0.5 mm) device.

Table 9 • **Power-Supply Decoupling Capacitors—MPF200T - FCSG325 (0.5 mm)**

Pin Name	Ceramic									Tantalum
	1 nF	2.2 nF	4.7 nF	10 nF	0.1 µF	1 µF	4.7 µF	10 µF	47 µF	330 µF
V_{DD}					4	1				2
V_{DD18}					2				2	
V_{DD25}					5			1		
V_{DDA}		1	1	1	1				1	
V_{DDA25}	1				1				1	
V_{DDIO3}					2			1		
V_{DDAUXx}[1]					2				1	
GPIO Bank[2]					2				1	
HSIO Bank[3]					2				1	
VDD_XCVR_CLK					2			1		
XCVR_VREF					2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF100T-FCSG325 (0.5 mm) device.

Table 10 • **Power-Supply Decoupling Capacitors—MPF100T - FCSG325 (0.5 mm)**

	Ceramic									Tantalum
Pin Name	**1 nF**	**2.2 nF**	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}					4	1				1
V_{DD18}					2				2	
V_{DD25}					5			1		
V_{DDA}		1	1	1	1				1	
V_{DDA25}	1				1				1	
V_{DDIO3}					2			1		
V_{DDAUXx}[1]					2				1	
GPIO Bank[2]					2				1	
HSIO Bank[3]					2				1	
VDD_XCVR_CLK					2			1		
XCVR_VREF					2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the MPF100T-FCVG484 (0.8 mm) device.

Table 11 • **Power-Supply Decoupling Capacitors—MPF100T - FCVG484 (0.8 mm)**

	Ceramic									Tantalum
Pin Name	**1 nF**	**2.2 nF**	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}					4	1				1
V_{DD18}					2				2	
V_{DD25}					5			1		
V_{DDA}		2		2	1				1	
V_{DDA25}	1				1				1	
V_{DDIO3}					2			1		
V_{DDAUXx}[1]					2				1	
GPIO Bank[2]					2				1	
HSIO Bank[3]					2				1	
VDD_XCVR_CLK					2			1		
XCVR_VREF					2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

Table 12 • **Power-Supply Decoupling Capacitors—MPF100T - FCG484 (1 mm)**

	Ceramic							Tantalum
Pin Name	**4.7 nF**	**10 nF**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**	**47 µF**	**330 µF**
V_{DD}		2	2					1
V_{DD18}			2				2	
V_{DD25}			5			1		
V_{DDA}	3	1	6				1	
V_{DDA25}			4				1	
V_{DDIO3}			2			1		
V_{DDAUXx}[1]			2				1	
GPIO Bank[2]			2				1	
HSIO Bank[3]			2				1	
VDD_XCVR_CLK			2			1		
XCVR_VREF			2					

1. Required Decoupling Capacitor for each VDDAUXx.
2. Required Decoupling Capacitor for each GPIO bank.
3. Required Decoupling Capacitor for each HSIO bank.

Decoupling capacitors other than those listed in the previous tables can be used if the physical sizes of capacitors meet or exceed the performance of the network given in this example. Substitution would require analyzing the resulting power distribution system's impedance versus frequency to ensure that no resonant impedance spikes the result. See Figure 1, page 4 for power supply design.

For more information about the internal package capacitance for power supplies associated with PolarFire packages, see section 2.4.2.1 section of *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*.

The following table lists the required decoupling capacitors for PolarFire packages.

Table 13 • **Recommended Decoupling Capacitors For PolarFire Devices**

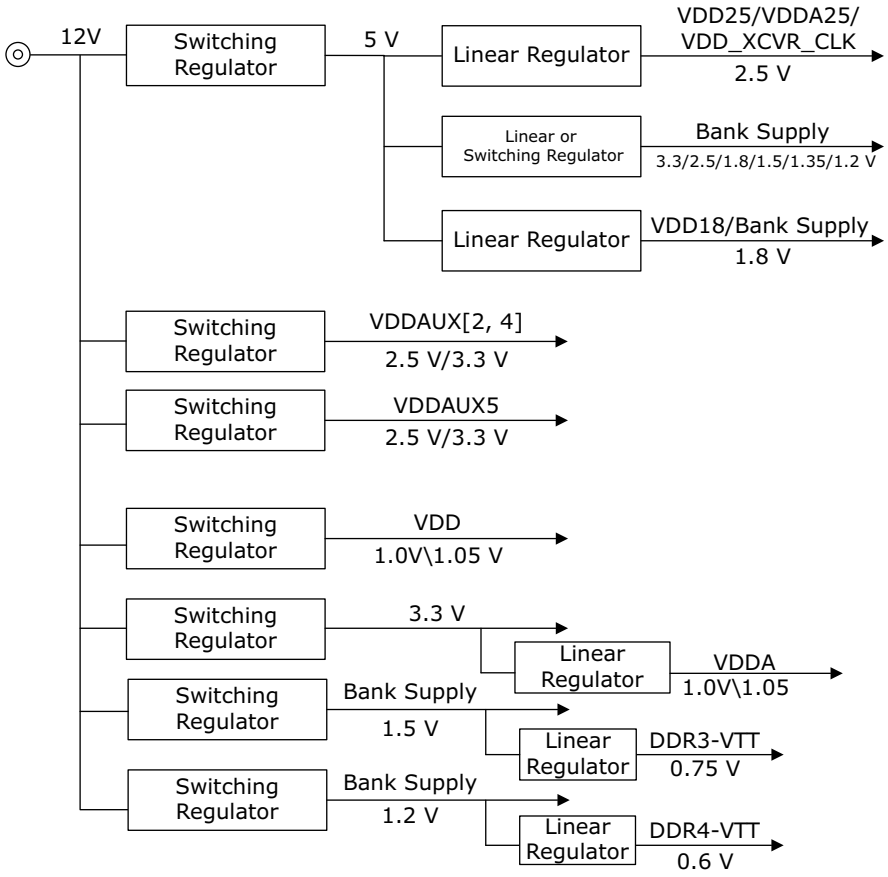
De-Cap Value	Part Number	Package	Description
0.1 µF	GRM155R71C104KA88D	0402	For 1 mm package
10 nF	GRM15XR11C103KA86	0402	For 1 mm package
4.7 nF	GRM155R11H472KA01	0402	For 1 mm package
10 µF	GRM21BR71A106KE51	0805	Bulk Caps (for 0.5, 0.8, and 1 mm)
47 µF	GRM31CR61A476KE15	1206	Bulk Caps (for 0.5, 0.8, and 1 mm)
330 µF	T495D337K010ATE150	2917	Bulk Caps (for 0.5, 0.8, and 1 mm)
1 nF	GRM033R71C102KA01	0201	For 0.8/0.5 mm package
2.2 nF	GRM033R71A103KA01	0201	For 0.8/0.5 mm package
10 nF	GRM033R71A103KA01	0201	For 0.8/0.5 mm package
0.1 µF	GRM033C71C104KE14	0201	For 0.8/0.5 mm package

Note: The user can use equivalent capacitor values from a different vendor.

2.2.2 Power-Supply Topology

PolarFire FPGAs require multiple power supplies. Figure 2, page 12 shows a power supply topology example for generating the required power supplies from a single 12 V source. This example is based on the PolarFire MPF300-FCG1152 device with DDR3 and DDR4 interfaces.

Figure 2 • **Example Power-Supply Topology**



2.2.3 Unused Power Supply

The following figures shows the recommended unused connections for power supplies and I/O banks.

Figure 3 • **Option 1 for Unused Connections**

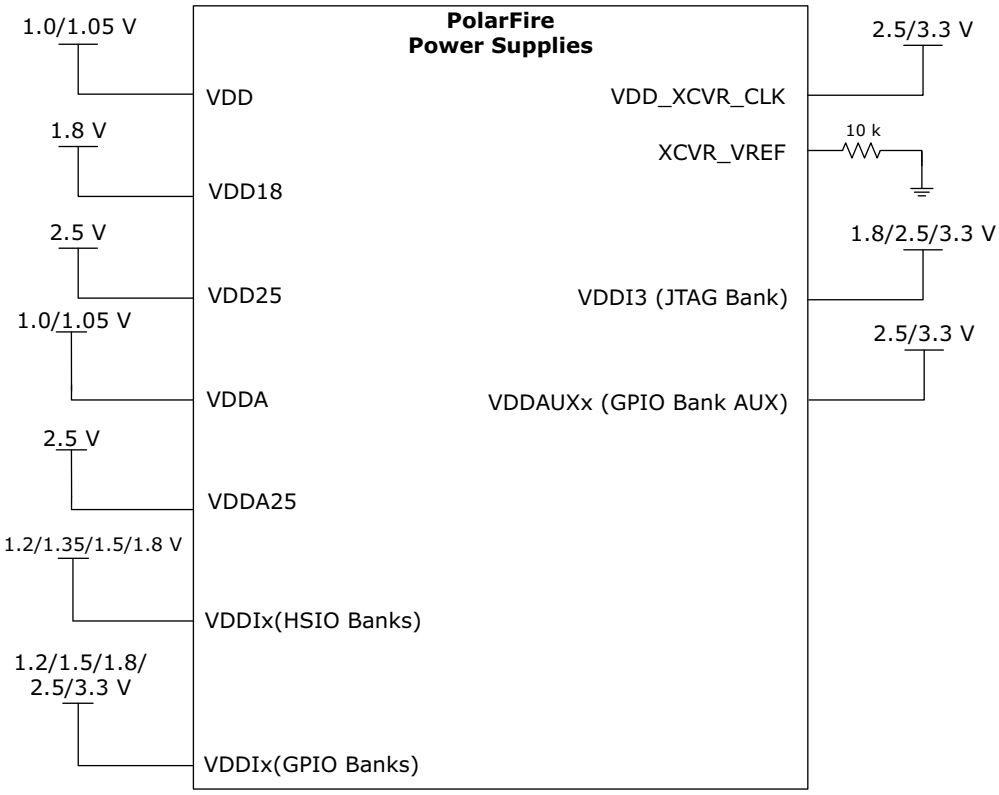
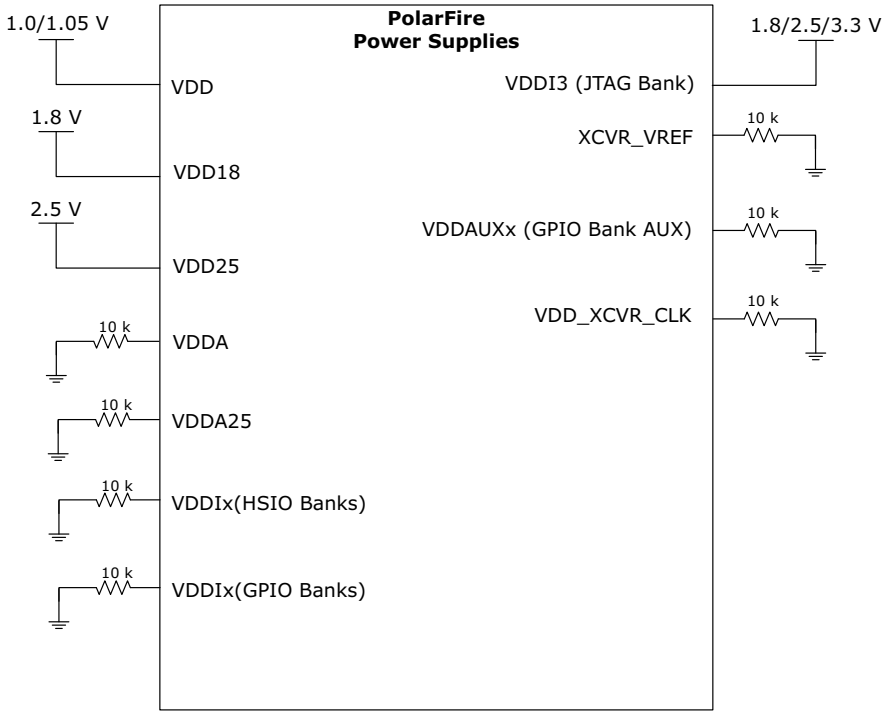


Figure 4 • **Option 2 for Unused Connections**



Note: To simplify the board-level routing, multiple 10 kΩ resistors can be used as required. Or the power supplies can also be grouped into a single 10 kΩ resistor and tied-off to VSS.

2.2.4 Pin Assignment Tables

The Packaging Pin Assignment Table (PPAT) is available on the Microsemi PolarFire documentation web page (*https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#documentation*). PPAT contains information about the recommended DDR pin-outs, PCI EXPRESS capability for XCVR-0, DDR Lane information for IO CDR, generic IOD interface pin placement, and unused condition for package pins.

2.3 I/O Glitch

For GPIO/HSIO outputs, PolarFire devices may undergo a glitch at power-up. The glitch may occur before or after the device reaches a functional state. For GPIOs, a maximum glitch of 1V with a 0.8 ms width, whereas a maximum glitch of 0.5V with a 0.4 ms width may be seen for HSIOs. In either cases, the device is not affected with any reliability issues.

The glitch is caused by a short-term capacitive charging and does not cause any issues in user designs if the system includes a robust reset design that ignores any glitches that inadvertently occur at power-up.

When the glitch cannot be ignored in the user design, it can be mitigated:

- If the user follows the power-up sequence of bringing up VDDI (IO), VDD (Core), and VDDAUX (Auxiliary for GPIO)/VDD18 (Programing and Aux supply for HSIO) respectively.
- If the user does not follow the following power-up sequences:
  - VDD (Core), VDDIO(GPIO), VDDAUX(GPIO-Auxiliary)
  - VDDIO (GPIO), VDDAUX (GPIO-Auxiliary), VDD (Core)

For power-up sequences other than the above-mentioned, a 100K pull-down resistor can be used to mitigate the glitch at each output I/O. This is needed only for critical output nets like resets and clocks. This usage avoids any trigger or event on another device on the clock or reset signals. The resistor can be of any size and tolerance with a minimum voltage of 6V and a minimum power rating of 0.1W.

2.4 User I/O

PolarFire FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2 V to 1.8 V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2 V to 3.3 V.

Note: When the HSIO bank is configured as an LVDS receiver, the concerned I/Os must be connected externally by a 100 Ω resistor

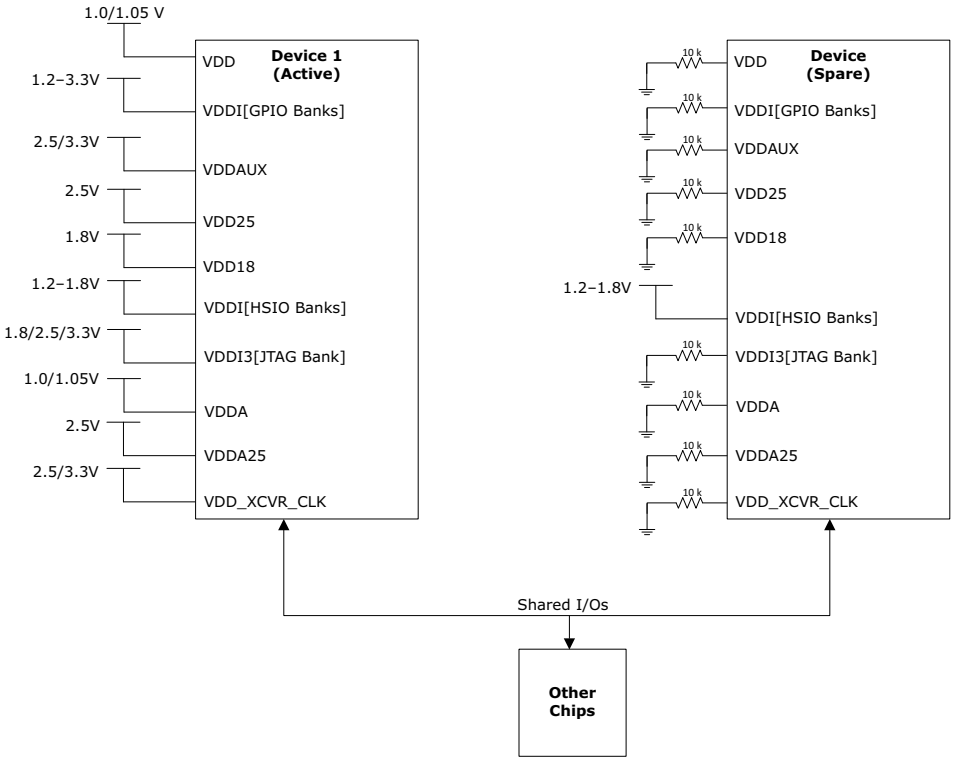
For more information about key features of I/O buffers and supported standards, see *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide* and *UG0686: PolarFire FPGA User I/O User Guide*.

2.4.1 Cold Sparing

PolarFire devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two PolarFire devices in parallel and the devices share I/O. The spare device has its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes. As a result, low power and a protected state for the spare device is established.The spare device can be changed to active device by powering-up all the supplies. The active device can be changed to spare device by powering down all the supplies except HSIO VDDI banks.

A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure.

Figure 5 • **Cold Sparing**



Note: Transceiver and JTAG pins do not support the cold sparing feature.

2.4.2 Hot Socketing (GPIO Only)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the PolarFire FPGA if, at any time, voltage is detected at I/O while the device is powered off. It also helps prevent disruptions that may occur in the rest of the system if the I/O of a device are connected without a valid power supply.

Only GPIOs support hot socketing. In hot socketing, GPIOs are in high-impedance (hi-Z) state.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- V_{DDAUx} is greater than or equal to 1.6 V
- V_{DDIx} is greater than or equal to 0.8 V
- V_{DD} and V_{DD25} are both high and the PolarFire FPGA controller has asserted the global I/O ring signal (IO_EN)

Note:

2.4.2.1 Over-Voltage Tolerance for GPIO

If GPIO is configured with the following settings, GPIO supports over-voltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the V_{DDIx} power supply.

Table 14 • **Over-Voltage Tolerance**

Standard	OE	Clamp Diode	V_{REF} (Input)	Weak Pull-Up/ Pull-Down	Termination	Hot-plug
PCI	x	On	On	On	On	Disabled
GPIO	1	On	On	On	On	Disabled
	0	Off	Off	Off	Off	Enabled

For recommended operating conditions about over-voltage tolerance, see *DS0141: PolarFire FPGA Datasheet*.

2.5 Clocks

PolarFire devices offer two on-chip RC oscillators (one 2 MHz and one 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in PolarFire devices.

Table 15 • **RC Oscillator Count**

Resource	Supported Range (MHz)	MPF100	MPF200	MPF300	MPF500
On-chip oscillator	2	1	1	1	1
	160	1	1	1	1

For more information about clocking in PolarFire devices, see *UG0684: PolarFire FPGA Clocking Resources User Guide*.

2.6 Reset

For designing a robust system users may use the dedicated DEVRST_N pin or a general purpose reset signal using any GPIO/HSIO as a global system level reset.

For the following cases the users must use the DEVRST_N as a warm reset for the device:

- A user design modifies auto-initialized fabric RAMs or PCIe configuration during operation.
- A user design is using PCIe, transceivers or user crypto.

For all other use cases, it is recommended to use a general purpose reset signal using any GPIO/HSIO IO because they take much shorter time for design to come out of reset.

If the dedicated DEVRST_N is not used for warm resets, the DEVRST_N pin must be configured using one of the following methods:

- Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted till the system/clocks are stable and the chip is properly powered up.
- Connect DEVRST_N to VDDI3 through a 1 kΩ resistor per pin without sharing with any other pins.
    - In this case the user needs to ensure that all clocks are stable going to the device before the user design is released from power-on reset. The details of the minimum time taken for the fabric design to be activated after power-on is specified in the PolarFire datasheet (Power-Up To Functional section).

2.7 DDR

PolarFire devices support DDR3, DDR3L, LPDDR3, and DDR4. For more information about the DDR support in PolarFire devices, see *DS0141: PolarFire FPGA Datasheet*.

The reliability of the DDR interface depends on the quality of the layout. For detailed information on board layout and routing, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

2.8 Device Programming

The PolarFire device can be programmed using one of two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI master mode programming
- SPI slave mode programming

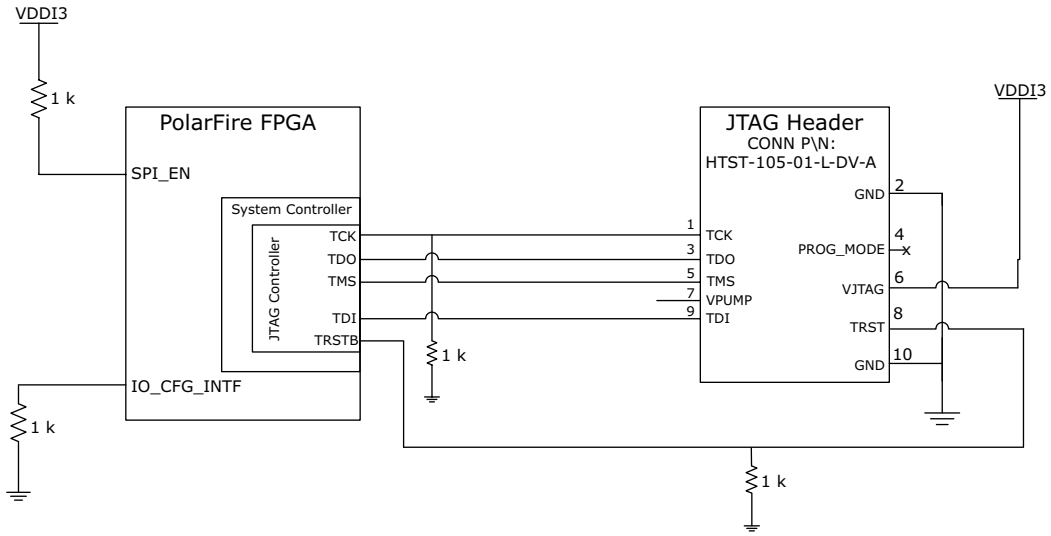
The PolarFire FPGA supports programming modes through the internal system controller using SPI master mode, or an external master using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see *UG0714: PolarFire FPGA Programming User Guide*.

2.8.1 JTAG Programming

The JTAG interface is used for device programming and testing, or for debugging firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are not accessible. JTAG I/Os are powered by Bank 3 V_{DDI}.

The following illustration shows the board-level connectivity for JTAG programming mode in PolarFire devices.

Figure 6 • **JTAG Programming**



The following table lists the JTAG pin names and descriptions.

Table 16 • **JTAG Pins**

Pin Names	Direction	Unused Condition	Description
TMS	Input	DNC	JTAG test mode select.
TRSTB	Input	Must be connected to V_{DDI3} through a 1 kΩ resistor	JTAG test reset. Must be held low during device operation.

Table 16 • **JTAG Pins** ***(continued)***

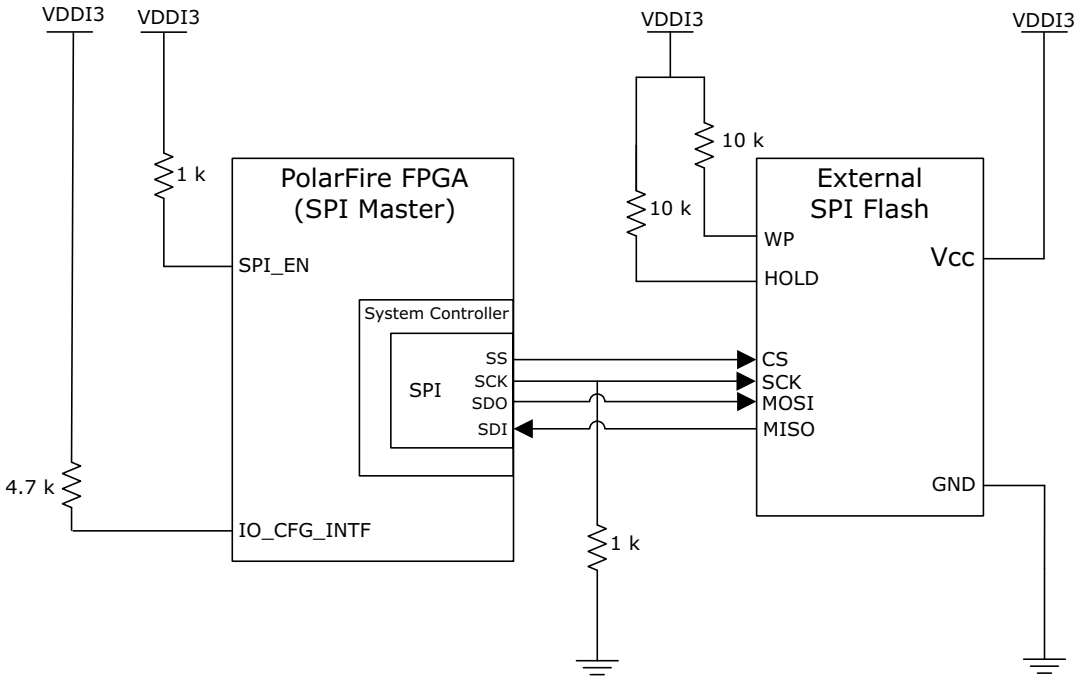
Pin Names	Direction	Unused Condition	Description
TDI	Input	DNC	JTAG test data in.
TCK	Input	Must be connected to VSS through a 10 kΩ resistor	JTAG test clock.
TDO	Output	DNC	JTAG test data out.

2.8.2 SPI Master Mode Programming

The embedded system controller contains a dedicated SPI block for programming, which can operate in master or slave mode. In master mode, the PolarFire device interfaces are used to download programming data through the external SPI flash. In slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following illustration shows the board-level connectivity for SPI master mode programming in PolarFire devices.

Figure 7 • **SPI Master Mode Programming**



The following table lists the SPI master mode programming pins.

Table 17 • **SPI Master Mode Programming Pins**

SPI Pin Name	Direction	Unused Condition	Description
SCK	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI clock.[1]
SS	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI slave select.[1]

Table 17 • **SPI Master Mode Programming Pins *(continued)***

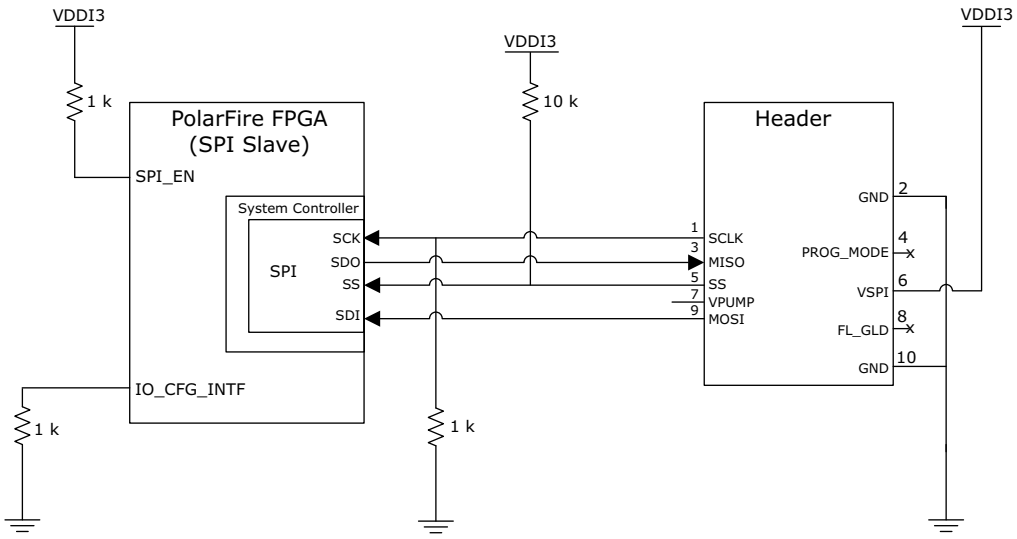
SPI Pin Name	Direction	Unused Condition	Description
SDI	Input	Connect to V_{DDI3} through a 10 kΩ resistor	SDI input.[1]
SDO	Output	DNC	SDO output.[1]
SPI_EN	Input	Connect to VSS through a 10 kΩ resistor	SPI enable. 0: SPI output tri-stated 1: Enabled Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Connect to VSS through a 10 kΩ resistor	SPI I/O configuration. 0: SPI slave interface 1: SPI master interface Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a master or slave.

1. The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

2.8.3 SPI Slave Mode Programming

The following illustration shows the board-level connectivity for SPI slave mode programming in PolarFire devices.

Figure 8 • **SPI Slave Mode Programming**



2.8.4 Special Pins

For information about special pins, see Table 13 of *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*.

2.9 Transceiver

The following table lists the transceiver features supported in PolarFire devices, and transceiver blocks are located on the east corner of the device. PolarFire devices support PCIe interface supports only Transceiver quad 0.

For more information about implementing PCIe interfaces, see *UG0685: PolarFire FPGA PCI Express User Guide*. For more information about implementing other transceiver based interfaces and power supplies, see *UG0677: PolarFire FPGA Transceiver User Guide*.

The following table lists the number of transceivers supported in various PolarFire devices.

Table 18 • **Transceiver Support in PolarFire Devices**

Device	Transceiver Lane	Tx PLL	Reference Clock I/O
MPF100	8	6	12
MPF200	16	11	22
MPF300	16	11	22
MPF500	24	15	30

For more information about supported I/O standards, see *UG0686: PolarFire FPGA User I/O User Guide*.

2.9.1 Reference Clock

A transceiver reference clock is delivered to each transmit PLL for transmit functions and to each receiver lane for receive clock data recovery (CDR).

2.9.1.1 Transceiver Reference Clock Requirements

The following are requirements for the transceiver reference clock:

- When differential clock input is provided to the reference clock:
  - ODT must be enabled for transceiver reference clock pins.
  - Must be within the range of 20 MHz to 400 MHz.
- Must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board. The reference I/O standards such as LVCMOS25, SSTL18, LVDS25, and HCSL25 are supported. For more information, see *UG0677: PolarFire FPGA Transceiver User Guide*.

See the *PCI Express Base specification Rev 2.1* for detailed PHY specifications. Also, see the *PCIe Add-in Card Electro-Mechanical (CEM)* specifications.

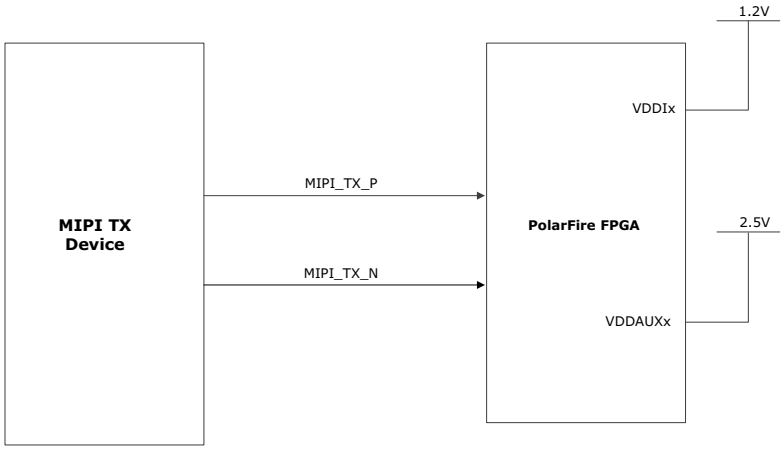
2.10 MIPI Hardware Design Guidelines

The following sections discuss the guidelines for MIPI RX and TX interface with PolarFire device.

2.10.1 MIPI RX

The MIPI RX is supported only in GPIO Bank. The corresponding Bank voltage (VDDI), and VDDAUX voltage must be connected as shown in the following figure.

Figure 9 • **MIPI RX Connection**



MIPI RX signal connections are as follows:

- Four data and clock must be within one DDR_Lane.
- Connect the data signals to adjacent DDR_Lanes, if more than four data signals are available.
- The MIPI RX clock must be connected to a CLKIN pin.

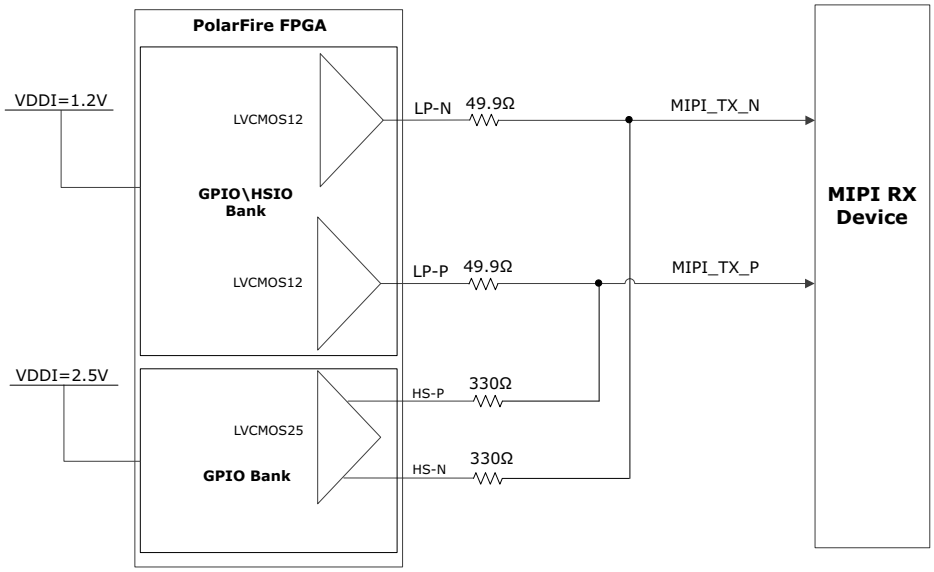
For more information about the DDR_Lane information, see the package pin assignment tables available at https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#documentation.

2.10.2 MIPI TX

The MIPI LP (Low Power) signals should be connected to a 1.2 V GPIO\HSIO Bank supply and High-speed signals should be connected to a 2.5 V GPIO Bank supply. Select the HS and LP pins in adjacent pins to minimize the LP stub. The HS data and clock signals should be in one DDR_Lane. For more information about DDR_Lane information, see the package pin assignment tables available at https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#documentation.

The MIPI TX standard can be implemented by using the resistor divider network for LP (Low Power) and HS (High speed) signals, as shown in the following figure. The resistor values mentioned in the following provide a throughput upto of 1 Gpbs.

Figure 10 • **MIPI TX Connections**



Note: Run the PDC verification in the Libero tool before moving to layout. To know about MIPI RX electrical characteristics, refer the *DS0141: PolarFire FPGA Datasheet*.

For information about the MIPI layout guidelines, see MIPI, page 27.

2.11 AC and DC Coupling

Each transmit channel of a PCIe lane must be AC-coupled to allow link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, Microsemi recommends that a PolarFire device receives inputs that are AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to *DS0141: PolarFire FPGA Datasheet* electrical specifications.

For lower data rates as per the data sheet, DC coupling is supported by PolarFire Transceiver Tx and Rx interfaces through a configuration option. If a PolarFire transmitter is used to drive a PolarFire receiver in DC-coupled mode, select the lowest common mode setting for the transmitter.

2.12 Brownout Detection

The PolarFire FPGA functionality is guaranteed only if V_{DD} is above the recommended level specified in the Datasheet. Brownout detection occurs when V_{DD} drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout. The V_{DD} supply is protected by an built-in brownout detection circuit.

3 Board Design Checklist

This chapter provides a set of hardware board design checks for designing hardware using Microsemi PolarFire FPGAs. The checklists provided in this chapter are a high-level summary checklist to assist the design engineers in the design process.

3.1 Prerequisites

Ensure that you have gone through the following chapters before reading this chapter:

- PolarFire FPGA Board Design, page 3
- Appendix: General Layout Design Practices, page 27

This checklist is intended as a guideline only. The PolarFire family consists of FPGAs ranging from densities of 100 K to 500 K logic elements (LEs).

3.2 Design Checklist

The following table lists the various checks that design engineers must take care while designing the system.

Table 19 • **Design Checklist**

Guideline	Yes/No	Remarks
Prerequisites		
– See *DS0141: PolarFire FPGA Datasheet* – See *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide*		
Refer to the board-level schematics of PolarFire Evaluation Kit		
Device Selection		
Check for available device variants for PolarFire FPGA – Select a device based on I/O pin count, transceivers, package, phase-locked loops (PLLs), and speed grade		
Check device errata in PolarFire FPGA Errata		
Design Checklist		
Power Analysis Download the *PolarFire Power Estimator* and check for the power budget.		
Power Supply Checklist See Figure 1, page 4 for used power rails, and Figure 3, page 13 and Figure 4, page 13 for unused rails.		
Decoupling Capacitors Follow PolarFire Decoupling Capacitors, page 5. Perform PI Analysis for any deviation from the recommended capacitors.		
Clocks		
For more information about dynamic phase shift ports, see Table 6 of *UG0684: PolarFire FPGA Clocking Resources User Guide*. The XCVR reference clock ranges from 20 MHz to 400 MHz.		

Table 19 • **Design Checklist *(continued)***

Guideline	Yes/No	Remarks
The global clock network can be driven by any of the following: – Preferred clock inputs (CLKIN_z_w) – On-chip oscillators – CCC (PLL/DLL) – XCVR interface clocks **High-Speed I/O Clocks** High-speed I/O clock networks can be driven by I/O or CCCs. The high-speed I/O clocks can feed reference clock inputs of adjacent CCCs through hardwired connections. **CCC** The CCC can be configured to have a PLL or DLL clock output, driving a high-speed I/O clock network.		
Global buffer (GB) can be driven through the dedicated global I/O, CCC or fabric (regular I/O) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets. Dedicated global I/O drive the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network. For more information about global clock network, see *UG0684: PolarFire FPGA Clocking Resources User Guide.*		

Table 19 • **Design Checklist *(continued)***

Guideline	Yes/No	Remarks
Reset		
For more information about DEVRST_N and user reset, see Reset, page 16.		
DDR Interface		
For more information about DDR routing and topology, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.		
Programming and Debugging Scheme For programming and debugging information, see Device Programming, page 17.		
XCVR		
For more information about XCVR, see *UG0677: PolarFire FPGA Transceiver User Guide*.		
For I/O gearing interfaces, place the clocks and data based on the defined requirements by selecting the correct I/O. For more information about the placement of User I/O, see *UG0686: PolarFire FPGA User I/O User Guide*.		
There is one IO_CFG_INTF pin available, which can be used as input.		
See the bank location diagrams in the *UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide* to assess the preliminary placement of major components on PCB.		

3.3 Layout Checklist

The following table lists the layout checklist.

Table 20 • **Layout Checklist**

Guideline	Yes/No
Power	
Are the 0402 or lesser size capacitors used for all decapacitors?	
Is the required copper shape provided to core voltage?	
Are the required copper shape and sufficient vias provided to voltages?	
Are VREF planes for the DDRx reference supply isolated from the noisy planes?	
Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply?	
Is one 0.1 µF capacitor for two VTT termination resistors used for DDRx?	
Is the VTT plane width sufficient?	
DDR Memories	
Are the length-match recommended by Micron followed for DDR memories?	
XCVR	
Are the length-match recommendations for XCVR followed?	
Are DC blocking capacitors required for PCIe interface?	
Is tight-controlled impedance maintained along the XCVR traces?	
Are differential vias well designed to match XCVR trace impedance?	
Are DC blocking capacitor pads designed to match XCVR trace impedance?	

Table 20 • **Layout Checklist *(continued)***

Guideline	Yes/No
Dielectric Material	
Is proper PCB material selected for critical layers?	

4 Appendix: General Layout Design Practices

This chapter provides guidelines for the hardware board layout that incorporates PolarFire devices. Good board layout practices are essential to achieve the expected performance from PCBs and PolarFire devices. They help achieve high-quality and reliable results such as low-noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter is intended for readers who are familiar with the PolarFire FPGA chip, experience in digital board layout, and know about line theory and signal integrity.

4.1 MIPI

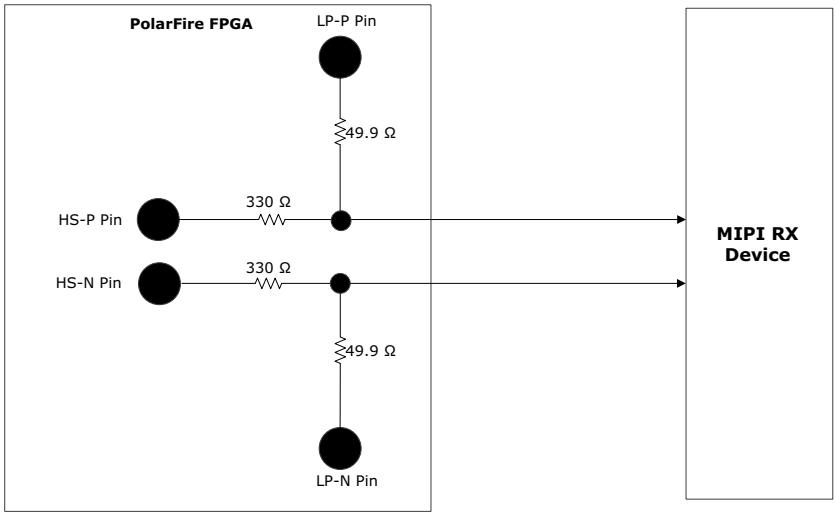
MIPI RX Layout Guidelines:

The data and clock must be matched within 20 mils in PCB.

MIPI TX Layout Guidelines:

As shown in Figure 11, page 27, the LP and HS resistors must be close to the PolarFire device pin. The HS signals should be routed to LP resistors to minimize the LP signals PCB stub length. The LP signals stub should be less than 500 mils. The data lane and clock should be length matched within 20 mils. 8 inches is the maximum length supported.

Figure 11 • **MIPI TX Layout**



4.2 Transceiver

Collateral material of the PolarFire FPGA transceiver enables the system implementation easier for the designer by providing the system solution. Transceivers are high-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 12.7 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications, transceivers technology, or RF/microwave PCB design. However, the PCB design can be evaluated by a knowledgeable high-speed digital PCB designer.

4.2.1 Layout Considerations

This section describes differential traces and skew matching, which must be taken care while designing the PCB layout.

4.2.1.1 Differential Traces

A well-designed differential trace must have the following qualities:

- No Mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

- The traces should be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals in Common mode signals.
- The differential pair should be routed such that the skew within differential pairs is less than 5 mils. The length match should be used by matching techniques.

4.2.1.2 Skew Matching

The length of differential lanes should be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

Differential pairs should be routed symmetrically in-to and out of structures, as shown in Figure 13, page 28.

The following figure shows the skew matching.

Figure 12 • **Skew Matching**

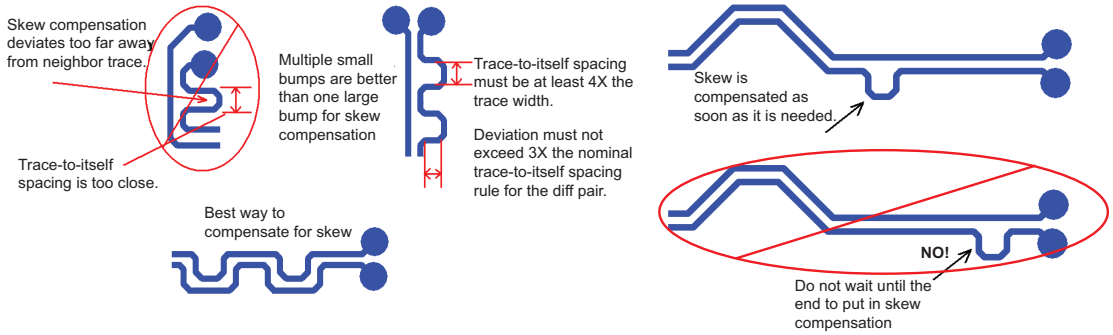


Figure 13 • **Example of Asymmetric and Symmetric Differential Pairs Structure**

Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low dissipation factor (DF) PCB materials such as Nelco 4000-13EP SI. Cost is significantly higher than FR4 PCB material, but FR4 PCB material cannot provide increased eye-opening when longer trace interconnections are required. Ensure that a 85 - 100 Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

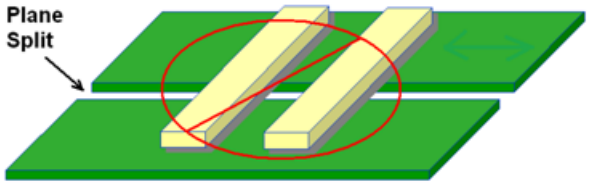
Instruct the fabrication vendor to use these PCB materials before manufacturing.

Transceiver traces must be kept away from the aggressive nets or clock traces. For example, on MPF300 devices, the transceiver and DDR traces should not be adjacent to each other. Trace stubs must be avoided.

It is recommended to use low roughness, that is, smooth copper. As the speed increases, insertion loss due to the copper roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. Microsemi recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

Split reference planes should be avoided. Ground planes must be used for reference for all transceiver lanes.

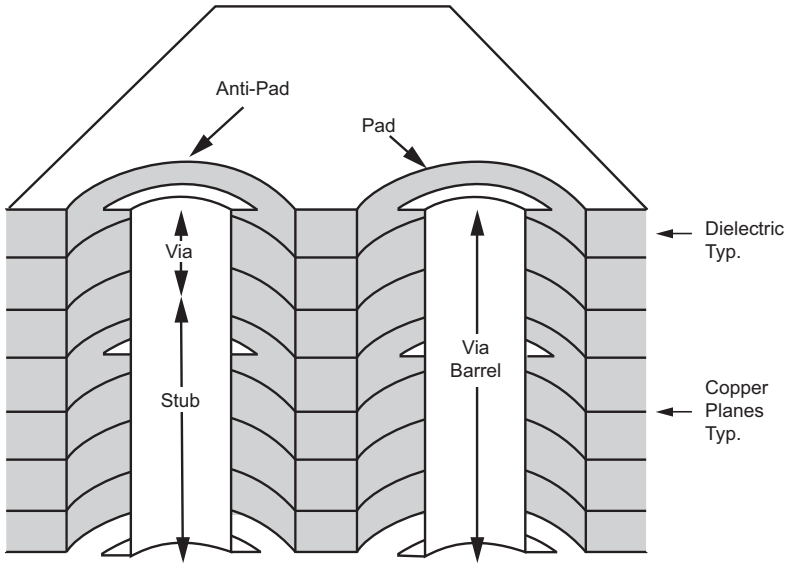
Figure 14 • **Ground Planes for Reference**



4.2.1.3 Via

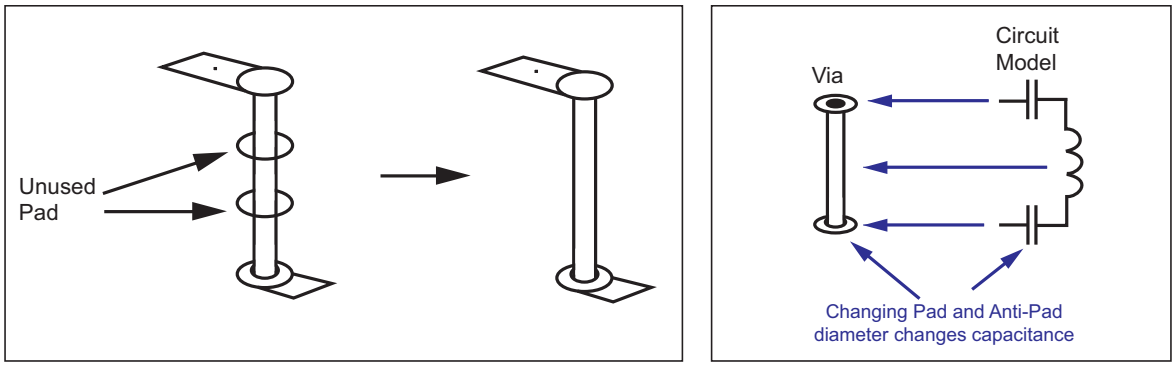
The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

Figure 15 • **Via Illustration**



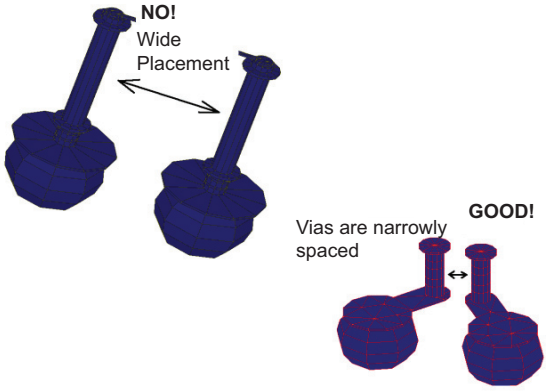
- Many vias on different traces should be avoided, or minimized as much as possible.
- The length of via stubs should be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- If feasible, non-functional pads should be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 16 • **Non-Functional Pads of Via**



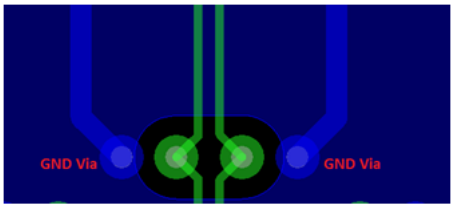
Using tight via-to-via pitches helps reducing the effect of crosstalk, as shown in the following figure.

Figure 17 • **Via-to-Via Pitch**



Symmetrical ground vias (return vias) should be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path for TX and RX to GND. Return vias help maintain the continuity.

Figure 18 • **GND Via or Return Via**



4.2.2 DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed, as shown in the following figure, to match the impedance of the pad to 50 Ω.

Figure 19 • **Capacitor Pad Reference Plane**