Libero SoC v11.7 SP3

Release Notes

01/2017

Microsemi
Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.1

Edited the “PCN 17005.1” section to add a methodology to upgrade System Builder based designs.

Added a known issue and workaround for new designs created using System Builder.

Revision 1.2

Linked to updated version of release that addresses System Builder issue. Moved related known issue content to section 1.1. Minor edits to sections 1.6 and 1.7.1. Added section 1.9.6 – Slack mismatch in SmartTime.

Contents

1 Libero SoC v11.7 SP3 Release Notes

Microsemi Libero® System-on-Chip (SoC) design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's power-efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry-standard synthesis and simulation tools—Synopsys Synplify Pro® and Mentor Graphics ModelSim, respectively—with best-in-class constraints management, debug capabilities, and secure production programming support.

Libero SoC v11.7 Service Pack 3 (SP3) contains critical timing data updates for SmartFusion2 and IGLOO2 families. Microsemi highly recommends that you open your SmartFusion2 and IGLOO2 designs created with Libero SoC v11.7 SP2 or an earlier release in Libero SoC v11.7 SP3, update cores as necessary, and rerun the **Verify Timing** step.

Libero SoC v11.7 SP3 can be used for designing with Microsemi RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion® SoC FPGAs, IGLOO®2, IGLOO, ProASIC3®, and Fusion® FPGA families.

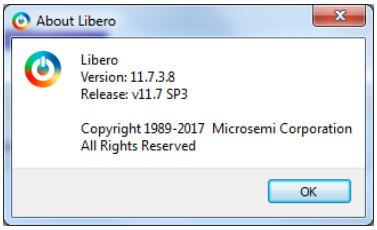
To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

1.1 Update to Libero SoC v11.7 SP3

The Libero SoC v11.7 SP3 software was updated to fix an issue with System Builder.

If you downloaded Libero SoC v11.7 SP3 between 1/18/2017 and 1/27/2017, you may be affected by this issue. To find out whether you're affected, click Help -> About Libero. A version number of "11.7.3.7" indicates that your install is susceptible to the System Builder issue, and needs to be updated.

An updated version of Libero SoC v11.7 SP3 is now available (download links in Section 1.4 below), and addresses the issue. You can install it on top of your existing installation of Libero SoC v11.7 SP3, or, if you have not yet installed Libero SoC v11.7 SP3, you can install it over any previous 11.7 version. After installation, click Help -> About Libero; the version number should be "11.7.3.8" (screenshot below).



Details of the System Builder issue, for reference, are as follows: When creating new System Builder instances in Libero SoC v11.7 SP3 for some SmartFusion2/IGLOO2 die/package combinations, System Builder failed to open, displaying error messages of the form "IO connection not supported for MM_UART_0:RXD" or "IO connection not supported for MSS_SPI_1:CLK". This issue affected the following die-package combinations:

SmartFusion/IGLOO2 dies affected (including S/T/TS variants)	Packages affected for die
M2S/M2GL005	144 TQ 256 VF 400 VF 484 FBGA
M2S/M2GL010	144 TQ 256 VF
M2S/M2GL025	256 VF 325 FCSBGA
M2S/M2GL050	325 FCSBGA
M2S/M2GL060	325 FCSBGA
M2S/M2GL090	325 FCSBGA

1.2 Product/Process Change Notification PCN 17005

PCN 17005, which relates to SmartFusion2 and IGLOO2 devices and Libero 11.7 SP3, is briefly described in the following sections.

1.2.1 PCNs Pertaining to Libero SoC v11.7 SP3

Libero 11.7 SP3 contains software updates and fixes that address the following issues listed in the PCN.

PCN 17005.1: Registers in the SYSREG Block

Application traffic across the FIC_0 interface could cause certain bits in the SYSREG block to change state if these bits are changed from their default power-up values during runtime. Libero SoC v11.7 SP3 introduces a new MSS configurator to address this issue. The MSS configurator now allows you to specify values for all affected SYSREG bits. After the values are specified, these bits are stored in the non-volatile flash component of the FPGA and can no longer be affected by application traffic.

To modify any of the affected SYSREG bits at runtime:

1. Open the project in Libero SoC 11.7 SP3.
2. Update the MSS core version to 1.1.500. To do this:
    a. If you are using System Builder:
        i. Open your System Builder instance (e.g. double-click on it in SmartDesign)
        ii. If you have internet access, System Builder will automatically download the updated cores
        iii. In the System Builder wizard, click “Next” on each page
        iv. Click “Generate” on the last page
    b. If you are not using System Builder:
        i. Download the latest MSS core version (v.1.1.500).

ii. In Design Hierarchy, right-click the **MSS** IP, select **Replace Component Version**, and choose **1.1.500** from the **Change to Version** list.

c. Save and regenerate the SmartDesign instance containing the MSS or System Builder

3. Rerun the entire Libero SoC design flow:
   a. Use incremental layout to minimize impact on already timed designs.
   b. Verify the timing reports.
4. Reprogram the device.

PCN 17005.2: Timing Model Adjustments for SmartFusion2 and IGLOO2 Devices

Libero SoC v 11.7 SP3 includes adjustments to the timing model for SmartFusion2 and IGLOO2 devices. The following components have changes to the timing model, such as arcs added or removed, delay values specified for existing arcs, or updates made to the algorithms for hold time calculations:

- SerDes to fabric nets
- FDDR/MDDR to fabric nets
- MSS to fabric nets
- User I/O to fabric nets
- CCC divider circuitry
- Fabric to MSS interrupts and embedded trace macrocell

If your 11.7 SP2 or earlier design uses any of the affected components, you must

- Open the design in Libero SoC v11.7 SP3, and rerun Verify Timing.
- For any timing violations:
  - Rerun Timing-Driven Place and Route (TDPR), or
  - Make RTL changes and rerun synthesis and optimize for speed.

PCN 17005.3: PLL Lock Window Default Settings

If internal RC oscillators are used as the PLL reference clock in a SmartFusion2 or IGLOO2 device and the PLL fails to lock, the Lock Window setting values need to be increased. Steps to modify Lock Window Settings are as follows

1 Open the CCC Configurator and go to the PLL Options tab (CCC Configurator > PLL > Lock Window).
2 For the 25/50 MHz RC oscillator as the PLL Reference Clock, set the Lock Window to 16,000 or 32,000 ppm, depending on the PLL configuration.
3 For the 1 MHz RC oscillator as the PLL Reference Clock, set the Lock Window to 64,000 ppm.
4 Check that the new Lock Window setting does not trigger any warning messages in the CCC Configurator.
5 Regenerate the CCC.

1.3 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

Note: A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

For Linux OS setup instructions, see the Libero SoC Documents web page.

1.3.1 Operating System Support

Supported

- Windows 7, Windows 8.1
- RHEL 5* and RHEL 6, CentOS 5*, and CentOS 6
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: *RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating system.
- Windows XP.
- Support ceasing in the first half of 2017:
  - Solaris Flexlm license daemon support; Libero SoC is not supported on Solaris.
  - Libero SoC software support for RedHat Enterprise Linux 5 and CentOS 5.

1.4 Downloading Libero SoC v11.7 SP3

The Libero SoC v11.7 SP3 service pack can be installed directly on top of any one of the following:

- Libero SoC v11.7 production release
- Libero SoC v11.7 SP1
- Libero SoC v11.7 SP1.1
- Libero SoC v11.7 SP2

Note: Installation requires administrator privileges to the system.

Click the following links to download Libero SoC v11.7 SP3 on Windows and Linux operating systems:

- Windows Download
- Linux Download

1.5 Downloading SoftConsole 3.4/4.0

The Libero SoC v11.7 SP3 is compatible with SoftConsole v3.4 SP1 and SoftConsole v4.0. The following links contain the download packages, and explain the steps for downloading SoftConsole on different operating systems:

- Download SoftConsole v4.0 for Windows
- Download SoftConsole v4.0 for Linux
- Download SoftConsole v3.4 SP1 for Windows

1.6 Silicon Feature Support

Libero SoC 11.7 SP3 introduces support for the following die/package combination for RTG4.

Family	Die	Pin/Package	Speed Grade	Core Voltage	Temperature
RTG4	RT4G150	352-CQFP	STD	1.2 V	MIL

Note: For 352-CQFP, programming is not enabled, timing numbers are in advance, and package power and design-specific IBIS and BSDL model details are not yet available.

1.7 Software Enhancements

The software enhancements described in this section apply to SmartFusion2, IGLOO2, and RTG4 devices, unless otherwise noted.

1.7.1 RTG4 LSRAM Configurators Enhancement

If you generated a large SRAM (LSRAM) configuration with depth-wise cascading (address space fracturing) and a dynamic REN signal in Libero SoC v11.7 SP2 or a prior release, when the read-address jumps from one RAM block to another while the REN is de-asserted, the multiplexed output is not held to the previous block. The RTG4 Two-port LSRAM Configurator in Libero SoC v11.7 SP3 has been changed to not use the REN pin when the configuration requires multiple blocks depth-wise. The REN pin is used if the configuration has multiple blocks width-wise, and the read-data does not become zero when de-asserted.

The RTG4 Dual-port Configurator disables the PortA/B Read Enable signal (A/B_REN), when the depth×width configuration or optimization selection causes depth-wise cascading (address space fracturing). In Libero SoC v11.7 SP3, the A/B_REN signal cannot be enabled. This eliminates possibility of read error at the Port A/B read registers even if the A/B_REN signal is enabled and then de-asserted.

For more information, see the RTG4 Dual-Port LSRAM Configurator User Guide.

1.7.2 RTG4 CCC Divider Timing Model Change

When the divider in the CCC block is used, the algorithm used to calculate external hold time has been updated to ensure that max delay is utilized along the entire clock path from the input pin to the clock input of a flip flop. Both Y and GL outputs are impacted.

1.7.3 SmartFusion2 and IGLOO2 – Macro Library Guide Updated to Include Back Annotated Macros

The Macro Library Guide is updated with descriptions for the following macros: `GB, GBM, RGB, CFG2, CFG3, CFG4, ARI1_CC, CC_CONFIG, DDR_OE_UNIT,IOIN_IB, IOPAD_IN, IOPAD_TRI, IOINFF, IOOEFF`.

1.8 Resolved Issues

The issues listed in the following table are resolved in Libero SoC v11.7 SP3.

Customer Case Number	Description
493642-2187467664	Fixed the algorithm for post-divided frequency comparison when PLL is in spread spectrum modulation mode.
493642-2134957879	Constraint coverage report shows a lot of unconstrained paths for "CLK_CONFIG_APB".
493642-2176028198	FDDR_LOCK does not become active under certain frequency/divider settings.
493642-1971787847	Add Su/Hd arcs for the MSS Interrupt signals.
493642-2096643137, 493642-2128727254	Some back-annotated macros are not documented.
	G4: MSS: TIMER SOFTRESET default setting change to "Active".

1.9 Known Limitations, Issues, and Workarounds

Known issues in the Libero SoC v11.7 SP2 also apply to the Libero SoC v11.7 SP3, unless mentioned in the preceding Resolved Issues list. For known issues in Libero v11.7SP2, see the Libero SoC v11.7 SP2 Release Notes.

1.9.1 RTG4 – SpaceWire Channels may Result in Hold Violations

When two SpaceWire channels run at 200 MHz (400 Mbps) for -1 speed-grade with SET Mitigation turned off, hold time violations may occur under the worst case conditions.

Clock	Index	Type	Corner	Circuitry	Type	Package Pin
1	5	D	NE1	0	MSIOD	SPWR_NE1_0_RX_DATA_P, SPWR_NE1_0_RX_DATA_N
3	3	D	SE1	1	MSIO	SPWR_SE1_1_RX_DATA_P, SPWR_SE1_1_RX_DATA_N

1.9.2 RTG4 - Single Event Transient (SET) Mitigation ON may Result in Hold Violations

Turning SET Mitigation ON may result in hold time violations in some register to MATH block paths. Enable **Repair Minimum Delay Violations** in Place and Route options to have the Place and Route tool mitigate hold time violations.

1.9.3 RTG4 - Single Event Transient (SET) Mitigation Option Change Does Not Revert Design to Pre-Compile/Pre-Synthesis State

Changing the SET Mitigation option (from OFF to ON or vice versa) does not revert the design to the pre-Compile (for Classic Constraint Flow) or pre-Synthesis (for Enhanced Constraint Flow) state. Rerun Compile or Synthesis and continue with the design flow.

1.9.4 RTG4 - SmartDebug: Device Resets During JTAG Operations with SmartDebug

After performing one or more JTAG operations, if a user closes and reopens the SmartDebug tool (either standalone or within the Libero SoC software), the device resets itself.

Workaround:

The device reset problem can be avoided by using the FlashPro5 programmer and setting a value of **1** on the def variable **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET.**

- For standalone SmartDebug:
  - When invoking the tool from the command line, add the following argument:

    Console >

    ./sdebug.exe **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET**:1
  - When invoking the tool from the GUI, edit the sdebug.def file and change the value of def variable to '1' in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
- For SmartDebug invoked from Libero SoC:
  - Edit the sdbg.def file and change the value of def variable to "1" in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE

- Add the following line in the libero.def file:

  data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 1 OVERRIDE

- For Tcl script-driven batch mode operation, add the following def variable and the value in a Tcl script:

  defvar_set -name **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET** -value 1

Note: When the def variable is set to 1, the LiveProbe set in the previous SmartDebug session is not retained when a subsequent SmartDebug session is invoked.

1.9.5 RTG4 - Custom Flow with uPROM: uPROM Content must be a Single Line File

If you use the custom flow and import the uPROM content using the import_component_data command, the uPROM memory file must not have any newlines.

1.9.6 SmartFusion2, IGLOO2 and RTG4 – Slack mismatch in SmartTime - Path list vs. Expanded paths

In the SmartTime UI, there is a discrepancy between the slack value reported in the path-list (summary) vs. the path-details (expanded). This will only occur for design involving a generated clock constraint in conjunction with another constraint on an output, related to the generated clock domain (e.g. an output delay constraint).

Path-details has the correct slack value. The slack in the path-list is more conservative than the correct slack. The domain browser (on the left of the SmartTime screen) shows status for timing (met or not) with a green check- mark or a red X-mark, based on the slack value from the path-list. This means that this issue could cause false violations to be reported in the domain browser.

However, true violations will always be flagged in both path-list and path-details. Timing reports (summary and expanded paths) are not affected by this issue.

1.9.7 SmartFusion2, IGLOO2 and RTG4 – Place and Route Tool does not Support get_nets or get_clocks SDC Commands

The placer does not support the get_nets and get_clocks object access commands when used with SDC timing constraints. To ensure that the SDC timing constraints are honored by the placer tool, do not use get_nets or get_clocks commands in the SDC timing constraints.

Workaround: Use the get_pins command instead.

Example:

The following constraint uses the get_nets command:

```
create_generated_clock -name {sys_clk} -divide_by 1 -source [ get_ports { CLK_40M } ] -
phase 0 [ get_nets { u_PLL/my_pll_0/GL0_net } ]
```

Rewrite the constraint to use the get_pins command instead:

```
create_generated_clock -name {sys_clk} -divide_by 1 -source [ get_ports { CLK_40M } ] -
phase 0 [ get_pins { u_PLL/my_pll_0/CCC_INST/GL0 } ]
```

1.9.8 SmartFusion2/IGLOO2/RTG4 - Chip Planner Displays Some Unplaced Macros after Layout in Enhanced Constraint Flow

This is a Chip Planner display issue. It can be ignored if layout is successful.

- If the **Repair Minimum Delay Violations** option is enabled in layout options and the layout tool adds buffers to do the repair, opening Chip Planner after layout may display the added buffers as unplaced macros.
- If nets on Row Globals or local asynchronous resets for RTG4 are constrained to a user-created exclusive region in Chip Planner before layout is run, re-opening Chip Planner may display the macros connected to those constrained nets as unplaced macros even though the layout process has successfully completed.

1.9.9 SmartFusion2, IGLOO2, and RTG4 - Enhanced Constraint Flow Limitations

The following tools and flows are not supported in the Enhanced Constraint Flow in the Libero SoC v11.7 SP3 release:

- Precision synthesis
- I/O Advisor
- Netlist Viewer
- Block flow
- Design Separation Flow using MSVT

1.9.10 Extra Pop-Up Messages from SynplifyPro

When SynplifyPro synthesis is invoked interactively, it displays a pop-up message about the completion of Tcl script file execution, if any one of the following is true prior to the interactive invocation of SynplifyPro, ignore the messages and click OK to continue with the SynplifyPro synthesis

- Additional user-specified synthesis options are configured in a Tcl script and passed by Libero to SynplifyPro.
- The Synthesis Option is entered in the Configure Synthesis Option dialog box as a command line entry and passed to SynplifyPro.

1.9.11 Programming – Programming Recovery not Working after Programming Interruption

Exporting a SPI bitstream with programming recovery enabled with another programming file type (STAPL, DAT) erases and reprograms the programming recovery setting. If a programming interruption occurs before the programming recovery setting is reprogrammed with the following programming methods (Auto Update, Auto Programming, or IAP/ISP services), programming recovery does not occur.

To work around this issue, export SPI bitstream only without any other programming file type. This will be resolved in Libero SoC v11.8.

1.9.12 Programming - Libero Crashes when Exporting FlashPro Express Job for UEK1 or UEK2 with eNVM

Libero SoC crashes when the Export FlashPro Express Job tool is invoked to generate a programming job encrypted using UEK1/UEK2 where eNVM is the only selected component.

Workaround: Select both fabric and eNVM components for exporting the programming job encrypted using UEK1 or UEK2.

1.9.13 Programming - SPPS Flow: export_hsmtask fails when set_security_overwrite is Followed by set_envm_update

If the user Tcl script has the security overwrite command followed by the eNVM update command, the export of the HSM job fails. In other words, if set_security_overwrite is followed by set_envm_update, the export_hsmtask fails.

Workaround:

If both the security overwrite command and the eNVM update command are required, make sure that the eNVM update command is executed prior to the security overwrite command. Put the set_envm_update Tcl command before the set_security_overwrite Tcl command in the Tcl script.

1.9.14 Programming - No Programming Support for Virtual Machines

Programming is supported for physical machines only and not supported on any virtual machine (VM).

1.9.15 Programming - Inspect Device Feature Disabled in FlashPro

The Inspect Device feature is disabled in FlashPro for SmartFusion2/IGLOO2 devices beginning with the Libero SoC v11.7 release. Use standalone SmartDebug instead.

1.9.16 Programming - SmartFusion Encrypted STP File Generation

Generating the encrypted STP files for SmartFusion takes 50 times longer than generating the non-encrypted plain STP.

1.9.17 SoftConsole - Restricts ARM® Cortex®-M3 Debug with Debug Pass Key

SoftConsole does not support this feature.

1.9.18 Documentation - Web-based Documentation

Starting with the Libero SoC v11.7 release, most users guides for SmartFusion2, IGLOO2, and RTG4 are available on the Microsemi website. Libero SoC and Programming/Debug tools include links to the website.

If the machine on which the Libero SoC software is installed does not have access to the internet, you (or a site administrator) can download all the Libero SoC v11.7 user guides from the Libero SoC documentation site.

1.9.19 Documents on Linux: Firefox Requirement for Online Help and User Guides

Libero SoC v11.7 SP3 requires the “Firefox” executable to be in your PATH variable on Linux. Alternatively, you can access the reference manuals on the Microsemi website, or by clicking **Help > Reference Manuals** in Libero. For the Libero SoC v11.7 SP3 release, the “Web Browser” selection in the Libero Preferences dialog box is only used by online help and for some user guide links.

1.9.20 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield wizard displays a pop-up message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

1.9.21 Antivirus Software Interaction

Many antivirus and host-based intrusion prevention system (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security settings by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

1.9.22 Installation Issue on Linux

After installation of Libero SoC on Linux, the attempt to run the udev_install script for FlashPro setup fails with the following message:

```
% ./udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:

The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, hence, is not a valid shell script.

Workaround:

Run the `dos2unix` command on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
%. /udev_install
```

If the `dos2unix` command is not available, install the command first, and then run `dos2unix`, and `udev_install`:

```
% sudo yum install dos2unix
% dos2unix udev_install
%. /udev_install
```