UG0741
User Guide
RTG4 FPGA I/O

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.0

The following is a summary of the changes made in this revision.

- Information about SSTL Termination, page 12 was added.
- Information about Schmitt receiver was updated. See Table 5, page 14.
- Information about Pre-Emphasis, page 15 was updated.
- Information about Programmable Schmitt-Trigger Input and Receiver, page 17 was updated.
- Information about Failsafe Mode for Differential Receivers, page 36 was updated.
- Information about Failsafe LVDS using Dynamic ODT, page 37 was added.
- Information about Calibrating ODT/Driver Impedance Using Fixed Calibration Codes, page 20 was updated.

1.2 Revision 6.0

The following is a summary of the changes made in this revision.

- Added the ODT behavior during power-down, POR (DEVRST), and user-reset scenarios in On-Die Termination, page 6.
- Updated the I/O Banks, page 7 section to include information about the CQ352 package.
- Added Figure 4, page 8 to show the I/O Bank locations on the CQ352 package.
- Added I/O Bank details of CQ532 package in Table 1, page 9.
- Updated Table 2, page 9 to show that:
  - HSTL18I standard is supported for MSIO, MSIOD and DDRIO Banks.
  - HSTL1 standard is supported for MSIO and MSIOD Banks.
- LVCMOS25 does not support programmable slew rate, updated the Programmable Slew Rate Control, page 16 section accordingly.
- Added a footnote in Table 5, page 14 directing the user to see page 148 of the Libero Design Constraints User Guide for more information about I/O types and Banks that supports ODT.
- Added the I/O Register Combining, page 35 section.
- Added information about the support for failsafe mode, see Failsafe Mode for Differential Receivers, page 36.
- Added DEVRST_N behavior during POR, see Device Reset I/Os, page 28.

1.3 Revision 5.0

The following is a summary of changes made in this revision.

- Added the guidelines for making MSIOD complaint with LVCMOS 3.3V, see 5 V-Input Tolerance and Output Driving Compatibility (only MSIO), page 24.
- Added information about ODT timing during power-up and power-down, see On-Die Termination, page 6.

1.4 Revision 4.0

The following is a summary of changes made in this revision.

- Information about programmable output drive strength was updated. See Table 8, page 17.
- Information about SSTL18 I/O standard was updated. See Table 2, page 9.

1.5 Revision 3.0

Added the Status of the V_{REF} Pin Assigned Rule for IOA table (see Table 4, page 11).

1.6 Revision 2.0

The following is a summary of changes made in this revision.

- Added more information about bi-directional buffers in the Radiation Hardening section. For more information, see Radiation Hardening, page 7.
- Added information about pre-emphasis. For more information, see Pre-Emphasis, page 15.
- Added a new table for ODT I/O standards that support ODT ON. For more information, see Table 13, page 22.
- Re-arranged the I/O bank positions as required. For more information, see Figure 3, page 8.
- Added notes for HCSL, Mini LVDS, Bus LVDS, and MLVDS. For more information, see Table 2, page 9.
- Restructured the content as required and updated the diagram. For more information, see 5 V-Input Tolerance and Output Driving Compatibility (only MSIO), page 24.

1.7 Revision 1.0

The first publication of this document.

2 I/O Overview

RTG4™ FPGAs have several types of I/Os such as MSIO, MSIOD, double-data-rate I/O (DDRIO), and dedicated I/Os for various functions. For more information about I/O naming conventions and I/O descriptions, see *DS0130: RTG4 FPGA Pin Descriptions*.

MSIO, MSIOD, and DDRIO provide programmable I/O features such as drive strength, slew rate, input delay, weak pull-up, and weak pull-down for several voltages. The programmable I/O features are explained in detail in the *I/O Programmable Features,* page 14.

DDRIO is an MSIO optimized for LPDDR/DDR2/DDR3 performance. In RTG4 devices, a DDR subsystem is used to control an external DDR memory called FDDR. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. For more information about DDR subsystem, see *UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide*.

MSIO, MSIOD, and DDRIO can be configured as fabric I/Os, whereas dedicated I/Os can be used for a single purpose such as serializer/deserializer (SerDes), device reset, or for clock functions. Dedicated I/Os cannot be used by any other circuits.

Using the Libero® SoC, MSIO, MSIOD, and DDRIO are automatically configured at power-up by fabric-related flash bits, which initialize the register blocks.

2.1 Functional Description

RTG4 I/Os are classified into the following three categories depending on their functional usage:

- MSIO, MSIOD, and DDRIO
- JTAG I/O
- Dedicated I/Os

2.1.1 MSIO, MSIOD, and DDRIO

DDRIOs are shared between the fabric logic and FDDR. When the FDDR controller is used, Libero SoC automatically assigns and configures the FDDR controller signals to the respective DDRIOs. The SPIO_SEL signal (as shown in the following figure) determines whether the fabric logic or the FDDR peripheral must be connected to the corresponding I/Os. The I/Os are set automatically selected by Libero SoC during programming. When the FDDR controller is not used, the respective DDRIOs are available to the fabric logic as shown in the following figure.

MSIO and MSIOD are directly connected to the fabric logic. For the fabric logic, each I/O port of the design must be individually assigned to I/Os in the Libero SoC.

Figure 1 • **I/O Interconnection**

The following figure shows the top-level view of I/O interconnections between the fabric logic and FDDR.
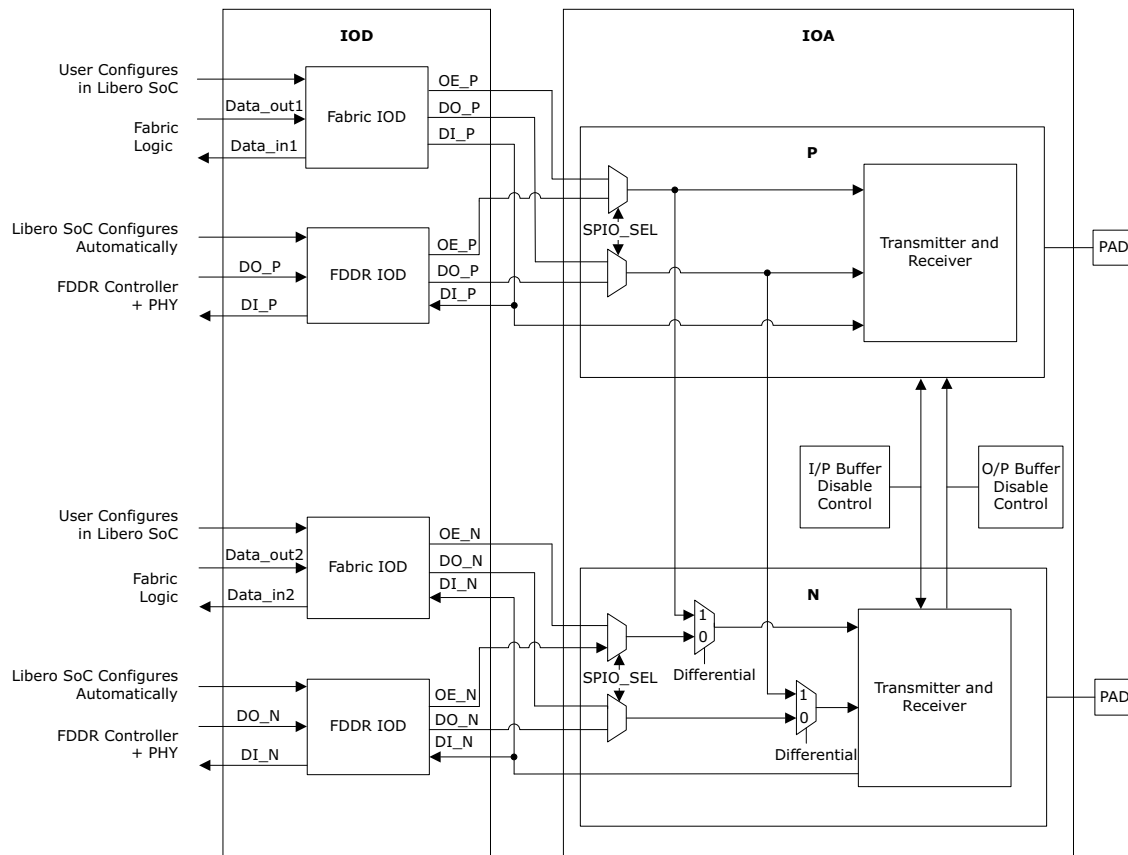
Each I/O has a highly-featured bi-directional I/O buffer. The I/O has the following two main parts, as shown in Figure 1, page 4:

- Digital IO (IOD) (includes fabric and FDDR)
- Analog IO (IOA)

IOD generates output enable (OE), data out (DO), and data in (DIN) signals for both P and N. For more information about IOD, see *UG0574: RTG4 FPGA Fabric User Guide*.

Each pair of P and N cells in an IOA block forms a differential pair as shown in Figure 2, page 6. Each differential pair supports differential and pseudo-differential modes of operations. It is composed of a true and complement IOA. The true IOA is called P, with positive polarity relative to the DO/DIN data signals of the P cell. The complement IOA is called N, with negative polarity relative to the DO/DIN data signals of the N cell.

IOA blocks form a ring around the periphery of the device, excluding the SerDes channel edge. The top and bottom edges of the IOA device order start with P on the left and N on the right. The left and right edges use N on the top and P on the bottom. There is one IOD for each pair of IOAs.

To support a variety of differential standards, RTG4 devices use a pair of regular P and N I/O cells. The P and N I/O cells of MSIO, MSIOD, and DDRIO can be configured as separate single-ended I/Os or as one differential I/O pair. In differential output mode, the output data signal is driven out on both the P and N cells as a differential pair, where the true signal is on the P pad and the complement signal is on the N pad.

The P and N output signals are complementary as required by the DDR1, DDR2, and DDR3 standards for CK and DQS signals. The P and N cells have to be laid out next to each other, as a pair, in order to minimize the skew rate between the two output signals of the differential pair.

The IOA part has transmitter and receiver buffers for the P and N pair. The main circuits in the IOA are transmit and receive buffers (shown in the following figure), which support various I/O standards and contain the following modules:

- Transmit buffer
- Receive buffer
- Input programming delay
- On-die termination (ODT)

2.1.2   Transmit Buffer

Transmit and receive buffers transfer signals between the FPGA fabric and the IOA and also transfer signals between FDDR and the IOA.

The OE_P and OE_N pins control the direction of I/O buffers, as shown in the following figure. When an I/O is operated as a single-ended I/O, the OE_P and OE_N pins individually control the P and N I/O buffers. When an I/O is operated as a differential I/O, OE_P controls both the P and N I/O buffers.

Depending on the current status of an output buffer, the dynamic OE enables or disables the buffer for all the standards.

2.1.3   Receive Buffer

Enabling and disabling of the input buffer are controlled automatically by Libero SoC.

The I/O receiver can operate in four different modes, as shown in the following figure. These modes are selected based on the flash configuration bits, which are configured during programming or after power-on. The four modes of the receiver are:

- True differential
- Pseudo-differential
- Single-ended
- Schmitt trigger

In true differential mode, the P and N pad inputs are fed to the comparator, whereas in pseudo-differential mode, each pad's input is compared to an external reference voltage. The following figure shows the detailed IOA structure of an I/O.

The I/O input can be configured as a Schmitt trigger receiver or a single-ended receiver. When Schmitt trigger inputs are selected, the input buffers present hysteresis, which filters the noise at the receiver and prevents double glitching caused by noisy input edges.

2.1.4   Input Programming Delay

Input delays can be used to improve the hold time of the input register by increasing input pin to input register delay. For more information about input programming delay, see I/O Programmable Features, page 14.

2.1.5 On-Die Termination

ODT improves the signaling environment by reducing the electrical discontinuities introduced with off-die termination; thus, it enables reliable operation at higher signaling rates.

The following points summarize the ODT behavior during power-down, POR (DEVRST), and user-reset scenarios:

- During power-up, ODT activation is same as inbuf timing.
- During power-down, the ODT behavior is determined by the brown-out condition. RTG4 devices do not support brown-out detection and brown-out detection varies die to die. The
- brown-out point is mentioned in AC439. Once device hits brown-out voltage on VDD, the fabric is not functional and all the I/O configurations driven by PC bits are lost. Hence, any ODT set using PC bits will not be available at that time.
- If the RTG4 device is held in reset using DEVRST, I/Os are tristated and hence ODT is not available.
- During user reset there is no impact on ODT because user reset is only for registers and not for I/O configurations.

For more information about the programmed ODT values for DDRIO, MSIO, and MSIOD, see the I/O Programmable Features, page 14.

Figure 2 • **IOA Architecture**
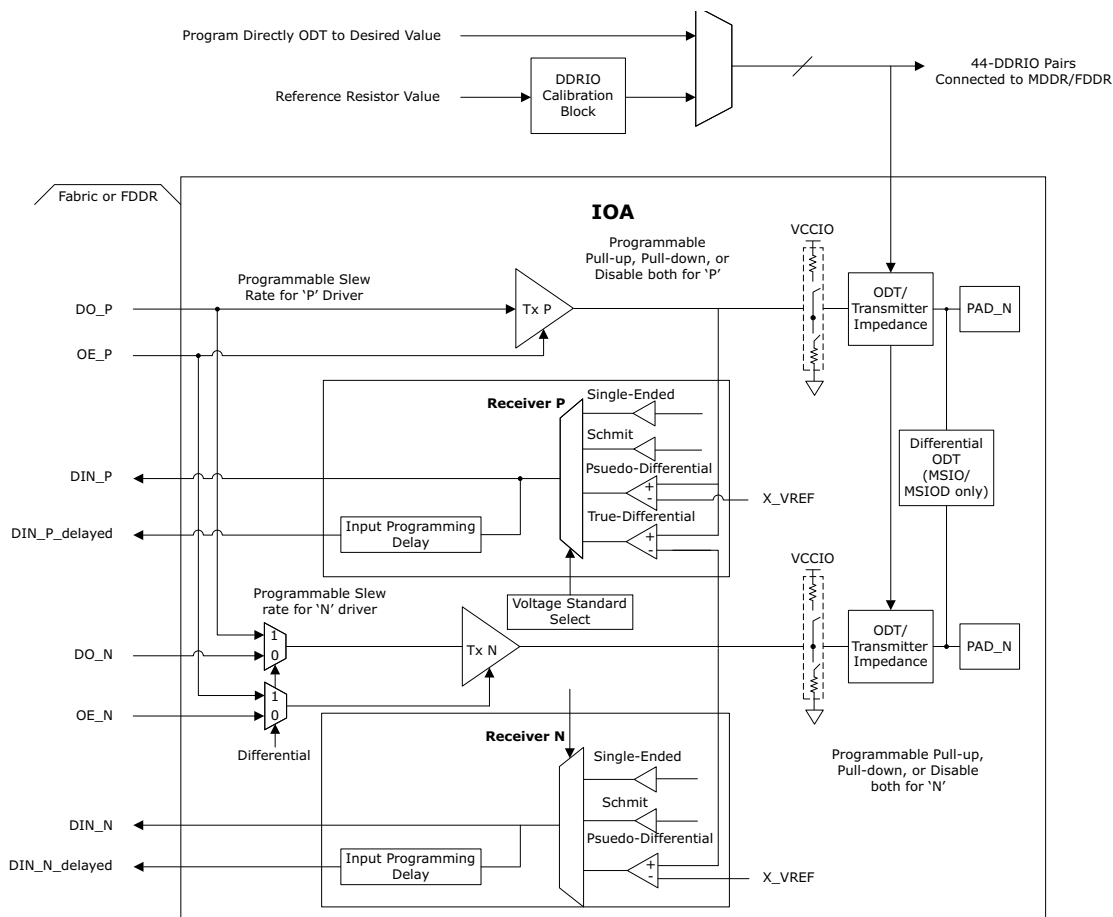
Note: The DIN_P and DIN_N pins provide the DIN_P_delayed and DIN_N_delayed input signals. The input programmable delay is provided using the I/O Constraints Editor in Libero SoC.

During the power-up cycle, ODT activation occurs at the time of activation input buffers. During the power-down cycle, the time of ODT deactivation is determined by the brown-out condition. The time at which ODT is deactivated varies from die to die because brown-out detection is absent in RTG4. The brown-out point is mentioned in *AC439: Board Design Guidelines for RTG4 FPGAs Application Note*.

Once the device hits the brown-out voltage on VDD, the fabric is not functional and the I/O configuration driven by flash bits is not available including ODT.

If the device is held in reset using DEVRST_N, IOs are tristated. As a result, ODT is not available. A design reset has no impact on ODT because design reset is for registers and not for the I/O configuration.

2.2 Radiation Hardening

Radiation hardening is the act of making systems resistant to damage or malfunctioning caused by ionization radiation such as particle radiation and high-energy electromagnetic radiation, which are encountered in space, high-altitude flights, and so on. The term *hardened*, in context of FPGAs, refers to radiation hardened.

RTG4 devices have hardened input buffers for receiving clock inputs or other critical signals. There are 24 primary clock inputs on an RTG4 device. Hardening is available only on MSIO and MSIOD receivers. The DDRIO receivers are not hardened, meaning they are susceptible to radiation.

Each hardened receiver uses the triple modular redundancy (TMR) logic, that is, each receiver block is composed of three receivers with wired or connection at the output. Each hardened receiver in MSIO and MSIOD supports the following modes of operations:

- Single-ended ratio receiver mode (LVTTL/LVCMOS) that can be programmed ON or OFF
- Reference receiver mode (SSTL/HSTL)
- Differential input mode (LVDS/RSDS)

In RTG4 devices, hardening is used only when an I/O is configured as a receiver. Therefore, when an I/O is configured as bi-directional, it is not hardened. Bi-directional buffers contain both outbuf and inbuf. Only inbuf is hardened, but not outbuf. As Bidirectional Buffer (BIBUF) contains both, on the whole it is not considered as hardened.The hardened input has a programmable on-die termination and programmable weak pull-up/pull-down (ON/OFF) per pad.

2.2.1 Built-in Radiation Mitigation for RTG4 I/Os

In RTG4 FPGAs, SEL mitigation is done by design in all components of the device, including I/Os. SET mitigation is built in for all MSIO and MSIOD input buffers except the input buffer of bi-directional I/Os.

- Mitigation on inputs is done by the TMR logic where three input buffers are processed in parallel. The buffer TMR is built in and made transparent when the I/O is configured as an input.
- Clock and global signals have a dedicated radiation mitigated route on the device to the global clock routing and/or CCC blocks. If the global clock routing and/or CCC blocks are not used for these hardened clock or global signals, their inputs can be routed to the fabric like any other I/Os. For non-clock and non-global inputs, the routing on-chip is not radiation hardened and thus they must use SET mitigated flip-flops in the fabric or I/O input flip-flops for any cones of logic from those inputs. Mitigation is only done on MSIO and MSIOD input buffers because of performance-power trade-off.

DDRIO requires high performance and uses twice as many buffers so the DDR input buffers are not triplicated. SEL and SET mitigations are built in for the 24 global clocks/resets as driven by MSIO or MSIOD input buffers. SET mitigation is done by triplicating global buffers and global clock tree, including any connections to/from the CCC blocks found in the corners of the device. SEU and SET mitigations are built-in for all I/O registers because they are the same as the fabric registers.

2.3 I/O Banks

I/Os are grouped into banks on the basis of I/O voltage standards. Each I/O bank has a dedicated I/O supply and ground voltages and uses standards compatible with the voltage supplied to the bank. There are 10 I/O banks as shown in the following figure. Every I/O bank has input and output buffers to support a wide range of standards, which require different VDD and reference voltages (V_{REF}) for voltage-referenced standards. These voltages are externally supplied and are connected to device pins, which serve the I/O banks.

This section provides I/O Bank details of the RT4G150 device for the CG1657 and CQ352 packages.

- The CG1657 package includes 10 banks— three MSIO banks, four MSIOD banks, two DDRIO banks, and one JTAG bank.

- The CQ352 package includes four banks—three MSIO banks and one JTAG bank.

Figure 3 and Figure 4 show I/O Bank locations and number of I/Os in CG1657 and CQ352 packages. For more information about RTG4 FPGA pin descriptions, supply pins, unused conditions, and packaging details, see the *DS0130: RTG4 FPGA Pin Descriptions*.

Figure 3 • **RT4G-CG1657 I/O Bank Locations**
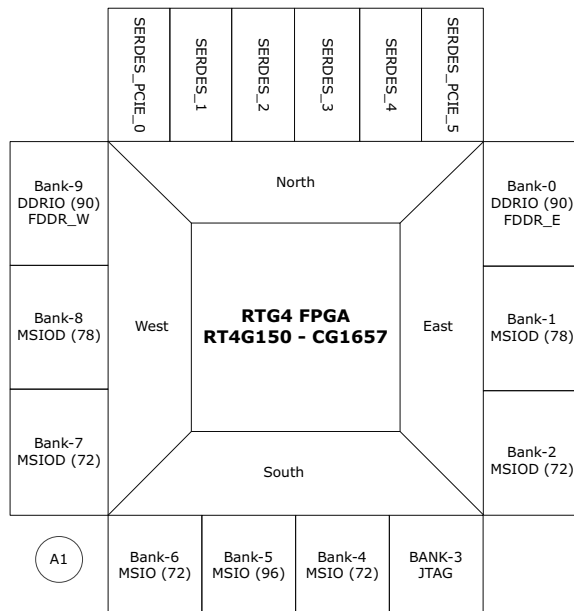
Figure 4 • **RT4G-CQ352 I/O Bank Locations**
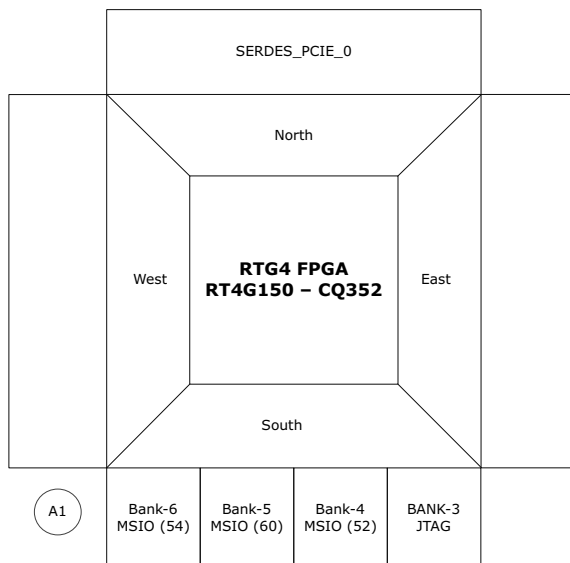
MSIOs are divided into banks, each of which may be configured to support one of the standards listed in Table 2, page 9. RTG4-CQ352 package does not include MSIOD or DDRIO pins.

The following table shows the organization of I/O banks in the RTG4 devices.

Table 1 • **RTG4 Device I/O Banks**

CG1657 Package		CQ352 Package	
I/O Bank	**Function**	**I/O Bank**	**Function**
Bank 0	DDRIO for FDDR or fabric	Bank 3	MSIO for JTAG
Bank 1	MSIOD for fabric	Bank 4	MSIO for fabric
Bank 2	MSIOD for fabric	Bank 5	MSIO for fabric
Bank 3	MSIO for JTAG	Bank 6	MSIO for fabric
Bank 4	MSIO for fabric	-	-
Bank 5	MSIO for fabric	-	-
Bank 6	MSIO for fabric	-	-
Bank 7	MSIOD for fabric	-	-
Bank 8	MSIOD for fabric	-	-
Bank 9	DDRIO for FDDR or fabric	-	-

2.4 Supported I/O Standards

The following table shows the supported voltage standards for various I/O types.

Table 2 • **Supported Voltage Standards**

I/O Standard	Single-Ended	Differential	MSIO (Max 3.3 V)	MSIOD (Max 2.5 V)	DDRIO (Max 2.5 V)
LVTTL	Yes		Yes		
PCI	Yes		Yes		
LVPECL (input only)		Yes	Yes		
LVCMOS33	Yes		Yes		
LVCMOS25	Yes		Yes	Yes	Yes
LVCMOS18	Yes		Yes	Yes	Yes
LVCMOS15	Yes		Yes	Yes	Yes
LVCMOS12	Yes		Yes	Yes	Yes
SSTL2I	Yes	Yes	Yes	Yes	Yes (DDR1)
SSTL2II	Yes	Yes	Yes		Yes (DDR1)
SSTL18I	Yes	Yes	Yes	Yes	Yes (DDR2)
SSTL18II	Yes	Yes	Yes	Yes	Yes (DDR2)
SSTL15I (only for I/Os used by MDDR/FDDR)	Yes	Yes			Yes (DDR3)
SSTL15II (only for I/Os used by MDDR/FDDR)	Yes	Yes			Yes (DDR3)
LPDDRI	Yes	Yes			Yes
LPDDRII	Yes	Yes			Yes
HSTLI	Yes	Yes	Yes	Yes	Yes

Table 2 • **Supported Voltage Standards** *(continued)*

I/O Standard	Single-Ended	Differential	MSIO (Max 3.3 V)	MSIOD (Max 2.5 V)	DDRIO (Max 2.5 V)
HSTLII	Yes	Yes			Yes
HSTL18I	Yes	Yes	Yes	Yes	Yes
LVDS25 [1]		Yes	Yes	Yes	
LVDS33 [2]			Yes		
HCSL [1]		Yes	Yes	Yes	
RSDS [1]		Yes	Yes	Yes	
MINILVDS [1]		Yes	Yes	Yes	
BUSLVDS		Yes	Yes	Yes (Only Input)	
MLVDS		Yes	Yes	Yes (Only Input)	

1. When VICM > 1.5 V, an external differential termination of 100 Ω (typical) or 200 Ω (typical) is required to meet the minimum input differential voltage specification of 200 mV. A 200 Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100 Ω on-die termination (ODT). For example, a 2.5 mA current produces 500 mV of differential voltage across the 200 Ω termination, whereas it produces only 250 mV across a 100 Ω termination. When using external termination, ensure ODT is disabled in Libero SoC software.
2. An external differential termination of 200 Ω (typical) is required to meet the minimum input differential voltage specification of 500 mV since the LVDS33 receiver no longer supports ODT. Libero SoC v11.8 SP1 software disables ODT for LVDS33 I/O standards. When a design with ODT-enabled LVDS33 I/Os is first opened in Libero SoC v11.8 SP1 software, the Generate Programming step is invalidated. To continue designing in this software release, disable ODT for all impacted I/O standards. If a design contains ODT-enabled LVDS33 I/Os for high-speed serial interfaces (for example, SERDES REFCLK is ODT-enabled LVDS33 I/O), these configurations with ODT-enabled are no longer supported in this software release. To continue designing in Libero SoC v11.8 SP1 software, regenerate these configurations with ODT disabled.

For more information about I/O pin naming and assignments to specific banks, see the *DS0130: RTG4 FPGA Pin Descriptions*.

2.4.1 Single-Ended Standards

Single-ended I/O standards use a push-pull CMOS output stage with a voltage referenced to the system ground. The input buffer configuration, output drive, and I/O supply voltage (VDDI) vary among I/O standards. The advantage of these standards is that a common ground can be used for multiple I/Os. This simplifies board layout and reduces system cost. The reduced slew rate of these I/O standards minimizes electromagnetic interference (EMI) on the board.

2.4.1.1 Low-Voltage Transceiver Transistor Logic (LVTTL)

This is a general-purpose standard (EIA/JESD8-B) for 3.3 V applications. It uses an LVTTL input buffer and a push-pull output buffer. The LVTTL output buffer can have up to eight different programmable drive strengths.

2.4.1.2 Low Voltage CMOS (LVCMOS)

RTG4 devices provide five different kinds of LVCMOS:

- LVCMOS 3.3 V—an extension of the LVCMOS standard (JESD8-B compliant) used in MSIO for general-purpose 3.3 V applications.
- LVCMOS 2.5 V—an extension of the LVCMOS standard (JESD8-5-compliant) used for general-purpose 2.5 V applications.
- LVCMOS 1.8 V—an extension of the LVCMOS standard (JESD8-7-compliant) used for general-purpose 1.8 V applications.
- LVCMOS 1.5 V—an extension of the LVCMOS standard (JESD8-11-compliant) used for general-purpose 1.5 V applications.
- LVCMOS 1.2 V

The VDDI values for these standards are 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.2 V, respectively. For MSIOs, all the versions use a 3.3 V-tolerant CMOS input buffer and a push-pull output buffer. Similar to LVTTL, the output buffer has up to eight different programmable drive strengths.

2.4.1.3 3.3 V Peripheral Component Interface (PCI)

This standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. With the aid of an external resistor, this I/O standard can be 5 V-compliant.

2.4.2 Voltage-Referenced Standards

I/Os are referenced to an external reference voltage (V_{REF}).

2.4.2.1 Input Reference Voltage

Each I/O bank supports a reference voltage (V_{REF}). For MSIO or MSIOD banks, any I/O in a bank can be configured as the input-reference voltage pin to be used in conjunction with voltage reference input and bi-directional buffers. A V_{REF} pin is a regular MSIO/MSIOD that is configured as a reference voltage input in the design. MSIO/MSIOD allow any pin to be a V_{REF} pin, but DDRIOs have dedicated V_{REF} pins. To support SSTL and HSTL inputs, the reference voltage is typically powered with a voltage of one-half that of the bank's VDDI level.

In general, mixing of a single-ended voltage-referenced I/O with a non-referenced I/O is permitted in MSIO and MSIOD banks. The mixing of signals allows the combinations of LVCMOS, HSTL, and SSTL I/O types as long as they share the same VDDI level. However, I/O type mixing within a bank must follow the placement I/O pair restrictions between the positive differential I/O pin (IOP) and negative differential pin (ION) within an IOA block.

The following table lists the valid and invalid pairs that can be created in IOA block pins.

Table 3 • **IOA Pair Design Rules**

IOP	ION	Valid/Invalid
HSTL/SSTL	Unused	Valid
HSTL/SSTL	HSTL/SSTL	Valid
HSTL/SSTL	LVCMOS/LVTTL/PCI	Invalid

- The rules mentioned in this section apply only to MSIO/MSIOD I/O types.
- The rules apply to all HSTL/SSTL Class I or Class II input, output, or bi-directional I/O.
- According to JEDEC standards, HSTL/SSTL outputs and bi-directional pins must be terminated to VTT, and inputs referenced to VTT.
- Lack of SSTL/HSTL termination or use of a non-HSTL/SSTL combination results in excessive V_{REF} leakage. Such leakage can reduce the V_{REF} voltage level on the board and affect the reliability of the device.
- Input V_{REF} leakage is specified in the device datasheet.

The following table lists the assignment of ION signal, when IOP signal is assigned for V_{REF} pin of MSIO/MSIOD banks.

Table 4 • **Status of the V_{REF} Pin Assigned Rule for IOA**

IOP	ION	Status
V_{REF}	Output	Invalid
	Tristate	Invalid
	Bi-directional	Invalid
	Input	Valid

2.4.2.2 High-Speed Transceiver Logic (HSTL) Class I

HSTL I is a general-purpose, high-speed 1.5 V bus standard (EIA/JESD8-6) for signaling between integrated circuits. The signaling range is 0 V to 1.5 V, and signals can be either single-ended or differential. HSTL requires a differential amplifier input buffer and a push-pull output buffer. This standard is used in the memory bus interface, with a data-switching capability of up to 400 MHz. Other advantages

of this standard are low power and fewer EMI concerns. HSTL has four classes, of which RTG4 devices support Class I. The reference voltage (V_{REF}) for this standard is 0.75 V.

2.4.2.3 Stub-Series Terminated Logic 2.5 V (SSTL2) Class I and II

SSTL2 Class I and II are general-purpose 2.5 V memory bus standards (JESD8-9) designed specifically for driving the DDR SDRAM modules used in computer memory. The SSTL2 requires a differential amplifier input buffer and a push-pull output buffer. The V_{REF} for these standards is 1.25 V.

2.4.2.4 Stub-Series Terminated Logic 1.8 V (SSTL18) Class I and II

SSTL18 Class I and II are general-purpose 1.8 V memory bus standards (JESD8-15), designed specifically for driving the DDR2 SDRAM modules used in computer memory. SSTL18 requires a differential amplifier input buffer and a push-pull output buffer. The V_{REF} for these standards is 0.9 V.

2.4.2.5 SSTL Termination

SSTL2/SSTL18 FPGA circuitry incorporates a calibrated termination which no longer require external "stub" resistors. This implementation saves cost and board space. The circuitry provides JEDEC compliant signaling and maintains accurate signal integrity.

2.4.3 Differential Standards

Differential standards require two I/Os per signal, called a signal pair. Logic values are determined by the potential difference between the lines, not with respect to ground. This is why differential drivers and receivers have much better noise immunity than single-ended standards. Differential standards offer higher performance and lower power consumption than their single-ended counterparts. Two I/O pins are used for each data transfer channel; resistor termination is required on both the I/Os.

2.4.3.1 Low-Voltage Positive Emitter Coupled Logic (LVPECL)

When the power supply is +3.3 V, it is commonly referred to as LVPECL. LVPECL requires that one data bit is carried through two signal lines; thus two pins are needed per input. The voltage swing between the two signal lines is approximately 850 mV.

2.4.3.2 Low-Voltage Differential Signaling (LVDS)

LVDS is a differential I/O standard. As with all differential signaling standards, LVDS requires that one data bit is carried through two signal lines, and it has inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350 mV. External V_{REF} or board termination voltage (VTT) is not required. LVDS requires the use of two pins per input or output.

2.4.3.3 Reduced Swing Differential Signaling

Reduced swing differential signaling (RSDS) is a signaling standard that defines the output characteristics of a transmitter and input characteristics of a receiver along with the protocol for a chip-to-chip interface between flat-panel timing controllers and column drivers.

2.4.3.4 B-LVDS/M-LVDS

Bus LVDS (B-LVDS) refers to bus interface circuits based on LVDS technology. Multi-point LVDS (M-LVDS) specifications extend the LVDS standard to high-performance multi-point bus applications. Multi-drop and multi-point bus configurations may contain any combination of drivers, receivers, and transceivers. The LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the bus load.

The driver requires series terminations to improve signal quality and to control the voltage swing. Termination is also required at both ends of the bus because the driver can be located anywhere on the bus. The RTG4 MSIOD has an internal circuit isolation, and when using M-LVDS, the bus isolation must be implemented in the design external to the FPGA.

2.4.3.5 Mini-LVDS

Mini-LVDS is a serial, intra-flat panel solution that serves as an interface between the timing control function and an LCD source driver.

2.4.3.6 HCSL

HCSL is for PCI Express (PCIe) reference clock inputs, and is also available for many industry standard clock-generation devices.

2.4.4 Checking the Constraint Flow

The following section describes a constraint flow that is followed for RTG4 devices.

2.4.4.1 SSTL/HSTL

The design combines SSTL/HSTL I/O types with non-SSTL/HSTL I/O types such as LVCMOS, LVTTL, or PCI in a single MSIO or MSIOD bank. In an I/O pair, an SSTL/HSTL input or SSTL/HSTL bi-directional I/O is placed on PADP and a non-SSTL/HSTL I/O on PADN.

When an existing RT4G150 project created with a release prior to Libero SoC 11.7 SP1.1 is opened in the current release, a placement check on the SSTL/HSTL I/Os is triggered.

- If the design fails to the SSTL/HSTL I/O check, the design is reverted to the pre-synthesis state for an enhanced constraint flow or to the pre-compile state for the classic constraint flow.
- To continue with the design flow after the check fails, change the I/O standards or package pin assignment to remove the violation and rerun the design flow.

Note: For new projects created with the current release, the SSTL/HSTL I/O check is implemented as part of the design flow.

In MSIO or MSIOD banks, the design uses SSTL/HSTL I/O inputs or SSTL/HSTL bi-directional pins without ODT or on-board terminations.

- If on-board termination is not in place, the ODT I/O attribute must be enabled in the Constraint Manager.
- The board has MSIO or MSIOD banks with unterminated pins, which can be driven completely low tied to the VSS (0 V) rail or hard tied to VSS. The pins are paired with SSTL/HSTL I/O inputs on PADN or SSTL/HSTL bi-directional pins on PADP. It is recommended to revise the board design to eliminate this condition and avoid any leakage current. For more information about board design guidelines, see *AC439: Board Design Guidelines for RTG4 FPGAs Application Note*.

3   I/O Features

This chapter describes the following I/O features that are supported in the RTG4 FPGA:

- I/O Programmable Features
- Cold Sparing
- I/Os Shared By Fabric and FDDR
- JTAG I/Os
- Dedicated I/Os
- Dedicated Global I/Os
- I/O Register Combining
- Failsafe Mode for Differential Receivers

3.1   I/O Programmable Features

RTG4 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P and N) supports the following programmable features:

- Programmable input delay
- Pre-emphasis
- Programmable slew rate control
- Programmable output drive strength
- Programmable weak pull-up/pull-down
- Programmable Schmitt trigger input and receiver
- Configurable ODT and driver impedance

These features can be configured using Libero SoC or in a PDC file. For more information about I/O programmable features, see the *Libero SoC User Guide*.

The following table lists the features supported for single-ended and differential I/Os.

Table 5 •   **RTG4 I/O Features**

I/O Features	MSIO	MSIOD	DDRIO
Single-Ended Transmitter			
Programmable drive strength	Yes	Yes	Yes
Programmable weak pull-up and pull-down	Yes	Yes	Yes
Configurable ODT[1]	Yes	Yes	Yes
LVTTL/LVCMOS 3.3 V outputs compatible with external 5 V TTL inputs	Yes		
Pre-emphasis capability		Yes	
Programmable slew rate			Yes
Single-Ended Receiver			
5 V-tolerant with minimal use of external circuitry	Yes	Yes	
Schmitt receiver	Yes	Yes	Yes
Programmable input delay	Yes	Yes	Yes
Differential Transmitter			
Programmable weak pull-up and pull-down	Yes	Yes	Yes
Configurable ODT	Yes	Yes	Yes
Programmable slew rate			Yes

Table 5 • **RTG4 I/O Features** *(continued)*

I/O Features	MSIO	MSIOD	DDRIO
Differential Receiver			
100 Ω differential ODT	Yes	Yes	
Schmitt receiver	No	No	No
Programmable input delay	Yes	Yes	Yes
Programmable Slew rate			Yes

1. ODT is not supported for LVCMOS18 in any Bank. See the table on page 148 of the *Libero Design Constraints User Guide* for more information about I/O types and Banks that supports ODT.

3.1.1   Programmable Input Delay

When configured as an input, each I/O can be programmed with different input delays. The input delay is calculated using the following equation:

```
Delay = D + N x 0.1 ns
```

where N ranges from 0 to 63.

D is the intrinsic delay or circuit delay of an input (without additional delay), when N is 0. The total delay range is between D ns to D + 6.3 ns. The intrinsic delay varies depending on the slew rates—SLOW (SS), MEDIUM (TT), and FAST (FF).

Therefore, there are 65 input delay values that can be selected and configured using the I/O Constraints Editor in Libero SoC for MSIO, MSIOD, and DDRIO.

Note: Input delays can be used to improve the hold time of the input register by increasing the input pin to match with the input register delay.

3.1.2   Pre-Emphasis

Pre-emphasis is supported in transmitting high-speed signal through long cable connection. When a serial of data is transmitted through long cables, there are chances of losing the original data at the receiver end. Therefore, the serial data rate is increased by reducing losses in copper interconnect or long cables. Pre-emphasis is supported in LVDS of MSIOD banks.

Pre-emphasis is only supported in the MSIOD User IO Bank.

Pre-emphasis is used to temporarily boost the differential drive during a transition of signal from low to high or high to low. This is a temporary boost of the drive strength. The boost strength (amplitude) is programmable in multiples of the base drive strength. The boost length (width) is delay based and not PVT compensated.

The base driver of the RTG4 is 1.25 mA. Based on the legal combinations, the "required" LVDS Tx drive strength is 2.5 mA (called 2x mode). There are three options for LVDS IO type modes:

*   2x drive mode (no pre-emphasis)"= IO constraint NONE"
*   3x drive mode (2x base drive + additional 1x pre-emphasis)"= IO constraint MIN"
*   4x drive mode (2x base drive + additional 2x pre-emphasis) "=IO constraint MAX"

The base RSDS Tx drive strength is 1.25 mA (called 1x mode). There are four options for RSDS IO type modes:

*   1x drive mode (no pre-emphasis)"= IO constraint NONE"
*   2x drive mode (1x base drive + additional 1x pre-emphasis)"=IO constraint MIN"
*   3x drive mode (1x base drive + additional 2x pre-emphasis)"=IO constraint MED"
*   4x drive mode (1x base drive + additional 3x pre-emphasis)'=IO constraint MAX" .

Note: In MSIOD, pre-emphasis is supported only on the differential output.

3.1.3 Programmable Slew Rate Control

MSIO and MSIOD do not support a user programmable slew rate, although, the MSIO and MSIOD output drive slew rate is managed, to some extent, with staggered output pre-drive stages. Each output buffer has multiple transistors connected in parallel and driven by corresponding pre-driver circuits. Delay circuit is introduced to stagger the pre-driver turn-on times and control overshooting of the switching current.

DDRIO has two bits of programmable slew control on the non-differential drive outputs. LVCMOS18, LVCMOS15, and LVCMOS12 support the minimum, medium, and maximum slew controls.

The DDRIO output drive slew rate is also managed through staggered-output pre-drive stages and by use of an impedance matched output driver.

3.1.4 Programmable Weak Pull-Up/Pull-Down

All I/O standards support the weak pull-up, weak pull-down, and none state. The default configuration is none. These states can be configured using the I/O Constraints Editor in the Libero SoC. The weak pull-up and weak pull-down are mutually exclusive and weakly hold the output to VDDI or VSS through a 10 K Ω resistor.

The following table lists the weak pull-up and weak pull-down support for various I/O standards.

Table 6 • **Weak Pull-Up/Pull-Down Support**

I/O Standard	MSIO	MSIOD	DDRIO
LVTTL33	None		
	Down		
	Up		
LVCMOS33	None		
	Down		
	Up		
PCI	None		
	Down		
	Up		
LVCMOS12	None	None	None
	Down	Down	Down
	Up	Up	Up
LVCMOS15	None	None	None
	Down	Down	Down
	Up	Up	Up
LVCMOS18	None	None	None
	Down	Down	Down
	Up	Up	Up
LVCMOS25	None	None	None
	Down	Down	Down
	Up	Up	Up

3.1.5 Programmable Schmitt-Trigger Input and Receiver

The MSIO, MSIOD, and DDRIO inputs can be configured as a Schmitt-trigger receiver. Schmitt Triggers are supported for only CMOS/LVTTL Type single-ended standards. When the Schmitt trigger inputs are enabled, the input buffers present a hysteresis, filter out the noise at the receiver, and prevent double glitching caused by noise at input edges. This feature can be enabled or disabled using a physical design constraints (PDC) command or using the I/O Constraints Editor in Libero SoC. The Schmitt-trigger receiver is disabled by default.

The following table lists standards that support the Schmitt receiver feature.

Table 7 •   **Schmitt Receiver Support**

I/O Standard	MSIO	MSIOD	DDRIO
LVTTL33	Off		
	On		
LVCMOS33	Off		
	On		
PCI	Off		
	On		
LVCMOS12	Off	Off	Off
	On	On	On
LVCMOS15	Off	Off	Off
	On	On	On
LVCMOS18	Off	Off	Off
	On	On	On
LVCMOS25	Off	Off	Off
	On	On	On

3.1.6 Programmable Output Drive Strength

The programmable current drive output buffers can be programmed to select current drive capabilities ranging from 2 mA to 16 mA. Programmable values are available only for LVTTL and LVCMOS standards, as listed in the following table. These values can be programmed for the selected I/O standards using the I/O Constraints Editor in Libero SoC.

Table 8 •   **Recommended Output Drive Strengths**

I/O Standard	MSIO (mA)	MSIOD (mA)	DDRIO (mA)
LVTTL	2		
	4		
	8		
	12		
	16		

Table 8 • **Recommended Output Drive Strengths** *(continued)*

I/O Standard	MSIO (mA)	MSIOD (mA)	DDRIO (mA)
LVCMOS33	2		
	4		
	8		
	12		
	16		
LVCMOS12	2	2	2
	4	4	4
			6
LVCMOS15	2	2	2
	4	4	4
	6	6	6
	8		8
			10
			12
LVCMOS18	2	2	2
	4	4	4
	6	6	6
	8	8	8
	10	10	10
	12		12
			16
LVCMOS25	2	2	2
	4	4	4
	6	6	6
	8	8	8
	12	12	12
	16		16

3.1.7 Configuring ODT and Driver Impedance

MSIO, MSIOD, and DDRIO have the ODT or transmitter impedance feature, which is calibrated depending on the I/O standard used. Only DDRIO supports calibrated ODT and driver impedance. If the impedance feature is enabled, DDRIO ODT and driver impedance can be programmed to the desired value in three ways:

• Using calibration block
• Using fixed calibration codes
• Statically and directly to desired value

There are two DDRIO calibration blocks in each RTG4 device, one of which is in the FDDR. Each calibration block calibrates ODT/driver impedance for all 44 DDRIO pairs (P and N). Table 2, page 9 shows the impedance configuration for DDRIO.

3.1.7.1 Calibrating the DDRIO ODT/Driver Impedance Using Calibration Block

The I/O calibration block automatically calibrates the I/O drivers to an external resistor. The impedance controller identifies the digital values, PCODE<5:0> and NCODE<5:0>. These values are fed to the soft enter pull-up/pull-down reference network to match the impedance values with external resistor values. After matching the PCODE and NCODE register values with the external resister values, they are latched and sent to the drivers.

The calibrated impedance value can be configured statically by enabling ODT_STATIC, or dynamically by enabling ODT_DYN. ODT_STATIC selects the ODT value set in the flash configuration bits programmed during power-on, whereas ODT_DYN selects the ODT value provided at run time. For more information about how to enable the calibration block, see *UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide*.

The following table lists ODT impedance calibrated for the various I/O standards.

Table 9 •   **Calibrated ODT Impedance**

Driver Mode	Reference Resistor (Ω)	Calibrated Impedance
ODT, DDR3/SSTL 1.5, 1.5 V	240	120
		60
		40
		30
		20
ODT, DDR2/SSTL 1.8, 1.8 V	150	150
		75
		50
ODT, HSTL	191	47.8

To calibrate a driver or a transmitter impedance for an I/O, configure it to the calibrated impedance according to the flash configuration bits for the appropriate I/O standard. The recommended reference resistor values listed in Table 9, page 19 are used for calibration.

The following table lists the driver and transmitter impedance values calibrated for various standards.

Table 10 •   **Calibrated Driver/Transmitter Impedance**

Driver Mode	Reference Resistor (Ω)	Calibrated Impedance
Transmitter, DDR3 SSTL 1.5 V	240	34
		40
Transmitter, DDR2 SSTL 1.8 V	150	20
		42
Transmitter, DDR1 SSTL 2.5 V	150	20
		42
Transmitter, LPDDR SSTL 1.8 V	150	20
		42
Transmitter, HSTL 1.5 V	191	25.5
		47.8

Table 10 • **Calibrated Driver/Transmitter Impedance** *(continued)*

Driver Mode	Reference Resistor (Ω)	Calibrated Impedance
LVCMOS 1.2 V and 1.5 V	300	75
		66.7
		50
LVCMOS 1.8 V	150	75
		50
		33
		25
LVCMOS 2.5 V	150	75
		50
		33
		25

3.1.7.2 Calibrating ODT/Driver Impedance Using Fixed Calibration Codes

DDRIO can use fixed impedance calibration for different drive strengths, and these values can be programmed using the I/O Constraints Editor in the Libero SoC for the selected I/O standards. For more information about I/O Constraints Editor, see *Libero SoC User Guide*.

The following table lists the recommended DDRIO output drive strength values. PCODE and NCODE values are used to define internally calibrated impedance and drive strengths of the IO. Libero SoC generally programs the required PCODE/NCODE values but these values can be modified when necessary. The PCODE<5:0> and NCODE<5:0> registers are accessible through the dedicated APB configuration interface.

Table 11 • **Recommended PCODE and NCODE Values**

I/O Standard	NCODE	PCODE
DDR1 Full Drive/SSTL2 II	42	44
DDR1 Half Drive/SSTL2 I	42	44
DDR2 Full Drive/SSTL18 II	58	61
DDR2 Half Drive/SSTL18 I	58	61
LPDDR Full Drive	58	61
LPDDR Half Drive	58	61
HSTL II	53	56
HSTL I	53	56
LVCMOS25 16 mA	42	44
LVCMOS25 12 mA	42	44
LVCMOS25 8 mA	42	44
LVCMOS25 6 mA	42	44
LVCMOS25 4 mA	42	44
LVCMOS25 2 mA	42	44
LVCMOS18 16 mA	58	61
LVCMOS18 12 mA	58	61

Table 11 • **Recommended PCODE and NCODE Values** *(continued)*

I/O Standard	NCODE	PCODE
LVCMOS18 10 mA	58	61
LVCMOS18 8 mA	58	61
LVCMOS18 6 mA	58	61
LVCMOS18 4 mA	58	61
LVCMOS18 2 mA	58	61
LVCMOS15 12 mA	53	56
LVCMOS15 10 mA	53	56
LVCMOS15 8 mA	53	56
LVCMOS15 6 mA	53	56
LVCMOS15 4 mA	53	56
LVCMOS15 2 mA	53	56
LVCMOS12 6 mA	40	42
LVCMOS12 4 mA	40	42
LVCMOS12 2 mA	40	42

3.1.7.3 Configuring ODT/Driver Impedance Statically to Desired Value Directly

ODT/drivers can directly be calibrated to a desired value by providing PCODE<5:0> and NCODE<5:0> values through the dedicated APB configuration interface—FIC2. When this is done, the values are overwritten with the existing values. For more information about how to configure the PCODE and NCODE values, see the FDDR I/O Calibration Control register of the System Register Block in the *UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide*.

The following tables list the recommended ODT values for MSIO, MSIOD, and DDRIO for various I/O standards.

Table 12 • **ODT Values**

I/O Standard	MSIO (Ω)	MSIOD (Ω)	DDRIO (Ω)
SSTL18I and SSTL18II (DDR2)	50	50	50
	75	75	75
	150	150	150
SSTL15I and SSTL15II (DDR3)			20
			30
			40
			60
			120
HSTL18I and HSTL18II	50	50	50
	75	75	75
	150	150	150
LPDDRI and LPDDRII			50
			75
			150

Note: BUSLVDS, MLVDS, and LVDS33 do not support 100 Ω ODT in Libero SoC. Use a 100 Ω external termination for BUSLVDS and MLVDS.

Table 13 • **Supported ODT Values**

I/O Standard	MSIO (Ω)	MSIOD (Ω)	DDRIO (Ω)
LVPECL33	100		
LVDS25	100	100	
RSDS	100	100	
MINILVDS	100	100	

3.1.7.4   I/O External Termination

If ODT is not used, I/O standards require termination for better signal integrity. Serial termination refers to driver and parallel termination refers to the receiver. Voltage-referenced standards typically have both serial and parallel termination whereas differential standards only have a parallel termination.

The following table lists the external termination schemes supported for DDRIO, MSIO, and MSIOD when the ODT/driver impedance calibration feature is not used.

Table 14 • **Supported Termination Schemes**

I/O Standard	External Termination Scheme
SSTL 1.5 single-ended (Class I and II)	Single-ended SSTL I/O standard termination
SSTL 1.8 single-ended (Class I and II)	
SSTL 2 single-ended (Class II)	
HSTL 1.5 single-ended (Class II)	Single-ended HSTL I/O standard termination
SSTL 2.5 differential (Class I and II)	Differential SSTL I/O standard termination
SSTL 1.8 differential (Class I and II)	
SSTL 1.5 differential (Class I and II)	
HSTL 1.5 differential (Class II)	Differential HSTL I/O standard termination
LVCMOS 2.5	No external termination required
LVCMOS 1.8	
LVCMOS 1.5	
LVCMOS 1.2	
LVDS	100 Ω, parallel termination
MLVDS	100 Ω, parallel termination
BLVDS	100 Ω, parallel termination
RLVDS	100 Ω, parallel termination
Mini LVDS	100 Ω, parallel termination
LVPECL	100 Ω, parallel termination

Note: The RTG4 device does not support bus keeping feature.

For more information about electrical characteristics, see the *DS0131: RTG4 FPGA Datasheet*.
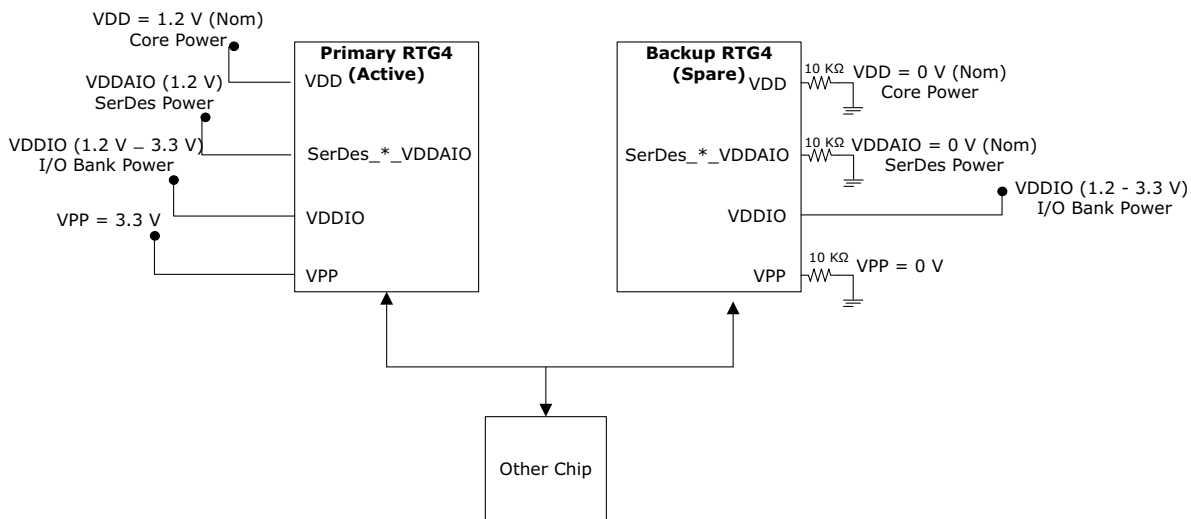
3.2 Cold Sparing

In cold-sparing applications, voltage can be applied to device I/Os before and during power-up. The RTG4 device supports cold-sparing applications, which have the following strategies:

- The system board integrates two parallel RTG4 devices on the board with shared or common I/O connections.
- The primary RTG4 device has its core such as VDD and SerDes VDDAIO powered and fully functional until a point is reached when swap of devices is determined to be necessary.
- The backup (spare) RTG4 device has its I/O banks powered and fabric core unpowered to prevent I/O leakage through the internal ESD diodes. The backup (spare) RTG4 VPP, fabric core, and SerDes supplies are unpowered to establish low power and a protected state.
- At any point, primary and backup devices may be swapped by powering down VPP, VDD, and SerDes VDDAIO of the primary RTG4 device, and by powering up VPP, VDD, and SerDes VDDAIO of the backup RTG4 device and going through the device configuration sequence.
- The parts in primary and backup devices are identical.
- Only one of the two devices may be active at one time.
- Core VDD high activates the device and low de-activates the device.
- The inactive device must have VPP, VDD, and SerDes VDDAIO tied to the ground through 10 kΩ resistors and must not be floating.
- All active bank VDDIO supplies must be powered on the inactive device.

The advantages of cold sparing are as follows:

- Driving a Rx lane on an unpowered RTG4 from a Tx lane on a powered RTG4 is allowed.
- The device can be powered up in any sequence. Specific power supply sequencing is not required.
- The backup (spare) device is in inactive mode.
- All banks with active I/Os must be powered.
- The I/O buffers of the backup spare device are disabled but powered.
- During the cold sparing process, excess device leakage does not occur in the backup (spare) device.

Figure 5 •   **Cold Sparing**

The backup RTG4 device functions as a replacement for the primary device. The following table lists the pin names and their cold sparing board tie-off conditions.

Table 15 •   **Cold Sparing Board Tie-Off**

Supply	Cold Sparing Board Tie-Off	Description
VDD	10 KΩ to VSS	Low voltage core power
VDDPLL	Supplied or 10 KΩ to VSS	PLL power
VDDI3	Supplied	Power for JTAG I/Os
VPP	10 KΩ to VSS	Power for the programming blocks. Power for the programming analog blocks.
SERDES_*_VDDAIO	10 KΩ to VSS	SERDES analog supplies
SERDES_*_VDDAPLL	Supplied or 10 KΩ to VSS	SERDES PLL supplies
SERDES_VDDI	Supplied	Power for SerDes RefClk receiver
VDDI*	Supplied	I/O power
VREF*	10 KΩ to VSS	FDDR voltage reference pins
SERDES_VREF	10 KΩ to VSS	All SerDes RefClk receivers voltage reference pin

3.2.1   5 V-Input Tolerance and Output Driving Compatibility (only MSIO)

3.2.1.1   5 V-Input Tolerance

I/Os can support 5 V inputs in LVTTL 3.3 V and LVCMOS 3.3 V configurations when one of the three techniques described in this section is used to reduce the voltage at the I/O. All the solutions meet a common requirement of limiting the voltage at the input to 3.45 V or less. The I/O absolute maximum voltage rating is 3.45 V, and any voltage above 3.45 V may cause long-term gate oxide failures.

3.2.1.1.1   Solution 1

To ensure long-term reliability, the board-level design must ensure that the waveform reflecting at the pad does not exceed the limits specified in the recommended operating conditions in the *DS0131: RTG4 FPGA Datasheet*.

This scheme also works for a 3.3 V PCI configuration, but the internal diode must not be used for clamping, and the voltage must be limited by two external resistors. Relying on diode clamping creates an excessive pad DC voltage of 4 V (3.3 V + 0.7 V).

This solution requires two board resistors. Here are some examples of possible resistor values based on a simplified simulation model with no line effects and with 10 Ω transmitter output resistance.

where,

`Rtx_out_high = [VDDI – VOH] / IOH and Rtx_out_low = VOL / IOL).`

Example 1 (high speed, high current)

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 × 0.95 + 36 × 0.95 + 10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low-medium speed, medium current)

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 × 0.95 + 390 × 0.95 + 10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V when the transmitter sends a logic 1.

This range of Vin_dc(rx) must be ensured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

The following figure shows solution 1 for 5 V input tolerance.

Figure 6 •   **5 V Input Tolerance–Solution 1**

Requires Two Board Resistors LVCMOS 3.3 V I/Os
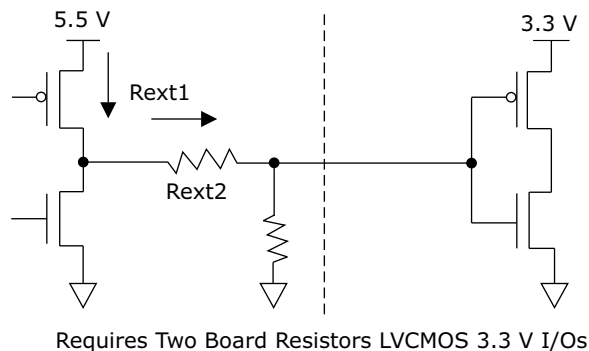
3.2.1.1.2   Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed the voltage overshoot/undershoot limits provided in the datasheet. This is a requirement to ensure long-term reliability. This scheme also works for a 3.3 V PCI configuration, but the internal diode must not be used for clamping, and the voltage must be limited by the external resistors and Zener. Relying on the diode clamping would create an excessive pad DC voltage of 3 V + 0.7 V = 4 V.

The following figure shows the solution 2 of 5 V input tolerance.

Figure 7 •   **5 V Input Tolerance–Solution 2**

Requires One Board Resistor, One Zener 3.3 V Diode,
and LVCMOS 3.3 V I/Os
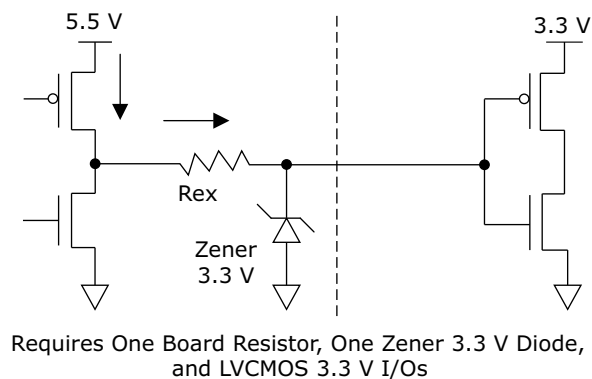
3.2.1.2 5 V Output Driving Compatibility

RTG4 I/Os must be set either to 3.3 V LVTTL mode or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical to ensure that there is no external I/O pull-up resistor to 5 V because this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and, consequently, cause damage to the I/O. When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, the I/Os can directly drive signals into the 5 V TTL receivers. VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the VIL and VIH requirements of 5 V TTL receivers, which are 1.8 V and 2 V respectively. Therefore, level 1 and level 0 are recognized correctly by 5 V TTL receivers.

Note: To make MSIOD complaint with LVCMOS 33 (3.3V). Ensure that:

- Input signals do not exceed (VDDI ± 5%).
- Input signals meet the min VIH requirement of the LVCMOS 2.5V when the I/O is powered at 2.5V.
- Input signals meet the max VIL requirement of the LVCMOS 2.5V when the I/O is powered at 2.5V.
- Slew rates required by the application (thereby, IO speed) are satisfied.
- All the components needed for reducing the voltage seen by the pad must be space graded for space applications.

3.2.2 Temperature Sensing

The temperature sensing feature is used as an internal thermometer to provide a way for monitoring the die temperature. This is a temperature sense diode located in lower left corner of the device. The temperature sensing diode has one dedicated pin–PTEMP–connected to the anode of the diode. The cathode of the diode is connected to the VSS of the die. The diode is a passive device, and the pins are always attached to the die. The PTEMP pin can be left floating if the feature is not being used. There is nothing that needs to be programmed in the software to enable this feature. To use the temperature sensing diode, the diode must be calibrated by user software and/or circuits. To measure the temperature, check the voltage drop between PTEMP and VSS.

3.3 I/Os Shared By Fabric and FDDR

3.3.1 DDRIO with FDDR

If FDDR is selected, Libero SoC automatically connects FDDR signals to the DDRIOs. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. Unused DDRIOs are available to connect to the FPGA fabric.

3.3.2 DDRIO with Fabric

If FDDR is not selected, DDRIOs are available to the FPGA fabric. The DDRIOs must be configured manually in Libero SoC.

3.3.3 MSIO/MSIOD with Fabric

There are two macros in the silicon called DDR_IN and DDR_OUT that can be connected to a DDR controller soft IP core in fabric. The MSIO and MSIOD I/O standards can be used for DDR controllers that cannot be supported by a dedicated DDRIO bank. MSIOs/MSIODs are available to the FPGA fabric and must be configured manually in Libero SoC.

3.4 JTAG I/Os

The system controller implements the functionality of a JTAG slave with IEEE 1532 support, which also implies IEEE 1149.1 compliance. JTAG communicates with the system controller using a command register that conveys the JTAG instruction to be executed and a 128-bit data I/O buffer that transfers any associated data.

The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). The I/O voltage of this interface is set by powering the VJTAG power pin with the desired I/O voltage. Core voltage must also be powered for the JTAG state machine to operate, even if the device is in bypass mode. VJTAG power alone is insufficient. Both VJTAG and core voltage to the RTG4 part must be supplied to allow JTAG signals to transit the RTG4 device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility

with supply selection and simplifies the power supply and PCB designs. If the JTAG interface is not used and also not planned for future use, the VJTAG pin, together with the TRSTB pin, must be tied to VSS.

The TAP controller is a state machine that controls the behavior of the JTAG system. Its transitions are controlled by the TMS signal. The TAP controller uses 8-bit instructions consistent with the older Microsemi product families.

There are two types of TAP controllers: Fabric TAP and Auxiliary TAP.

The following table lists the JTAG pin names available in the RTG4 device.

Table 16 • **JTAG Pin Description**

Name	Type	Bus Size	Description
TCK	In	1	Test clock that provides serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to VSS or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. To operate at all VJTAG voltages, the resistor values mentioned in Table 6-13 on page 112 are recommended.
TDI	In	1	Serial test data input for JTAG boundary scan, ISP, and UJTAG usage has a 10 K internal weak pull-up resistor.
TDO	Out	1	Serial test data output for JTAG boundary scan, ISP, and UJTAG.
TMS		1	Test Mode Select. Controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRSTB). Has a 10 K internal weak pull-up resistor.
TRSTB		1	Boundary scan reset pin. Functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. Has a 10 K internal weak pull-up resistor. If JTAG is not used, an external pull-down resistor must be included to ensure the TAP is held in reset mode. The resistor values must be selected from Table 17, page 27 and must satisfy the parallel resistance value requirement. The values in Table 17, page 27 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected through a JTAG chain. In safety critical applications and in a radiation mission critical environment (Avionics mode), an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends tying off TRSTB to VSS through a resistor placed close to the FPGA pin. This keeps JTAG circuitry in reset state.

Table 17 • **Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[1, 2]
VJTAG at 3.3 V	200 Ohm to 1 K Ω
VJTAG at 2.5 V	200 Ohm to 1 K Ω
VJTAG at 1.8 V	500 Ohm to 1 K Ω
VJTAG at 1.5 V	500 Ohm to 1 K Ω

1. The TCK pin can be pulled-up/down. If it is pulled-up, it must be based on the VJTAG voltage.
2. The TRSTB pin can only be pulled down. If there is more than one device on a JTAG chain, all the devices must have equal parallel resistance.

3.5 Dedicated I/Os

RTG4 devices have two types of dedicated I/Os: device reset I/Os and SerDes I/Os.

3.5.1 Device Reset I/Os

RTG4 devices have a dedicated input reset pin, named DEVRST_N. If then, at any time, this reset is asserted, the whole chip is reset as if a POR has occurred. The device reset feeds the system controller, which then generates the system reset for the reset controller to reset the entire device. The DEVRST_N pin cannot be used to reset the device during programming. When DEVRST_N is asserted before or during the supply ramp and deasserted after all supplies are up, the time taken by the device to come out of reset is less than or equal to the normal power-up to functional time (PUFT) (when DEVRST_N is not asserted at all). For more information about device reset, see *UG0576: RTG4 FPGA System Controller User Guide*.

The following figure shows the full chip reset flow from the device reset I/Os. Libero SoC allows the configuration of reset controller using the System Builder. Note that other resets such as the GRESET described in the Global Asynchronous Reset are meant for the digital reset of the device in user mode while the DEVRST_N pin is meant to re-start the device as if a POR has occurred.

Figure 8 • **Chip Level Resets From Device Reset I/Os**
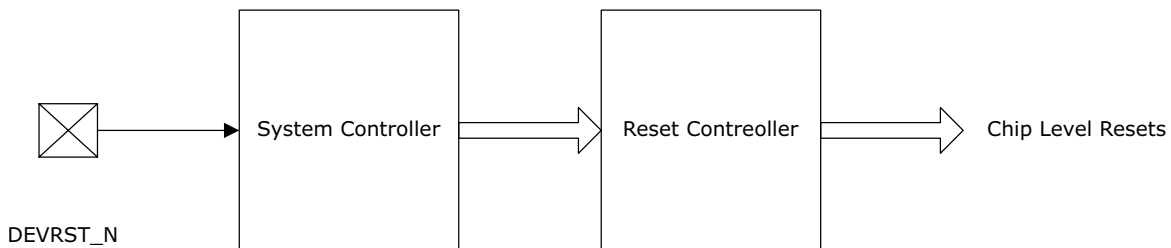
3.5.1.1 Port List and I/O Pins

The following table lists the port name and other details for the device reset.

Table 18 • **Device Reset I/O Pin Details**

Pin	Type	I/O	Description
DEVRST_N	Analog	Input	Device reset, asserted low, and powered by VPP.

3.5.2 SerDes I/Os

The SerDes I/Os available in RTG4 devices are dedicated to high-speed serial communication protocols. For more information about SerDes, see the *UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide*. The SerDes I/O supports protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid I/O (SRIO), and any user-defined high-speed serial protocol implementation in the fabric. These protocols access the SerDes lanes through the physical media attachment (PMA) and physical coding sub layer (PCS) of SerDes interface. The detailed configuration of the SerDes interface for various protocols is explained in the SerDesIF Block chapter of the *UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide*.

This section describes the SerDes I/O pins, banks, standards, and board-level design considerations for RTG4 devices.

3.5.2.1 SerDes I/O Banks

SerDes I/Os reside in dedicated I/O banks. The number of SerDes I/Os depends on the device size and pin count. For example, the RT4G150 device has four SerDes_IFs (SERDES_IF0, SERDES_IF1, SERDES_IF2, and SERDES_IF3) that reside in four I/O banks.

For more information about I/O bank locations and electrical specifications, see the *UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide*.

3.5.2.2 SerDes I/O Pins

Each SerDes interface in an RTG4 device has four SerDes I/O data lanes or 16 SerDes I/Os available for accessing the SerDes interface (SERDESIF block). Each data lane has two pairs of differential signals. The TxDP and TxDN signals are for transmit data and the RxDP and RxDN signals are for receive data. Data lanes are multiplexed to support different serial protocols and are scalable to various link widths such as ×1, ×2, and ×4. These settings can be configured in the SERDES_IF macro using Libero SoC. Each SERDES_IF macro has two sets of dedicated power, clock, and reference signals. One set for data lanes 0 and 1 and another for data lanes 2 and 3. For more information about SerDes I/Os, and for power pin names and descriptions, see *DS0130: RTG4 FPGA Pin Descriptions*.

3.6 Dedicated Global I/Os

Dedicated global I/Os are dual-use I/Os that can drive the global blocks directly or through clock conditioning circuits (CCC). They can also be used as regular user I/Os. Global I/Os are the primary source to bring external clock inputs into the RTG4 device.

Unused dedicated global I/Os behave similar to unused regular user I/Os (MSIO, MSIOD, and DDRIO). Libero SoC configures unused user I/Os as the input buffer, which is disabled by default and the output buffer is tristated with weak pull-up. RTG4 devices have 36 I/Os dedicated for global clocks, and have12 of clocks dedicated for SerDes clocks.

The GRESET block generates a global asynchronous reset signal during power-up or programming, and allows the user to apply an asynchronous reset on the fabric flip-flops globally. For more information about Global I/Os, see *UG0586: RTG4 FPGA Clocking Resources User Guide*.

3.6.1 Global Asynchronous Reset

An RTG4 device contains the following chip-wide resources to implement asynchronous reset/set signals. Note that regardless of the user selected asynchronous reset function during power-on and programming all fabric and IP blocks in the design are set or reset globally. See the power-up-to-functional information in the *UG0576: RTG4 FPGA System Controller User Guide* to show when the device's controlled reset is released to allow the following user resets to take effect:

- **GRESET**: This is a single resource that has hardwired connections from four semi-dedicated MSIO I/O pads. It can also be driven by an internal fabric signal. A GRESET macro in the design is mapped to this resource. If the MSIO pads are not used for the GRESET function, they behave similar to regular user I/Os and can be used for other I/O interface pins. The output of the GRESET block is the ARST_N signal that is routed to the RGRESET block and can be selected as an option for each half-row of the device as needed.
- **Global Resources**: Up to 17 half-chip global resources asynchronous reset per vertical half-row of the device. These signals must drive the RGRESET block to control the asynchronous reset of a half-row of the fabric. This feature is not available in the RT4G150_ES device.
- **Asynchronous Resets**: Up to 206 asynchronous resets are available. This is the number of half-row fabric interfaces that are driven by the RGRESET block on the RT4G150 device.
- **RGRESET**: This is a single resource that serves each half-row of logic clusters in the fabric and resides in the two RGB stripes of a device. Each RGRESET resource spans half a row. It has a hardwired connection from the GRESET resource. In addition, it has hardwired connections from 17 GB resources through an RGB resource (for all RTG4 devices except the RT4G150_ES device). It can also be driven by three internal fabric signals, the drivers of which are triplicated from the same source, which must be either three separate SET mitigated flip-flops or three separate input buffers. An RGRESET macro in the design is mapped to this resource. This feature is not available in the RT4G150_ES device.
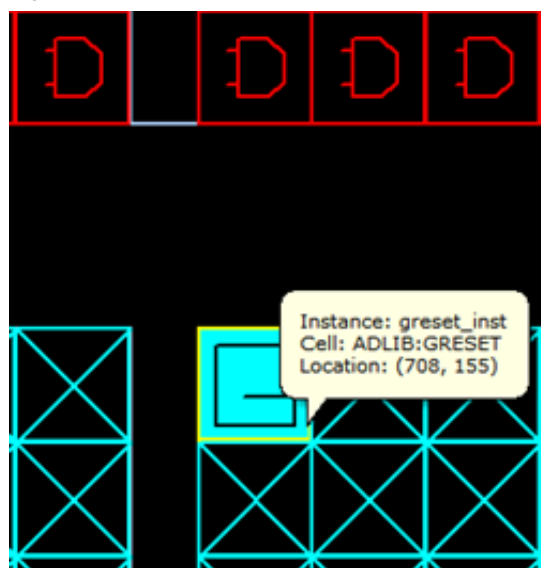
The following figure shows the asynchronous reset/set.

Figure 9 • **Asynchronous Reset/Set**
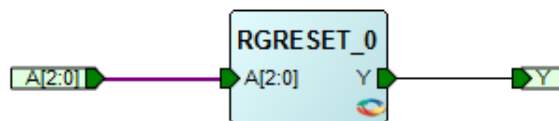
3.6.1.1 Software Implementation

When the design uses an asynchronous reset signal, the software automatically instantiates the GRESET macro, and the output of this macro drives the asynchronous reset ports of all the flip-flops in the design, including RAM flip-flops, mathblock flip-flops, fabric flip-flops, and I/O flip-flops if used. The software automatically instantiates a GRESET macro where the output of that macro is the ARST_N signal that feeds to the entire chip, as shown in the following figure.

Note: The GRESET macro can be instantiated only once.

Figure 10 • **GRESET I/O Chip Layout**

Instance: greset_inst
Cell: ADLIB:GRESET
Location: (708, 155)

The three dedicated GRESET pads are multifunction I/Os. The pads:

- Serve as regular MSIO,
- Directly feed specific GBs, and
- Are directly hardwired to the GRESET.

The following figure shows the three I/Os in the CG1657 package.

Figure 11 • **Dedicated GRESET I/O**

	Pin Number	Port Name	Macro Cell	Function		Locked	User Reserved	Dedicated	Vref	Bank Name
14	A17	Unassigned		MSIO292PB5/GB9/GRESET		☐	☐	☐	☐	Bank5
1020	E19	Unassigned		MSIO293PB5/GB11/GRESET		☐	☐	☐	☐	Bank5
1064	F22	Unassigned		MSIO307PB5/GB13/GRESET		☐	☐	☐	☐	Bank5
1269	L22	Unassigned		MSIO308PB5/GB15/GRESET		☐	☐	☐	☐	Bank5

3.6.1.2 Use Models

In RT4G150_ES silicon, row global asynchronous reset is directly sourced from the GRESET block. In production silicon, row global asynchronous reset can be programmed to keep the same configuration as that of revision A and revision B to tie with the global reset signal from GRESET block. Alternatively, it can use the routing resource from the clock network (physically located at RGB block) to select the local reset.

This section describes different methods users may use to drive the asynchronous reset, including software examples for each scenario.

3.6.1.2.1 Case 1

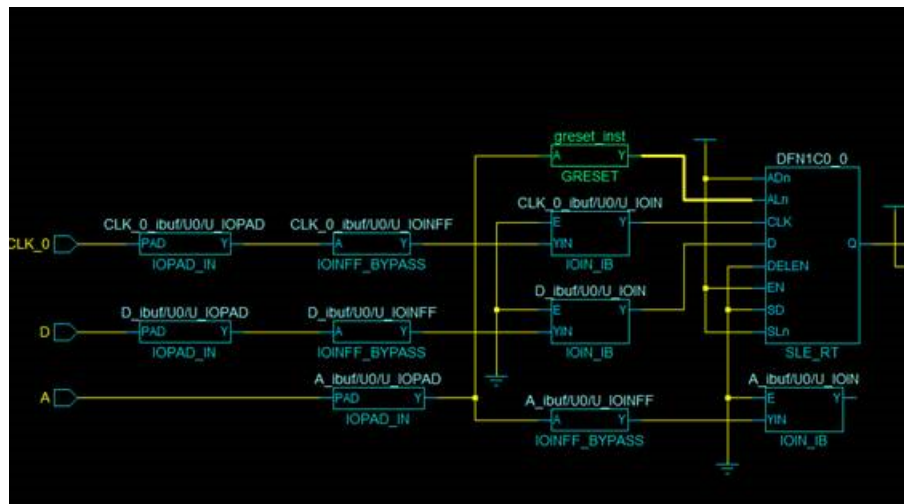Dedicated reset pad > **CLKINT** > **RST**.

The following figure shows Pin A assigned to one of the dedicated reset pads in this scenario.

Figure 12 • **Software Netlist Viewer Optimized View**
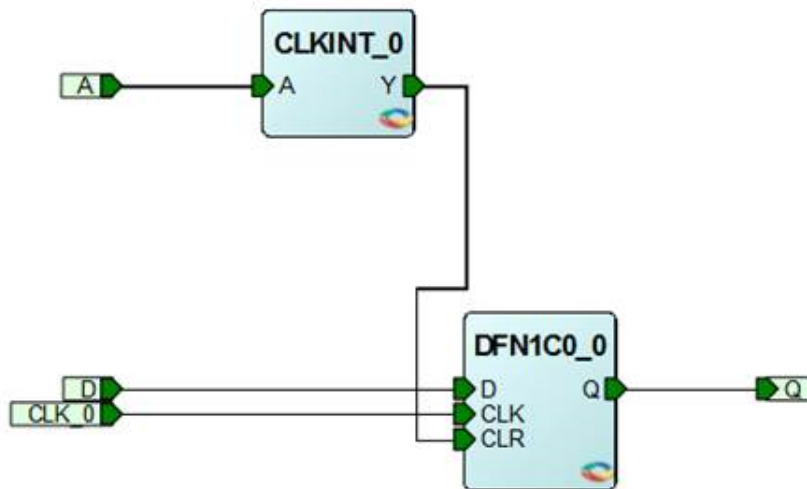
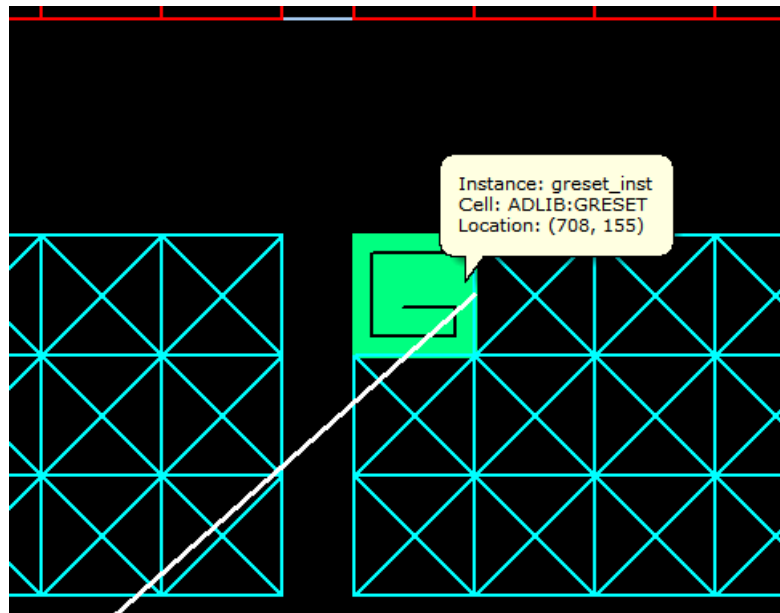CIKINT is optimized out. The net highlighted in yellow, which is the output of the GRESET, is hardwired.

Figure 13 • **GRESET Output – Case 1**

The software automatically instantiates a GRESET instance macro. The output of this macro is the ARST_N signal that is fed to the entire chip.

The following figure shows the ARST_N signal on the chip.

Figure 14 • **ARST_N Signal**

3.6.1.2.2 Case 2

Regular **I/O pad** > **CLKINT** > **RST**.

The following figure shows the pin A assigned to a regular I/O pad in this scenario.

Figure 15 • **Regular I/O Pad – Case 2**
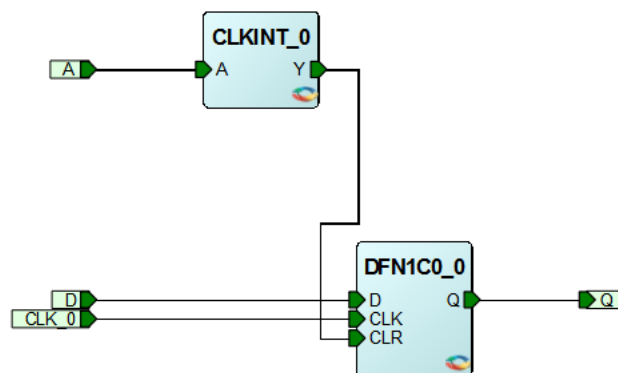
*Figure 16* • **GRESET Output – Case 2**
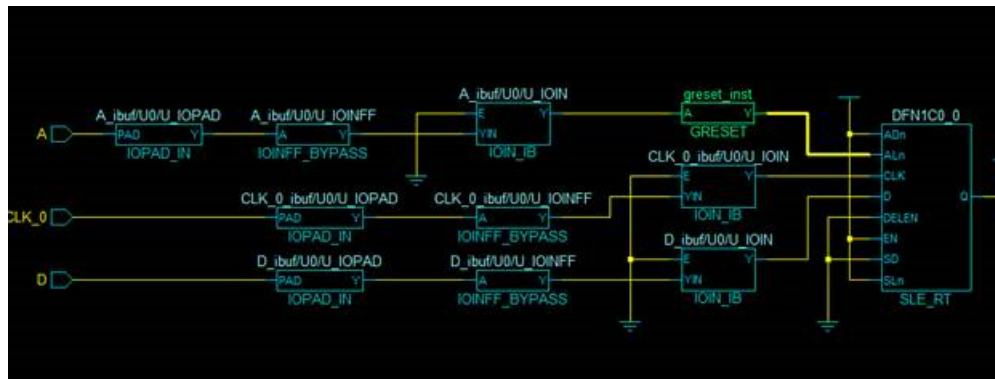
3.6.1.2.3 Case 3

Regular I/O pad > **Fabric Routing** > **CLKINT** > **RST**.

The CLKINT signal is removed by the software. The signal is routed from port A to AND2_0; from AND2_0:Y, the GRESET signal is routed, and from GRESET:Y, the reset pin of the flip flop is hardwired.

The following figure shows how a regular I/O pad is routed in this scenario.

Figure 17 • **Regular I/O Pad – Case 3**
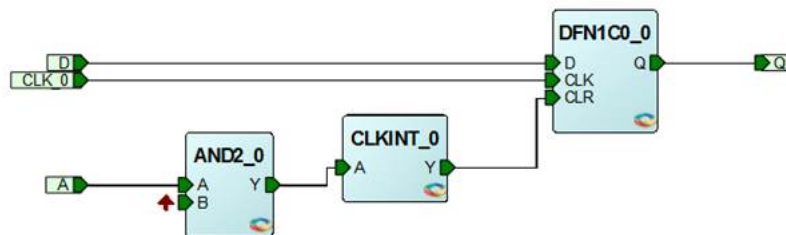
Figure 18 • **GRESET Output – Case 3**
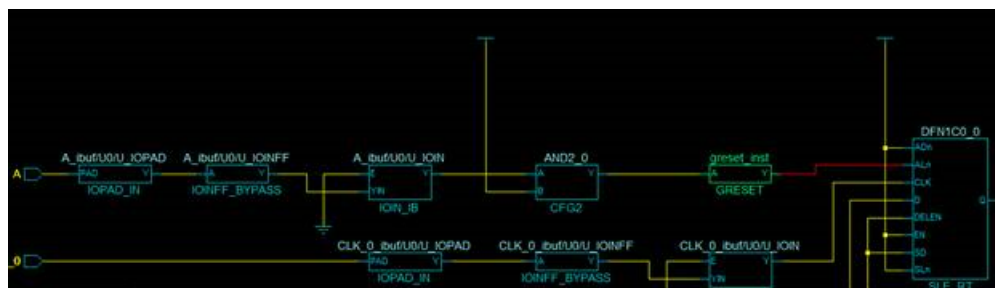
3.6.1.2.4 Case 4

Dedicated **GRESET I/O pad** > **Fabric Routing** > **CLKINT** > **RST**.

Similar to Case 3, the CLKINT is removed by the software. From port A to AND2, the signal is routed; from AND2:Y, the GRESET signal is routed; and from GRESET:Y, the reset pin of the flip flop is hardwired.

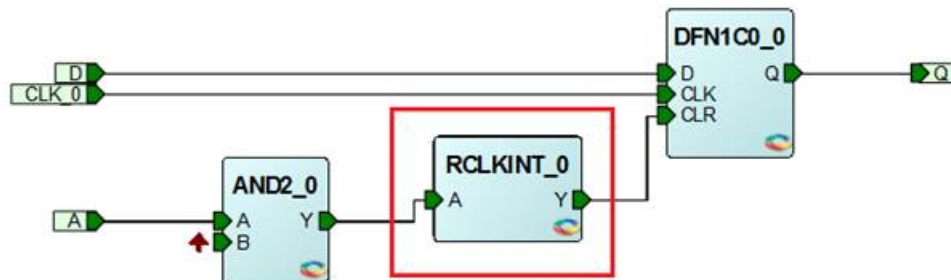*Figure 19 •* **Regular I/O Pad – Case 4**
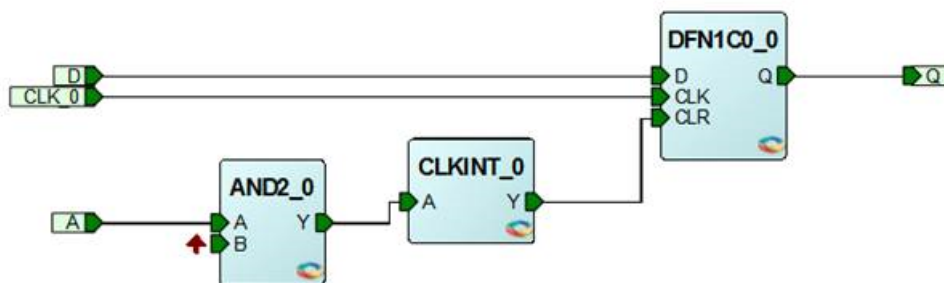
Figure 20 • **GRESET Output– Case 4**
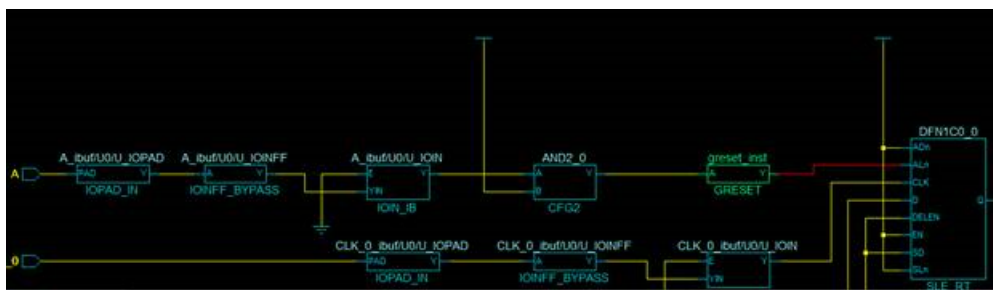
3.6.1.2.5 Case 5

Dedicate **GRESET I/O pad** > **Fabric Routing** > **RCLKINT** > **RST**.

Similar to cases 3 and 4, the RCLKINT is removed by the software. From port A to AND2, the signal is routed; from AND2:Y, the GRESET signal is routed; and from GRESET:Y, the reset pin of the flip flop is hardwired.

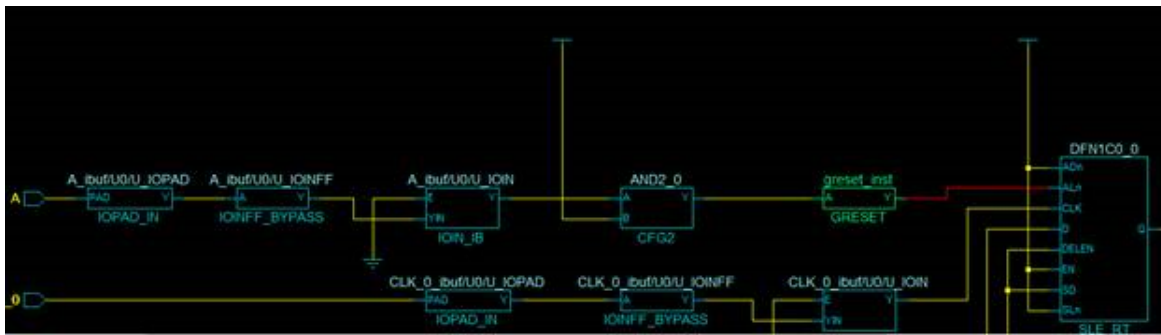*Figure 21 •* **Regular I/O Pad – Case 5**

Figure 22 • **GRESET Output– Case 5**

3.7 I/O Register Combining

I/Os are combined with a register to achieve better clock-to-out and input-to-clock timing. When combining these registers at the I/O buffer, some design rules must be met. This feature is supported by all I/O standards.

The I/O register combining rules are as follows:

- Registers combined on the Output and Output Enable must have the same configuration.

  Example: If the output register is DFN1C0, the Output Enable register must also be DFN1C0.

- All registers (Input, Output, and Output Enable) connected to an I/O must share the same clear (CLR) or preset (PRE) pin.
- If one of the registers has a CLR pin, all the other registers that are candidates for combining in the I/O must have a CLR pin.
- If one of the registers has a PRE pin, all the other registers that are candidates for combining in the I/O must have a PRE pin.
- If one of the registers has neither a CLR nor a PRE pin, all the other registers that are candidates for combining must have neither a CLR nor a PRE pin.
- If the CLR or PRE pins are present, they must have the same polarity.
- If the CLR or PRE pins are present, they must be driven by the same signal (net).
- The fan-out between an I/O pin (D, Y, or E) and a register must be equal to 1.
- The register pin connected to the I/O must be the 'D' or 'Q' pin.
- Registers connected to an I/O on the Output and Output Enable pins must have the same clock and enable function.
- Both the Output and Output Enable registers must have an E pin (clock enable) or none at all.
- If the E pins are present, they must have the same polarity. The CLK pins must also have the same polarity. In some cases, you may want registers to be combined with the input of a BIBUF while maintaining the output as is. This can be achieved by using PDC commands as follows:

  ```
  set_io <signal name> -REGISTER yes: register will combine
  ```

  ```
  set_preserve <signal name>: register will not combine
  ```

In libero SoC, users can use the `set_ioff` command for I/O Register Combining.

The `set_ioff` command specifies whether or not a register is combined with an I/O during Synthesis. This command is placed in a Compile Netlist Constraint (*.ndc) file that the Constraint Manager passes to Synthesis as a constraint in the Libero SoC Enhanced Constraint Flow. The syntax is as follows:

```
set_ioff {<portname>}\
        [-in_reg yes|no]\
        [-out_reg yes|no]\
        [-en_reg yes|no]
```

Where:

<portname>: It specifies the name of the I/O port to be combined with a register. The port can be an input, output, or inout port.

-in_reg: It specifies whether the input register is combined into the port <portname>. Valid values are "yes" or "no".

-out_reg: It specifies whether the output register is combined into the port <portname>. Valid values are "yes" or "no".

-en_reg: It specifies whether the enable register is combined into the port <portname>. Valid values are "yes" or "no".

The Netlist Attributes tab allows you to manage netlist attribute constraints to optimize your design during the synthesis and/or compile process.

1. Go to Constraint Manager – > Netlist Attributes tab
2. Available operations are as follows:
- New: It creates a new FDC or NDC netlist attribute constraints file in the <Project_location>\constraint folder.
- Import: It imports an existing FDC or NDC netlist attribute constraints file into the Libero SoC project. The FDC or NDC netlist attribute constraints file is copied into the <Project_location>\constraint folder.
- Link: It creates a link in the project's constraint folder to an existing FDC or NDC netlist attribute constraints file (located and maintained outside of the Libero SoC project).
- Check: It checks the legality of the FDC and NDC file(s) associated with the Synthesis or Compile tools.

Figure 23 • **Netlist Attributes**

3.8 Failsafe Mode for Differential Receivers

The RTG4 MSIO/MSIOD buffers support the failsafe mode for differential receivers to remain in a known and safe state. The failsafe mode is used when the input pins are not driven externally. An ideal use case of the failsafe mode is at power-up in a system where the driving chip may be powered after the receiving chip. When an external differential driver is not powered and is in a high-Z state, the inputs to the receiving chip can float causing uncontrolled oscillations at the receiver.

The RTG4 failsafe mode is implemented using a 100Ω differential termination (ODT) and a weak pull-up or pull-down on the PAD as shown in Figure 24, page 37. RTG4 differential receiver pins can be configured for the failsafe mode by doing the following:

- Enabling differential termination across a differential input pair.
- Using the weak pull-up/pull-down modes on the required input pair.
    - A weak pull-up is enabled on the True PAD.
    - A weak pull-down is enabled on the Complement PAD.

Note: Pull-up and pull-down can be swapped between the True and Complement PADs.

Note: LVDS33 cannot implement the failsafe circuitry.

Note: The SerDes Rx Inputs and SerDes reference clock inputs do not include fail-safe circuitry.

Figure 24 • **LVDS Failsafe Mode**
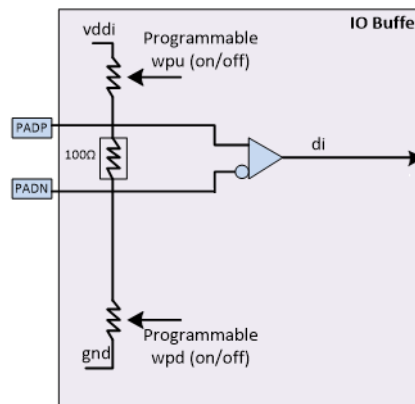
During failsafe, the weak pull-up and weak pull-down are on all the time.
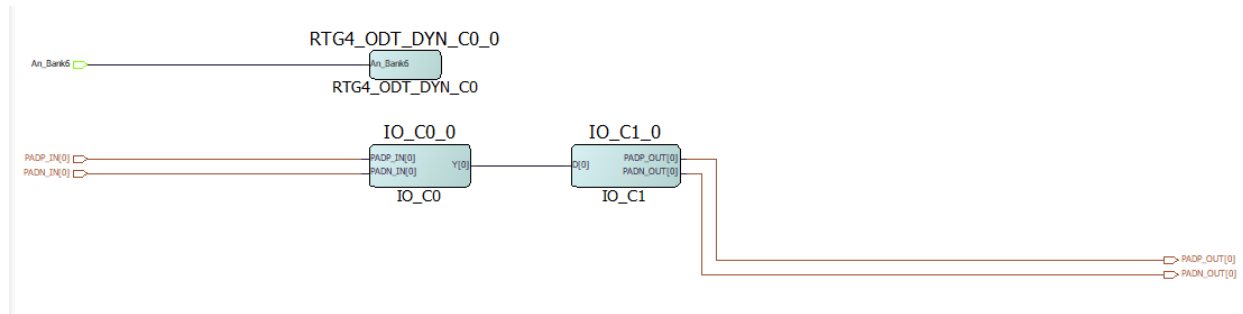
3.8.1 Failsafe LVDS using Dynamic ODT

- The receiver is kept in a safe state when implemented using a differential termination across a differential input pair. The termination is disabled when required to support fail-safe allowing the weak pull-up and pull-down to safely protect the pins.
- A per IO bank dynamic, ODT_DYN signal from the fabric is used to enable or disable the differential termination at each pair.
    - When ODT_DYN signal=0, termination is on. When ODT_DYN signal=1, termination is off.
    - ODT_DYNAMIC PDC option for the differential pins using the ODT_DYN signal should be set to ODT_DYNAMIC= OFF
- A programmable bit (ODT_STATIC) is used per IO. Each IO has a PC bit to support or not support the bank signal ODT_DYN.
    - OFF - do not honor the ODT_DYN bank signal. ON - honor the ODT_DYN bank signal.
    - The differential pins requiring failsafe should have ODT_STATIC = ON
- It is required to enable the weak pull modes on the differential pair. A weak pull-up is enabled on the PADP. A weak pull-down is enabled on the PADN.

With failsafe implementation, the weak pull-up and weak pull-down are on all the time. ODT_DYN is used to disable the differential termination when the Pads are not driven externally. The ODT_DYN signal is fabric controlled from user design.

Figure 25 • **ODT Control for Fail-Safe Operation**
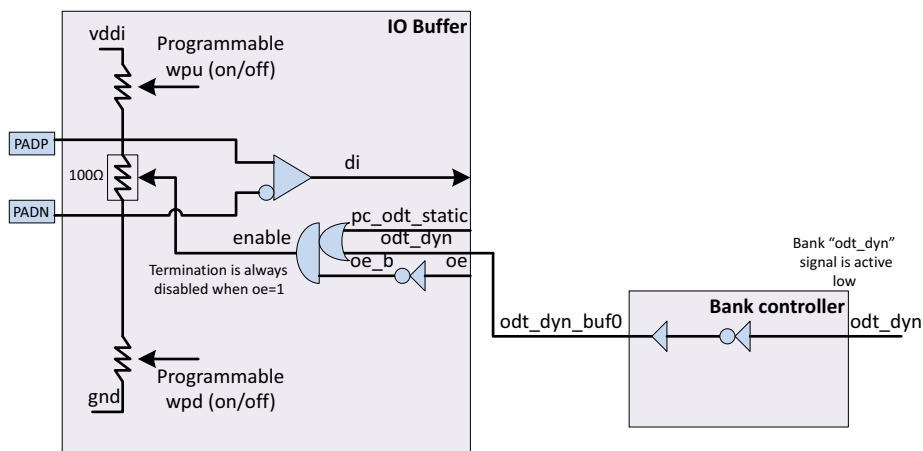
To implement in Libero SoC, the design is required to instantiate a RTG4_ODT_DYN macro for the bank that is hosting the differential receiver as shown in following figure.

Figure 26 • **Simple SmartDesign for Failsafe using Dynamic ODT**

Figure 27 • **IOEditor Example with Failsafe Settings**

Following are the PDC constraints for Failsafe receiver

```
set_io {PADN_IN[0]}    \
     -pinname A5        \
     -fixed yes         \
     -iostd LVDS        \
     -ODT_STATIC On     \
     -RES_PULL Up       \
     -DIRECTION INPUT


set_io {PADP_IN[0]}    \
     -pinname A4        \
     -fixed yes         \
     -iostd LVDS        \
     -ODT_STATIC On     \
     -RES_PULL Up       \
     -DIRECTION INPUT
```

Note: There is a known issue only in the IO Editor and the pin report. It is specific to a software limitation where different values cannot be entered for the P and N sides. Currently, both must have the same value.

Libero does program the P and N side correctly,

• If the RES_PULL is Up on both PADP and PADN, it means the N side is program as Down.
• If the RES_PULL is Down on both PADP and PADN, it means the N side is program as Up.

RTG4 SerDes receivers and SerDes reference clock inputs do not support internal fail-safe circuitry. Microchip does not have any recommended external failsafe terminations. Unused SerDes receivers can be powered-off through the SerDes control registers when not in use.