# Challenges of Designing a Radiation Tolerant Motion Control System on Chip

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## Abstract

Complex motion control systems encompass power drive electronics, sensor electronics and digital control algorithms. The system functions can be partitioned into several integrated circuits to optimize the IC processes for sets of functions with common characteristics. Applications typically have a degree of commonality that can be exploited to provide versatility for a given chip set. Versatility is also facilitated in the IP blocks developed for the control algorithm. Radiation tolerance is achieved by process choices and radiation tolerance by design. Radiation testing includes total ionizing dose, enhanced low dose radiation sensitivity, and single event effects.

## I. INTRODUCTION

The system design challenges involve conceptualizing a versatile part to support a wide range of motion control applications. The design challenges for developing a radiation tolerant motion controller involve partitioning the circuit into realizable functions that can be implemented within the limitations of the intended power and voltage rating of the IC process used for a particular block. The challenge for the process engineer is finding or developing a radiation tolerant IC process technology that can effectively implement the blocks. The circuit design of the motion control circuit blocks are challenging given the ground differences and level shifting required implementing some analogue functions. The circuit design task is complicated even more due to the unavailability of certain generally available devices that can't be used due to their radiation intolerance; this presents a challenge for the circuit designer to find innovative techniques to work around these limitations. Digital code must be written for the controller to implement the necessary algorithms and proven on the test bench. Finally the test engineer must prove functionality of the part over the environmental extremes as well as under radiation exposure.

Table 1: Challenges for Motion Control System Implementation

- System definition and specification
- Design partitioning
- Process development and characterization
- Circuit Design
- Package Design or selection
- Digital IP block development
- Functional testing
- Radiation testing

## II. DISCUSSION

System definition begins by analyzing the applications and their requirements. In a motion control system there is typically an electric motor that provides the electric to mechanical energy conversion and position feedback to monitor the progress of the movement. Motors are typically three phase and either brushless DC (BLDC) motors or stepper motors. [1] Motor drive currents vary depending on the motor size and torque it delivers. Motors are typically powered from the satellite bus power rail which can range from 22V to 150V, and may have a ground potential difference to the isolated control electronics. The motor shaft movement can be monitored using an encoder, hall-effect sensors or a resolver. Resolvers are also used to monitor rotation of structures such as antennas. If movement is linear as results from an actuator, a Linear Variable Differential Transformer (or LVDT) may be used. Since the position information is often used in a motion control system, it was decided to integrate a generic position sensing interface with a high power switch driver. In the LX7720, the motor driving switches are external and so can be optimized for the voltage and current requirements of the motor.
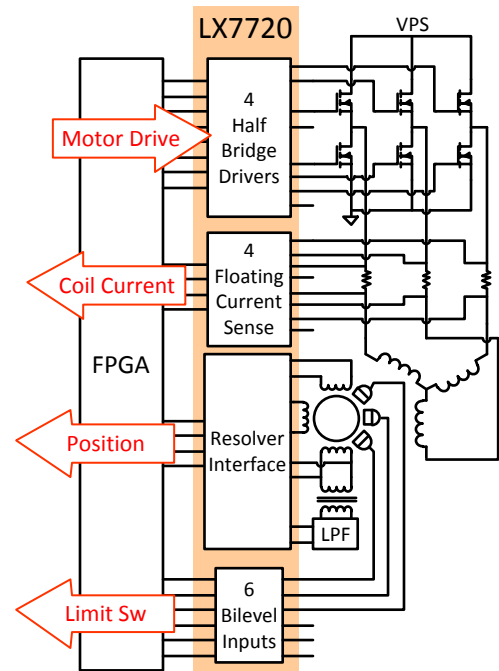


Figure 1: Block diagram of Motor Control System

The first step in partitioning a versatile design approach is to look for the common elements in all the different

applications. BLDC motors require some type of switching device to sequence and regulate current to the motor coils, many applications require a pulse width modulated switch in a half bridge configuration. Stepper motors may use a high side, a low side or a half bridge driver and in cases of a bipolar stepper motor requires two full bridge outputs. See Figure 2.
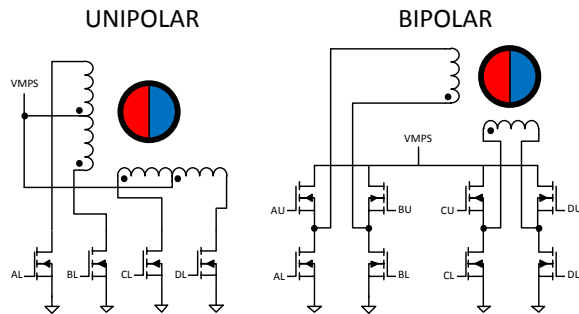


Figure 2: Two phase stepper motor configurations

When designing a half bridge driver, it's common knowledge that an N channel MOSFET is typically better performing as a switch than an equivalently sized P channel MOSFET; therefore a size and cost efficient system will utilize all NMOS power switches and floating high side drivers. All closed loop motor control algorithms require current sensing since the motor torque is proportional to the coil current; a versatile system design will provide floating current sensing that can be configured as power line (high side) sensing, ground current sensing and motor terminal (in-line) current sensing. Figure 3 shows current sensing that is referenced to the switched node of a half-bridge configuration; this presents the challenge of extracting a tiny current sense voltage from a large common mode voltage signal and extremely fast common mode slew rate.
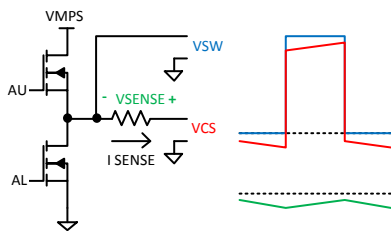


Figure 3: In-line current sense on switch node

Position sensors such as resolvers or LVDTs consist of a transformer primary driven by an exciter reference as shown in Figure 4. The transformer secondary must be sampled to extract the position information. A closed loop system known as tracking conversion can compensate for a known latency based on the acceleration, speed and position errors.
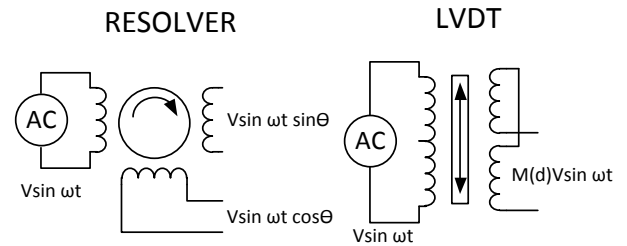


Figure 4: Resolver and LVDT

The algorithms used to control a Permanent Magnet Synchronous Motor (PMSM) are much different than what is required to control a stepper motor; a versatile system has programmable logic to adapt to the application. A versatile system with consideration for all the fore mentioned attributes is shown in Figure 1. [2]

The motion control electronics can be partitioned into three specific IC process requirements. Since motors in spacecraft can operate from voltage rails up to 150V, a process that can withstand these higher voltages is required. Also since the MOSFET drivers typically require high currents, a DMOS process is the most effective. For the signal processing and logic for the sigma delta modulator, a lower voltage process with higher density and greater bandwidth is needed. For the FPGA, a very small geometry CMOS process is required.

Processes that are adopted from commercial processes that were not specifically designed for use under radiation exposure require the development of special Process Design Kit models that take into account the effects of radiation exposure. [3] This involves exposing the devices to radiation and modeling their behavior. Later, when simulations are performed before and after radiation exposure simulations are conducted. When circuit designer uses these PDK models to design circuitry this takes into account the anticipated radiation effects and helps make the resulting circuit topologies radiation tolerant by design.

An example of a function that is partitioned between the three different ICs in this system is the floating current sense as shown in Figure 5. The floating current sense uses the wide dynamic range of the high voltage IC to interface to the current sense resistor. There is an initial gain stage implemented in the high voltage process that feeds its output to an instrumentation amplifier implemented in the 5V process. The 5V IC shares the same signal ground with the FPGA. Once level shifted from floating high voltage to a signal ground referenced, the analog signal is sampled using a second order sigma delta modulator implemented in the BiCMOS process. The lower voltage process can implement functions in less space and at higher bandwidth due to the attributes of its smaller geometry. The output of the modulator is "ones density" data stream that is voltage compatible with the FPGA. The data stream consumes just one package pin as it is routed between the analog front end (AFE) and the FPGA.
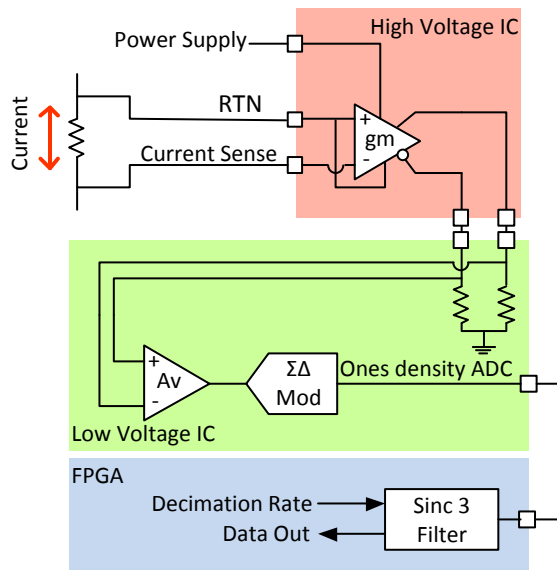
Figure 5: Floating current sense design

In the FPGA a specialized IP block performs a sinc3 filter and decimation function. In the FPGA this can be done at a speed that could not be supported in the AFE 5V process. This pipeline from sense resistor to FPGA control loop takes full advantage of the unique capabilities of each of the ICs it passes through. The high voltage and low voltage analog silicon chips can be co-packaged as a device that appears from the pins out to be a single IC even though it contains two chips. Figure 6 shows that a technique of wire bonding between the chips has been demonstrated successfully in production. This co-packaging of chips exploits the advantages of each process.
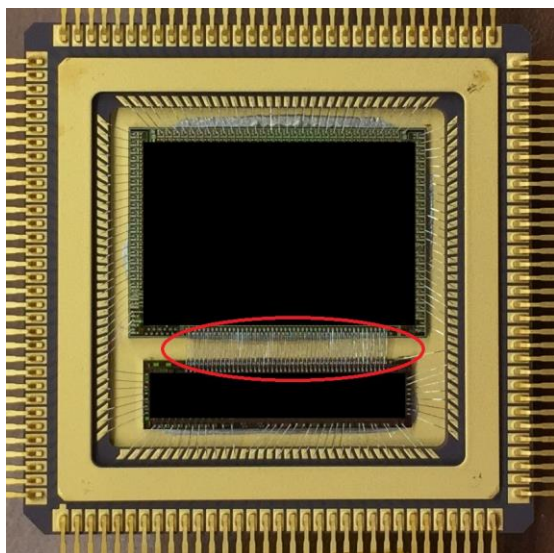


Figure 6: Interconnection between two co-package die

The use of a radiation tolerant FPGA alongside a versatile analog front end as its companion chip is the essence of our "System Manager" total system approach. The digital signal processing of the motor control function can be partitioned into functional blocks to provide the greatest level of IP reuse. Figure 7 is a block diagram of existing motor control IP blocks for a three phase BLDC motor that were developed for the SmartFusion2 fabric with the addition (in red) of new blocks that provide an interface to the sigma delta modulator outputs of the LX7720 sensor interface and the fault monitoring pins unique to the LX7720. An FPGA, such as RTG4, which includes math blocks, is recommended for this implementation.
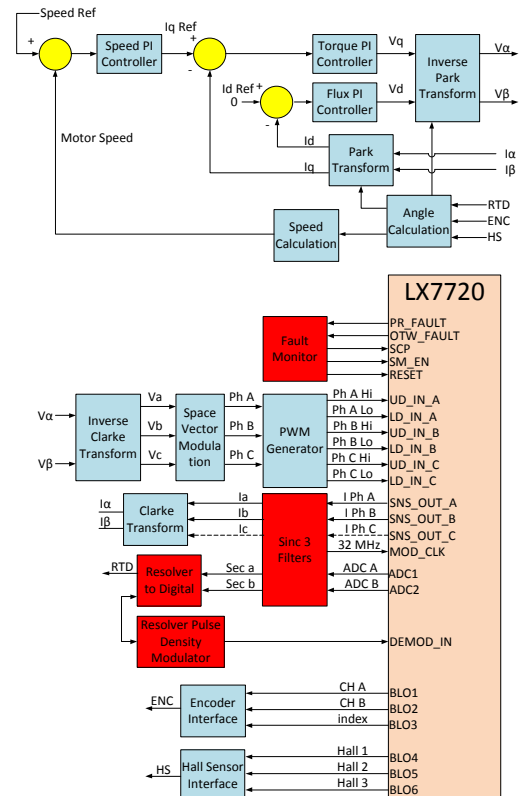


Figure 7: PMSM IP blocks using LX7720

Functions can be added or removed to an application depending on what type of control algorithm is needed. Individual blocks can be customized by setting variables. An example of a variable that controls a performance tradeoff is decimation rate setting in the sinc3 filter IP block; signals with a higher oversample rate will have higher resolution at the cost tradeoff of longer latency [4]. See Figure 8. A CAD design tool such as Libero SoC allows blocks to be configured and customized.
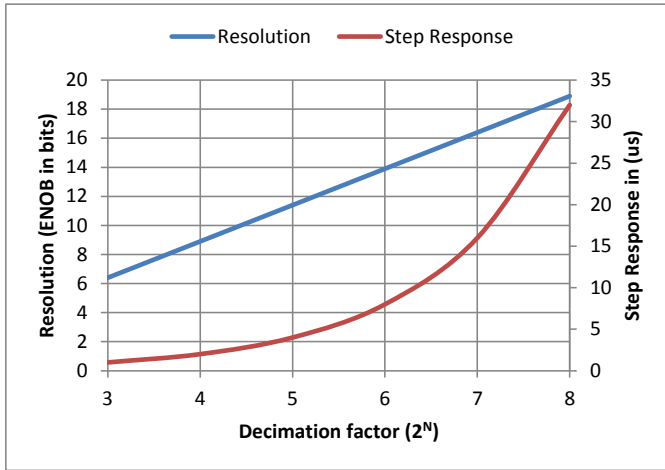
Figure 8: Decimation Trade-offs on Latency and Resolution

Table 2 shows the design flow we've used for developing the new IP blocks involves specification of the inputs and outputs of the required function. Next a top down system design of the required function, followed by a bottom up development of a working mathematical model; we used Matlab Simulink to design, simulate and fine tune our conceptual design. The next step was to generate the HDL code for our functional block; this can be generated from Simulink or coded separately. The HDL code can then be imported into Libero SOC Smart Design where it can be integrated with the existing IP blocks to create the total device model. After this point, the design is system tested with hardware and compared with Matlab results. The overall performance of the hardware is verified to meet the specifications.

Table 2: Design Flow for IP Block Development

- Determine block inputs and outputs
- Specify system requirements
- Develop system mathematical model
- Generate HDL code
- Create hierarchal block
- Simulate at top level
- Test on the hardware

An example of this IP development procedure is demonstrated with the procedure is the development of the resolver and demodulator. An example of the Matlab model is shown in Figure 9. The blocks within the model can be drilled down to the actual algorithm implementation. The Simulink output shows the shaft angle in radians vs. time for a spinning resolver. The implementation of the IP block in Smart Design shows the inputs and outputs as well as variables.
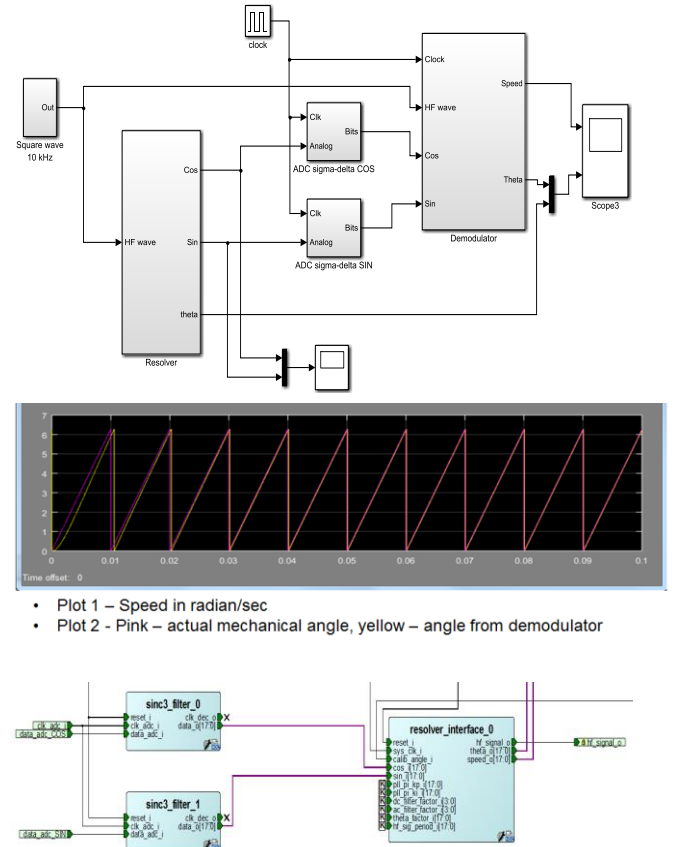


- Plot 1 – Speed in radian/sec
- Plot 2 - Pink – actual mechanical angle, yellow – angle from demodulator



Figure 9: Development of Resolver to digital IP Blocks

Radiation tolerance for this design will be demonstrated by testing for TID to100krad total ionizing dose at approximately 50 rad/sec, ELDRs to 50krad using an enhanced low dose rate of 0.0035 rads/sec and (SEE) single event effects using a fluence of $1 \times 10^8$ parts/cm and linear energy transfer of approximately 85 MeV/mg-cm$^2$. [5] [6] Single event latchup (SEL) is measured with the power supply rails adjusted to their maximum voltage levels. Single Event Transients (SET) tests monitor supply rail input currents and regulated output voltages. We also monitor the sensor modulated outputs and driver outputs for glitches and excursions. Cold spared vulnerability to SET is tested with the power rail removed. For Single Event Upset (SEU) we run a scan chain test routine that cyclically monitors the integrity of the latched data. Single Event Functional Interrupts (SEFI) can occur on Power on Reset or UVLO lines that could initiate and erroneous reset. A typical radiation test set up is shown in Figure 10.
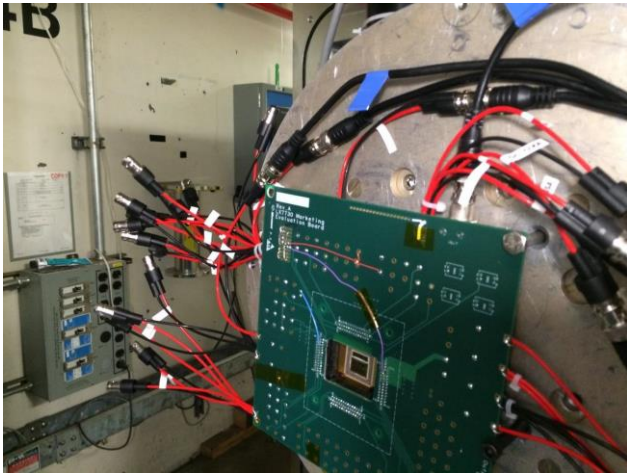
Figure 10:    LX7730 in the SEU test set up at UC Berkeley

## III. SUMMARY

The development of a radiation tolerant motion control analog front end proposed many challenges for the mixed signal design team at Microsemi. The analog front end was partitioned into two chips, a high voltage BCD process and a low voltage BiCMOS process to take advantage of the different process attributes. The designs were performed using proprietary design guidelines and simulated using proprietary Process Design Kits. Both chips were co-packaged in a 132 lead ceramic quad flat pack with interconnecting bond wires between the dies. New IP blocks were added to the motor control IP library to provide a resolver interface. The parts will undergo radiation tolerance testing for TID, ELDRs and SEE.

## IV. REFERENCES

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[2]  LX7720, Rad Hard Spacecraft Power Driver with Rotation and Position Sensing, Datasheet, Microsemi (available on request)
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