IGLOO® and ProASIC®3 FPGAs

Low-Density FPGAs for CPLD-Based Applications

More Capabilities in Low-Density Devices

Instant-On

Lowest Power

Flash Security

Exceptional Reliability

Microsemi
Power Matters.™

Feature-Rich, Low-Density IGLOO and ProASIC3 FPGAs

Microsemi's IGLOO and ProASIC3 FPGA families address a broad range of CPLD requirements for various markets such as consumer, industrial, communications, gaming, defense, and medical applications. These devices provide a breakthrough in performance and features for applications that are constrained by cost, area, and power. All devices are available in commercial and industrial temperatures; some are also available in an automotive-qualified version and with specialized screening for military systems.

Superior Capabilities for Lower Total Cost of Ownership

- Instant-On—No boot PROM or flash MCU required to load configuration
- Lowest Power—Low static power, no in-rush current, no configuration current
- Flash Security—FlashLock and 128-bit AES, secure your designs from theft, tampering, and cloning
- Cost-optimized Packages—Including chip scale and QFP (3×3, 4×4, 5×5, 6×6, and so on)
- Exceptional Reliability—SEU immune or zero FIT rate FPGA configuration
- Product Longevity—Support for over 20 years


Communications


Industrial


Defense


Medical

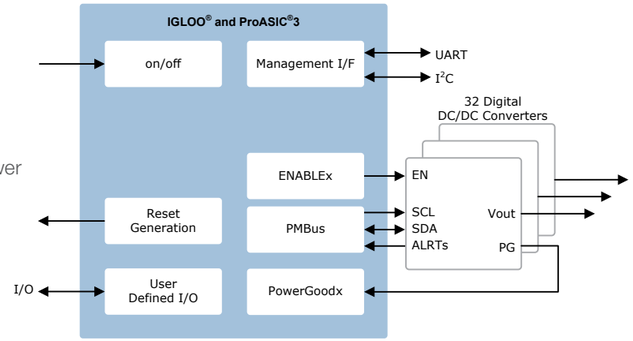

Automotive

General Purpose Solutions

Microsemi's IGLOO and ProASIC3 FPGAs integrate more capabilities in low-density devices, providing an ideal solution for CPLD implementations.

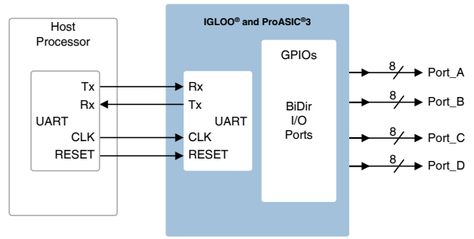
Power Sequencing

- Provides power sequencing for a system, or for any multiple-supply device
- Stores power sequencing data in internal FlashROM
- Generates enable signals upon power-up for the power regulators
- Reference design available for PMBus



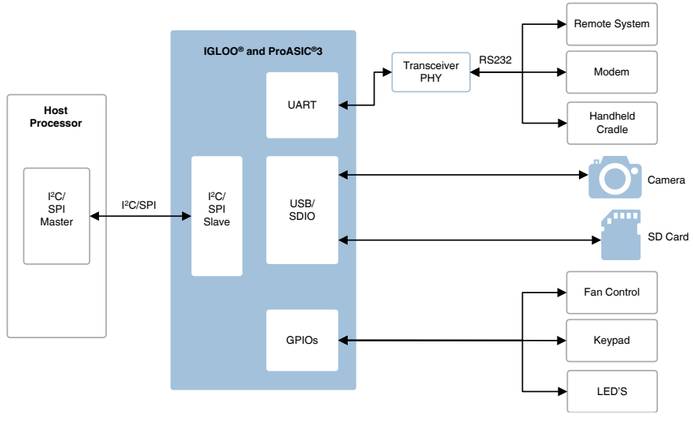
I/O Expansion

- Cost-effectively increases the quantity of I/O pins on ASSP or MCUs
- Easily configures different I/O banks working at different voltage levels
- Flexibly customizes I/O for various standards



Protocol Bridging

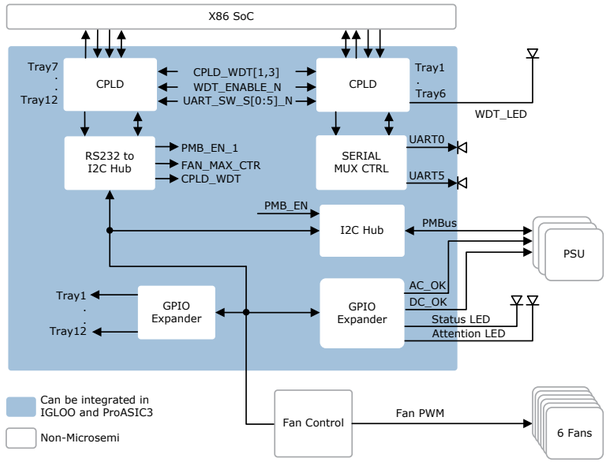
- Supports multi-protocol, multi-I/O standards
- Transfers data across protocols
- Easily converts proprietary to industry-standard bus and serial-to-parallel or parallel-to-serial



General Purpose Solutions (continued)

Chassis Management

- Implements I/O expansion, protocol bridging and muxing, reset and LED management, and glue logic with lowest power consumption
- Provides BOM-cost reduction through integration of CPLDs, RS232 to I²C, Serial Mux Ctrl, I²C Hub, and GPIO expander
- Enables transfer of data across multiple protocols (including UART, I²C, SPI, I²S, and PMBus)
- Provides flexibility and programmability, enabling simple software and hardware design

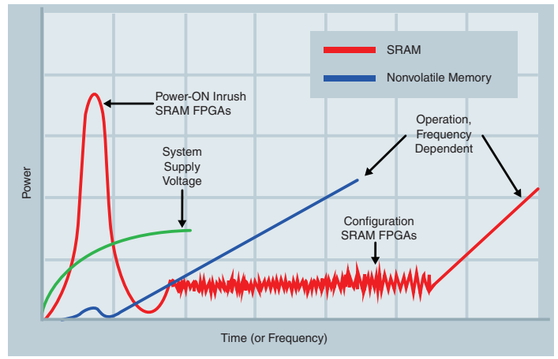


Microsemi IGLOO and ProASIC3 Advantages

Microsemi's IGLOO and ProASIC3 FPGAs bring clear, differentiated advantages to CPLD-based applications by reducing power consumption, simplifying design, reducing cost, and increasing reliability.

Lowest Power Design

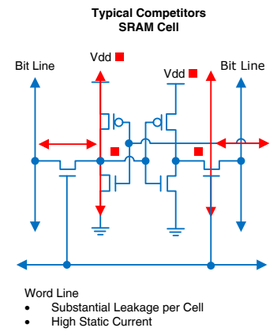
Demand for low-power designs is growing rapidly. SRAM FPGAs power up in an unconfigured state and need to complete the initial power up and reset sequence. A current surge is thus created, resulting in an in-rush power. To mitigate this current spike, many SRAM FPGAs add complex power sequencing requirements to the system. IGLOO and ProASIC3 FPGAs, on the other hand, are non-volatile and do not need external configuration devices for re-programmability. The core cells enter a defined state immediately to minimize power-up switching and deliver the lowest power without sacrificing performance

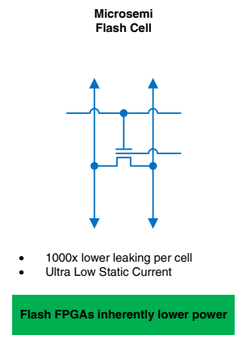


IGLOO and ProASIC FPGAs use a single cell to form an interconnect, resulting in lower current leakage and power consumption (unlike SRAM cells, which are typically built using six transistors). IGLOO and ProASIC3 FPGAs come with Flash*Freeze mode, which enables power as low as 2 µW with no additional components required to turn off I/Os or clocks while preserving the design information, SRAM content, and registers. I/Os can maintain their state during Flash*Freeze mode. Entering and exiting Flash*Freeze mode takes less than 1 µs. Additionally, the Low-Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO device is completely functional in the system, maintaining I/Os, SRAM, registers, and logic functions. This allows the IGLOO device to control the system power management based on external inputs while consuming minimal power

Advantages of Low-Power Design

- No high in-rush current or battery-sapping configuration current each time the system is powered up
- Dramatically extends battery life relative to SRAM and hybrid PLD alternatives
- Full-featured devices including clock conditioning analog PLLs, on-chip SRAM, and non-volatile user memory storage, all of which help eliminate parts and reduce total system power consumption and cost



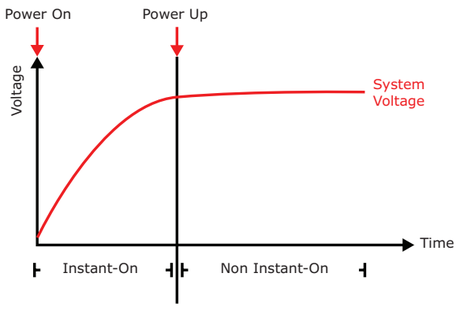


Microsemi IGLOO and ProASIC3 Advantages (continued)

Instant-On

The time it takes for your FPGA to power-up has a significant impact on the complexity of your system design and the total cost of your system. Some applications require instant system initialization and cannot wait for device configuration on power-up. Some examples of such applications are medical applications performing critical operations such as life assistance systems, battery operated portable applications, automotive engine start-up control, and military applications such as missile startup controls.

Microsemi IGLOO and ProASIC3 FPGAs support instant-on functionality and can assist in system startup tasks, system configuration, and supervision during voltage ramp up to eliminate the need for additional instant-on circuitry.



Advantages of Instant-On

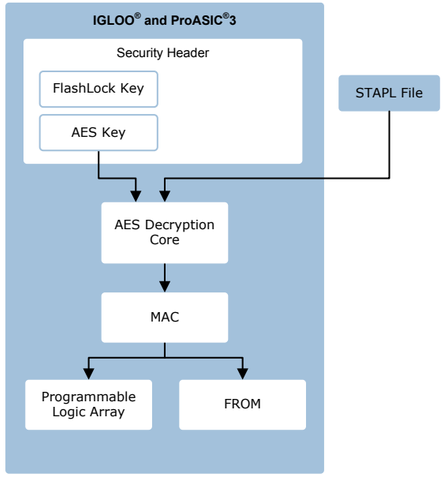
- Operational before power-up
- Provides best-in-class power-up time of less than 50 µs
- Enables short system initialization time
- Reduces number of components required for system power-up
- Reduces total cost of ownership

FlashLock Security

Poor design security can expose you not only to the theft of intellectual property and loss of revenue, but also to brand defamation, liability, and risk of product tampering.

IGLOO and ProASIC3 devices protect configuration data by on-chip security—FlashLock. This feature also offers the option of permanently locking the device, rendering all device readback impossible.

IGLOO and ProASIC3 devices also support encryption of the configuration bitstream using a 128-bit AES cipher. This encrypted bitstream is then deciphered by an on-chip engine, providing the highest level of security for upgradeable systems.



Advantages of FlashLock Security

- No exposed bitstream at power-up
- Supports secure updates over public networks using 128-bit AES encryption
- FlashLock converts the devices to one-time-programmable (OTP) devices

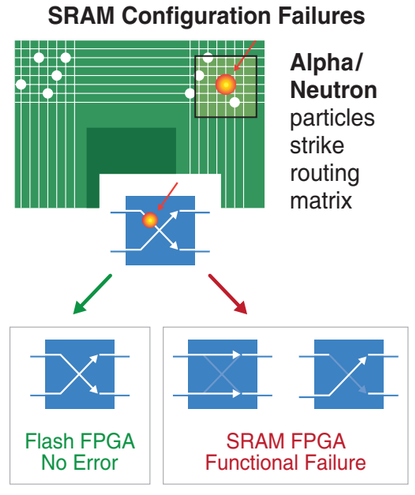
Microsemi IGLOO and ProASIC3 Advantages

Exceptional Reliability

Malfunctions in integrated circuits due to radiation from high-energy neutrons or alpha particles at ground level are a major concern, especially for life-critical and safety-critical applications such as aviation, industrial automation, medical devices, and automotive electronics.

Neutrons and alpha particles cause configuration and data upsets in SRAM-based FPGA configuration elements. This phenomenon is called single event upset (SEU) or firm error.

Microsemi IGLOO and ProASIC FPGAs reduce overall system cost because they are not susceptible to configuration loss due to SEU caused by alpha or neutron radiation, and require no event error mitigation techniques for configuration upsets.



Configuration Advantages

- No mitigation techniques for configuration upsets required
- IGLOO/ProASIC3s maintain system integrity at high altitudes and sea level

Advanced I/O Standards and Wide Range of Support

The flexible I/O structure of the IGLOO and ProASIC3 FPGAs supports wide range I/O operation from 1.2 V to 3.3 V, as well as:

- Single-ended I/O standards such as LVTTL, LVCMOS, and PCI
- Differential I/O standards such as LVPECL and LVDS
- Voltage-referenced standards including HSTL, SSTL2, SSTL3, GTL, and GTL+

Advantages of I/O Structure

- Wider I/O range reduces BOM cost by eliminating the need to include power supplies or power conditioning components on the board
- Wide range eases I/O bank management and provides enhanced protection from system voltage spikes
- Offers hot-swappable and cold sparing support

Microsemi IGLOO and ProASIC3 Feature Summary

	Cortex-M1 Support	VersaTiles	I/Os	Core Voltages (V)	System Performance (MHz)	I/O Voltages (V)	Quiescent Current (Typical; µA)	Typical Static Power (µW)	Power Modes	Packages	Temperature Grade
IGLOO nano		260–6.1K	23–71	1.2–1.5	160–250	1.2–3.3	2–16	2	Flash*Freeze	µCS, CS, QFN, QFP	C, I
IGLOO/e	Yes	768–75.3K	34–620	1.2–1.5	160–250	1.2–3.3	5–137	5	Flash*Freeze	µCS,CS, FBGA, QFN, QFP	C, I
IGLOO Plus		792–3.1K	120–212	1.2–1.5	160–250	1.2–3.3	2–16	5	Flash*Freeze	CS, QFP	C, I
ProASIC3 nano		260–6.1K	34–71	1.5	350	1.5–3.3	0.9–3.3	900	Sleep	QFN, QFP	C, I
ProASIC3/e	Yes	768–75.3K	34–620	1.5	350	1.5–3.3	3–37.5	3000	Sleep	FBGA, CS, QFN, QFP	C, I, T, M
ProASIC3L	Yes	6.1K–75.3K	68–620	1.2–1.5	250–350	1.2–3.3	0.9–3.3	400	Flash*Freeze	FBGA, QFP	C, I, M

C= Commercial
I= Industrial
T= Automotive
M= Military

	IGLOO Series Lowest-Power FPGAs			ProASIC3 Series Low-Power FPGAs		
	IGLOO nano	IGLOO/e	IGLOO Plus	ProASIC3 nano	ProASIC3/E	ProASIC3L
Overview	Industry's lowest power and smallest size solution.	Ultra-low-power and programmable solution.	Low-power FPGA with enhanced I/O capabilities.	Lowest-cost solution with enhanced I/O capabilities.	Low-power, low-cost FPGA solution	FPGA that balances low–power, performance, and low-cost
Applications	Designed for consumer, industrial, medical, and other high-volume, low-power applications.	Ideal for battery-operated or power-conscious applications, when power and size are key requirements. Provides improved battery runtime or lower operational temperatures.	Addresses the need for compact logic density with high I/O count and capability. Ideal for bridging, I/O expansion, level-shifting, and memory- interfacing applications optimized for low power.	Specifically designed for consumer, industrial, medical, and other high-volume, cost-sensitive applications. Cost-effective replacement for ASICs or ASSPs, delivering faster time-to-market, security, and I/O expansion.	Perfect for designs that require low-cost, low-power, and performance in small, medium, and large logic densities.	Use in applications that require a balance of performance and low-static dynamic power. Targets applications requiring secure, high-density programmable logic.
Low Power Modes	Flash*Freeze technology enables industry-leading micropower consumption while maintaining FPGA content and holding I/O states.	Flash*Freeze technology enables 5 µW static power consumption while maintaining FPGA content.	Flash*Freeze mode preserves FPGA content and holds I/O states while the device consumes lowest power.	Supports Sleep mode for power reduction when device is not used.	Supports Sleep mode for power reduction when device is not used.	Flash*Freeze technology enables quick switching to and from low-power mode to reduce dynamic power when FPGA operation is not required.
Packaging	Largest selection of small-footprint packages, as small as 3 mm × 3 mm.	Small-footprint packages for portable and area-constrained applications, as small as 4 mm × 4 mm.	High I/O count, small-footprint, and low-cost packaging.	Broad selection of small-footprint packages, (routable with 2-layer boards in most cases).	Selected small-footprint and low-cost packages, as well as high-pin-count packages.	Low-cost packages with high pin count.

Microsemi IGLOO Package Summary

	Type	UC36	QN48	QN68	UC81	VQ128	VQ176	CS81	VQ100	CS121	CS196	CS201	CS281	CS289	FG144	FG256	FG484	FG896
	Pitch (mm)	0.4						0.5						0.8	1.0			
	Length × Width (mm)	3 × 3	6 × 6	8 × 8	4 × 4	14 × 14	20 × 20	5 × 5	14 × 14	6 × 6	8 × 8	8 × 8	10 × 10	14 × 14	13 × 13	17 × 17	23 × 23	31 × 31
	Device	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
IGLOO nano	AGLN010	23	34															
	AGLN020			49	52			52										
	AGLN060							60	71									
	AGLN125							60	71									
	AGLN250							60	68									
IGLOO	AGL030		34	49	66			66	77									
	AGL060								71	96								
	AGL125								71	96	133				97			
	AGL250								68		143				97			
	AGL400										143				97	178	194	
	AGL600												215		97	177	235	
	AGL1000												215		97	177	300	
IGLOOE	AGLE600															165	270	
	AGLE3000																341	620
IGLOO Plus	AGLP030					101						120		120				
	AGLP060						137					157		157				
	AGLP125												212	212				

Microsemi ProASIC3 Package Summary

	Type	QN48	QN68	VQ100	CS121	TQ144	PQ208	FG144	FG256	FG324	FG484	FG676	FG896
	Pitch (mm)	0.4		0.5				1.0					
	Length × Width (mm)	6 × 6	8 × 8	14 × 14	6 × 6	20 × 20	28 × 28	13 × 13	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
	Device	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
ProASIC3 nano	A3PN010	34											
	A3PN020		49										
	A3PN060			71									
	A3PN125			71									
	A3PN250			68									
ProASIC3	A3P030	34	49	77									
	A3P060			71	96	91		96					
	A3P125			71		100	133	97					
	A3P250			68			151	97	157				
	A3P400						151	97	178		194		
	A3P600						154	97	177		235		
	A3P1000						154	97	177		300		
ProASIC3 E	A3PE600						147		165		270		
	A3PE1500						147				280	444	
	A3PE3000						147			221	341		620
ProASIC3L	A3P250L			68			151	97	157				
	A3P600L						154	97	177		235		
	A3P1000L						154	97	177		300		
	A3PE3000L						147			221	341		620

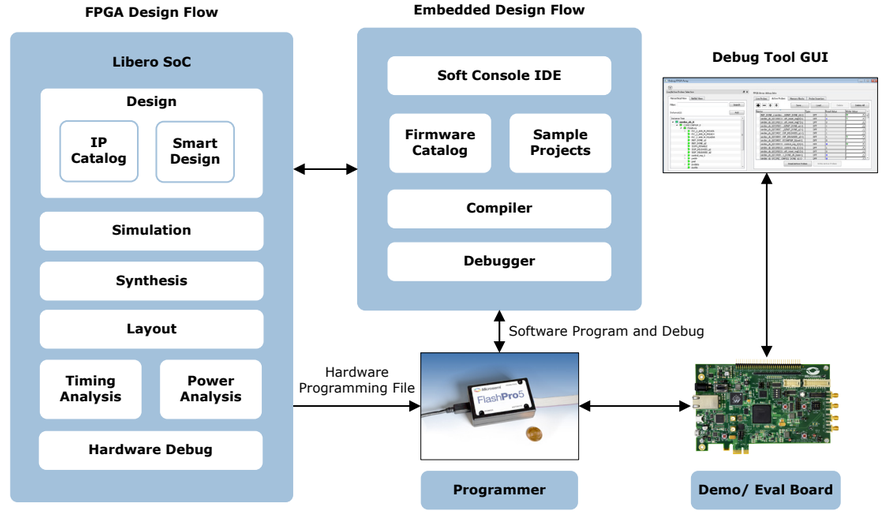
Microsemi IGLOO and ProASIC Software Tools and Evaluation Boards

The Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with Microsemi's power-efficient flash-based IGLOO and ProASIC3 devices. The suite integrates industry standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming, and push button design flow.

This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt single-click synthesis to programming flow integrates industry-standard third-party tools, a rich IP library of DirectCores and CompanionCores, and supports complete reference designs and development kits.

Libero SoC is available for IGLOO and ProASIC3 devices through the free silver license.

Download your free tool at:
http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#licensing



Kits	Part Number	Price
IGLOO nano starter kit	AGLN-NANO-KIT	$99
IGLOO PLUS starter kit	AGLP-EVAL-KIT	$299
Cortex-M1-enabled IGLOO development kit	M1AGL1000-DEV-KIT	$600
ProASIC3 starter kit	A3PE-STARTER-KIT-2	$580
Cortex-M1-enabled ProASIC3L development kit	M1A3PL-DEV-KIT	$600

For more information about available kits, see:
http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits-boards

Microsemi is continually adding new products to its industry-leading portfolio.

For the most recent updates to our product line and for detailed information and specifications, please call, email, or visit our website.

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