Low-Density FPGAs for CPLD-Based Applications

More Capabilities in Low-Density Devices
- Instant-On
- Lowest Power
- Flash Security
- Exceptional Reliability

Microsemi
Power Matters.
Microsemi’s IGLOO and ProASIC3 FPGAs integrate more capabilities in low-density devices, providing an ideal solution for CPLD implementations.

**Power Sequencing**
- Provides power sequencing for a system, or for any multiple-supply device
- Stores power sequencing data in internal FlashROM
- Generates enable signals upon power-up for the power regulators
- Reference design available for PMBus

**I/O Expansion**
- Cost-effectively increases the quantity of I/O pins on ASSP or MCUs
- Easily configures different I/O banks working at different voltage levels
- Flexibly customizes I/O for various standards

**Protocol Bridging**
- Supports multi-protocol, multi-I/O standards
- Transfers data across protocols
- Easily converts proprietary to industry-standard bus and serial-to-parallel or parallel-to-serial
General Purpose Solutions (continued)

**Microsemi IGLOO and ProASIC3 Advantages**

**Lowest Power Design**

Demand for low-power designs is growing rapidly. SRAM FPGAs power up in an unconfigured state and need to complete the initial power up and reset sequence. A current surge is thus created, resulting in an in-rush power. To mitigate this current spike, many SRAM FPGAs add complex power sequencing requirements to the system. IGLOO and ProASIC3 FPGAs, on the other hand, are non-volatile and do not need external configuration devices for re-programmability. The core cells enter a defined state immediately to minimize power-up switching and deliver the lowest power without sacrificing performance.

IGLOO and ProASIC FPGAs use a single cell to form an interconnect, resulting in lower current leakage and power consumption (unlike SRAM cells, which are typically built using six transistors). IGLOO and ProASIC3 FPGAs come with Flash*Freeze mode, which enables power as low as 2 μW with no additional components required to turn off I/Os or clocks while preserving the design information, SRAM content, and registers. I/Os can maintain their state during Flash*Freeze mode. Entering and exiting Flash*Freeze mode takes less than 1 μs. Additionally, the Low-Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO device is completely functional in the system, maintaining I/Os, SRAM, registers, and logic functions. This allows the IGLOO device to control the system power management based on external inputs while consuming minimal power.

**Advantages of Low-Power Design**

- No high in-rush current or battery-sapping configuration current each time the system is powered up
- Dramatically extends battery life relative to SRAM and hybrid CPLD alternatives
- Full-featured devices including clock conditioning analog PLLs, on-chip SRAM, and non-volatile user memory storage, all of which help eliminate parts and reduce total system power consumption and cost.

**Chassis Management**

- Implements I/O expansion, protocol bridging and muxing, reset and LED management, and glue logic with lowest power consumption
- Provides BOM-cost reduction through integration of CPLDs, RS232 to I²C, Serial Mux Ctrl, I²C Hub, and GPIO expander
- Enables transfer of data across multiple protocols (including UART, PC, SPI, I²S, and PMBus)
- Provides flexibility and programmability, enabling simple software and hardware design
Microsemi IGLOO and ProASIC3 Advantages (continued)

Instant-On

The time it takes for your FPGA to power-up has a significant impact on the complexity of your system design and the total cost of your system. Some applications require instant system initialization and cannot wait for device configuration on power-up. Some examples of such applications are medical applications performing critical operations such as life assistance systems, battery operated portable applications, automotive engine start-up control, and military applications such as missile startup controls.

Microsemi IGLOO and ProASIC3 FPGAs support instant-on functionality and can assist in system startup tasks, system configuration, and supervision during voltage ramp up to eliminate the need for additional instant-on circuitry.

Advantages of Instant-On

- Operational before power-up
- Provides best-in-class power-up time of less than 50 µs
- Enables short system initialization time
- Reduces number of components required for system power-up
- Reduces total cost of ownership

FlashLock Security

Poor design security can expose you not only to the theft of intellectual property and loss of revenue, but also to brand defamation, liability, and risk of product tampering.

IGLOO and ProASIC3 devices protect configuration data by on-chip security—FlashLock. This feature also offers the option of permanently locking the device, rendering all device readback impossible.

IGLOO and ProASIC3 devices also support encryption of the configuration bitstream using a 128-bit AES cipher. This encrypted bitstream is then deciphered by an on-chip engine, providing the highest level of security for upgradeable systems.

Advantages of FlashLock Security

- No exposed bitstream at power-up
- Supports secure updates over public networks using 128-bit AES encryption
- FlashLock converts the devices to one-time-programmable (OTP) devices

Exceptional Reliability

Malfunctions in integrated circuits due to radiation from high-energy neutrons or alpha particles at ground level are a major concern, especially for life-critical and safety-critical applications such as aviation, industrial automation, medical devices, and automotive electronics.

Neutrons and alpha particles cause configuration and data upsets in SRAM-based FPGA configuration elements. This phenomenon is called single event upset (SEU) or firm error.

Microsemi IGLOO and ProASIC FPGAs reduce overall system cost because they are not susceptible to configuration loss due to SEU caused by alpha or neutron radiation, and require no event error mitigation techniques for configuration upsets.

Configuration Advantages

- No mitigation techniques for configuration upsets required
- IGLOO/ProASIC3s maintain system integrity at high altitudes and sea level

Advanced I/O Standards and Wide Range of Support

The flexible I/O structure of the IGLOO and ProASIC3 FPGAs supports wide range I/O operation from 1.2 V to 3.3 V, as well as:

- Single-ended I/O standards such as LVTTL, LVCMOS, and PCI
- Differential I/O standards such as LVPECL and LVDS
- Voltage-referenced standards including HSTL, SSTL2, SSTL3, G1, and G1+

Advantages of I/O Structure

- Wider I/O range reduces BOM cost by eliminating the need to include power supplies or power conditioning components on the board
- Wide range eases I/O bank management and provides enhanced protection from system voltage spikes
- Offers hot-swappable and cold sparing support
## Microsemi IGLOO and ProASIC3 Feature Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>IGLOO nano</th>
<th>IGLOO/e</th>
<th>IGLOO Plus</th>
<th>ProASIC3 nano</th>
<th>ProASIC3/e</th>
<th>ProASIC3L</th>
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<tbody>
<tr>
<td>Core</td>
<td>1.2–1.5</td>
<td>1.2–1.5</td>
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<td>Voltage (V)</td>
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<td>160–250</td>
<td>150</td>
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<tr>
<td>System Performance (MHz)</td>
<td>2–16</td>
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<td>3–37.5</td>
<td>3–37.5</td>
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<td>Quiescent Current (Typical, µA)</td>
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<td>900</td>
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<td>Typical Static Power (µW)</td>
<td>Flash/Freeze</td>
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<td>Power Modes</td>
<td>µCS, CS, QFN, QFP</td>
<td>µCS, CS, QFN, QFP</td>
<td>CS, QFP</td>
<td>CS, QFP</td>
<td>CS, QFP</td>
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<tr>
<td>Temperature Grade</td>
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</table>

### IGLOO Series Lowest-Power FPGAs

- **IGLOO nano**: Ultra-low-power and programmable solution. Lowest-cost solution with enhanced I/O capabilities. Supports Sleep mode to reduce dynamic power when device is not used.
- **IGLOO/e**: Ideal for industrial, medical, and high-volume, low-power applications. Addresses the need for high-speed, high-density FPGA content and holding I/O states.
- **IGLOO Plus**: Supports Sleep mode for power reduction when device is not used.
- **ProASIC3 nano**: For applications requiring secure, high-density, and low-cost logic.
- **ProASIC3/e**: Perfect for designs that require low-cost, low-power, and performance in small, medium, and large logic densities.
- **ProASIC3L**: Ultra-low-power, low-cost FPGA that balances low-power performance and low-cost FPGA content.

### Applications

- **Industries**: Industrial/medical and automotive. 
- **Applications**: Ultra-low-power and programmable solution, ideal for battery-operated devices and industrial/medical applications.

### Low Power Modes

- **Flash/Freeze technology**: Enables industry-leading micropower consumption while maintaining FPGA content and holding I/O states.
- **Sleep mode**: Supports Sleep mode for power reduction when device is not used.

### Packaging

- **Small footprint packages**: As small as 3 mm x 3 mm. 
- **Large footprint packages**: As small as 6 mm x 6 mm.

## Microsemi IGLOO Package Summary

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<tr>
<th>Type</th>
<th>UC36</th>
<th>QH36</th>
<th>CN88</th>
<th>UC91</th>
<th>VQ236</th>
<th>VQ178</th>
<th>CS81</th>
<th>VQ100</th>
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<th>CS196</th>
<th>CS281</th>
<th>CS289</th>
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<td>Length x Width (mm)</td>
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<td>8 x 8</td>
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<td>14 x 14</td>
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The Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with Microsemi’s power-efficient flash-based IGLOO and ProASIC3 devices. The suite integrates industry standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming, and push button design flow.

This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt single-click synthesis to programming flow integrates industry-standard third-party tools, a rich IP library of DirectCores and CompanionCores, and supports complete reference designs and development kits.

Libero SoC is available for IGLOO and ProASIC3 devices through the free silver license.

Download your free tool at: [http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#licensing](http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#licensing)

For more information about available kits, see: [http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits-boards](http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits-boards)
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