UG0733
User Guide
Sinc3 Filter v4.2

a MICROCHIP company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.1

The following is a list of changes done in revision 2.1 of this document.

- Figure 1, page 3 - Block Diagram of Sinc3 Filter, is edited to replace the input signal hold_i with reg_rst_i.
- Table 1, page 4 - Inputs and Outputs of Sinc3 Filter, is edited to replace the input signal, hold_i with reg_rst_i and its description.

1.2 Revision 2.0

The following is a list of changes done in revision 2.0 of this document.

- Table 2, page 4 - Configuration Parameters, is updated to add the configuration parameters g_BIPOLAR and g_NEGATE_OUTPUT and their descriptions.
- A new equation to calculate the equivalent resolution of the Sinc3 filter output with respect to decimation factor is added in Hardware Implementation, page 3 below Figure 2, page 3.
- Figure 1, page 3 - Block Diagram of Sinc3 Filter, is edited to add the input signal hold_i.
- Table 1, page 4 - Inputs and Outputs of Sinc3 Filter, is edited to add the input signal, hold_i and its description.

1.3 Revision 1.0

Revision 1.0 (Published in September 2016) was the first publication of this document.

2 Introduction

Sinc3 filter is a low-pass filter, which removes all high frequency components above the cutoff frequency without affecting the frequencies below the cutoff frequency. An ideal Sinc3 filter requires an infinite delay. A practical Sinc3 filter has three stages of integration and three stages of differentiation at a decimated clock.

Sinc3 filter is used to:

- De-modulate data from a delta-sigma modulator, which is widely used in delta-sigma type analog-to-digital converter (ADC).
- Convert the serial bitstream from ADC to parallel data.

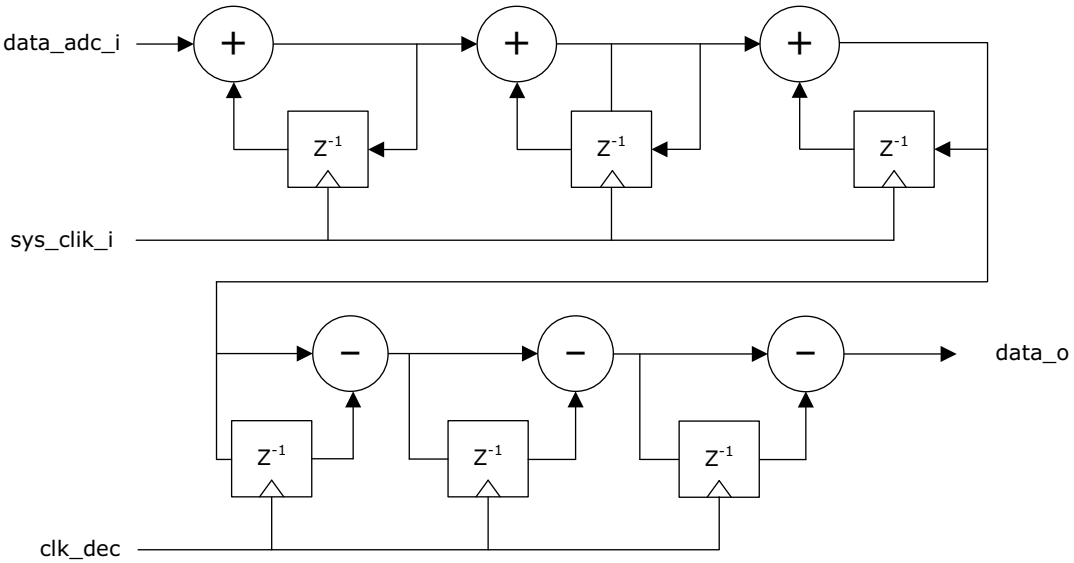
3 Hardware Implementation

The following figure shows the block diagram of Sinc3 filter.

Figure 1 • **Block Diagram of Sinc3 Filter**

The following figure shows the hardware implementation of Sinc3 filter.

Figure 2 • **Hardware Implementation of Sinc3 Filter**



The clk_adc_i signal is the modulator clock from the ADC to the Sinc3 filter. The filter implements three sequential integrations at the rate of clk_adc_i. A decimated clock is generated internally based on configuration parameters as shown in the following equation. The output of the third integrator is differentiated serially three times with respect to decimated clock to generate the output.

$$f_{clk\_dec\_o} = f_{clk\_adc\_i} \times 2^{g\_DECIMATION\_FACTOR}$$

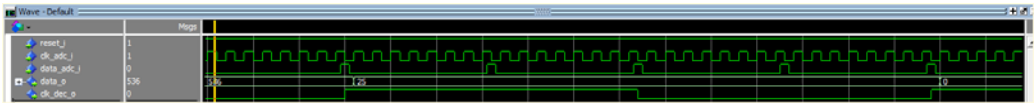
The equivalent resolution of the Sinc3 filter output with respect to decimation factor is represented by the following equation.

$$\text{Equivalent Resolution (in bits)} = (2 \times \text{Decimation Factor})$$

3.1 Timing Diagram

The following figure shows the timing diagram of Sinc3 filter.

Figure 3 • **Timing Diagram of Sinc3 Filter**



3.2 Inputs and Outputs

The following table lists the input and output ports of the Sinc3 filter.

Table 1 • **Inputs and Outputs of Sinc3 Filter**

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design.
clk_adc_i	Input	Modulator clock coming from ADC.
data_adc_i	Input	Data bitstream from the modulator in ADC.
reg_rst_i	Input	When 1, resets all the registers. When 0, filter is normally operated.
clk_dec_o	Output	Decimated clock output. This is the same clock used for differentiator. The output of the filter updates at the rising edge of this output.This signal is not generated when res_rst_i is high.
data_o	Output	Filtered data output.

3.3 Configuration Parameters

The following table lists the configuration parameters used in the hardware implementation of the Sinc3 filter. These are generic parameters that vary according to the application requirements.

Table 2 • **Configuration Parameters**

Name	Description
g_STD_IO_WIDTH	Width of the input and output signals.
g_DECIMATION_FACTOR	Division factor used to generate the decimated clock from the system clock input.
g_BIPOLAR	Select 0 if the ADC is unipolar, Select 1 if ADC is bipolar.
g_NEGATE_OUTPUT	Select 0 if the data at the data_o port should be negated. Select 1 if the data at data_o port should be passed through.

3.4 Resource Utilization

The following table lists the resource utilization of the Sinc3 filter IP implemented on SmartFusion2® and IGLOO2® devices with g_STD_IO_WIDTH_value equal to 18.

Table 3 • **Resource Utilization**

Resource	Usage
Sequential	220
Combinational Logic	160
MACC	0
RAM 1kx18	0
RAM 64x18	0