Introduction

This application note provides detailed layout guidelines for the implementation of a POE PD system, based on Microsemi's PD70210(A) or PD70211 controllers. PD70210(A) is a PD front-end controller, while PD70211 combines PD front-end and PWM.

Applicable DocumentsPD70210(A) datasheet, catalog number DS_PD70210_PD70210A

- PD70211 datasheet, catalog number DS_PD70211
- PD70211EVB51F12_UG evaluation board user guide

Background

Microsemi's PD70210(A) and PD70211 devices are part of PD device family; these devices are targeted for implementing the 802.3at, HDBT, and other 2-pair/4-pair configurations. The PD interface device family includes the following:

Device type	Power capability	Integrates PWM controller
PD70100	IEEE 802.3at Type 1 (IEEE 802.3 af)	No
PD70101	IEEE 802.3at Type 1 (IEEE 802.3 af)	Yes
PD70200	IEEE 802.3at Type 2	No
PD70211	IEEE 802.3at Type 2	Yes
PD70210/A	IEEE802.3at Type 2 (2/4 pair) HDBaseT (95W)	No
PD70211	IEEE802.3at Type 2 (2/4 pair) HDBaseT (95W)	Yes

Due to its high power handling, it is very important to follow the guidelines specified in this application note in order to have noise robustness and a solution with good thermal behavior.

PD70210(A) has thermal pad, which should be connected on PCB to VPN_IN pin.

PD70211 is comprised of two dies: PD front-end die like PD70210A and PWM controller die. It also has the thermal pad – pin 37 in the schematics, referenced to PD front-end input and internally connected to VPN_IN pin. Please refer to the datasheet for more information.

All layout recommendations for front section of PD70211 apply to PD70210(A) as well.

Ground planes

PD70211-based systems include a number of "ground" types:

1. VPN_IN

This is the negative rail of the voltage received from the PSE side. It is connected to VPN_OUT through the isolation switch under normal operation. This switch remains ON as long as the input voltage is a valid PSE voltage and there are no faults in downstream DC-DC.

2. Power Ground (PGND)

This is return of DC/DC power circuitry and PWM controller's MOSFETs gate drivers PG and SG. PGND should be connected to VPN_OUT, which is the negative side output of the PD device front end. Ideally, this connection should be done near bulk capacitor Cin.

3. Signal ground (GND)

This is PWM controller's "quiet" ground used for the return path of the low-power control signals.

GND and PGND should be connected together in a single point near controller to eliminate the switching currents affecting the control signals. Usually this connection is done via zero-ohm resistor to separate the nets.

4. Digital ground

In isolated systems, there is also the secondary output (digital) ground of the DC-DC converter. Secondary ground should have 1500 VRMS isolation from all of the above ground types.

5. Earth ground

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This ground may present only in systems with grounded metal enclosure. Earth ground connects to the shells of RJ45 connectors, to common mode filter capacitors, and to mounting screws. This ground should likewise have 1500 VRMS isolation from all primary side grounds (VPN_IN, PGND and GND), but it may be tied to secondary digital ground.

Figure 1 illustrates an implementation of ground planes in PD70211-based flyback converter.

Please note that copper planes for various grounds are just means for low impedance connections. They should not be poured over entire board area and should only cover the areas under the components referenced to the respective grounds.

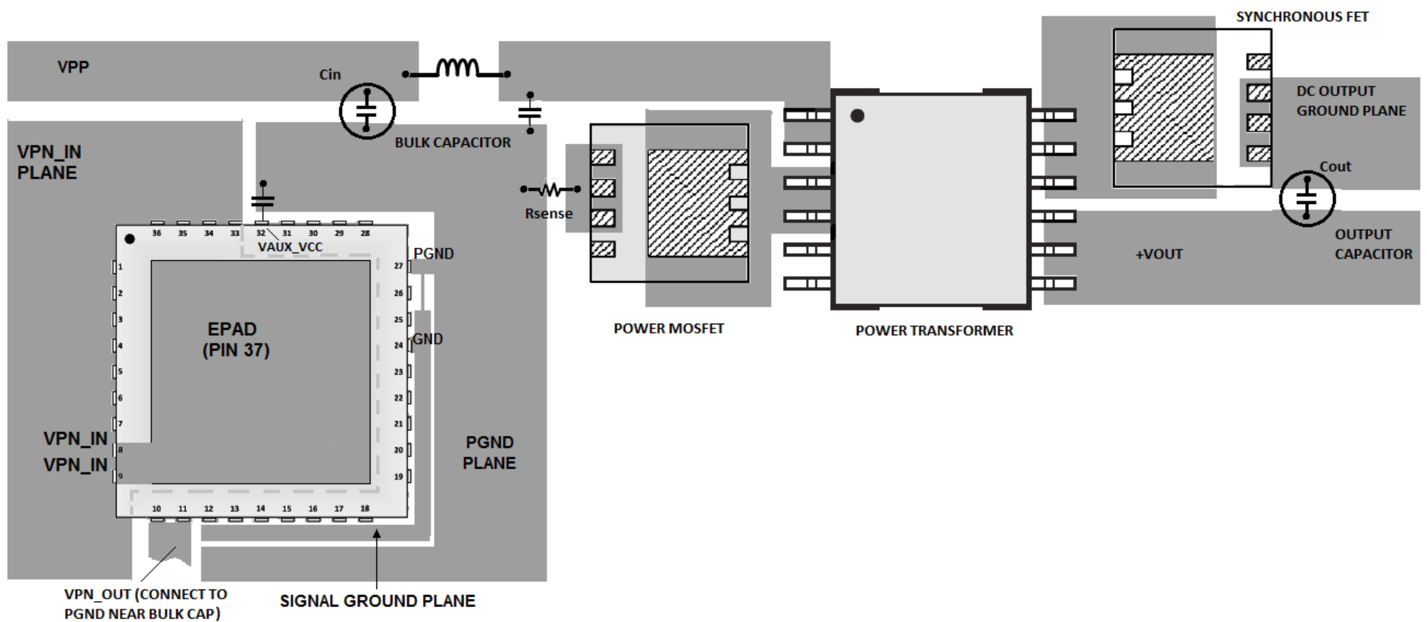


Figure 1: An example of copper planes implementation in a PD70211-based system

Power flow in PD70211-based systems

A PD is comprised of the following generic stages:

- Input stage;
- DC-DC converter stage;
- Output stage.

Figure 2 illustrates the current flow through these stages for a PD70211-based flyback converter. Below we will discuss each of these stages.

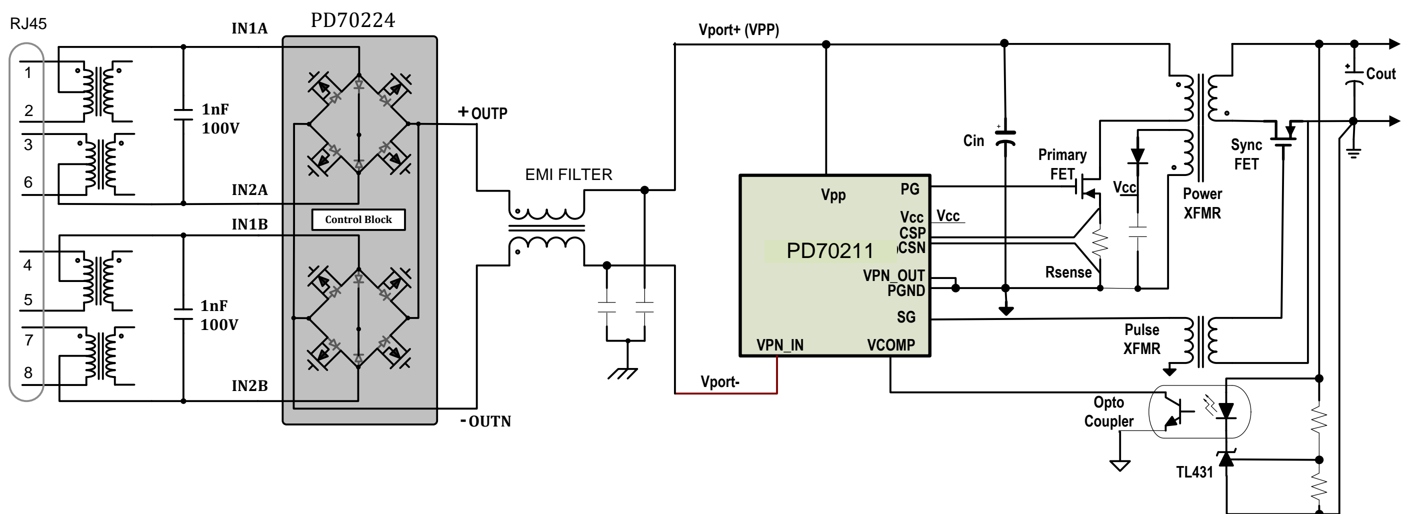


Figure 2: Power flow in a typical PD70211-based system

Input Stage

Input stage includes the following elements:

- Input RJ45 connectors
- Line transformer
- Diode bridge
- Common mode filter
- PD70210 or PD70211 device
- Bulk capacitor for DC-DC input filter.

In this set of elements, the current is DC (non-switched), except for detection/classification and initial power up.

The first 4 elements should be placed next to each other in order to enable the common mode choke to filter the noise close to RJ45 connector.

For low EMI radiation design, the positive and the negative rails should run parallel as close as possible to each other.

Among the above elements the diode bridges and PD device are the main parts that dissipate power and get heated. These parts should have sufficient copper lands for heat sinking according to their datasheet recommendations.

PD controller 70210(A) or PD70211

70210(A) or PD70211 power dissipation is mainly a function of the device's internal pass FET resistance and system current.

$P = Rdson \times (Max\ current)^2$

- Place both the PD chip and its peripheral on the top side so that the bottom layer will be used as a heat dissipation layer.
- Use the pattern land shown in **Error! eference source not found.**. Vias under the device are used for heat transfer between layers.
- If there are inner layers, use them too for extended copper land under the device to improve heat dissipation.
- Place 0.82uF/100V ceramic capacitor between VPP and VPN_IN (pins 32 and 8-9 of PD70211 or pins 1 and 7-8 of PD70210/A) as close as possible to the chip.
- Place 1uF/25V ceramic bypass capacitor between Vaux_Vcc pins and PGND as close as possible to the chip.

DC-DC section contains high-frequency high-current switching loops shown in yellow in Figure 3.

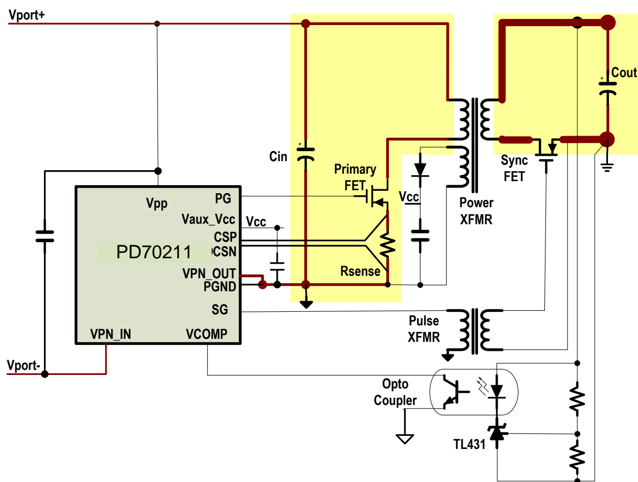
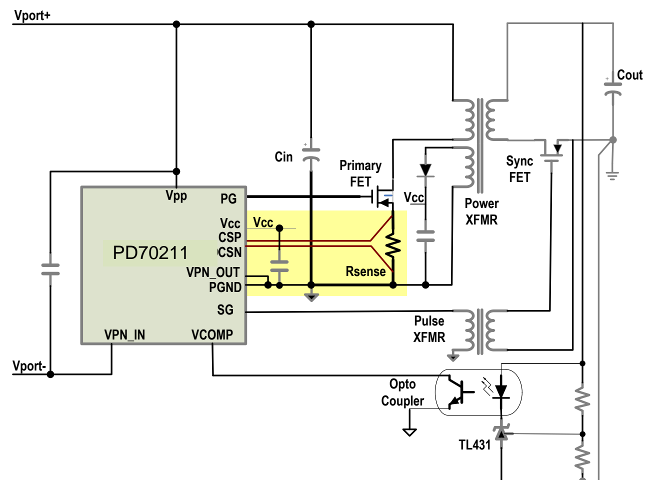


Figure 3: High current traces layout

Sense Resistors:

Sensing of the primary loop current is done using 1% +/-100ppm low resistance resistors connected as a shunt.
Figure 4 depicts the proper way to layout the power supply sense resistors.

The designer should calculate sense resistor's power dissipation and choose resistor size and number of paralleled resistors according to calculation result.
The sense resistors' voltage is in the range of 0 to 200mV and exists in an environment of fast transitions of up to 180V. The form of the current sense signal is very important and its integrity must be maintained.
Therefore, the sense voltage traces layout should be maintained carefully. In order to simplify the integrity challenge, PD70211 has a differential sampling mechanism built of pins CSP & CSN.
Route differential traces from sense resistor terminals to CSN and CSP input pins. They should be connected as a Kelvin connection, as close as possible to the resistors pads, and should not be part of the high current path to the resistors. This way, voltage measurement is not influenced by voltage drop on the high power traces.
These two sense lines should be routed together close to each other in order to maintain good noise immunity. For the resistor high current trace, use a wide trace or copper planes to decrease trace voltage drop.



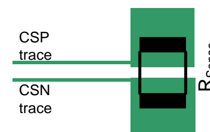


Figure 4: Sense Resistor Layout

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Primary and Secondary MOSFETs

Primary and secondary MOSFETs are high power devices. These devices should have sufficient copper lands to enable heat transfer from their junctions to the environment.

Copper land is a function of the MOSFET package power dissipation, junction to pad and junction to ambient thermal resistances, ambient temperature and the system requirements.

For a given application, you need to calculate power dissipation in the MOSFETs and choose their package and thermal pad size according to calculation results.

MOSFET PLACEMENT DESIGN EXAMPLE:
SYSTEM SPECIFICATIONS:

$Tja_abs_\max = 150°C$ (absolute maximum taken from data sheet);

$Tja_\max = 120°C$ (design margin from data sheet absolute maximum value);

T_{MAX} = 70ºC (maximum ambient temperature);

ΔT = $Tja_\max$ - T_{MAX} = 50ºC (MAXIMUM ACCEPTABLE TEMPERATURE RISE ON MOSFET CASE);

P_{MOSFET} = 1.3W (AN EXAMPLE OF MAXIMUM FET POWER DISSIPATION BASED ON STATIC AND DYNAMIC LOSSES CALCULATION).

GIVEN THE MOSFET HIGH POWER DISSIPATION, WE WILL CHOOSE MOSFET PACKAGE POWER-SO8 (5X6), WHICH HAS ΘJA=50 ºC/W WHEN MOUNTED ON PCB COPPER PAD SIZE OF 1X1 INCH (25.4X25.4 MM) OF 2 OZ COPPER.

With such copper pad, in our example the junction temperature will be:

$\Delta Tja = 35 \times 1.3 = 45.5°C$, which is within system specification.

In there is a PCB area limitation, the thermal pad can be split between several layers connected by vias under the drain of the MOSFET.

Isolation

For an isolated DC-DC design such as Flyback, Isolation level is based on IEEE 802.3AT standard.

IEEE 802.3AT standard defines 1500V_{rms} isolation to be obtained between all accessible external conductors including frame ground (if any), RJ45 connector leads, and all internal leads of the PD such as secondary side traces.

So, the isolation should be maintained between DC-DC converter primary and secondary sides and between Frame ground and primary side.

1500V_{rms} isolation is obtained by having a gap of 60mil between the traces of the primary domain and the secondary domain and frame.

The isolation line of separation should include power transformer, secondary gate pulse transformer, opto-couplers, and primary/secondary 2000V capacitors.

The capacitor should be located close to the power transformer to help lowering conducted emission.

Do not mix in the layout the two isolated sides. Mixing the sides on PCB may cause unwanted signals coupling and difficulty in maintaining the isolation.

Use a physical isolation line as shown by dashed red line in Figure .

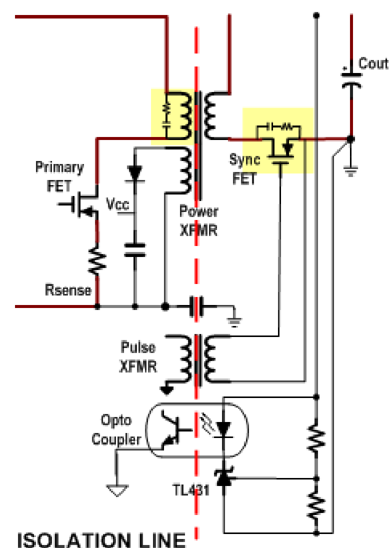

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Figure 5: An example of the isolation line

From EMI standpoint, there should not be any copper planes, traces and components under the power transformer and power inductors (if any).

Driving MOSFETs

Gate drive pulses are supplied to the primary and secondary gates and are generated by the PWM controller section of the PD70211 device.

In order to increase efficiency and decrease the temperature rise of the MOSFETs, a fast slew rate pulses should be obtained.

PD70211 device drivers have internal serial output resistance. To overcome this internal resistance and also the distance of the controller from the MOSFETs, additional driving components may be used (please refer for example to user guide D70211EVB51F12_UG). For proper operation of the driving elements, pull up transistor, pull down transistor, and bypass capacitor should be as close as possible to the referenced FET.

Snubbers

Snubbers are elements that are aimed to protect MOSFETs from high voltage spikes that are produced due to system parasitic, primarily transformer leakage inductance.

To lower the primary side spikes, a snubber is placed parallel to the primary winding as close as possible to it. This is very important to minimize the voltage spikes on the Drain-Source of the primary MOSFET.

The best location for primary snubber is in the bottom side under the transformer, which yields a low inductance connection. The snubber can be comprised of serial resistor and capacitor (RC), resistor capacitor and diode (RCD), or active snubber that also uses inductor.

The secondary side snubber is usually an RC snubber. It should be located very close to the secondary MOSFET, between its drain and source.

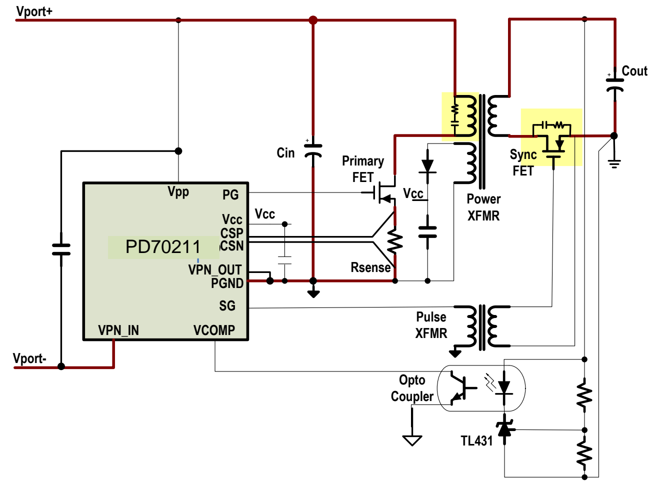

Figure 6: Snubbers Location

Heat Sinking

The components that dissipate the major portion of power and as a result heat up are:

- Input bridge
- Primary MOSFET
- Secondary MOSFET(s)
- Power Transformer
- PD70211 device
- Primary snubber components
- Secondary snubber components.\

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Board design should provide an adequate copper lands for dissipating the heat of those components.

For PD70211 for the layout use the recommended pattern lands shown in Figures 7-9. Vias under the device are used for heat transfer between layers. We recommend 25 mil vias for effective heat transfer between layers. As a first priority use external layers for the heat dissipation. Internal layers can be used as well for good heat transfer.

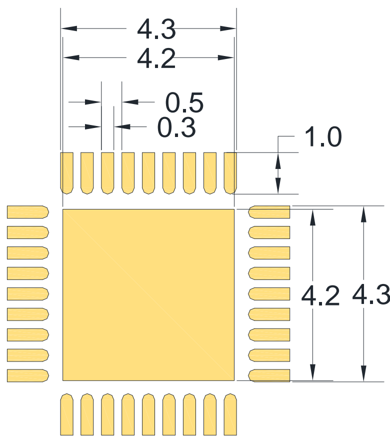


Figure 7: PD70211 Recommended PCB Layout for Thermal Pad Array (mm)

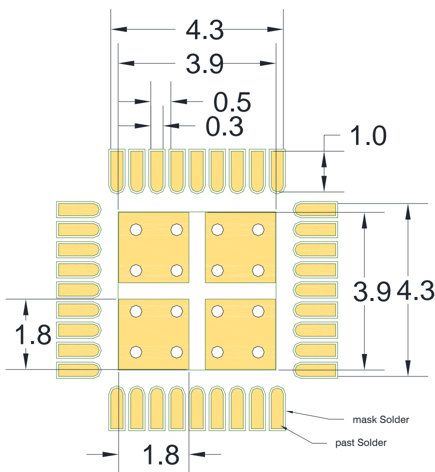


Figure 8: PD70211 Top Layer Solder Mask, Solder Paste and Vias Recommended PCB Layout (mm)

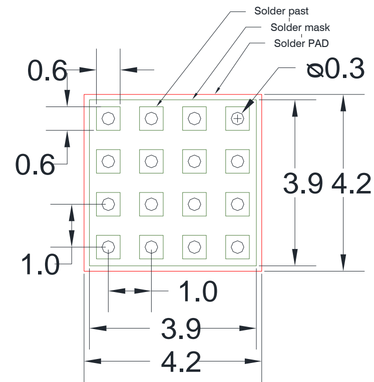
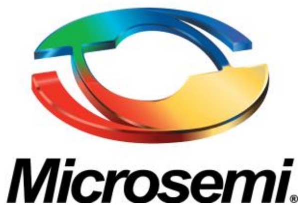


Figure 9: PD70211 Bottom Layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)



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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 29-July-2016	-	Initial Release – preliminary version

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