Triple Channel Clock Translator

Features

- Three independent OTN De-Synchronizers
- Excellent jitter performance of 180 fs rms in 12 kHz to 20 MHz band meets jitter requirements of 10G/40G and 100G PHYs
- Three programmable ultra-low jitter synthesizers generate any frequency from 1 Hz to 900 MHz.
- One programmable general purpose synthesizer generates any clock from 1 Hz to 180 MHz
- 6 differential (CML) or 12 single ended (CMOS) ultra-low jitter outputs plus two general purpose CMOS outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs

Ordering Information

ZL30174LDG6*	100 Pin aQFN	Trays
	*Pb Free Tin/Silver/Copper	

Package size: 10 x 10 mm

-40°C to +85°C

- Up to three programmable digital PLLs/NCOs with loop bandwidth from 14 Hz to 470 Hz synchronize to any clock rate from 1 kHz to 900 MHz
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 10 ppb

Applications

- OTN Transponders/Muxponeders
- OTN Switches
- Test Equipment

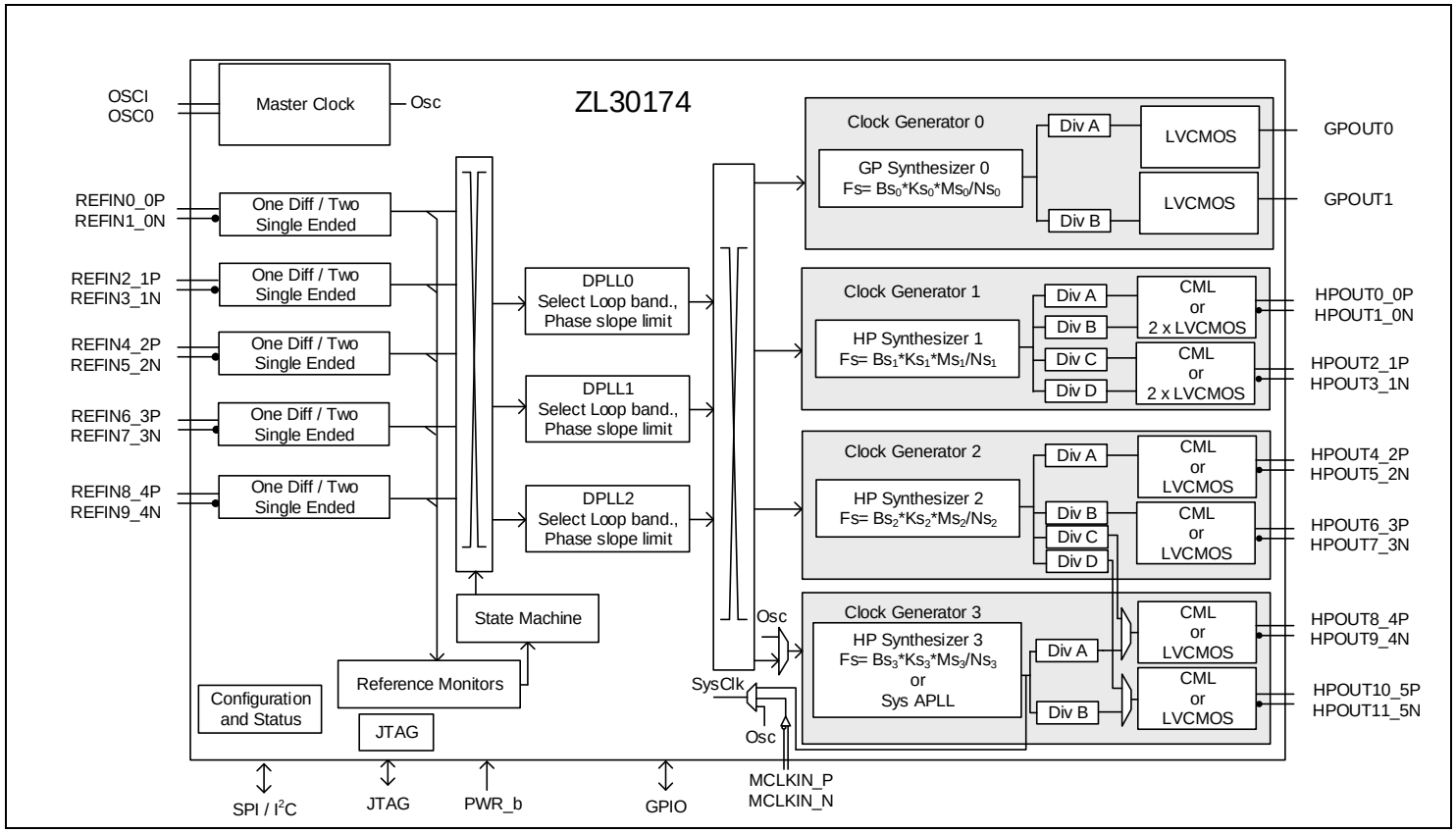

Figure 1. Functional Block Diagram

2 Feature List

2.1 General features

- Three independent clock channels
- Operates from a single crystal resonator or clock oscillator
- Configurable from SPI/I2C bus or from pre-configured flash memory

2.2 Electrical Clock Inputs

- Accepts up to 10 LVCMOS or 5 LVDS/HCSL/LVPECL/CML differential inputs
- Frequencies from 1 kHz to 180 MHz for LVCMOS
- Frequencies from 1 kHz to 900 MHz for LVDS/HCSL/LVPECL/CML
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities.
    - Each input reference has its own set of monitors which can be independently programmed.
    - Loss of signal (LOS)
    - Single Cycle Monitor (Triggers on glitches or variation in duty-cycle)
    - Coarse Frequency Monitor
    - Precise Frequency Monitor
- Locks to gapped clocks

2.3 Electrical Clock Engine

- Digital PLLs filter jitter from 14Hz up to 470 Hz
- Multiple modes of operation
    - Freerun
    - Forced holdover
    - Forced reference
    - Automatic
    - NCO
- Internal state machine automatically controls state
    - Locked
    - Acquiring
    - Holdover
- Automatic hitless reference switching and digital holdover on reference fail
- Programmable bandwidth
- Programmable damping & phase gain (gain peaking)
- Programmable lock and fast lock options
- Support for fast lock with lock times in seconds
- Support for hitless reference switching with typical performance 0.6 ns
- Holdover better than 1ppb with post holdover filter. Without the post holdover filter the initial holdover accuracy is better than 10ppb.
- Full rate conversion between input and output clock frequencies

2.4 Electrical Clock Generation

- Four programmable synthesizers
- Precision Synthesizers
  - Each ultra-low jitter output can be independently set to be differential (CML) or two CMOS
  - Six CML outputs
    - Generate clock rates from 1 Hz to 900 MHz
    - Jitter performance of 180 fs rms (12 kHz – 20 MHz)
    - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
  - Twelve LVCMOS outputs
    - Generate clock rates from 1 Hz to 180 MHz
    - Jitter performance of 290 fs rms (12 kHz – 20 MHz)
- General Synthesizer
  - Two LVCMOS outputs
  - Generate clock rates from 1 Hz to 180 MHz
  - Jitter performance of 17 ps rms (12 kHz – 20 MHz
- Programmable output advancement to accommodate trace delays or compensate for system routing paths
- Each output has its own power supply pin which can be hooked to 3.3V, 2.5V or 1.8V supplies. Outputs may be disabled to save power

3 Application

ZL30174 is multifunctional device which can be used in many OTN applications. It provides four independent PLL channels which can synchronize to any input frequency from 1KHz up to 900MHz. ZL30174 can generate any output frequency from 1Hz up to 180MHz for LVCMOS and up to 900MHz for CML outputs. Each channel is comprised of a DPLL and a Synthesizer.

ZL30174 with its three ultra-low jitter channels can be used in OTN Transponder OTU-4 applications as shown in Figure 4. To simplify the block diagram ZL30174 is split into two blocks each containing one PLL. Each PLL here comprises of DPLL with sub 300Hz loop bandwidth as required by OTN specs and a Synthesizer used to generate required frequency with ultra-low jitter required by Serializers. The third ultra-low jitter synthesizer is used to generate system clock.

Figure 2 shows one channel (PLL0) used as De-Synchronizer to filter gapped OTN line clock. The gapped clock is generated in demapper justification block by removing pulses from the extracted OTN line clock. The gapped clock needs to be cleaned from jitter before it can be used to drive 100G Ethernet CAUI Serializers. The second PLL (PLL1) is used to drive OTN line. It can be set in a free run mode where the clock is synchronized to free run crystal oscillator used as ZL30174 master clock or the OTN line can be synchronized to 100G client by synchronizing PLL1 to the Ethernet clock as shown in Figure 2.

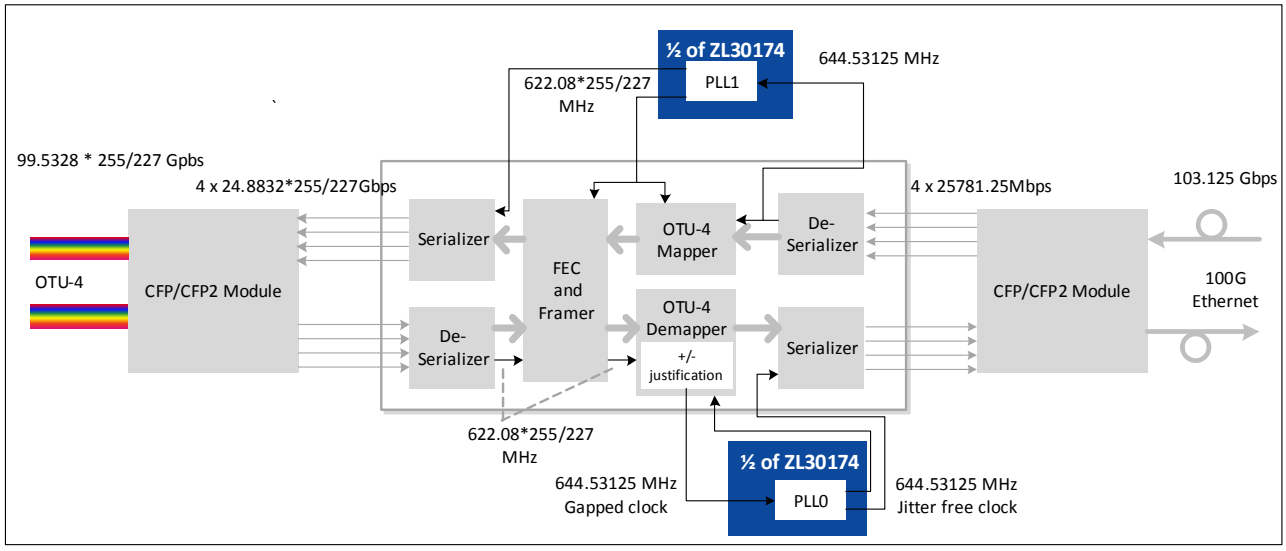

Figure 2. OTU-4 Transponder

An example of phase noise at the output of one of ultra-low jitter synthesizers is shown in following figure.

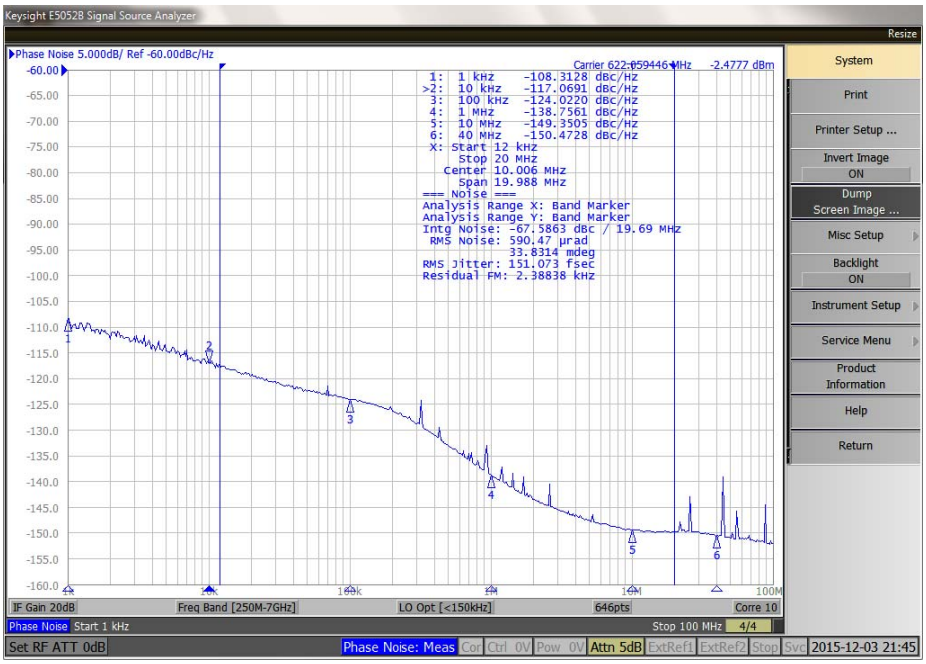

Figure 3. Phase noise plot for 622.08MHz output clock with 200MHz XO (151fs jitter in 12kHz to 20MHz band)

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