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Identify® Microsemi Edition Tool Set Release Notes

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About This Release

These release notes describe features and enhancements for the J-2015.03M and J-2015.03M-SP1 releases of the Identify Microsemi Edition tool set. The tool set is synchronized with the J-2015.03M-SP1-1 release of the Synplify Pro synthesis tool.

Enhancements

The J-2015.03M releases include the following enhancements:

- Support for the RTG4 device library (the J-2015.03M-SP1 release corrects a problem in the initial library release)
- Support for sample buffer sizes greater than 64Kbit
- UJTAG access to the design while it is being instrumented (see UJTAG Design Access below)
- Expanded jtag_server command syntax to include start and stop controls to support debugging on a remote machine.

UJTAG Design Access

The UJTAG access feature allows concurrent access to a design while it is being instrumented. To use this feature:

1. Replace the instantiation of the UJTAG macro in the design with an instance of UJTAG_WRAPPER.
2. Add the ujtag_wrapper.v file to the Libero project (a template file is located in /lib/di in the *identifyInstall* directory).
3. If you intend to instrument the design, include a `define IDENTIFY_DEBUG_IMPL Verilog definition in the file or, from the Synplify Pro Tcl prompt, enter:

```
set_option -hdl_define -set IDENTIFY_DEBUG_IMPL
```

This usage information is also given directly in the header of the lib/di/ujtag_wrapper.v file. For additional information, see Application Note AC227, *How to Use UJTAG*, on the Microsemi web site.

Device Support

The J-2015.03M-SP1 release supports the following Microsemi device families. Device selection is specified solely in the synthesis tool and passed to the Identify instrumentor in the synthesis project file. Specifying a library in the synthesis tool that is not supported in the Identify tool set results in a “device not supported” message when attempting to launch the Identify instrumentor.

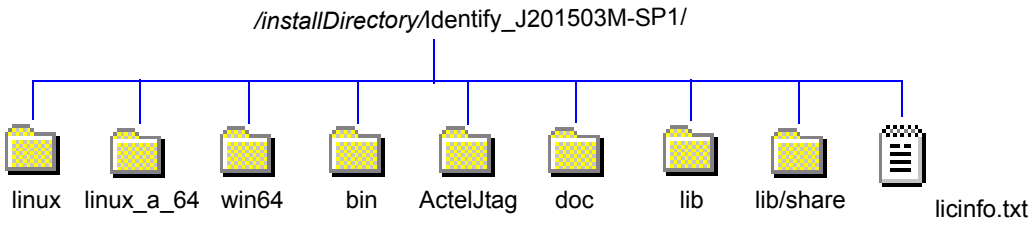
Fusion	SmartFusion	SmartFusion2	IGLOO
IGLOOe	IGLOO PLUS	IGLOO2	ProASIC
ProASIC PLUS	ProASIC3	ProASIC3E	ProASIC3L
RTG4			

Installation

The directory where Identify is installed is referred to as the *installDirectory*. The installation subdirectory name consists of the Identify product name and an associated version number, in the current case, Identify_J201503M-SP1 (for version J-2015.03M-SP1). This naming convention permits multiple versions to be installed in the same product directory. On Windows platforms, the start menus, desktop icons, and uninstall names have an associated version number, in the current case, Identify J-2015.03M-SP1. For a list of the compatible Windows-based platforms, see *Platform Support* on page 5.

Downloading the Software

The Identify software is installed directly from the downloaded exe file. Installing the software creates the Identify_J201503M-SP1 subdirectory in the installation directory. This directory contains the following files and subdirectories:



The contents of the files or sub-directories are as follows:

Directory	Contents
bin, linux, linux_a_64, win64	Executables for the Identify instrumentor and Identify debugger; debugger; linux and linux_a_64 are included with Linux installations, win64 is included with Windows installations.
ActelJtag	Drivers
doc	User documentation

Directory	Contents
lib	Program data files
lib/share	Includes the following subdirectories: • contrib – source directory for scripts executed on startup • synthesis – program specific data files • demo_design – the bus_demo and counter designs for the tutorials
Text Files	ASCII version of the Synopsys Software License and Maintenance Agreement

Platform Support

The Identify J-2015.03M-SP1 release is compatible with the following platforms and operating systems:

- Windows:
  - Windows 7 Professional or Enterprise (32/64-bit)
  - Windows 8.1 Professional or Enterprise (64-bit)
- Linux:
  - Red Hat Enterprise Linux 5 (32/64-bit)
  - Red Hat Enterprise Linux 6 (64-bit)
  - SUSE Linux Enterprise 10 (32/64-bit)
  - SUSE Linux Enterprise 11 (64-bit)

Synopsys FPGA Synthesis Tool Requirements

The J-2015.03M-SP1 release of the Identify tool set can only be used with the following Synopsys FPGA tools on the above platforms and operating systems.

Tool	Required Version
Synplify Pro synthesis tool	FPGA J-2015.03M=SP1-1

Machine Requirements

Machine memory requirements vary according to the size and complexity of your designs. At a minimum, 4 GBytes of RAM are generally required. Your machine's virtual memory (swap space) should be set to at least twice the capacity of the RAM.

Location of the cfg File

Windows platforms do not permit applications to write to the C:/Windows directory. Because the Identify tools must update the userprefs.cfg initialization file, this file is written to the following directory location:

```
C:\Users\userName\AppData\Roaming\Identify
```

Windows Memory Configuration

For all memory configurations, Windows uses a default virtual address space of 4 GBytes; 2 GBytes allocated to user processes (applications) and 2GBytes allocated to the operating system and kernel-mode drivers. On Windows systems that have 1 GByte or more of physical memory, the memory allocation between applications and operating system can be modified to increase the user-process memory allocation to 3 GBytes (and reduce the operating system memory allocation to 1 GByte). For the most up-to-date information for

reconfiguring memory allocation on a compatible system, see *How to Set the /3GB Startup Switch in Windows* and related topics on the Microsoft TechNet (http://www.microsoft.com/technet).

Identify Documentation

The following documentation is included with the J-2015.03M-SP1 release of the Identify tool set:

- Identify Microsemi Edition Tool Set Release Notes (this document)
- Identify Microsemi Edition User Guide
- Identify Microsemi Edition Reference Manual
- Identify Microsemi Edition Quick Start Guide
- Identify Microsemi Edition Tutorial
- Synopsys Software License and Maintenance Agreement

Accessing Documents using the Acrobat Reader

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

From within the software, you can open the PDF documents by selecting Help->Online Documents and selecting the appropriate PDF. You can also access PDF documents without running the software by going to Start->Programs->Synopsys->Identify J-2015.03M-SP1->Documents and selecting the desired PDF document.

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Resolved Issues

The following issues have been resolved by the Identify J-2015.03M releases:

Resolved Issue: When an implementation included an edf black-box module, the Identify instrumentor would error out complaining about an undefined module.

Resolved Issue: Cross-triggering caused the Identify Debugger to crash when a trigger condition was not set for each IICE.

Important Issues and Workarounds

The following issues have been identified with the Identify J-2015.03M releases:

System Controller Suspend Mode

When the System Controller suspend mode is enabled, a "no sampling clock found" error can occur when running the Identify debugger.

Solution: Exit the suspend mode, toggle TRSTB high, and power cycle the device before debugging (see the *Microsemi System Controller User Guide* for more information).

VHDL Trigger Signal

When using VHDL, if the trigger signal (scalar) is of type std_logic, the value must be enclosed in single quotes in both the UI and the shell as shown in the following command:

```
watch enable -iice IICE -condition 0 /my_signal {'0'}
```

Entering a scalar signal without quotes or in double quotes results in an error. Conversely, vectors must be entered without quotes as shown in the following command:

```
watch enable -iice IICE -condition 0 /my_bus {1010}
```

Solution: Make sure that all scalars are enclosed in single quotes and that vectors are entered without quotes.

Message Compression

The message suppression feature available with the synthesis tools cannot be used to suppress (or change the severity of) messages generated by the Identify tool set.

Solution: Be sure to disable message suppression when using an Identify implementation.

External Triggers

Use of external triggers via the import trigger mechanism causes an excessive use of internal block RAM due to sampling of the trigger as well as the creation of a look-up table. The problem is most notable when the maximum of eight imported triggers is selected. A better mechanism to import triggers that uses fewer resources will be available in a future release.

Solution: Add an extra input to the top-level RTL code and instrument the input as a trigger only.

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