Revision History

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<td>5</td>
<td>Fifth release</td>
</tr>
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<td>23 January, 2014</td>
<td>4</td>
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</tr>
<tr>
<td>07 August, 2014</td>
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<td>30 July, 2014</td>
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Confidentiality Status

This is a non-confidential document.
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Preface

About this document

This demo guide is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

The following designers use the IGLOO2 devices:

- FPGA designers
- System-level designers

References

Microsemi Publications

- UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide
- U0509: Implementing PCIe Control Plane Design in IGLOO2 FPGA Tutorial
- UG0450: SmartFusion2 SoC FPGA and IGLOO2 FPGA System Controller User Guide

For a complete and up-to-date listing of IGLOO2 device documentation, refer to the following web page:

**IGLOO2 FPGA PCIe Control Plane with Device Serial Number Demo**

**Introduction**

The IGLOO2 FPGA devices integrate a fourth-generation flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO2 high-speed serial interface (SERDES) provides a fully integrated peripheral component interface express (PCI®e) endpoint (EP) implementation and is compliant with the PCIe Base Specification Revision 2.0 and 1.1. Refer to the UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide for more information.

This demo shows how the embedded PCIe feature of the IGLOO2 FPGA devices can be used as a low bandwidth control plane interface. It also demonstrates device serial number (DSN) feature embedded in the IGLOO2 device. A sample design is provided to access IGLOO2 PCIe EP from host PC. It runs on both windows and RedHat Linux operating systems (OS). A GUI installer, host PC drivers for Windows OS and a Linux PCIe application for Linux OS are provided for reading and writing to the IGLOO2 PCIe configuration and memory space.

**Figure 1** shows the top-level block diagram of the PCIe control plane demo. The demo design uses an IGLOO2 PCIe interface with a link width of x1 lane to interface with a host PC PCIe Gen2 slot. The CoreGPIO IP controls the LEDs and switches on the IGLOO2 Evaluation Kit board through the PCIe interface. The host PC can read and write to the IGLOO2 large SRAM (LSRAM), and can also be interrupted by using the push button on the IGLOO2 Evaluation Kit board. It can read the 128-bit DSN system service.

![Figure 1 • PCIe Control Plane Demo Top-Level Block Diagram](image)
Design Requirements

Table 1 • Design Requirements

<table>
<thead>
<tr>
<th>Design Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>IGLOO2 Evaluation Kit</td>
<td>Rev D or later</td>
</tr>
<tr>
<td>• 12 V adapter</td>
<td></td>
</tr>
<tr>
<td>• FlashPro4 programmer</td>
<td></td>
</tr>
<tr>
<td>• USB A to Mini-B cable</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop with an available PCIe 2.0 Gen 1 or Gen 2 compliant slot</td>
<td>64-bit Windows 7 OS or 64-bit Red Hat Linux OS (Kernel Version: 2.6.18-308)</td>
</tr>
<tr>
<td>Express Card slot and PCIe Express card adapter (for Laptop only)</td>
<td>–</td>
</tr>
<tr>
<td><strong>Software Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Libero® System-on-Chip (SoC) for viewing the design files</td>
<td>v11.6</td>
</tr>
<tr>
<td>FlashPro Programming Software</td>
<td>v11.6</td>
</tr>
<tr>
<td>Host PC Drivers (provided along with the design files)</td>
<td>–</td>
</tr>
<tr>
<td>GUI executable (provided along with the design files)</td>
<td>–</td>
</tr>
</tbody>
</table>

*Note: The PCIe Express card adapter is not supplied with the IGLOO2 Evaluation Kit.*

Demo Design

**Introduction**

The design files for this demo can be downloaded from the Microsemi® website:
http://soc.microsemi.com/download/rsc/?f=m2gl_dg0532_liberov11p6_df

Design files include:

1. Libero project
2. Programming files
3. Host PC drivers for Windows OS
4. Host PC drivers and PCIe application for Linux OS
5. Source files
6. Readme.txt file
Figure 2 shows the top-level structure of the design files. For more information, refer to the readme.txt file.

Features

The demo design performs the following tasks:

- Displays PCIe link enable/disable, negotiated link width, and the link speed
- Controls the status of light emitting diodes (LEDs) on the IGLOO2 Evaluation Kit board
- Displays the position of dual in-line package (DIP) switches on IGLOO2 Evaluation Kit board
- Enables read and write to LSRAM
- Accepts and displays interrupts from the push button on the IGLOO2 Evaluation Kit board
- Shows the IGLOO2 PCIe configuration space
- Reads DSN
Description
The demo design accesses the IGLOO2 PCIe EP from the host PC. Figure 3 shows a detailed block diagram of the design implementation.

The PCIe EP device receives commands from the host PC via GUI or Linux PCIe application and performs corresponding memory writes to the IGLOO2 fabric address space.

The SERDES_IF_0 is configured for a PCIe 2.0, x1 link width with GEN2 speed. The PCIe interface to the fabric uses an advanced microcontroller bus architecture (AMBA®) high-performance bus (AHB). The AHB master interface of SERDESIF is enabled and connected to the slaves CoreAHBLSRAM and CoreGPIO using the CoreAHBLite, CoreAHBTOAPB, and CoreAPB3 bus interfaces.

SERDES_IF_0 is initialized by high performance memory subsystem (HPMS), which is configured by the System Builder.

The CoreSysServices Soft IP provides a user interface and AHB-Lite master interface to access the DSN System Service. This System Service fetches the 128-bit DSN. The DSN is unique to every device that is set during manufacturing. A simple Verilog logic is implemented to read the DSN using CoreSysServices IP and write the same to LSRAM.

Refer to the UG0450: SmartFusion2 SoC FPGA and IGLOO2 FPGA System Controller User Guide for more information on System Services.

The advanced extensible Interface (AXI) master windows of the SERDESIF PCIe provide address translation for accessing one address space from another address space as the PCIe address is different from the IGLOO2 AHB bus matrix address space. The AXI master window 0 is enabled and configured to translate the BAR0 memory address space to the CoreGPIO address space to control the LEDs and DIP switches.

The AXI master window 1 is enabled and configured to translate the BAR1 memory address space to the CoreAHBLSRAM address space to perform read and write from PCIe. The IGLOO2 PCIe BAR0 and BAR1 are configured in 32-bit mode.
CoreGPIO is enabled and configured as below:

- GPIO_OUT [8] connected to user logic to read the DSN
- GPIO_OUT [7:0] connected LEDs
- GPIO_IN[4] indicates that the device serial number is available in LSRAM to display
- GPIO_IN [3:0] connected to DIP switches

The PCIe interrupt line is connected to the SW4 on the IGLOO2 Evaluation Kit board. The FPGA clocks are configured to run the FPGA fabric at 50 MHz and HPMS at 100 MHz.

**Simulating the Design**

The design supports the BFM_PCIE simulation level to communicate with the SERDESIF block via the master AXI bus interface. Although, no serial communication uses the SERDESIF block, this scenario allows to validate the fabric interface connections. The SERDESIF_0_user.bfm file under the <Libero project>/simulation folder contains the BFM commands to verify the read or write access to CoreGPIO and CoreAHBLSRAM.

BFM commands added in the SERDESIF_0_user.bfm file do the following:

- Write to GPIO_OUT[7:0]
- Write to LSRAM
- Read-check from LSRAM

To run the simulation, double-click Simulate under Verify Pre-Synthesized Design in the Design Flow window of Libero project. ModelSim runs the design for about 200 us. The ModelSim transcript window displays the BFM commands and the BFM simulation completed with no errors, as shown in Figure 4.

---

**Figure 4 • SERDES BFM Simulation**
Figure 5 shows the waveform window with GPIO_OUT signals.

Setting Up the Demo Design

The following steps describe how to setup the demo:

1. Connect the FlashPro4 programmer to the J5 connector of the IGLOO2 FPGA Evaluation Kit board.
2. Connect the jumpers on the IGLOO2 FPGA Evaluation Kit board as shown in Table 2. CAUTION: Switch OFF the power supply switch SW7 while connecting the jumpers.

Table 2 • IGLOO2 FPGA Evaluation Kit Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin (from)</th>
<th>Pin (to)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J22</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J23</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>

3. Connect the power supply to the J6 connector.

Board Setup

Snapshots of the IGLOO2 Evaluation Kit board with the complete set up is given in the "Appendix 1: IGLOO2 Evaluation Kit Board" on page 39.
Programming the IGLOO2 Board

1. Download the demo design from:
   http://soc.microsemi.com/download/rsc/?f=m2gl_dg0532_liberov11p6_df
2. Switch ON the SW7 power supply switch.
3. Launch the FlashPro software.
4. Click New Project.
5. In the New Project window, type the project name as PCIe_Control_Plane.
6. Click Browse and navigate to the location where you want to save the project.
7. Select Single device as the Programming mode.
8. Click OK to save the project.
9. Click Configure Device on the FlashPro GUI.
10. Click Browse and navigate to the location where the PCIe_Demo_top.stp file is located and select the file. The default location is:
    <download_folder>M2GL_PCIE_Control_Plane_DSN_DF\programming_file\.

Figure 6 • FlashPro New Project
11. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

![FlashPro Project Configured](image)

*Figure 7 • FlashPro Project Configured*
12. Click **PROGRAM** to start programming the device. Wait until a message appears indicating that the **PROGRAM PASSED**.

---

**Connecting the Evaluation Kit Board to the Host PC**

The following steps describe how to connect the IGLOO2 evaluation kit board to the host PC:

1. After successful programming, power **OFF** the IGLOO2 Evaluation Kit board and shut down the host PC.

2. Use the following steps to connect the **CON1–PCIe Edge Connector** either to a host PC or laptop:
   a. Connect the **CON1–PCIe Edge Connector** to host PC PCIe Gen2 slot or Gen1 slot as applicable. This demo guide is designed to run in any PCIe Gen2 compliant slot. If the host PC does not support the Gen2 compliant slot, the design switches to Gen1 mode.
   b. Connect the **CON1–PCIe Edge Connector** to the laptop PCIe slot using the express card adapter. If you are using a laptop, the express card adapters typically support only Gen1 and the design works on Gen1 mode.

**Note:** Host PC or laptop should be powered **OFF** while inserting the PCIe Edge Connector. If the system is not powered **OFF**, the PCIe device detection and selection of Gen1 or Gen2 do not occur properly. It is recommended that the host PC or laptop must be powered OFF during the PCIe card insertion.
3. Figure 9 shows the board setup for the host PC in which IGLOO2 Evaluation Kit board is connected to the host PC PCIe slot. To connect the IGLOO2 Evaluation Kit board to the laptop using Express card adapter, refer to the "Appendix 2: IGLOO2 Evaluation Kit Board Setup for Laptop" on page 40.

Running the Demo Design

This demo can run on both Windows and RedHat Linux OS.

- To run the demo on Windows OS GUI, Jungo drivers are provided. Refer to "Running the Demo Design on Windows" section on page 15.
- To run the demo on Linux OS, native RedHat Linux drivers and command line scripts are provided. Refer to "Running the Demo Design on Linux" section on page 27.
Running the Demo Design on Windows

The following steps describe how to run the demo design on Windows:

1. Switch **ON** the SW7 power supply switch.
2. Power **ON** the host PC and open the host PC **Device Manager** for PCIe device, as shown in Figure 10. If the PCIe device is not detected, power cycle the IGLOO2 Evaluation Kit board and click **scan for hardware changes** in Device Manager.

   ![Device Manager](image)

**Figure 10 • Device Manager**

**Note:** If the device is still not detected, check whether or not the basic input/output system (BIOS) version in host PC is the latest, and if PCIe is enabled in the host PC BIOS.

If the host PC has any other installed drivers (previous versions of Jungo drivers) for the IGLOO2 PCIe device, uninstall them. To uninstall previous versions of Jungo drivers follow steps a and b.
a. To uninstall previous Jungo drivers, go to Device Manager and right-click DEVICE and click Uninstall, as shown in Figure 11.

![Device Uninstall](image)

**Figure 11 • Device Uninstall**

b. The DEVICE Uninstall window is displayed, as shown in Figure 12. Check **Delete the driver software for this device** check box. After uninstalling the previous Jungo drivers, ensure that the PCIe device is detected in the Device Manager window, as shown in Figure 10 on page 15.

![Confirm Device Uninstall](image)

**Figure 12 • Confirm Device Uninstall**
Drivers Installation

The PCIe demo uses a driver framework provided by Jungo WinDriverPro. To install the PCIe drivers on the host PC for IGLOO2 Evaluation Kit, use the following steps:

1. Extract the **PCIe_Demo.rar** to C:\ drive. The **PCIe_Demo.rar** is located in the provided design files:
   - `M2GL_PCIE_Control_Plane_DSN_DF\Windows_64bit\Drivers\PCIe_Demo.rar`
   
   **Note:** Installing these drivers require Host PC administration rights.

2. Run the batch file `C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat`

3. Click **Install**, if the window is displayed as shown in Figure 13.

   **Figure 13 • Jungo Driver Installation**

   **Note:** If the installation is not in progress, right-click on the command prompt and select **Run as administrator**. Run the batch file `C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat` from command prompt.

4. Click **Install this driver software anyway**, if the window appears as shown in Figure 14.

   **Figure 14 • Windows Security**
**PCIe Demo GUI Installation**

IGLOO2 PCIe demo GUI is a simple GUI that runs on the host PC to communicate with the IGLOO2 PCIe EP device. The GUI provides the PCIe link status, driver information, and demo controls. The GUI invokes the PCIe driver installed on the host PC and provides commands to the driver according to the user selection.

Use the following steps to install the GUI:

1. Download and extract the **PCIe_Demo_GUI_Installer.rar** from the provided PCIe Demo GUI Installer.
2. Double-click **setup.exe** in the provided GUI installation (**PCIe_Demo_GUI_Installer\setup.exe**). Apply default options as shown in **Figure 15**.

---

**Figure 15 • GUI Installation**
3. Click **Next** to complete the installation. After successful installation, the following window is displayed:

![Installation Complete](image1)

**Figure 16 • Successful GUI Installation**

4. Restart the host PC.
Running the PCIe GUI

The following steps describe how to run the PCIe GUI:

1. Check the host PC Device Manager for the drivers. If the device is not detected, power-cycle the IGLOO2 Evaluation Kit board and click scan for hardware changes in Device Manager window. Ensure that the board is switched ON.

Note: If a warning symbol is displayed on the DEVICE or WinDriver icons in the Device Manager, uninstall them and start from step1 of "Drivers Installation" on page 17.
2. Invoke the GUI from **ALL Programs > PCIeDemo > PCIe Demo GUI**. The GUI is displayed, as shown in Figure 18.

![PCIe Demo GUI](image)

*Figure 18 • PCIe Demo GUI*
3. Click **Connect** at the top-right corner of the GUI. **Figure 19** shows the messages displayed on the GUI.

![Figure 19 • Version Information](image)

**Note:** If the host PC does not support GEN2 slot, then this design runs at GEN1 speed.
4. Clicking **Demo Controls** in the GUI displays the LEDs options and DIP switch status, as shown in Figure 20.

![Image of Demo Controls](image)

**Figure 20 • Demo Controls**

5. Click LEDs on GUI to **ON/OFF** the LEDs on the IGLOO2 Evaluation Kit board.
6. Click **Start LED ON/OFF Walk** to blink the LEDs on IGLOO2 Evaluation Kit board.
7. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
8. Change the DIP switch positions on the IGLOO2 Evaluation Kit board (SW5) and observe the similar position of switches in **GUI SWITCH MODULE**.
9. Click **Enable Interrupt Session** to enable the PCIe interrupt.
10. Press **SW4** on the IGLOO2 Evaluation Kit board and observe the interrupt count on the **Interrupt Counter** field in GUI, as shown in Figure 21.

11. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.
12. Click **Config Space** to read details about the PCIe configuration space. *Figure 22* shows the PCIe configuration space.
13. Click **PCIe R/W** to perform read and writes to LSRAM memory through **BAR1** space. Figure 23 shows the PCIe R/W window. Enter **Address** between 0x0000 to 0x7FFC.

14. Enter **Data**. The data field accepts a 32-bit hexadecimal value.

---

**Figure 23** • Perform Read and Write to LSRAM Using PCIe
15. Click **Security** tab and click **Read** to read the DSN. Figure 24 shows the **Device Serial Number**.

![Figure 24 • Reading Device Serial Number](image)

16. Click **Exit** to quit the demo.

**Running the Demo Design on Linux**

The following steps describe how to run the demo design on Linux:

1. **Switch ON** the power supply switch on the IGLOO2 Evaluation Kit board.
2. **Switch ON** the Red Hat Linux Host PC.
3. **Red Hat Linux Kernel** detects the IGLOO2 PCIe end point as Actel Device.
4. **On Linux Command Prompt** Use `lspci` command to display the PCIe info.
   
   ```
   # lspci
   ```
Drivers Installation

Enter the following commands in the Linux command prompt to install the PCIe drivers:

1. Create the igl2 directory under home/.
   
   ```
   # mkdir /home/igl2
   ```

2. Bring the M2GL_PCIE_Control_Plane_DSN_DF/design files folder under /home/igl2 directory, which contains the Linux PCIe device driver files and Linux PCIe application utility files.

3. Copy the Linux PCIe Device Driver file (PCIe_Driver.zip) from M2GL_PCIE_Control_Plane_DSN_DF/design files folder.
   
   ```
   # cp -rf /home/igl2/M2GL_PCIE_Control_Plane_DSN_DF/Linux_64bit/Drivers/PCIe_Driver.zip
   # unzip PCIe_Driver.zip
   ```

4. /home/igl2 directory must contain PCIe_Driver/inc/ folders.
   
   Execute ls command to display the contents of /home/igl2 directory.
   
   ```
   # ls
   ```

5. Change to inc/ directory.
   
   ```
   # cd /home/igl2/inc
   ```

6. Edit the board.h file for IGLOO2 Evaluation Kit.
   
   ```
   #vi board.h
   #define IGL2
   #undef SF2
   ```

7. To save the selected file, perform [:wq]

8. To change the directory, use the following command:
   
   ```
   #cd /home/igl2/PCIe_Driver
   ```

9. To compile the Linux PCIe device driver code, execute make command on Linux Command Prompt.
   
   ```
   #make clean [To clean any *.o, *.ko files]
   #make
   ```

10. The kernel module, pci_chr_drv_ctrlpln.ko creates in the same directory.
11. To insert the Linux PCIe device driver as a module, execute `insmod` command on Linux Command Prompt.

```
# insmod pci_chr_drv_ctrlpln.ko
```

Root Privileges are required to execute this command.

---

Figure 26 • Edit board.h File

---

Figure 27 • PCIe Device Driver Installation

12. After successful Linux PCIe device driver installation, check `/dev/MS_PCI_DEV` got created by using the following Linux command:

```
# ls /dev/MS_PCI_DEV
```

**Note:** `/dev/MS_PCI_DEV` interface is used to access the IGLOO2 PCIe end point from Linux user space.

Linux PCIe Application Compilation and PCIe Control Plane Utility Creation

1. Change to `/home/igl2` directory.

```
# cd /home/igl2
```

2. Copy the Linux PCIe application utility file (`PCIe_App.zip`) from `M2GL_PCIE_Control_Plane_DSN_DF/` design files folder.

```
# cp -rf /home/igl2/M2GL_PCIE_Control_Plane_DSN_DF/Linux_64bit/UTIL/PCIe_App.zip /home/igl2
# unzip PCIe_App.zip
```
3. `/home/igl2` directory must contain `PCIe_App/` folder along with `led_blink.sh` and `pcie_config.sh` scripts. Execute `ls` command to display the contents in `/home/igl2` directory.
   
   ```shell
   # ls
   ```

4. Compile the Linux user space application `pcie_appln_ctrlpln.c` in `/home/igl2/PCIe_App` folder by using `gcc` command.
   
   ```shell
   # cd /home/igl2/PCIe_App
   # gcc -o pcie_ctrlplane pcie_appln_ctrlpln.c
   ```

   After successful compilation, Linux PCIe application utility `pcie_ctrlplane` creates in the same directory.

5. On Linux Command Prompt, run the `pcie_ctrlplane` utility as:
   
   ```shell
   # ./pcie_ctrlplane
   ```

   Help menu displays as shown in Figure 28.

---

**Figure 28 • Linux PCIe Application Utility**
Execution of Linux PCIe Control Plane Features

LED Control

LED1 to LED8 is controlled by writing data to IGLOO2 LED control registers.

```bash
# ./pcie_ctrlplane 1 0x000000FF [LED OFF]
# ./pcie_ctrlplane 1 0x00000000 [LED ON]
```

Figure 29 • Linux Command - LED Control

led_blink.sh, contains the shell script code to perform LED Walk ON where as Ctrl+C kills the shell script and LED Walk turns OFF.

```bash
#sh led_blink.sh
```

Run the led_blink.sh shell script using `sh` command.
SRAM Read/Write

32 KB SRAM is accessible for IGLOO2 Evaluation Kit.

```
#./pcie_ctrlplane 2 1 0xFF00FF00 0x1000 [SRAM WRITE]
#./pcie_ctrlplane 3 0 0x1000 [SRAM READ]
```

Figure 30 • Linux Command - SRAM Read/Write
DIP Switch Status
Dip switch on IGLOO2 Evaluation Kit board consists 4 electric switches to hold the device configurations. Linux PCIe utility reads the corresponding switches (ON/OFF) state.

```
# ./pcie_ctrlplane 4 [DIP Switch Status]
```

![Figure 31 • Linux Command - DIP Switch](image_url)
PCIe Configuration Space Display

PCIe Configuration Space contains the PCIe device data such as Vendor ID, Device ID, and Base Address 0.

Note: Root privileges are required to execute this command.

```
# ./pcie_ctrlplane 5 1 [Read PCIe Configuration Space]
```

![Image of PCIe Configuration Space Display](image)

Figure 32 • Linux Command - PCIe Configuration Space Display

Superseded
PCIe Link Speed and Width
Root privileges are required to execute this command.

#.pcie_ctlrplane 5 2 [Read PCIe Link Speed and Link Width]

Figure 33 • Linux Command - PCIe Link Speed and Width

Superseded
### Figure 34 • Linux Command - PCIe Link Speed and Width

<table>
<thead>
<tr>
<th>Capabilities</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0000</td>
<td>PCIe Gen 4x Width, Gen 3x Speed, Gen 2x Power, Gen 1x Data Rate</td>
</tr>
<tr>
<td></td>
<td>0001</td>
<td>PCIe Gen 5x Width, Gen 4x Speed, Gen 3x Power, Gen 2x Data Rate</td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>PCIe Gen 6x Width, Gen 5x Speed, Gen 4x Power, Gen 3x Data Rate</td>
</tr>
<tr>
<td></td>
<td>0100</td>
<td>PCIe Gen 7x Width, Gen 6x Speed, Gen 5x Power, Gen 4x Data Rate</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td>PCIe Gen 8x Width, Gen 7x Speed, Gen 6x Power, Gen 5x Data Rate</td>
</tr>
</tbody>
</table>

**Note:** The above table is a simplified representation of PCIe link state information. For a full understanding, please refer to the Linux kernel documentation or the system's PCIe configuration settings.
PCIe Interrupt Control (Enable/Disable) and Interrupt Counter

IGLOO2 Evaluation Kit enables/disables the MSI interrupts by writing data to its PCIe configuration space.

Interrupt counter holds the number of MSI interrupts got triggered by pressing the SW4 push button.

#. /pcie_ctrlplane 6 0 [Disable Interrupts]
#. /pcie_ctrlplane 6 1 [Enable Interrupts]
#. /pcie_ctrlplane 7 [Interrupt Counter Value]

Figure 35 • Linux Command - PCIe Interrupt Control

Read Device Serial Number

The IGLOO2 Evaluation Kit device serial number must be read by using the Linux PCIe application utility command.
Conclusion

This demo describes how to access the PCIe EP and display the device serial number feature of IGLOO2 by implementing a low bandwidth control plane design with BFM simulation. This demo provides a GUI for easy control of PCIe EP device via Jungo drivers for windows platform and also provides a Linux PCIe application for easy control of PCIe EP device via the Linux PCIe Device Driver.
Figure 1 shows IGLOO2 Evaluation Kit board.

Figure 1 • IGLOO2 Evaluation Kit Board
Figure 1 shows how to line up the IGLOO2 Evaluation Kit PCIe connector with the adapter card slot.

*Figure 1* • Lining up the IGLOO2 Evaluation Kit Board

**Note:** The Notch (highlighted in red) does not go into the adapter card.
Figure 2 shows IGLOO2 Evaluation Kit PCIe connector inserted into the PCIe adapter card slot.

Figure 2 • Inserting the IGLOO2 Evaluation Kit PCIe Connector
Figure 3 shows the PCIe adapter card and the IGLOO2 Evaluation Kit connected to the laptop.
The following table shows the important changes made in this document for each revision.

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