Development of Radiation-Hardened Flash-Based Field Programmable Gate Array RTG4

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Abstract

The development of the first radiation hardened Flash-based field programmable gate array, RTG4, is presented and discussed. Both total ionizing dose (TID) and single event effects (SEE) are hardened primarily by design techniques and secondarily by processing: TID hardenings are applied to the Flash configuration cells and high-voltage MOSFETs; SEE hardenings are applied to fabric flip-flops, fabric SRAMs, clock distribution networks, phase lock loops (PLL), SERDES blocks, and whole chip for single event latch-up (SEL). Radiation tests to investigate the efficacy of these hardening methods are performed, and the results demonstrate satisfactory radiation performance in every aspect.

Introduction

This paper presents and discusses the development of the first radiation-hardened Flash-based field programmable gate array (FPGA) —RTG4. The motivation of the challenging endeavor is to offer a unique solution for space electronics: a radiation-tolerant FPGA is both non-volatile and reconfigurable. The focus will be on the radiation-hardening part of the development. RTG4 uses the same 65 nm manufacturing technology as its non-hardened sibling SmartFusion2 (SF2) [1].

As shown in Fig. 1, RTG4 is a high-speed (300 MHz) and radiation tolerant (RT) FPGA targeting for signal processing applications. It is manufactured by a low-power 65 nm process with high reliability and radiation tolerance. It possess many advanced features: Flash-based FPGA fabric core has up to 150 K Logic Elements (LE), 462 18 bit x 18 bit Math Blocks, 5.12 Mbits of LSRAM, 315 Kbits of μSRAM, and 381 Kbits of μPROM; high speed clock conditioning circuit (CCC) has phase locked loops (PLL); high-speed interface includes 24 3.125 Gbit/sec SERDES lanes, 2 PCIe Endpoints, a DDR2/3 SDRAM controller, and SpaceWire Clock-and-Data Recovery Circuits; Input-Outputs (I/O) have 240 3.3 V MSIO, 300 2.5 V MSIOD, 180 2.5 V DDRIO, and 720 user IO.

For total ionizing dose (TID) effects, radiation-hardening by design (RHBD) techniques are applied at both the transistor and circuit level: the radiation-sensitive N-Flash configuration cell used in the commercial product SF2 is replaced by a complementary-Flash (C-Flash) latch [2] controlling a NMOSFET switch [3, 4]; the high-voltage thick-oxide NMOS (NHV) transistor, in the erasing and programming path, is redesigned at the shallow-trench isolation (STI) edge to eliminate the sub-threshold leakage; the new NHV, a.k.a. NHVX, is also back biased during the normal operation to reduce the radiation-induced threshold-voltage (V_T) shift.

For single event effects (SEE), the radiation hard by design (RHBD) techniques are applied both in the hardware and software: the flip-flop (FF) in the fabric LE is triple-module redundant (TMR) and it also has a filtering function to reduce the soft errors caused by the single event transients (SET); the fabric LSRAMs and μSRAMs are protected by the error detection and

correction (EDAC) technique of single error correction and double error detection (SECDED), and ,to avoid multiple bit upset (MBU) in a word, the minimum distance between separate bits in a word is extended to 9 bits at the layout stage; the global signals for clock distribution network and reset are hardened by triplicating and analog voting; the PLL is also TMR hardened; the high-speed SERDES blocks are hardened with TMR and SET filter. Finally, single event latch-up (SEL) is hardened through layout-design rules and well doping.
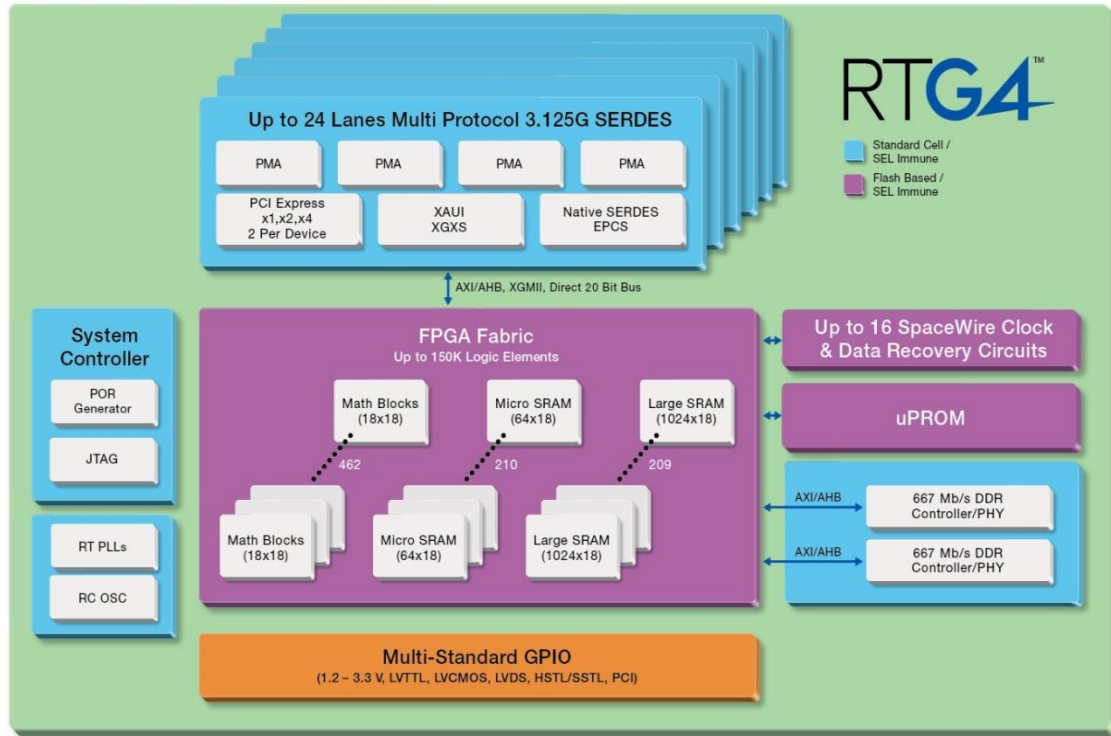

Fig. 1   Block diagram showing the functional components in the 65 nm radiation tolerant Flash-based FPGA—RTG4.

In the following sections, first a short radiation experimental description will be presented then followed by the TID and SEE hardening methods and test results on the first RTG4 product, RT4G150. Attempts to confirm the hardening goals will be the focus.

TID and SEE Experiments

TID tests on the first product in the RTG4 family, i.e. RT4G150, are performed at NASA-Goddard and DMEA using the gamma-ray irradiator: the dose rate is in the range of 3 to 5 krad(SiO$_2$)/min at ambient temperature; the annealing effects are deemed not significant and all the measurements are performed within an hour post-irradiation. X-ray irradiation using ARACOR Irradiator at Vanderbilt is used for transistor level tests: each measurement step is performed with a 2 min delay post-irradiation.

SEE tests on the product are performed at LBNL and TAMU using 16 MeV/n cocktail and 15 MeV/n beam respectively. Elevated temperatures of the range about $100 \pm 5°C$ are applied to the DUT for the single event latch-up (SEL) testing.

Since DUT being in CG1657 package is in a flip-chip form, test samples are back-grinded to within $100\ \mu m$ thickness for proper ion penetrations. For SEL testing using high LET ions at TAMU, the irradiation is performed in vacuum, again, for proper ion penetrations. At LBNL, the vacuum is always the irradiation environment.

RTG4 TID Hardening and Test Results

TID hardening techniques are applied to critical devices—Flash cells and high-voltage MOSFETs. The TID effects are measured both on the RT4G150 product and test devices: for product the critical electrical parameters are the propagation delay and standby power-supply current; for test devices the critical data are the sub-threshold leakage current and V_T shift of NHV devices.

Hardened Flash Cell—From N-Flash to C-Flash Cell

The original Flash configuration cell used in the non-hardened commercial product—SmartFusion2—is an N-Flash. As shown in Fig. 2, the N-Flash cell comprises two floating-gate transistors, called sense and switch respectively, who share the same stacked gate. Sense is the smaller one which is constructed into a large array architecturally equal to a NOR-Flash memory array. The write operation, erasing or programming, goes through this sense device to configure the switch which, when opens, passes the critical signal. For the purpose, the switch is designed as large as possible for the speed during normal operation. Consequently, the size of the floating-gate area in a configuration N-Flash is about 20 x of a Flash-memory's. That makes the N-Flash-configuration cells immune to heavy-ion induced upset which was often found in the Flash-memory cells.

During the normal operation a constant bias of 1.2 V is applied to the control gate: for the erased N-Flash cell, threshold voltage is low and the switch is turned on; for programmed cell, threshold voltage is high and switch turned off.
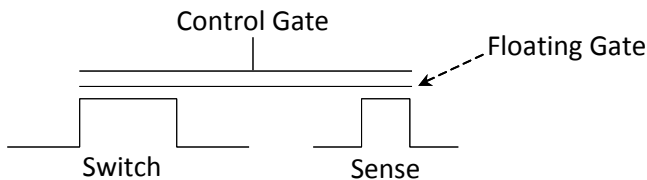
Fig. 2   Schematics show N-Flash cell: a larger Switch sharing the gates with a smaller sense.

The N-Flash based FPGA is not very tolerant to TID [5]. In normal operation under continuous irradiation, the worst-case electrical parameter is the propagation delay. Fig. 3a shows the TID testing results of 3 DUTs (device under test) each programmed with a long inverter chain with 7000 stages. Immediately at the start of the irradiation the degradation rises, and it reaches the 10% point (for the worst case among the three), the usual criterion for the tolerance, at approximately 24 krad(SiO_2). The degradation increases continuously super-linearly with the dose but the functionality is kept for TID as high as approximately 60 krad(SiO_2).

Fig. 3b illustrates a simplified schematics showing how two stages of inverter chain are connected by the Flash cell. An erased, i.e. turned on, switch connects two neighboring inverters. Basically TID will neutralize the charges stored in the floating gate like a natural decay behavior, and the V_T as a function of the total dose (γ) can be expressed as [6]:
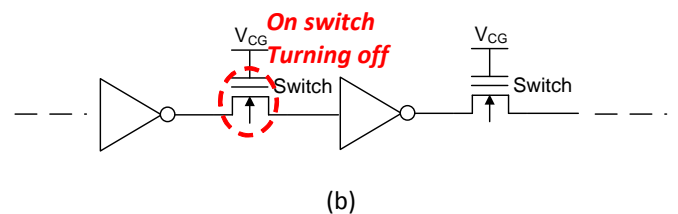
$$V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)] \cdot e^{-\gamma} \qquad (1)$$

Where $V_T(0)$ is the initial V_T and $V_T(\infty)$ the neutral V_T.

Therefore the V_T and the resistance of the on-state Flash switch will increase with TID, and subsequently the propagation delay degrades continuously with TID.

(a)

(b)

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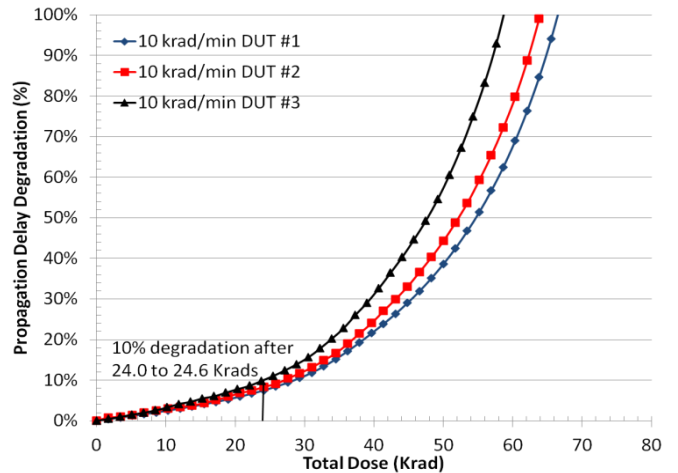
Fig. 3 Propagation-delay degradation versus TID in SF2: (a) the degradation increases right from the start and reach 10% around 24 Krad(SiO_2); (b) schematics show T turning off the Flash switch and increasing the propagation delay.

Another electrical parameter strongly affected by TID is the standby current of the core power-supply V_{DD} (1.2 V) that biases the Flash cells and functional logic elements. The test results showing the dependence on TID is in Fig. 4a. These data are acquired simultaneously with that of Fig. 3a: the current continuously increases slowly to a point and then shots up very quickly with a steep slope. This turning point for the worst data is approximately at 80 krad(SiO_2).

The root cause of the I_{DD}-TID characteristics is also due to the radiation effects on the Flash cell. As shown in Fig. 4b, a switch is often connected to the outputs of two buffers, and it has to be turned off to isolate them. In the other words, this isolation switch has to have high V_T to stay at the high-resistance off-state. According to equation (1), by TID effects, the high V_T will naturally decay toward to the neutral V_T and the isolation switch will be gradually turned on to cause a contention current flowing from V_{DD} to GND if the isolated buffers have different outputs. Note that in Fig. 4a the I_{DD}-TID characteristics are similar to the I_D-V_G of the NMOSFET: this is because that TID-induced decreasing V_T in the N-Flash is equivalent to increasing the bias V_G on its gate.
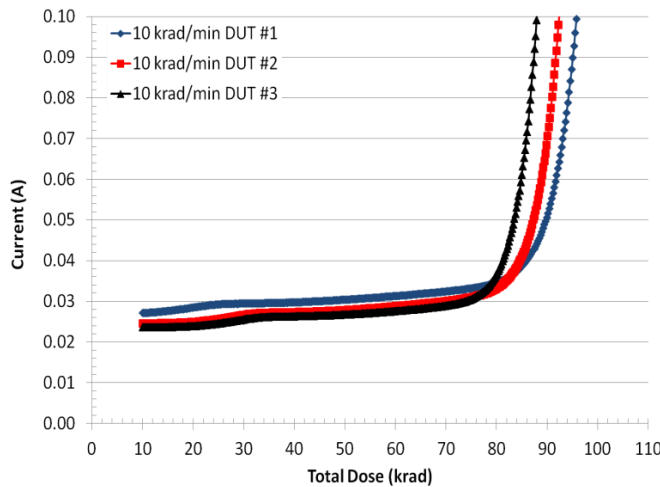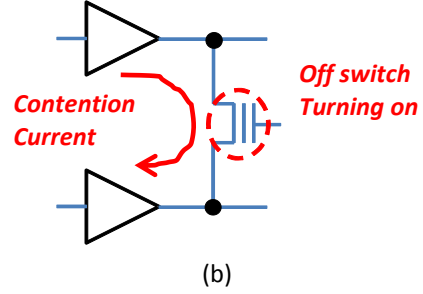
(b)

Fig. 4 Core power-supply current (I_{DD}) versus TID in SF2: (a) it increases slowly initially and then reaches to a turning point, approximately 80 krad(SiO_2), with a steep increasing slope afterwards; (b) schematics show TID turning on the isolation off-state Flash switch and increasing the contention current.

For the aerospace electronics, the TID tolerance has to be 100 krad(SiO_2) or above. Apparently, to reach this target the Flash configuration cell has to be hardened. In RTG4 the solution is using a radiation-hardened C-Flash cell to replace the N-Flash cell. As shown in Fig. 5, the C-Flash cell has a Flash memory part that controls a NMOSFET switch. This Flash memory is a complementary-Flash latch: it comprises a P-Flash pull-up and an N-Flash pull-down. There is also a constantly biased PMOS to serve as a load resistor to reduce the voltage drop between the P-Flash source and drain. This is to reduce band-to-band tunneling induced hot electron (BBHE) injection [7, 8] in the P-Flash when the C-Flash is at the off-state, as shown by the left-side schematics in Fig. 5.
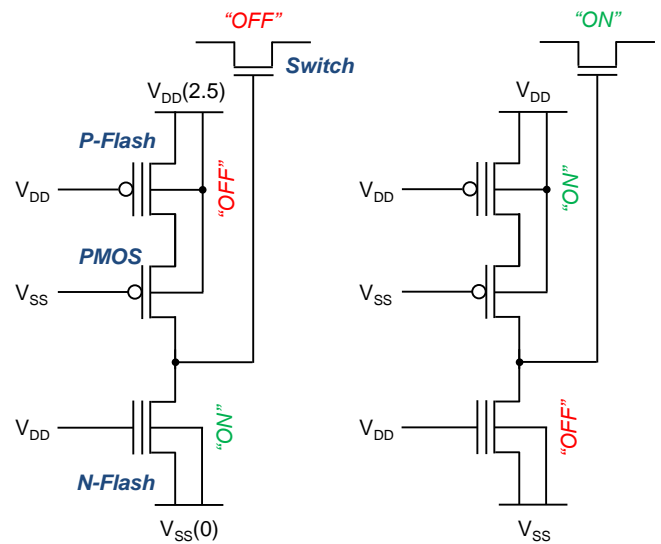

(a)

Fig. 5   C-flash cell: left is at the switch-off state; right at the switch-on state.

In this C-Flash configuration cell, the output of the Flash memory has a CMOS like therefore very sharp transition from V_{DD} to V_{SS} (or GND). TID will degrade the V_T of both the N-Flash and P-Flash cell towards to their neutral states and subsequently, as TID is increasing, an increasing totem current will flow from V_{DD} to V_{SS} through both the P-Flash and N-Flash. But as long as the CMOS-like transition point is not reached, the state of the Flash will hold and the switch's bias won't be degraded, and the drastic propagation-delay degradation in Fig. 3 and the power supply current exponentially surge at a critical point in Fig. 4 will not occur.

The TID testing results confirm the above theory. As shown in Fig. 6, using the same design of a 7000-stage inverter chain, up to 150 krad(SiO$_2$) the propagation delay has no measurable degradation and the core power-supply current (I_{DD}) increases only moderately.
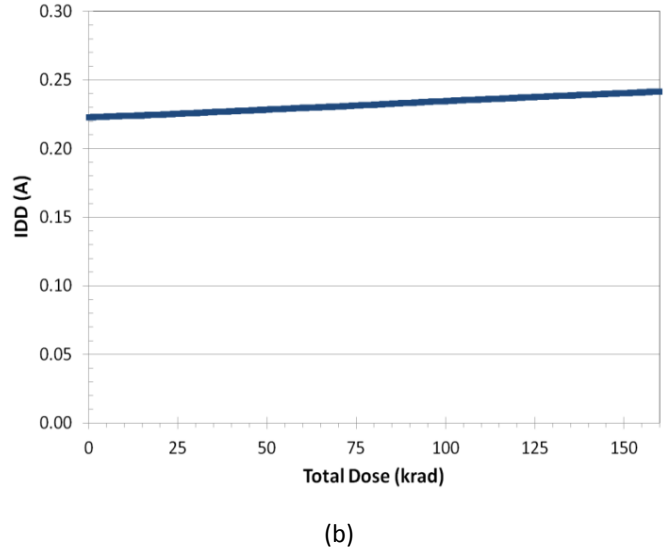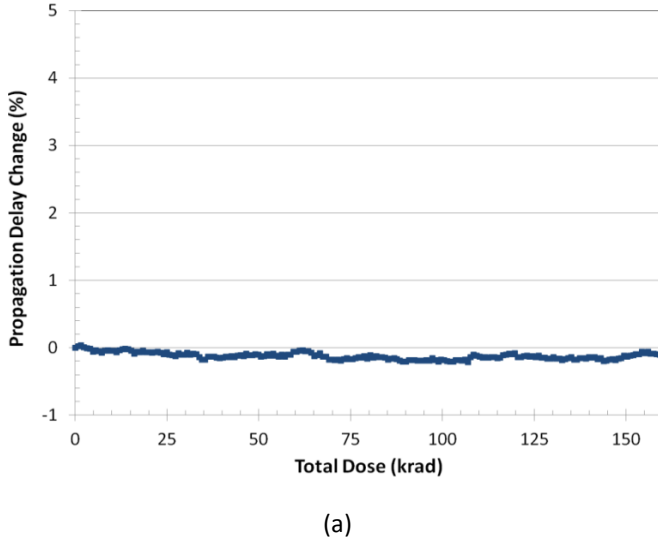

(b)

Fig. 6   RTG4 TID testing results: (a) propagation delay degradation versus TID; (b) power supply current (IDDA) versus TID.

High-Voltage NMOS Transistor Hardening

The high-voltage NMOSFET, i.e. NHV, in the programming circuits is also prone to adverse TID effects. The reasoning can be explained by examining a 2 x 2 C-Flash array as shown in Fig. 7. It shows a simplified biasing circuit during normal operation: V_{DD} (1.2 V) passes the turned-on high-voltage PMOSFET (PHV) to bias the P-Flash on the same row. This PHV is parallel to an NHV whose turn-on state will pass GND to the same P-Flash row.

This arrangement is necessary because the same circuit is used for the program/erase, and the same Fowler-Nordheim (FN) tunneling mechanism is used for both programming and erasing. Therefore both positive and negative high voltages have to be passed through from power sources to bias the Flash cells. The setting for positive bias is PHV-on and NHV-off and reverses the polarity for negative bias. During normal operation the TID effects turn on the closed NHV and degrade the bias on the Flash cell and subsequently endanger the functionality. Although there is no direct evidence on the circuit level that TID induced NHV degradation will cause an issue, for fool-proof, the NHV is hardened in RTG4.

For unhardened NHV, I_D-V_G plots in Fig. 8 indicate significant substrate leakage and V_T shift by TID effects. In RTG4 the NHV is redesigned to eliminate the edge,

(a)

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and the new device is called NHVX. Fig. 9 shows the improvement: comparing to Fig. 8, the sub-threshold leakage is completely gone. Also, not shown here, the V_T shift is further mitigated by back-bias technique. Test data shows that a negative 2.5 V bias on the body will reduce the 200 krad(SiO$_2$)-induced shift by half.

Note that, for the above testing data, the irradiation bias on NHV(X) is V_{DD}, while in normal operation such as that used in Fig. 6 the NHV is turn-off by biasing to GND. Nevertheless, the testing data are for qualitative reasoning and serve the purpose of demonstrating the hardening.
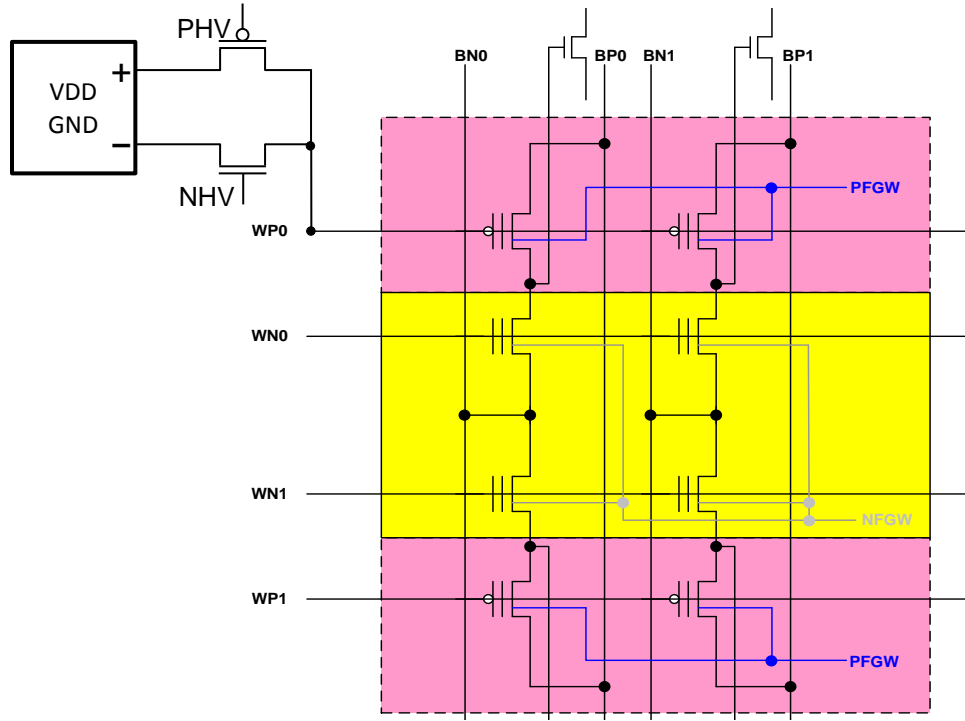

Fig. 7   Simplified Schematics shows how the word-line is biased in the C-Flash arrays: during operation PHV is turned on and NHV turned off to apply V_{DD} to the word-line.
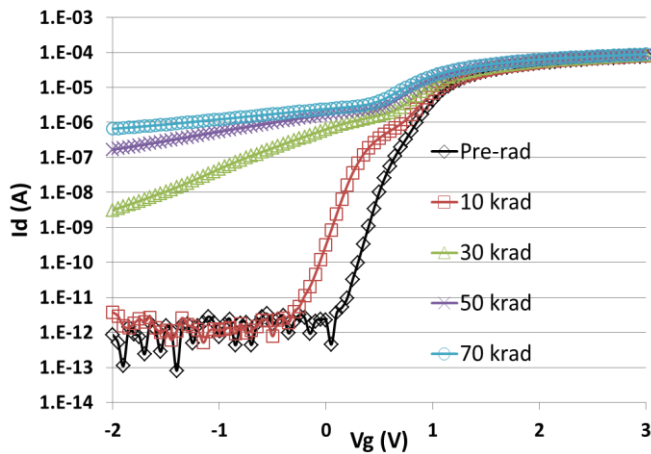

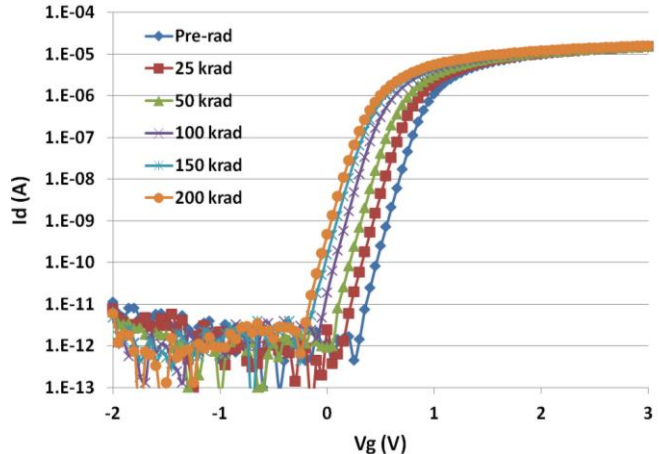Fig. 8 I_D-V_G plots show TID effects on NHV transistors.

Fig. 9 I_D-V_G plots show TID effects on NHVX transistors.

RTG4 SEE Hardening and Test Results

The SEE hardening has been pervasively applied to every particular functional circuit in the RTG4 product. Extensive tests are needed to cover all of them, and lessons have to be learned to complete some of them. This paper tries to cover the most important hardened circuits in RT4G150. However, some results are conclusive but some are preliminary and have to be further investigated. The SEE tested circuits and sub-systems include Flash configuration cells, fabric flip-flops, fabric imbedded SRAMs, phase lock loops (PLL), and SERDES blocks. Finally, SEL is tested in the scope of the whole chip.

Flash Cell SEE Hardening and Test Results

The C-Flash configuration cell is not only hardened for TID, it is also SEE hardened. The reasons are, first of all, the CMOSFET switch is not sensitive to SEE, and second, the same point as the TID hardening, both N-Flash and P-Flash in the same configuration cell has to be affected to possibly cause failures. Again the size factor is also important: comparing to the Flash-memory's cell, the size of either the N-Flash or P-Flash cell is significantly larger than that of a Flash memory, and they can easily tolerate a direct ion strike.

So far all the heavy-ion beam testing results at LBNL and TAMU support the above statement. More than 10 parts have been irradiated using various ions with effective LET from 1.16 to 103 MeV-cm^2/mg and the total accumulated fluence of them all are approximately 1×10^9 ion/cm^2; but not a single functional failure has been detected. Note that the functionality had been continuously monitored during the tests and about 10% of the total configuration cells are in the critical path. Also re-programming after heavy-ion irradiation is always successful, and the maximum equivalent TID of some DUTs exceed 100 krad(SiO$_2$).

In summary, under heavy-ion beam irradiation, the C-Flash configuration cell in RTG4 is significantly more tolerant than the N-Flash configuration cell in SF2 on the aspects of functionality and reprogramming ability.

Fabric Flip-Flop SEE Hardening and Test Results

The flip-flop in the FPGA fabric is hardened by SET-filtering and TMR. Fig. 10 shows the block diagram illustrating their operations. At the data input is the filter circuit to filter any voltage pulse shorter than 600 ps. The filtering principle is temporal voting. The later stage triplicates the signal and then performs the majority voting.
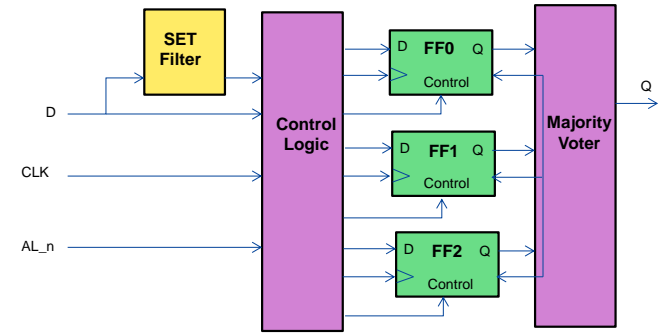

Fig. 10 Block diagram of STMRFF: TMR-hardened flip-flop and an SET filter circuit.

Fig. 11 shows the block diagram of the test design. The STMRFF is tested in a shift-register with 2000 stages; it is manually placed such that the upsets of row global buffers (RGB), used in the clock distribution networks, can be detected.

In the clock conditioning circuit (CCC) block, PLL generates four different frequencies simultaneously: 1 MHz, 50 MHz, 100 MHz, and 200 MHz. Each PLL output is connected to a counter/divider which generates a checkerboard data pattern at the negative edge. For each frequency, the clock and generated data pattern are fed into two shifter registers. The outputs of every two adjacent shift registers are connected to a triplicated comparison-error-count logic. Note that the PLL and divider/counter are in a separate control chip so they are not irradiated.

SEUs are collected simultaneously on all the channels. Once an error is latched in, an external circuit will collect the data and asynchronously reset the latch. If any SEU has occurred in the Flip-Flops, the XOR will evaluate to 1 and it will be latched. Both single SEU errors in a FF and burst errors caused by global SETs in the buffers of clock distribution networks (to be discussed in the next section) can be detected between two adjacent chains. Obviously, the ion-beam flux has to be optimized so each single event can be detected unambiguously.

Fig. 12 shows the STMRFF test results displaced as the cross section versus heavy-ion LET. That the cross

section continuously and significantly increases with the clock frequency indicates, above 50 MHz, SET induced soft errors to be dominant. CREME96 calculated error rates in the standard environment and shielding, GEO-minimum and 100 ml thick Aluminum, are listed in the Table I.

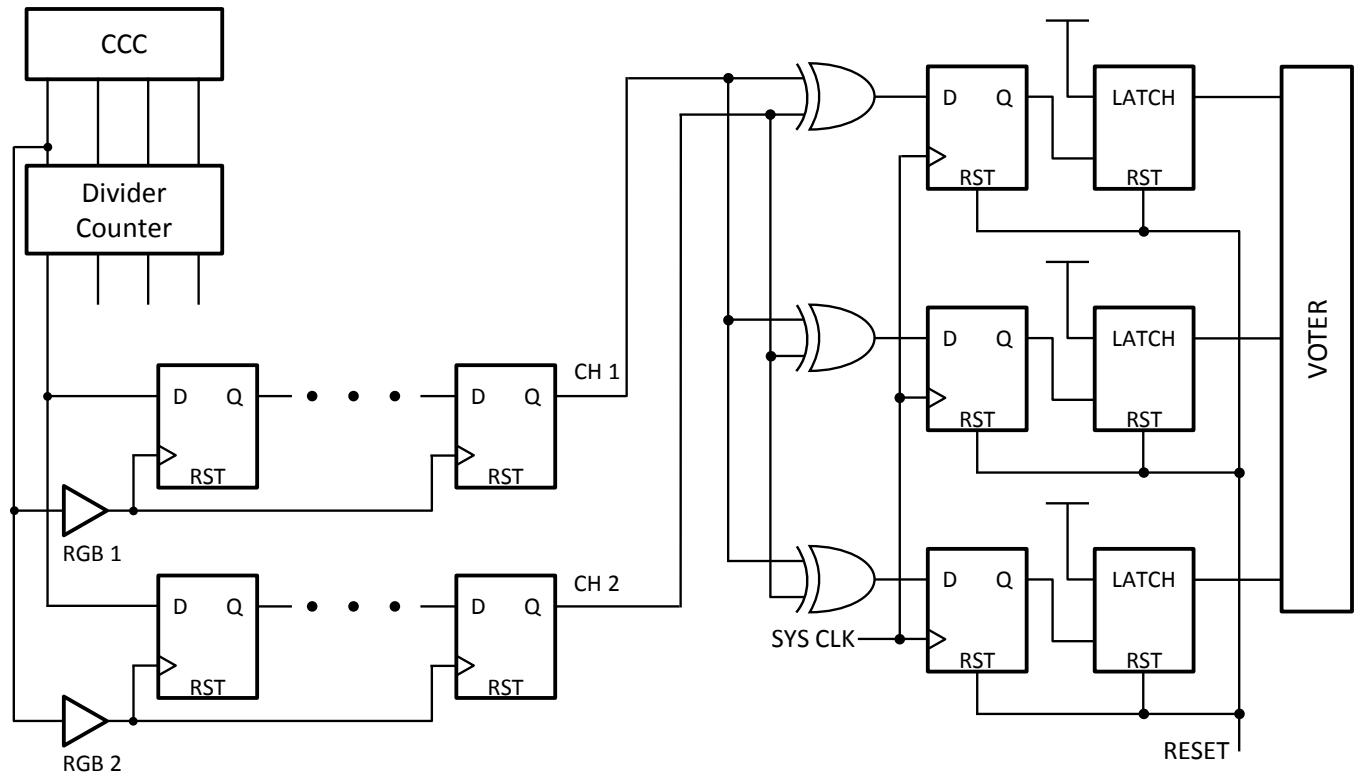| Frequency	Upset Rate
1 MHz	2.26×10^{-12} upset/bit/day
50 MHz	6.36×10^{-10} upset/bit/day
100 MHz	2.43×10^{-9} upset/bit/day
200 MHz	2.26×10^{-8} upset/bit/day

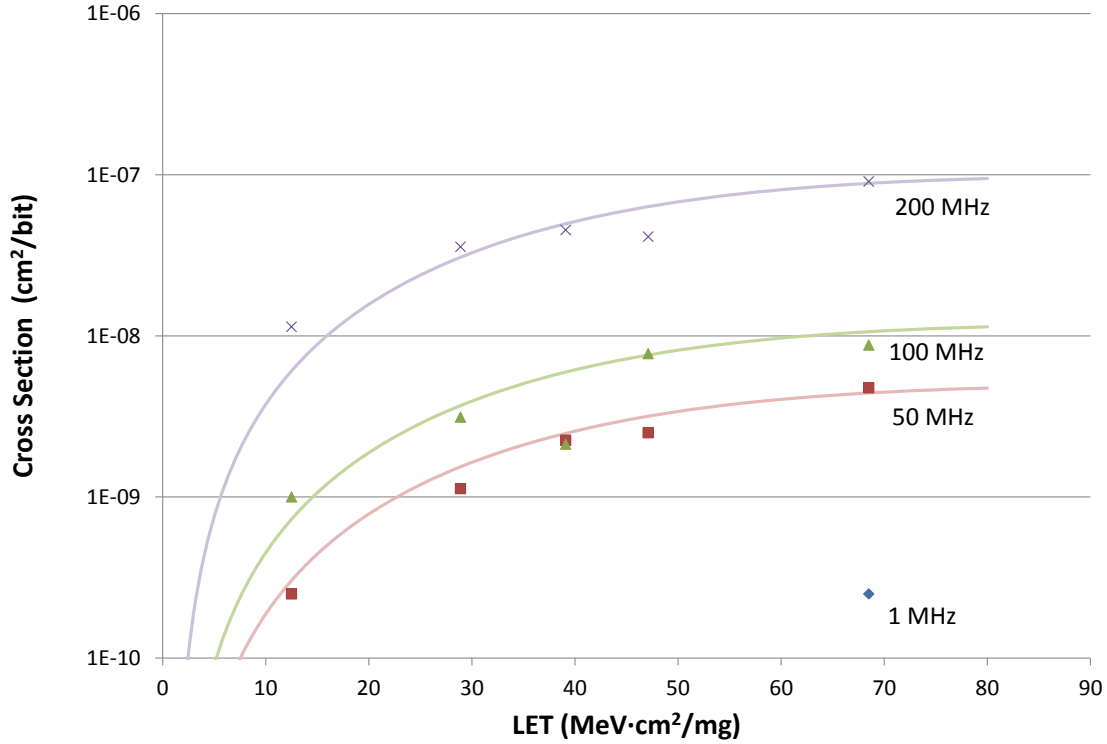Fig. 11   Block diagrams showing the STMRFF SEE testing design.

Fig. 12 SEU cross section versus LET of fabric STMRFF: the strong dependence of cross section on the frequency indicates SET induced soft errors dominating the high-frequency events.

Clock Distribution Networks Hardening and Test Results

The clock distribution network is hardened by various techniques to optimize the SET, speed, and area. The techniques include RC filtering, analog voting, and tuning capacitive load.

The test design is integrated with the STMRFF as shown in Fig. 11. The method to detect clock upset has been discussed in the previous sub-section. The results are that no clock upset is seen for LET 16.5-25 MeV-cm^2/mg with 1.2×10^8 ions/cm^2 fluence. The test is performed using a positive edge triggered clock operating at 10 MHz using a checkerboard pattern while observing for phase shift to a golden model. Additionally, no clock upset is seen when using a static clock for fluence of 9×10^7 ions/cm^2 at LET 16.5-25 MeV-cm^2/mg.

Although, in theory, clock upset is independent of the frequency, but it is still desired to confirm that by testing at higher frequencies—like 200 MHz used for the STMRFF testing. Unfortunately the noise in the high frequency testing prohibits collecting faithful data, and most global errors collected at high frequency are proved to be noise.

Fabric SRAM Hardening and Test Results

There are two types of SRAM in the FPGA fabric: the μSRAM and LSRAM. Both of them are hardened for single error correction and double errors detection (SECDED): the bits separation in the same word is 9-bit apart to eliminate double errors due to a single event; circuits to implement EDAC code for each word are SEU hardened.

First of all, for clearly definition of bit-errors in a word, the multiple-cell upset (MCU) is defined as more than one bit simultaneously upset by a single event, and multiple-bit upset (MBU) as more than one bit simultaneously upset in the same word by a single event. Therefore, MBU is a subset of MCU, and each MBU will cause an error in the EDAC word protected by SECDED mechanism.

The easily performed static and indirect tests without invoking EDAC-SECDED have been done on

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RT4G150 parts. Every bit-upset is time-tagged so MCU can be detected and its size can be measured by the number of bits. Also, the detected MCU is always a cluster of upset bits. Fig. 13 and 14 show the cross-section of MCU versus LET for μSRAM and LSRAM respectively. Each line represents a particular size of MCU. The largest MCU can be detected in μSRAM is 5-bit, and in LSRAM is 8-bit. Since the separation of two adjacent bits in both SRAMs is 9-bit, there is no possibility for the occurrence of MBU in them.

That the maximum MCU size (5-bit) in μSRAM is smaller than that (8-bit) in the LSRAM is likely due the cell-size difference: a μSRAM is about twice the size of a LSRAM.
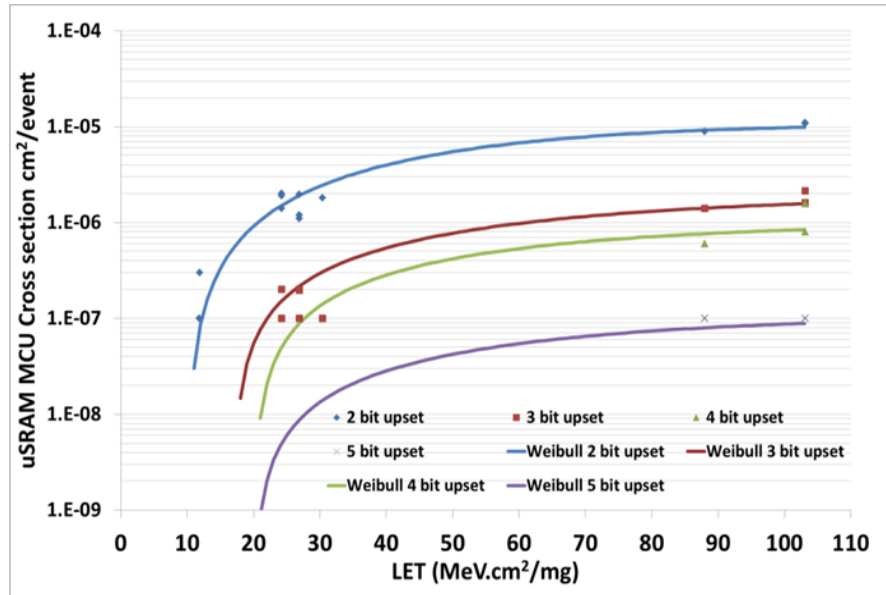

Fig. 13 Plots show the cross-sections versus LET for MCU of various sizes in μSRAM.
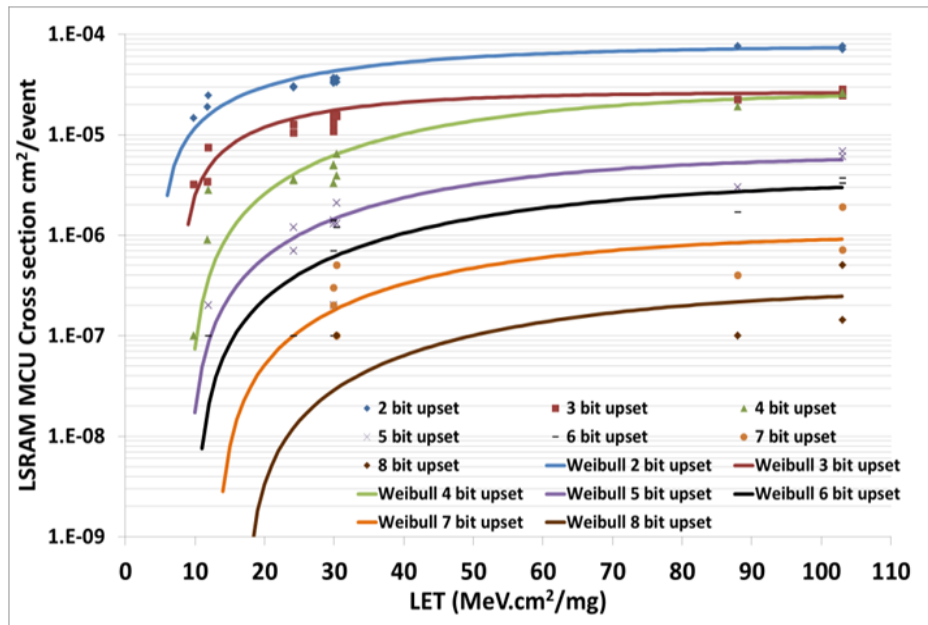

Fig. 14 Plots show the cross-sections versus LET for MCU of various sizes in LSRAM.

PLL Hardening and Test Results

Fig. 15 shows a block diagram of the TMR PLL. The outputs of three copies of PLL are voted to generate

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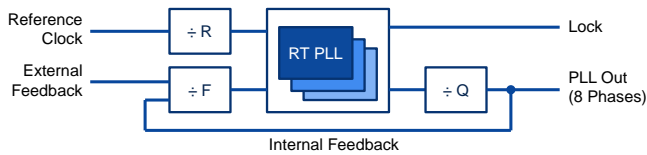clock signals. The maximum operation frequency is 400 MHz.

Fig. 15 Block diagram of TMR PLL.

The PLL can be configured with several feedback methods: *PLL Internal* mode is used for the hardened mode; *CCC (Clock conditioning circuit) Internal* or *CCC External* mode is available for unhardened modes and can be used to control skew or used in applications where higher frequencies and low jitter are required.

In the hardened case, the individual PLL Lock signals as well as the output is voted. If any of the internal 3 PLLs are out of lock, the individual PLL will automatically be restored.

The preliminary testing results show that the output of the PLL is hardened in the triplicated case, but the lock signal can have transient errors which will recover in 100-150 µs. In the unhardened mode, the PLL will lose lock and will need a PLL_PwrDwn_n signal assertion to recover. This power down signal is sufficient and does not require a power cycle on the supply pin.

Lastly, PLL hardening can impact SEU error rate due to jitters. In order to understand this, further beam testing is needed.

Fig. 16 shows the SEE testing design for PLL. The main purpose is to detect if PLL loses its lock and how it recovers when its lock is lost. The results are shown in Fig. 17: only self-recoverable lost-lock events have been observed, thus verifies the hardening. In

unhardened PLL in SF2, it has unrecoverable lost-lock events by SEE.

SERDES Hardening and Test Results

Radiation hardening techniques including custom design rules are applied to the internal SPLL, REFCLK and also PCIe FIFOs with ECC. Asynchronous resets are hardened using glitch-suppression filters and with use of hardened buffers for reset distribution.

SERDES configuration registers are programmed with the use of a soft processor or state machine. Although the SERDES configuration registers are not TMR'd and can have SEU, they can be read and refreshed through an APB interface. In the event of upset or link loss, the registers can be re-loaded with a known value using this soft processor or state machine. References about RTG4 SERDES can be found on the website [1].

Fig. 18 shows the block diagram of the SEE testing on SERDES: in each lane the SERDES block is configured as EPCS and totally four parallel lanes are tested simultaneously; a Master chip does the sending of the original PRBS (pseudo-random bit stream) signal and also comparing it with the loop-back signal; the Master also configures SERDES blocks through the CoreABC. The CoreABC, PRBS generator and PRBS checker on the DUT are generated by the SEE-hardened fabric logic, and therefore their contribution to the detectable SEE errors is negligible.

Fig. 19 shows the test results of two error-modes: there are transient SET soft errors and the SERDES function will self-recovers; unrecovered SERDES function failures exist, and they are proved due to the upset of the SERDES registers because the reseting registers through CoreABC can recover the functionality.
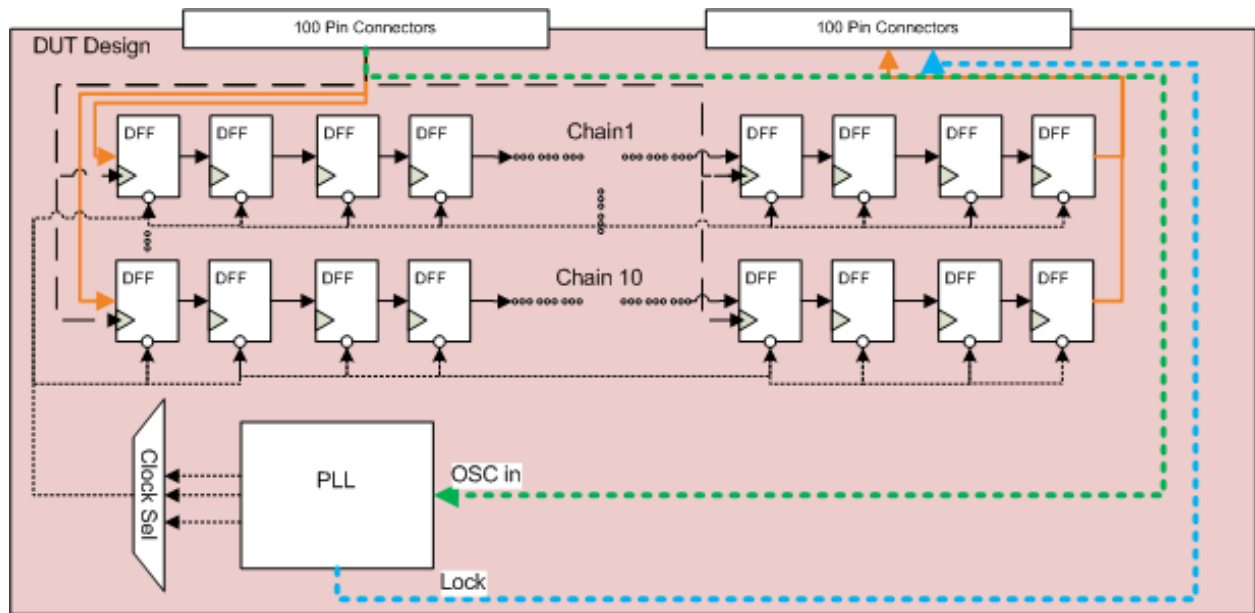
Fig. 16 Block diagram showing SEE testing design of PLL: the Lock signal is monitored to observe lost-lock events.
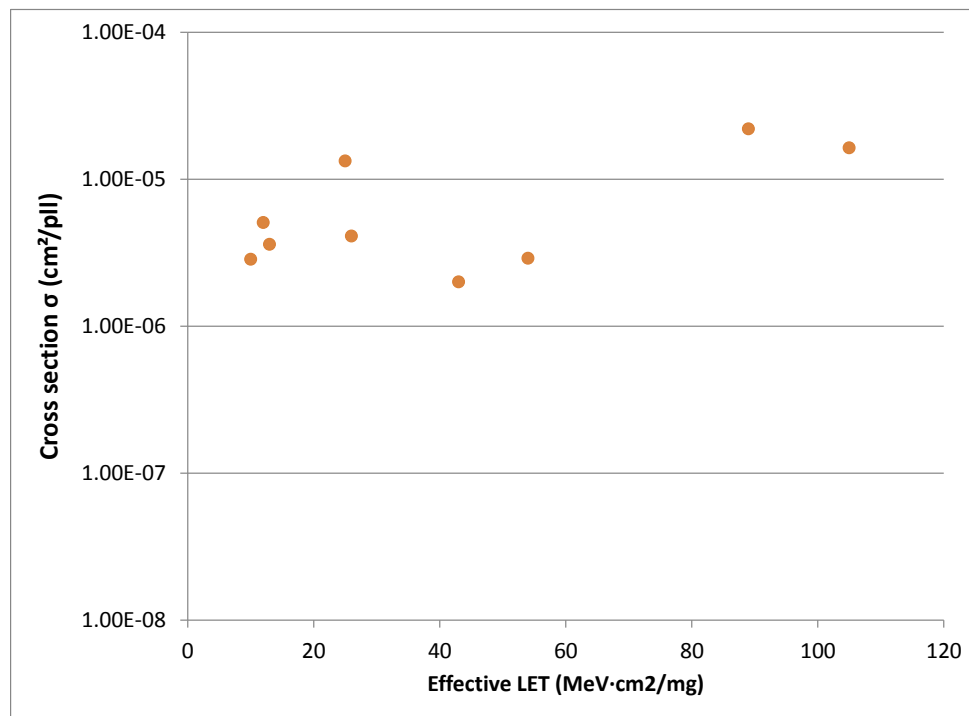

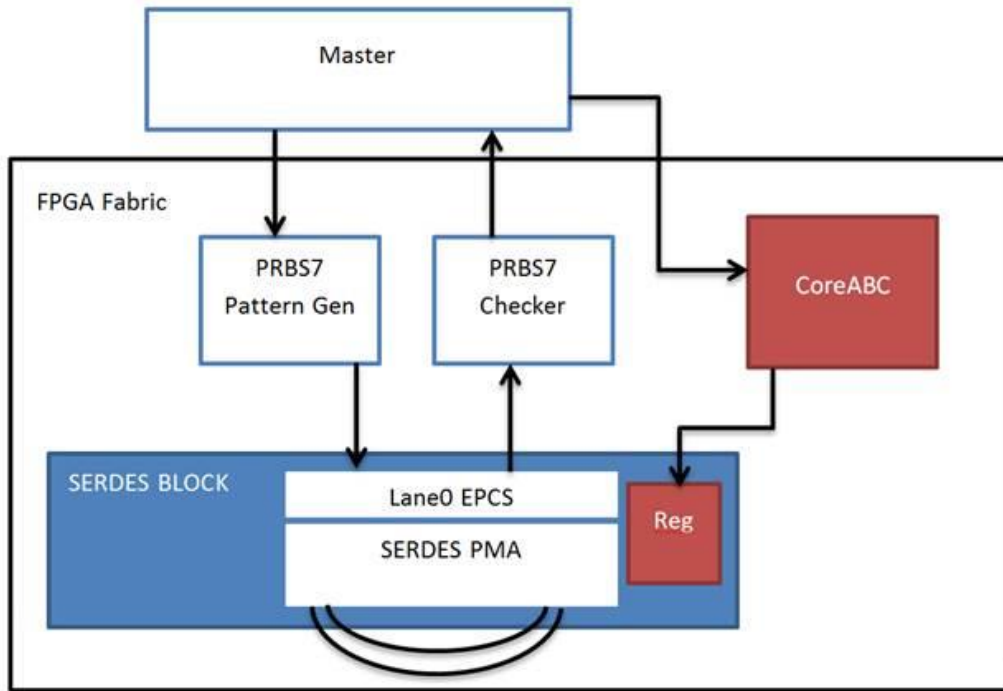Fig. 17 SEE cross section versus LET of PLL self-recoverable lost-lock.

Fig. 18 Block diagram showing SERDES SEE testing design: a Master chip sends a loop-back signal and does the comparison of the original signal with return signal; the Master configures the SERDES through the CoreABC processor on the DUT.
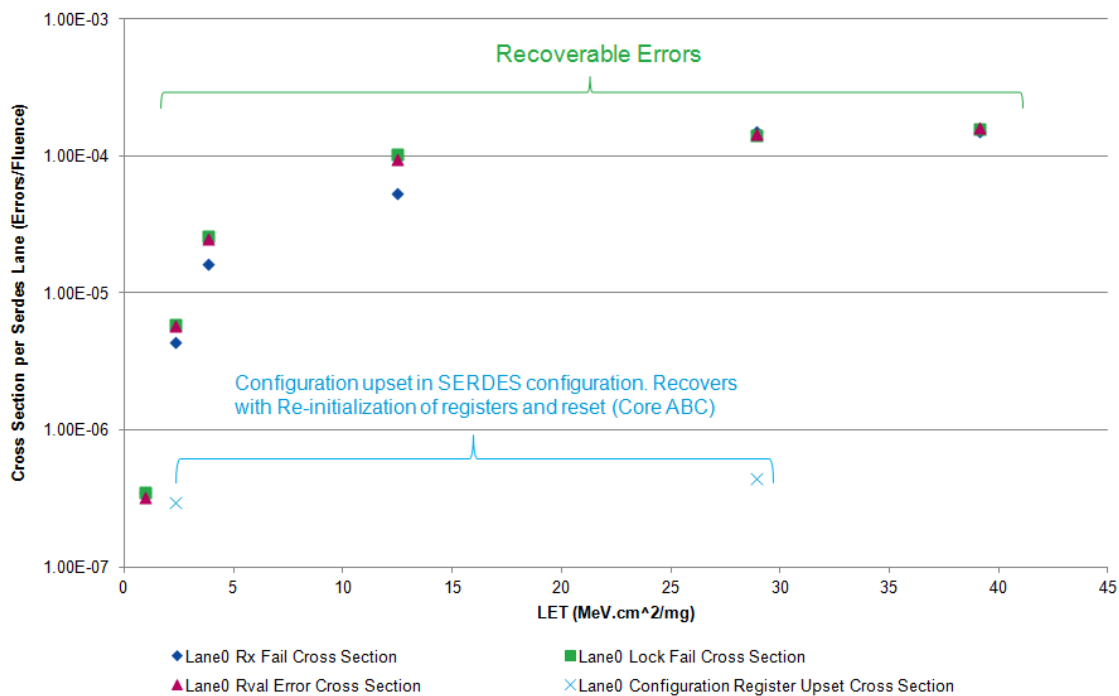

Fig. 19 SEE cross section versus LET of the SERDES block: transient SET-induced self-recoverable errors are dominant SEE; rare non-self-recoverable errors are due to SERDES configuration register upset and needs to be reset by CoreABC.

SEL Hardening and Test Results

The SEL hardening is implemented by design rules: the body ties have rules to ensure their high density;

the input-output (IO), which performs at 2.5/3.3 VDC, has guard rings at the well boundaries. Note that the process, although the same as commercial SF2, has been optimized to reduce the gain of the parasitic bipolar transistors in the loop to form the parasitic PNPN structure.

Test results on three RTG4 devices show that at 100° C no SEL event occurs by irradiated with ions with effective LET of 103 MeV-cm2/mg for total fluence of 1.25×10^8 ions/cm^2.

Table II

Temperature	LET (MeV.cm^2/mg)	SEL	Fluence (ions/cm^2)
	9.8	0	7.89x10^7
	13.74	0	1.10x10^8
	26.9	0	1.05x10^8
	31.06	0	5.00x10^7
	89	0	5.00x10^6
Room Temp	103	0	2.60x10^7
	58	0	4.00x10^7
	89	0	1.11x10^8
100 ºC	103	0	1.25x10^8

Conclusion

The first RHBD Flash-based FPGA has been tested for both TID and SEE to verify its hardness.

TID hardening is done on the configuration Flash cells and a new C-Flash cell replaces the non-hardened N-Flash. The propagation delay of the long inverter chain does not increase with TID up to 150 krad(SiO$_2$), and indicates that the on-state C-Flash is hardened. The standby power supply current of the core only increase moderately with TID up to 150 krad(SiO$_2$), and indicates that the off-state C-Flash is also hardened. For prevention measure, High-voltage NMOSFET is TID hardened by eliminating the field edge and thus the sub-threshold leakage and it also can be back-biased to reduce V$_T$ shift.

SEE hardenings are done in every possible functional block: fabric flip-flops are hardened by temporal filtering and TMR; the clock distribution networks are hardened by RC filtering analog voting and load capacitance tuning; fabric SRAMs are hardened by SECDED, and two adjacent bits in one word are spaced 9-bit apart in physical distance; PLL are hardened by TMR and special cares have been applied to Lock condition; SERDES blocks have been

hardened by design rules, glitch filters, and sizing; the whole chip is hardened for SEL by design rules and well doping. The SEE testing results indicate that the fabric elements have been completed hardened; the initial data for clock distribution networks, PLL and SERDES show various degrees of hardening; finally, the SEL is immune to LET of 103 MeV-cm2/mg at 100° C.

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