LiteFast

UG0701 User Guide

Microsemi
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Introduction

For applications, which are high speed and data intensive, there are many serial protocols that exist.

In order to provide the low cost, scalable, high speed solution, and light weight in terms of utilization Microsemi has designed the LiteFast, targeting the Microsemi next generation FPGA devices.

Similar to other serial protocols, the LiteFast has all those flavours like in built flow control to maintain the link activity when the applications are not involved in transfer of data.

LiteFast Transmitter embeds the application data into data frame and initiates the data transmission. LiteFast Receiver extracts the application data from data frame and delivers the application data to the user interface. An idle frame is transmitted when there is no application data for transmission, the physical link between systems is maintained by idle frames.

For a given system of targeted application, the received data is extracted from the data frame and then is written into a receiver buffer. If the available storage space of receiver buffer approaches to 0, LiteFast would notify the remote LiteFast Transmitter to pause data frame transmission to prevent receiver buffer's overflow. If available storage space of receiver buffer is greater than a threshold value, the LiteFast receiver would notify the remote LiteFast transmitter to resume data frame transmission. Threshold value should be at least 128 bytes and upper limit of threshold is fixed by user application.

LiteFast supports 1x or 2x or 4x lanes per SERDES. The data bus width for each lane for a SERDES can be minimum 8-bits or maximum 16-bits. When multiple lanes are used, then the data transferring bandwidth between two systems could be greater than a single SERDES maximal data transferring bandwidth.

Figure 1 shows LiteFast application diagram.

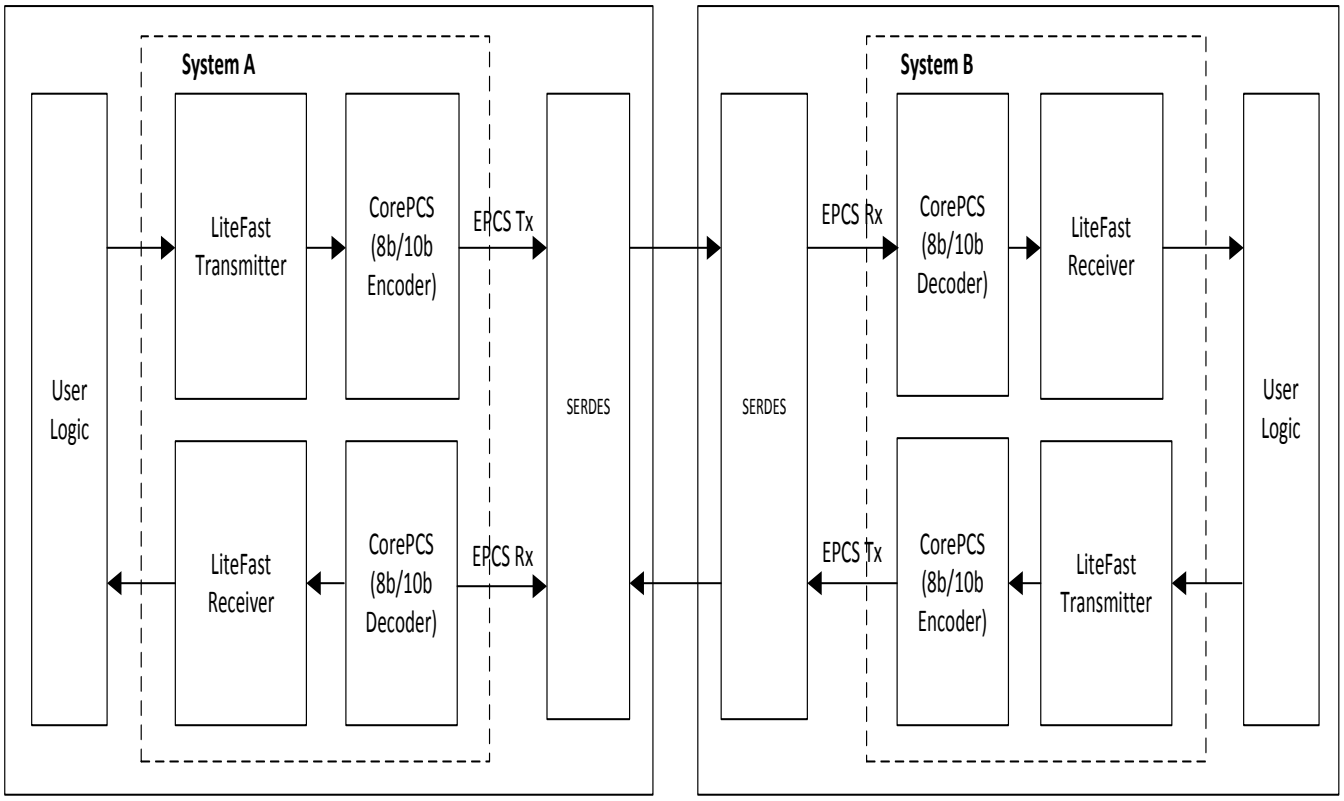

Figure 1 · Typical Application for LiteFast

As shown in Figure 1, System A and System B transfers data through a pair of high speed SERDES lane. Taking the direction from System A to System B to show how the system works.

In System A, LiteFast transmitter embeds the application data from user logic into the data frame, it also generates an idle frame when there is no application data. Data frame and idle frame are encoded to 10-bit data in 8B10B encoder module. The 10-bits data is send to System B through the high speed SERDES lane.

In System B, the parallel data stream from the SERDES back end receiver is decoded to 8-bits in 8B10B decoder module. LiteFast Receiver recognizes data frame and idle frame, it extracts application data from the data frame payload and drops the idle frame.

Key Features

The key features of LiteFast are:

- Idle frame for establishing and maintaining the link and data frame for user data
- Supports 1x or 2x or 4x per SERDES
- Supports cumulative speed from 4Gb/s to 10Gb/s for x4 lanes per SERDES
- Word alignment, block alignment and lane alignment for receive chain
- Independent of user application and device independent
- Serial full duplex or serial simplex operation
- Support for CRC-32
- Support for hot plug
- Data packet size: 1~128 bytes of application data. The length of payload must be multiple of 8, otherwise K28.4 bytes are filled to meet the requirement.
- Idle packet: 8 byte
- Flow control scheme: Token exchange
- Support for Little Endian for user logic

Core Architecture

Design Description

LiteFast uses the following two frames for data transfer and link establishment:

- Idle frame
- Data frame

For enabling point to point communication, LiteFast Transmitter uses IDLE frames to establish link. After serial link is up, LiteFast Transmitter embeds application data into data frames and sends it to remote LiteFast Receiver. When there is no data transmission, LiteFast IP uses IDLE frame to maintain the link.

Figure 2 shows the Idle frame structure.

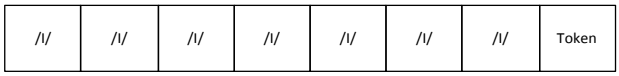

Figure 2 · Idle Frame Structure

Token is one byte. /I/ characters depicted from Figure 2 could be one of the following characters:

- /K/ character (K28.5).
- /R/ character (K28.0).
- /A/ character (K28.3).

The rules for /I/ character are:

- When multiple lanes are transmitting /I/ characters simultaneously, /I/ on all lanes must be the same character.
- /A/ character must be the first byte of idle frame.
- There must be at least 31 bytes between two /A/ characters.
- If a /I/ character is not /A/ character, it should be /K/ or /R/ character randomly.

When multiple lanes are used for data transfer, LiteFast Receiver makes all the lanes aligned by using /A/ character. The receiver may also use /K/ bytes to align the 10-bits word.

Flow control is established by token exchange.

Data frame includes application data. Figure 3 shows the data frame structure.

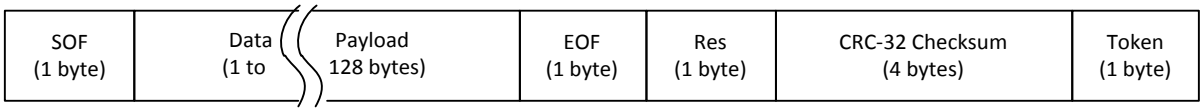

Figure 3 · Data Frame Structure

Data frame fields includes the following: Start of Frame (SOF), data payload, End of Frame (EOF), CRC-32 checksum, and token byte.

SOF segment includes: 1 K28.1 byte. LiteFast Receiver recognizes the header of data frame by SOF segment.

Data payload contains: 1~128 bytes of application data. The length of payload must be the multiple of 8, otherwise PAD (K28.4) bytes are filled to meet this requirement.

EOF is one K28.7. LiteFast Receiver recognize the end of data payload by EOF.

Res is reserved segment and is 1 byte.

CRC-32 field contains the CRC-32 check sum for data payload. The polynomial is as shown below.

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

EQ1

Flow Control

In order to avoid over-flow condition in receive chain, local receiver communicates the available buffers to local transmitter. Local Transmitter communicates the same to the remote receiver via tokens. The remote LiteFast Transmitter should pause data frame transmission when local receiver buffer is almost full, and the remote LiteFast Transmitter should resume data frame transmission when receiver buffer is not almost full.

The receive buffer's available storage space is encoded to Token byte, which ranges from: 0~255. Token is set to 1 when there are 0~127 available bytes in receiver buffer. Token is set to 2 when there are: 128~255 available bytes in receiver buffer. The rule of token calculation is as shown in the following equation.

$$Token = Int\left(\frac{Rx\ Buffer\ \text{available bytes}}{128}\right) \qquad (Int()\ means\ getting\ integer)$$

EQ2

Token field indicates the number of bytes available in remote receiver. Remote Transmitter pauses data frame transmission, if the local receiver buffer is not able to store more than one data frame. Figure 4 shows the flow control mechanism.

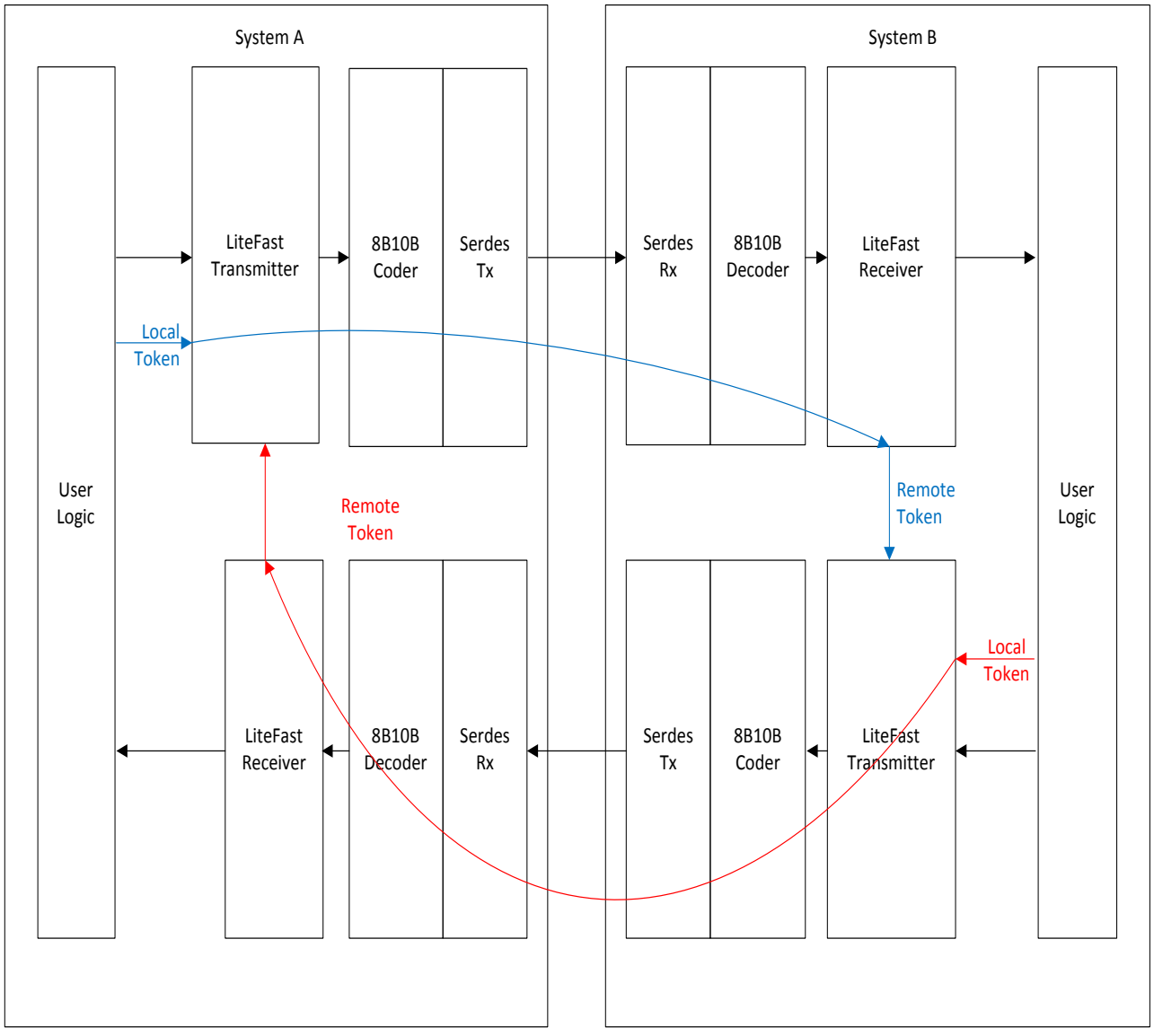

Figure 4 · Token Byte Transfer

Figure 4 shows, System A and System B utilizes SERDES and LITEFAST to transfer data over serial link. In System A, the available storage space of receiver buffer is encoded to token byte. Token byte is provided to the LiteFast Transmitter module and padded at the end of data frame and idle frame.

In system B, LiteFast receiver receives remote token from system A. LiteFast Transmitter determines whether it should send LiteFast data frame according to the value of remote token byte. System B also send the local token byte to System A, the flow control mechanism is implemented by transferring token bytes on both sides.

Multiple Lanes

In multiple lanes application, Data frame blocks are transmitted and received over multiple lanes:

- Data stream is cut into data blocks, each data block includes 8 bytes.
- Idle frame is one data block
- Data frame blocks. For example, block 0 is put on lane 3, block 1 is put on lane 2, block 2 is put on lane 1, and block 3 is put on lane 0.

Figure 5 shows the stripping process for a four lanes application.

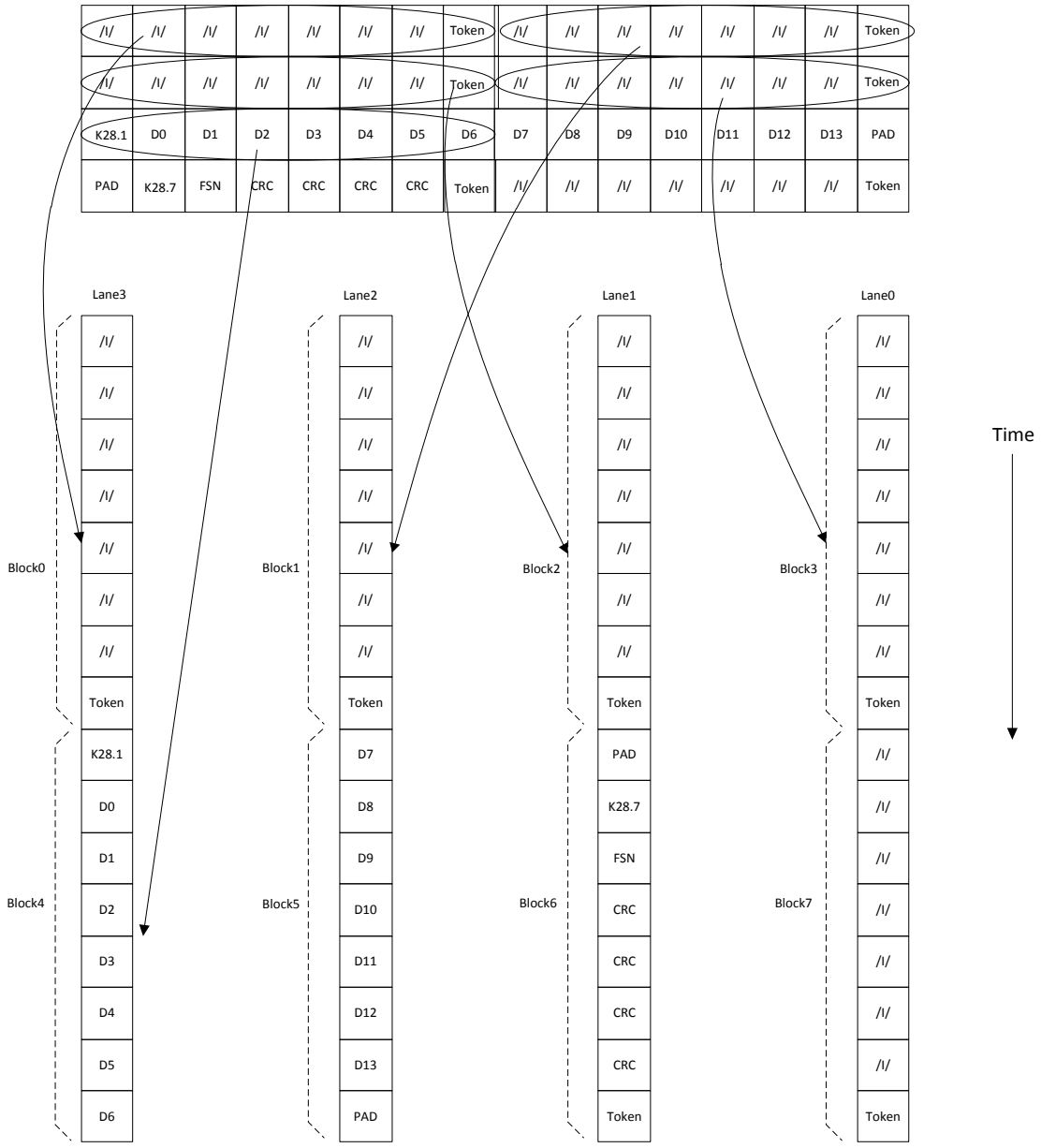

Figure 5 · Striping Process for 4 Lanes Application

In LiteFast Receiver, all lanes are aligned by using /A/ characters, and LiteFast data stream is recovered by using reversed stripping operation.

After the system is reset, LiteFast sends LiteFast idle frames to establish link between systems. LiteFast Receiver performs lane alignment with IDLE frames.

Typical Application

Single Lane Application

Figure 6 shows the single lane application.

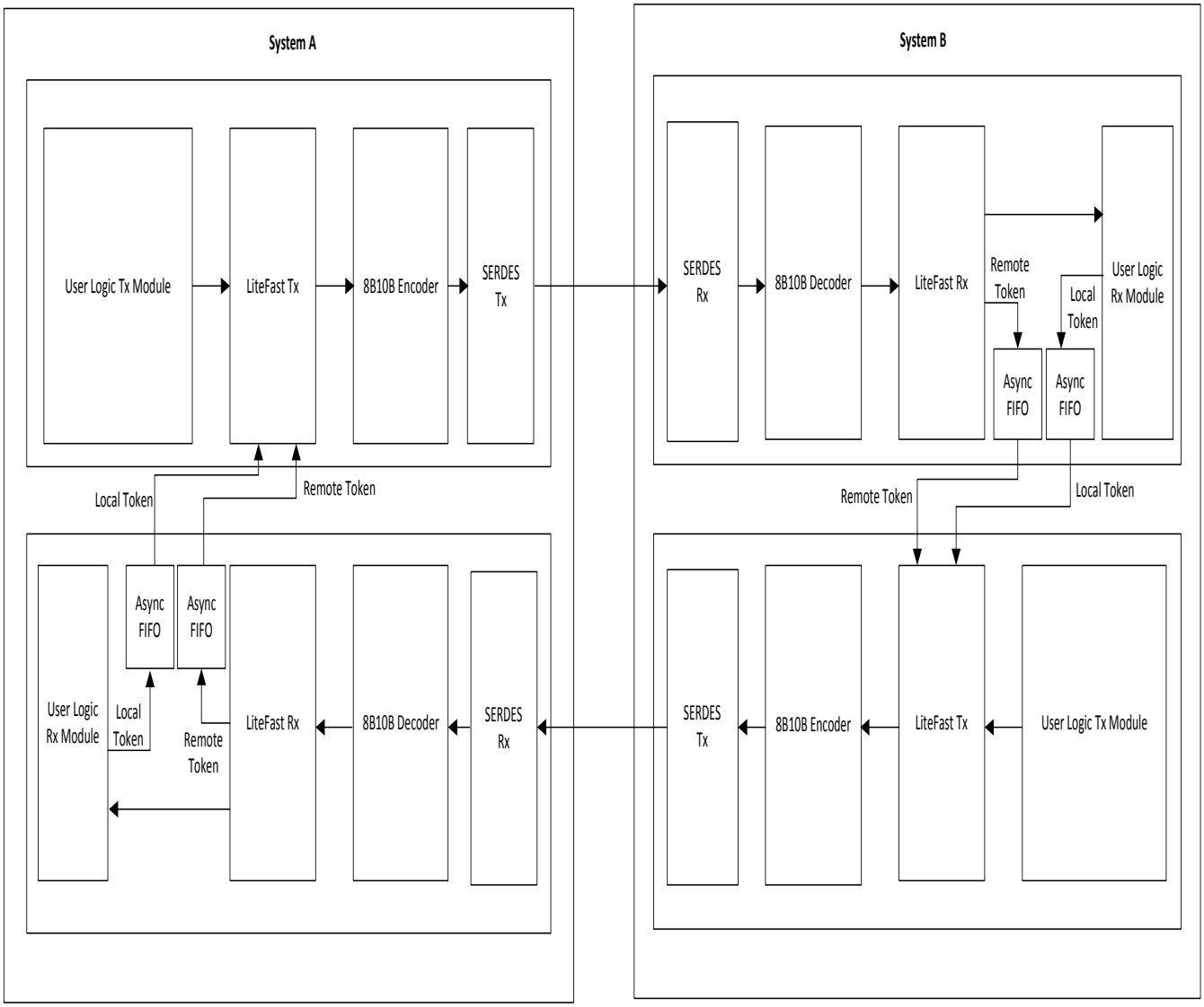

Figure 6 · Application for Single Lane

Figure 6 shows, system A and system B are transmitting data through a pair of SERDES.

For system A, LiteFast Transmitter embeds user data into LiteFast data frames, and it also generates LiteFast idle frame to build and maintain the link between two systems. LiteFast data stream is encoded to 10B words in 8B10B encoder, and then they are send to system B through SERDES transmitter.

In system A receiver, parallel data from SERDES back end is decoded to 8B words in 8B10B decoder. LiteFast Receiver recognizes idle frame and data frame and write data frame payload into RX FIFO, Remote Token information is extracted from LiteFast frames. From the perspective of System A, Remote Token information indicates

how much available storage space in System B RX FIFO, and Local Token indicates how much available storage space in System A RX FIFO. Figure 6 shows, LiteFast Transmitter and LiteFast Receiver work in different clock domain.

Multiple Lanes Application

Figure 7 shows the two lanes application.

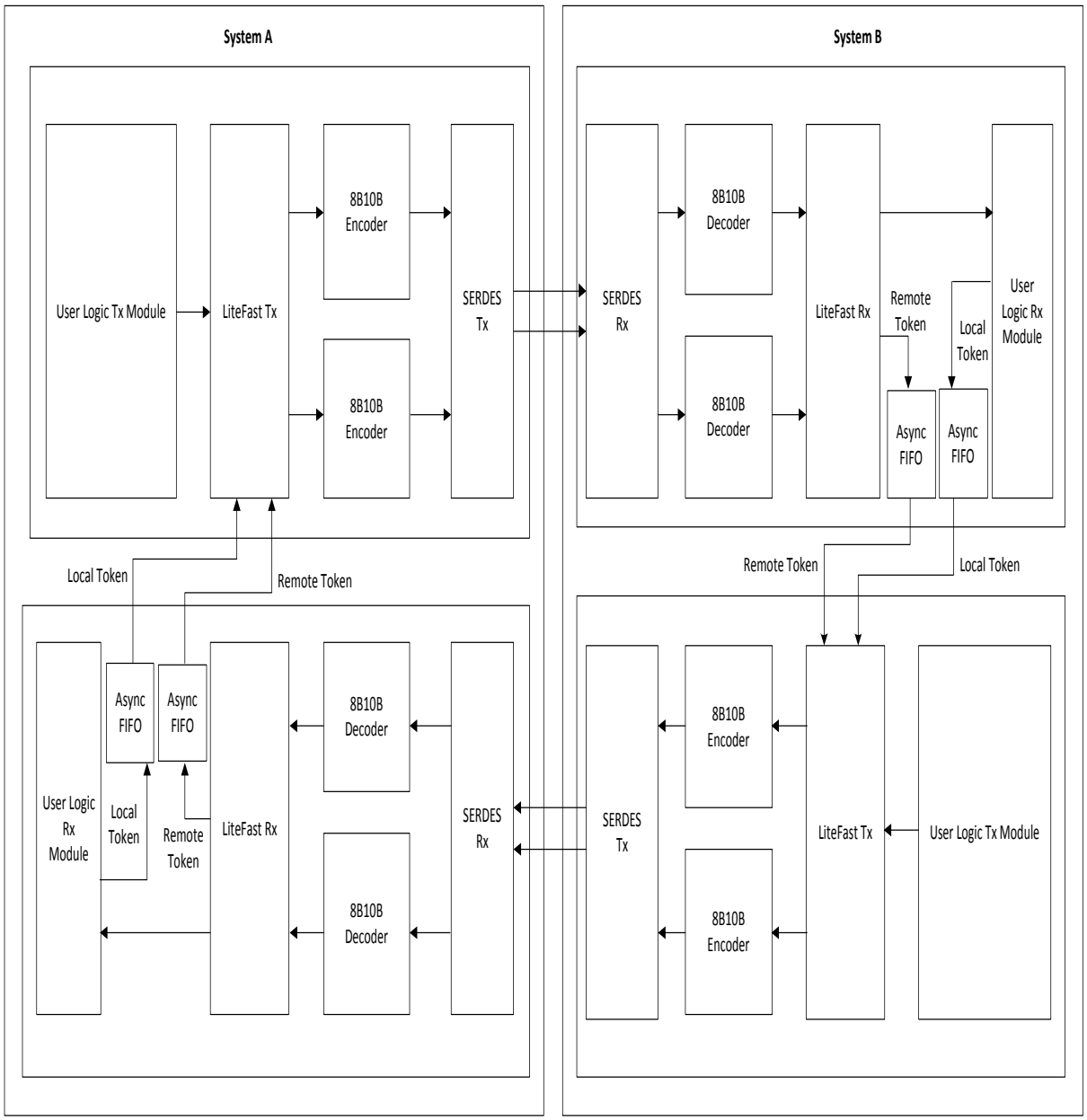

Figure 7 · Application for Two Lanes

Figure 8 shows the four lanes.

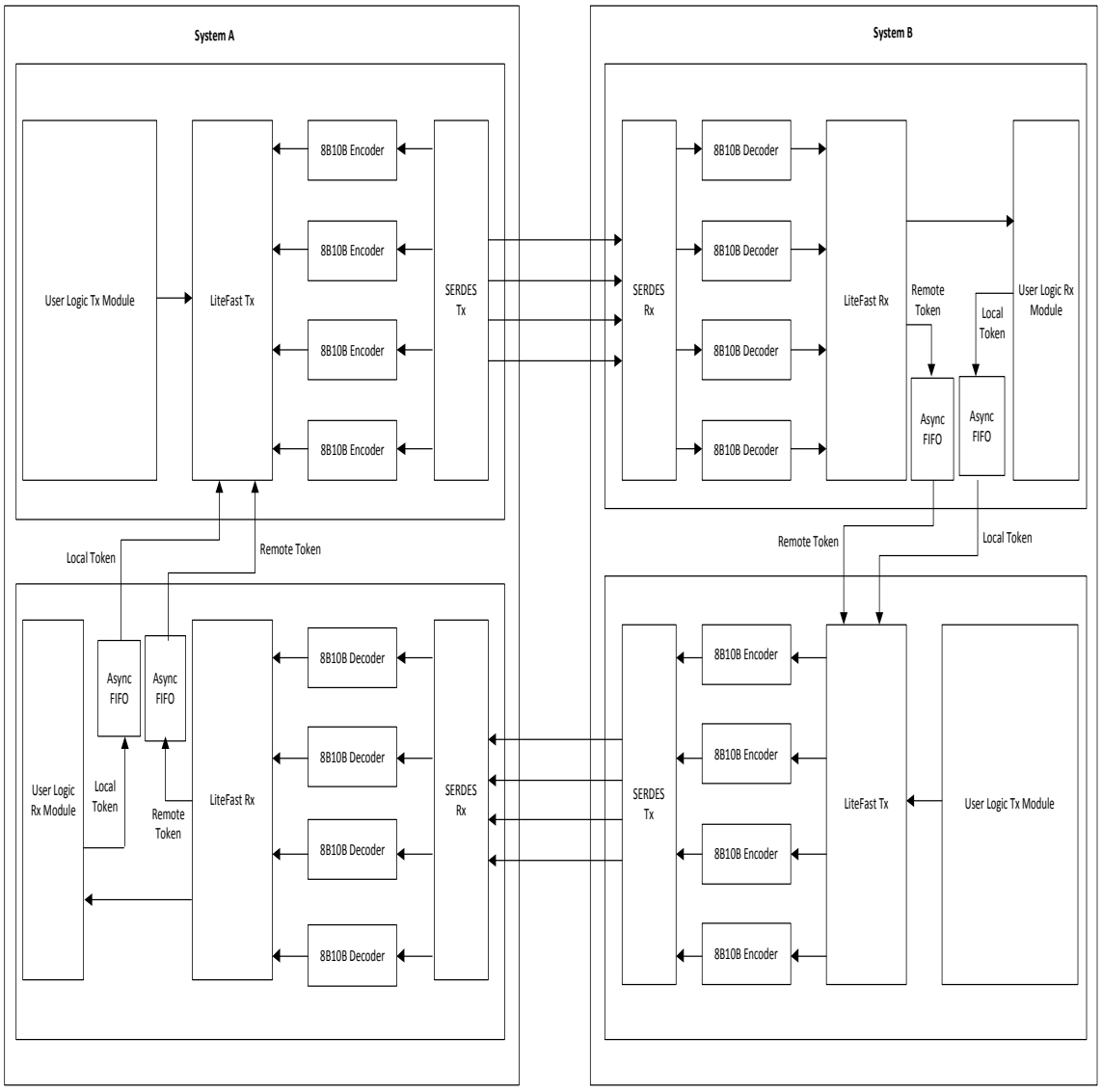

Figure 8 · Application for Four Lanes

Figure 8 shows, system A and system B are transmitting data through multiple pairs of SERDES.

For system A, LiteFast Transmitter embeds user data into LiteFast data frames, and it also generates LiteFast idle frame to establish and maintain the link between two systems. LiteFast data stream is stripped on multiple lanes and they are encoded to 10B words in 8B10B encoder, then they are send to system B through multiple SERDES transmitters. Each SERDES transmitter works in its own clock domain, a group of asynchronous FIFO are set for data synchronization between 8B10B encoder and SERDES. All clocks in System A transmitter should be from the same clock source.

In System A receiver, parallel data from SERDES back end is decoded to 8B words in 8B10B decoder. LiteFast performs lane alignment and recover LiteFast data stream by using reversed stripping process. LiteFast Receiver recognizes idle frame and data frame and write data frame payload into RX FIFO, Remote Token information is extracted from LiteFast frames. From the perspective of System A, Remote Token information indicates how much available storage space in System B RX FIFO, and Local Token indicates how much available storage space in System A RX FIFO. Figure 8 shows, LiteFast Transmitter and LiteFast Receiver work in different clock domain, Local Token and Remote Token is synchronized via asynchronous FIFO. Each SERDES receiver works in its own clock domain, a group of asynchronous FIFO are set for data synchronization between 8B10B decoder and SERDES receiver. All clocks in System A receiver should be from the same clock source.

Users can implement application specific user logic interfaced with LiteFast. Note that the LiteFast does not include 8b/10b encoder and decoder blocks. These blocks can be instantiated from Libero catalog. User need to configure SERDES in EPCS mode. LiteFast is device independent.

When the line speed is working at 2.5Gbps, the reference clock to SERDES is 125 MHz and it is provided from any of the following sources:

1. REFCLK0 (Differential)
2. REFCLK1 (Differential)
3. Fabric Clock (Single ended)

For more information about reference clock source, refer to SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration user guide.

Local and remote token exchanges happen across multiple clock domains. Therefore, care should be taken for clock domain crossing.

Interface Signals

Interface

LiteFast includes LiteFast Transmitter and LiteFast Receiver. Figure 9 shows the block diagram and interface signals.

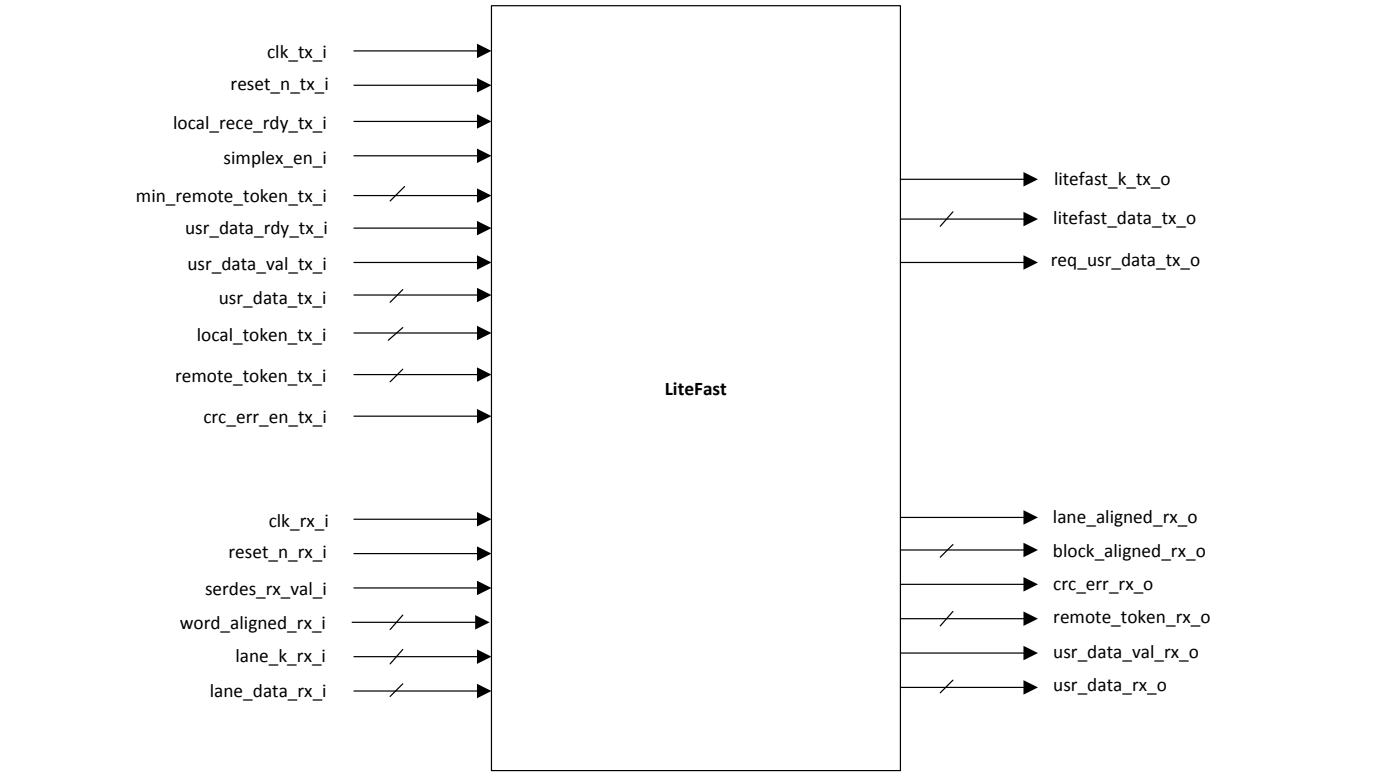

Figure 9 · LiteFast Interface Signal

Configuration Parameters

Table 1 shows the configuration parameters used in the hardware implementation of LiteFast. These are generic parameters and can be varied based on the application requirements.

Table 1 · Configuration Parameters

Name	Description
g_DATA_WID	LiteFast data bus width, it can be 8bits, 16bits, 32bits, or 64bits.
g_LANE_NUM	Lane number. It can be 1, 2, or 4. When g_DATA_WID = 8, it must be 1. When g_DATA_WID = 16, it could be 1 or 2. When g_DATA_WID = 32, it could be 1, 2, or 4. When g_DATA_WID = 64, it could be 1, 2, or 4.

Table 2 shows the user application data width.

Table 2 · User Application Data Width

User Application Data Width	1 Lane	2 Lanes	4 Lanes
8-bits	Support	No	No
16-bits	Support Maximum 16-bits in one lane	Support Maximum 8-bits per lane	No
32-bits	No	Support Maximum 16-bits per lane	Support Maximum 8-bits per lane
64-bits	No	No	Support Maximum 16-bits per lane

Table 3 shows the description of input and output ports.

Table 3 · LiteFast transmitter Interface signals

Interface	Input /Output	Width	Description
reset_n_tx_i	Input	1	Low active reset signal.
clk_tx_i	Input	1	Clock.
local_rece_rdy_tx_i	Input	1	Indicates local LiteFast Receiver is ready to receive data frame, it means SERDES / 8B10B decoder are in normal working mode and multiple lanes are aligned.
simplex_en_i	Input	1	Disable flow control feature.
min_remote_token_tx_i	Input	[7:0]	LiteFast Transmitter is allowed to send data frame only when remote token is greater or equal to this signal value.
usr_data_rdy_tx_i	Input	1	Indicates user logic module has data to be transmitted through LiteFast.
usr_data_val_tx_i	Input	1	Indicates whether data on usr_data_tx_i port is valid.
usr_data_tx_i	Input	[g_DATA_WID -1:0]	Data from user module, data on this port is wrapped into LiteFast data frame.
local_token_num_tx_i	Input	[7:0]	Indicates how much available storage space in local receiver buffer.

remote_token_num_tx_i	Input	[7:0]	Indicates how much available storage space in remote receiver buffer.
crc_err_en_tx_i	Input	1	Enable CRC error insertion, only for debug purpose.
req_usr_data_tx_o	Output	1	Require user data from user module.
litefast_k_tx_o	Output	[(g_DATA_WID / 8) - 1:0]	Indicates whether byte on LiteFast_data_tx_o port is an 8B10B special character. Bit[0] indicates the meaning for LiteFast_data_tx_o[7:0].
litefast_data_tx_o	Input	[g_DATA_WID -1:0]	LiteFast data stream. In multiple lanes mode, if lane data width is 8bits, bit[7:0] belongs to Lane 0. In multiple lanes mode, if lane data width is 16bits, bit[15:0] belongs to Lane 0.

Table 4 shows the description of input and output ports.

Table 4 · LiteFast receiver Interface signals

Interface	Input/ Output	Width	Description
reset_n_rx_i	Input	1	Low active reset signal.
clk_rx_i	Input	1	Clock.
serdes_rx_val_i	Input	[g_LANE_NUM -1:0]	Indicates whether SERDES receiver is ready for work.
word_aligned_rx_i	Input	[g_LANE_NUM -1:0]	Indicates whether 8B10B decoder is ready for work. In multiple lanes mode, bit[0] indicates the status for Lane 0.
lane_k_rx_i	Input	[(g_DATA_WID / 8) - 1:0]	Indicates whether byte on lane_data_rx_i port is an 8B10B special character. Bit[0] indicates the meaning for lane_data_rx_i[7:0].
lane_data_rx_i	Input	[g_DATA_WID - 1:0]	Input data stream. In multiple lanes mode, if lane data width is 8bits, bit[7:0] belongs to Lane 0. In multiple lanes mode, if lane data width is 16bits, bit[15:0] belongs to Lane 0.
crc_err_rx_o	Output	1	Indicates whether received CRC error.
usr_data_val_rx_o	Output	1	Indicates whether data on usr_data_rx_o port is valid.
usr_data_rx_o	Output	[g_DATA_WID -1:0]	User data from LiteFast data frame payload.
remote_token_rx_o	Output	[7:0]	Remote Token byte.
lane_aligned_rx_o	Output	1	Indicates whether multiple lanes are aligned and whether SERDES and 8B10B decoder are working fine.
block_aligned_rx_o	Output	[g_LANE_NUM -1:0]	Indicates whether each lane's data block is aligned. It is only for debug purpose. Bit[0] indicates the status of Lane 0.

Key Interface Description

local_rece_rdy_tx_i

The interface port local_rece_rdy_tx_i in LiteFast Transmitter should be connected with local LiteFast receiver's lane_algined_rx_o port.

min_remote_token_tx_i

For the purpose of flow control, LiteFast Transmitter pause data frame transmission when remote Token is less than min_remote_token_tx_i. When setting the value of min_remote_token_tx_i, the user should consider the maximal Remote Token transmission delay and maximal delay between LiteFast Transmitter and remote receiver buffer.

If user uses the integration design in Typical Application chapter, and the transmission delay between SERDES receiver pin and SERDES transmitter pin is less than 10ns. Table 5 shows the min_remote_token_tx_i setting details.

Table 5 · min_remote_token_tx_i settings

Data Width	Lane Number	min_remote_token_tx_i
g_DATA_WID = 8	g_LANE_NUM = 1	3
g_DATA_WID = 16	g_LANE_NUM = 1	6
	g_LANE_NUM = 2	6
g_DATA_WID = 32	g_LANE_NUM = 2	8
	g_LANE_NUM = 4	8
g_DATA_WID = 64	g_LANE_NUM = 4	16

req_usr_data_tx_o and usr_data_tx_i

LiteFast transmitter requires data from previous user logic module.

Timing Diagram

Figure 10 shows the timing of this operation.

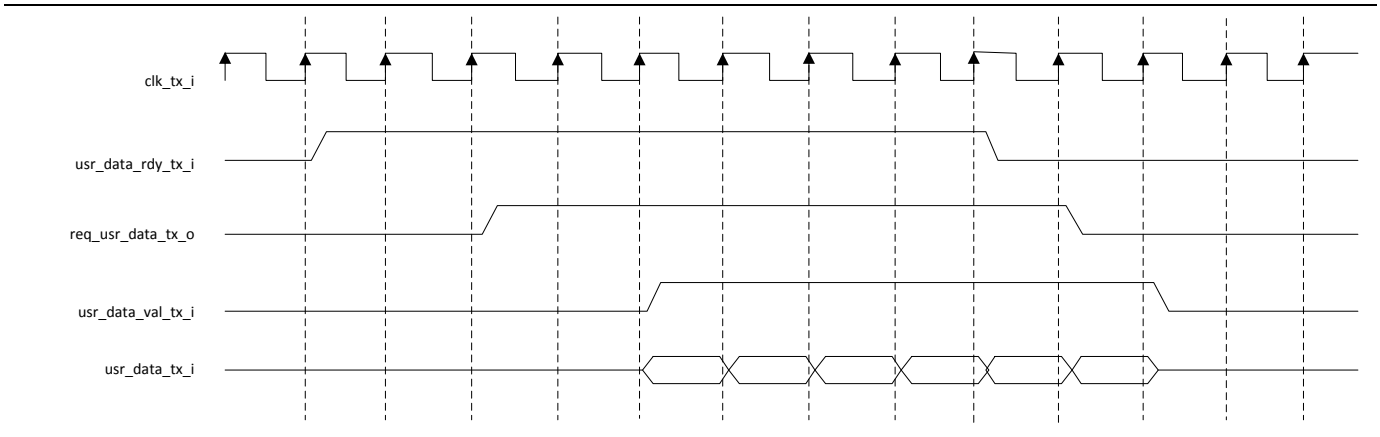

Figure 10 · Timing Diagram for LiteFast Transmitter

Resource Utilizations

Table 6 shows the resource utilization of the LiteFast block implemented in the SmartFusion®2 system-on-chip (SoC) FPGA device M2S150T-FBGA1152 package.

Table 6 · Resource Utilization of Pattern Generator

Working Mode	SLE	CFG	RAM64x18	RAM1K18
8 bits x 1 Lane	300	310	0	0
8 bits x 2 Lanes	1060	1250	2	0
8 bits x 4 Lanes	1850	2300	4	0
16 bits x 1 Lane	380	480	0	0
16 bits x 2 Lanes	1260	1450	4	0
16 bits x 4 Lanes	2220	2540	8	0

Supported Device Families

SmartFusion®2 (All devices that have transceiver)

IGLOO®2 (All devices that have transceiver)

RTG4™

References

The following documents are referred in this user guide.

Microsemi Publications

SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration

CorePCS Handbook

DG0720: LiteFast IP Demo Guide

List of Changes

The following table shows important changes made in this document for each revision.

Date and Revision	Change	Page
Revision 1 (July 2016)	Initial release.	N/A

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