Libero SoC v11.7 SP1.1 Release Notes

Note: The Libero SoC v11.7 SP1.1 release has code changes that affect designs targeting the RT4G150 production device only.
If you have an existing RTG4™ design with more than one asynchronous reset created in an earlier release, you must download and install this release, open the design in this release and regenerate the programming STAPL file.
Libero SoC users designing for RT4G150_ES device or families other than RTG4 are not affected by changes introduced in this release.

Microsemi Libero® System-on-Chip (SoC) Design Suite offers high productivity with its comprehensive, easy to learn, easy to adopt development tools for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and RT FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities and secure production programming support.

Libero SoC v11.7 SP1.1 is not required for designing with Microsemi SmartFusion®2 and SmartFusion® SoC FPGAs, and IGLOO®2, IGLOO®, ProASIC®3, and Fusion FPGA families. If it is installed, it will have no effect on these device families as it is targeted for the RTG4 production devices only.

To access Datasheets and Silicon User Guides, visit www.microsemi.com, select your Product, then click the Documentation tab. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the Design Resources tab.

Contents

What Has Changed in Libero SoC v11.7 SP1.1

RT4G150 Designs with more than one Asynchronous Resets

Libero SoC 11.7 SP1.1 introduces checks for designs with more than one asynchronous reset driving LSRAM, uSRAM or DSP Mathblocks. The check is to ensure that the correct programming file is generated for the RT4G150 production device.

- When an existing RT4G150 project created with a release prior to Libero SoC 11.7 SP1.1 is opened in this current release, the check is triggered. If the design fails the check, the design state is reverted to the pre-synthesis state (for Enhanced Constraint Flow) or pre-compile state (for Classic Constraint Flow).
- Rerun the design flow and regenerate the programming file.
- For new projects created with this current release, the check is implemented as part of the design flow.

RT4G150 SSTL and HSTL I/O Configuration

Libero SoC v11.7 SP1.1 addresses the Reference Voltage Circuitry leakage current referenced in **AC439: Board Design Guidelines for RTG4 FPGAs Application Notes**. The software implements checks and safeguards in the design flow to stop the conditions that may cause the current leakage. These conditions include:

- The design contains single-ended SSTL or HSTL I/O outputs in MSIO or MSIOD banks.

- When an existing RT4G150 project with a design containing SSTL or HSTL I/O outputs in MSIO or MSIOD bank is opened, Libero SoC 11.7 SP1.1 invalidates the Generate FPGA Array Data state.
- To continue with the design flow after the check fails, run Generate FPGA Array Data and re-export the Programming File.
- For new projects created with this current release, the check is implemented as part of the design flow.

- The design mixes SSTL/HSTL I/O types with non-SSTL/HSTL I/O types (such as LVCMOS, LVTTL or PCI) in a single MSIO or MSIOD bank and the placement of an I/O pair has an SSTL/HSTL input or SSTL/HSTL bidirectional I/O placed on PADP and an I/O other than SSTL/HSTL (such as LVCMOS, LVTTL or PCI) placed on PADN.
  - When an existing RT4G150 project created with a release prior to Libero SoC 11.7 SP1.1 is opened in this current release, a placement check on SSTL/HSLTL I/Os is triggered. If the design fails the check, the design state is reverted to the pre-synthesis state (for Enhanced Constraint Flow) or pre-compile state (for Classic Constraint Flow).
  - To continue with the design flow after the check fails, change the I/O Standard or package pin assignment to remove the violation and rerun the design flow.
  - For new projects created with this current release, the check is implemented as part of the design flow.

- The design uses SSTL/HSTL I/O inputs or SSTL/HSTL bidirectional pins without ODT or on-board terminations in MSIO or MSIOD banks.
  - If on-board termination is not in place, ODT I/O attribute must be enabled in the Constraint Manager.

- The board has MSIO or MSIOD banks with unterminated pins which can be driven completely low to the VSS (0V) rail or hard tied to VSS, and they are paired on PADN with SSTL/HSTL I/O inputs or SSTL/HSTL bidirectional pins on PADP.
  - It is recommended to revise your board to eliminate this condition and avoid any leakage current. For more information, refer to **AC439: Board Design Guidelines for RTG4 FPGAs Application Notes**.

Notes: The SSTL/HSTL software checks are only implemented for RT4G150, and not for RT4G150_ES device setting.

Known Limitations, Issues and Workarounds

Note: Unless stated otherwise, Known Issues from Libero SoC v11.7 SP.1 also apply to Libero SoC v11.7 SP1.1. Review the Libero SoC v11.7 SP1 Release Notes for Known Issues in Libero v11.7 SP1.

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

> The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

Antivirus Software Interaction

Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for any assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

RTG4

Chip Planner Displays Some Unplaced Macros after Layout in Enhanced Constraint Flow

This is a Chip Planner display issue. It can be ignored if layout is successful.

- If the “Repair Minimum Delay Violations” option is enabled in layout options and the layout tool adds buffers to do the repair, opening Chip Planner after layout may display the added buffers as unplaced macros.
- If nets on Row Globals or local asynchronous resets are constrained to a user-created exclusive region in Chip Planner before layout is run, re-opening Chip Planner may display the macros connected to those constrained nets as unplaced macros even though the layout process has successfully completed.

SmartTime Reports Incorrect Data Required Time for the IOINFF Macro

The timing model of input registers (IOINFF) is incorrect. The register data input is incorrectly modeled as sensitive to both the rising and falling edge of the clock. As a result the slack calculation for input to register paths uses half the clock period. This will be fixed in Libero 11.7 SP2**.**

Custom Flow with uPROM: uPROM content must be a single line file

If you are using the custom flow and are importing uPROM content using the import_component_data command, the uPROM memory file must not have any newlines.

Single Event Transient (SET) Mitigation ON may result in Hold Violations

Turning **SET Mitigation** ON may result in hold time violations in some cases. Enable **Repair Minimum Delay Violations** in Place and Route Options to have the Place and Route tool mitigate these and other hold time violations.

SmartDebug for RTG4: Device Resets during JTAG Operations with SmartDebug

After performing one or more JTAG operations, if a user closes and reopens SmartDebug (either standalone or within the Libero SoC software), the device resets itself.

Workaround:

The device reset problem can be avoided using FlashPro5 Programmer and by setting a value of “1” on the def variable “**SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET”.**

- For Standalone SmartDebug
    - When invoking tool from command line, add the following argument:
        - Console >
          ./sdebug.exe SMARTDEBUG**_RTG4_FLASHPRO5_DISABLE_RESET**:1
    - When invoking from GUI:
        - Edit the sdebug.def file and change the value of def variable to ‘1’ in the line below:
          data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
- For SmartDebug Invoked from Libero:
    - Edit the sdbg.def file and change the value of def variable to “1” in the line below:
      data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
    - Add the following line in the libero.def file:

data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 1 OVERRIDE

- For Tcl script-driven batch mode operation, add the following def variable and the value in a Tcl script:

  defvar_set -name **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET** -value 1

Please note that when this def variable is set to 1, the LiveProbe set in a previous SmartDebug session is not retained when subsequent SmartDebug session is invoked.

Extra Pop-Up Messages from SynplifyPro

When SynplifyPro Synthesis is invoked interactively, SynplifyPro pops up message windows about completion of Tcl script file execution, if and when prior to the interactive invocation of SynplifyPro:

- Additional user-specified Synthesis Options are configured in a Tcl script and passed by Libero to SynplifyPro.
- The Synthesis Option is entered in the Configure Synthesis Option dialog box as a command line entry and passed to SynplifyPro.

These pop-up messages can safely be ignored. Click **OK** to continue with the SynplifyPro synthesis.

Enhanced Constraint Flow

The following tools and flows are not supported in the Enhanced Constraint Flow in Libero SoC v11.7 SP1.1:

- Precision Synthesis
- IO Advisor
- Netlist Viewer
- Block Flow
- Design Separation Flow using MSVT

Programming

Programming Recovery Not Working After Programming Interruption

Exporting a SPI bitstream with Programming Recovery enabled with another programming file type (STAPL, DAT) will erase and reprogram the Programming Recovery setting. If a programming interruption occurs before the Programming Recovery setting is reprogrammed with the following programming method (Auto Update, Auto Programming, or IAP/ISP services), then Programming Recovery will not occur.

To workaround this issue, export SPI bitstream only without any other programming file type. This will be resolved in Libero v11.8.

Restricts ARM® Cortex®-M3 Debug with DPK (Debug Pass Key)

SoftConsole does not support this feature.

VALIDATE_USER_ENC_KEYS Not Shown in Drop-Down Menu in FlashPro Express

When an HSM task is loaded in FlashPro Express, the VALIDATE_USER_ENC_KEYS action is not available in the drop-down action menu.

Workaround:

Use the following Tcl script commands to run the action:

```
set_programming_action -name {dev_name} -action {VALIDATE_USER_ENC_KEYS}
run_selected_actions
```

No Programming Support for Virtual Machines (VM)

Programming is supported for physical machines only. Programming is not supported on any Virtual Machine (VM).

Documentation

Web-based documentation

Starting with Libero SoC v11.7, most Users Guides for SmartFusion2, IGLOO2, and RTG4 are available on the Microsemi website. Libero and Programming/Debug tools will include links to the website.

If the machine on which you have installed Libero does not have access to the Internet, you (or a site administrator) can download all Libero SoC v11.7 Users Guides from Microsemi's Libero SoC documentation site.

Linux: Firefox requirement for Online Help and Users Guides

Libero SoC v11.7 SP1.1 requires the "Firefox" executable to be in your PATH variable on Linux. Alternatively, you can access the Reference Manuals on the Microsemi website, or by clicking **Help > Reference Manuals** in Libero. For the Libero SoC v11.7 SP1.1 release, the "Web Browser" selection in the Libero Preferences dialog is only used by Online Help and for some user guide links.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. A 64-bit OS is required for designing SmartFusion2, IGLOO2, and RTG4 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents web page.

Operating System Support

Supported

- Windows 7, Windows 8.1.
- RHEL 5* and RHEL 6, CentOS 5* and CentOS 6.
- SuSE 11 SP4 (Libero only; FlashPro Express, SmartDebug, and Job Manager are not supported)

  ** RHEL 5 and CentOS 5 do not support programming using FlashPro5.*

Discontinued

- 32-bit operating systems are no longer supported.
- Windows XP is no longer supported.
- Support for the following Operating Systems will cease in the first half of 2017:
  - Solaris Flexlm license daemon support; Libero SoC is already not supported on Solaris.
  - Libero SoC software support for RedHat Enterprise Linux 5, and CentOS 5.

Download Libero SoC v11.7 SP1.1

This Service Pack is an incremental update and must be installed on top of Libero SoC v11.7 or v11.7 SP1.

Installation requires Admin privileges.

Download Libero SoC v11.7 SP1.1

Windows Download

Linux Download

SoftConsole 3.4/4.0

Libero SoC v11.7 SP1.1 is compatible with SoftConsole v3.4 SP1 and SoftConsole v4.0.

Download SoftConsole v4.0

Download SoftConsole v3.4 SP1

Installation Note:

After installation of Libero on Linux, the attempt to run the udev_install script for FlashPro setup fails with this message:

```
%. /udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:
The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, as such, is not a valid shell script.

Workaround:
Run the `dos2unix` command on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
% ./udev_install
```

If the `dos2unix` command is not available, install the command first, and then run `dos2unix, and udev_install`:

```
% sudo yum install dos2unix
% dos2unix udev_install
% ./udev_install
```

Revision History

Revision Number	Date	Author	Comment
1.0	7/19/2016	Microsemi	Initial Release
1.1	8/5/2016	Microsemi	Added Extra SynplifyPro Pop-Up Warning Messages In Known Issues
1.2	8/29/2016	Microsemi	Added to Known Issues • Chip Planner display issue • IOINFF Input-to-Reg slack calculation Issue
1.3	10/17/16	Microsemi	Added Programming Recovery to Known Issues

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Centre, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades; update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; Enterprise Storage and Communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 4,800 employees globally. Learn more at **www.microsemi.com.**

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