Libero SoC v11.7 SP1 Release Notes

Microsemi Libero® System-on-Chip (SoC) Design Suite offers high productivity with its comprehensive, easy to learn, easy to adopt development tools for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and RT FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities and secure production programming support.

The Libero SoC v11.7 SP1 release includes enhancements to RTG4™

- Timing and power data for RT4G150 devices
- Adds support for RTG4 Dynamic Clock Conditioning Circuitry (CCC) configuration

The Libero SoC v11.7 SP1 release includes enhancements to SmartFusion2™ and IGLOO2™

- The Lock Bit Configuration tool is introduced, enabling certain design security use models

Use Libero SoC v11.7 SP1 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and SmartFusion® SoC FPGAs, and IGLOO®2, IGLOO®, ProASIC®3, and Fusion FPGA families.

To access Datasheets and Silicon User Guides, visit www.microsemi.com, select your Product, then click the Documentation tab. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the Design Resources tab.

Refer to the Libero SoC Online Help for details about new software features and enhancements.

Contents

What's New in Libero SoC v11.7 SP1

Silicon Feature Support

Tie-Off of Unused RTG4 RAM Blocks

Libero SoC v11.7 SP1 software ties off any unused RAM block to reduce power consumption. Designs completed with Libero SoC v11.7 or earlier must be upgraded to Libero SoC v11.7 SP1 to take advantage of this improvement.

Even on used RAM blocks, if any clock is to be stopped during device operation, it must be stopped at the low state.

RTG4 Preliminary Timing and Power

Timing and Power data are updated in this release. The data state for timing and power for all RTG4 devices is now preliminary. Static power is reduced significantly compared to Libero SoC v11.7.

RTG4 Single Event Transient (SET) Mitigation per Flip-Flop

Libero SoC v11.7 SP1 supports SET mitigation on a per-flip-flop basis. Insert the following command in a Physical Design Constraint (*.pdc) file (for Classic Constraint flow) or a Netlist Design Constraint (*.ndc) file (for Enhanced Constraint flow) to enable or disable SET mitigation for individual flip-flops. This command overrides the project-wide global setting (**Project > Project Settings > Analysis Operating Conditions > Enable Single Event Transient Mitigation**).

```
set_mitigation -inst_name <instance_name> -mitigated <value>
```

A hierarchical instance name is accepted. The wildcard character "*" in the instance name is also supported. When the mitigation property is set on an instance that contains design elements such as MACC, RAM1K18_RT, RAM64x18_RT or SLE_RT that can take the SET mitigation property, all the design elements within that instance are set with the SET mitigation property.
Valid values for the mitigated value argument are Yes/No, On/Off, True/False or 1/0.

RTG4 Dynamic CCC Configuration

This release adds two use models for Dynamic CCC Configuration, enabling you to change the behavior of the CCC as part of the application (using an AMBA APB interface). Simulation and timing models are updated to support this behavior for validating solutions using Dynamic CCC Configuration before programming the device.

- To use Single Dynamic CCC instance in the design:
  1. Instantiate the RTG4FCCC SgCore.
  2. Check the "*Enable Dynamic Configuration*" checkbox.
  3. Check the "*Include Reconfiguration Logic*" checkbox.
  4. Connect the APB_SLAVE bus interface to the design.
  5. Insert timing constraints for APB.
  6. Fix any hardwired I/O connected to the RTG4FCCC to an appropriate semi-dedicated package pin with a function name that contains a CCC corner notation with suffix 0.

  Note: The CCC input can come from the Oscillator, a Fabric Input, or a Dedicated Input.

- To use Multiple Dynamic CCC instances in the design:
  1. Instantiate each RTG4FCCC SgCore.
  2. Check the "*Enable Dynamic Configuration*".
  3. Uncheck the "*Include Reconfiguration Logic*".
  4. Instantiate up to four RTG4CCCAPB_IF SgCores, one for every two RTG4FCCC instances.
  5. Connect a pair of RTG4FCCC instances to one RTG4CCCAPB_IF instance. All suffix 0 signals must connect to one CCC and all suffix 1 signals must connect to the other CCC.
  6. Connect the APB_SLAVE bus interface on the RTG4CCCAPB_IF to the design.
  7. Insert timing constraints for APB.
  8. Place each pair of RTG4FCCC instances in the same corner of the device:
     - In case of fabric inputs, make sure that the two RTG4FCCC instances are placed in the same corner of the device. The CCC connected to suffix 0 signals of the RTG4CCCAPB_IF should be on the left of the pair and the CCC connected to suffix 1 signals should be on the right.
     - In case of I/O inputs, make sure that the two I/Os are fixed to appropriate semi-dedicated package pins with a function name that contains the same CCC corner notation. The CCC connected to suffix 0 signals of the RTG4CCCAPB_IF should be assigned to a pin with a CCC corner name that has suffix 0 and the CCC connected to suffix 1 signals should be assigned to a pin with a CCC corner name that has suffix 1.

Update the RTG4FCCC core to the current version before modifying any RTG4FCCC configuration in a design created with Libero SoC v11.7 or earlier.

The Dynamic CCC feature is not available in the RT4G150_ES device. Customers who want to dynamically control CCC in an RT4G150-ES device should contact Microsemi Customer Support to migrate the design to the RT4G150 device.

SmartFusion2 and IGLOO2 Configure Register Lock Bits Tool

SmartFusion2 and IGLOO2 devices allow you to restrict access to MSS, SERDES, and FDDR configuration registers. Libero SoC v11.7 SP1 includes the Register Lock Bits Configuration tool (**Design Flow Window > Configure Register Lock Bits**) to lock these configuration registers and prevent them from being overwritten by MSS or Fabric Masters that have access to these registers. Note that simulation support for this feature is unavailable.

As part of this new feature, the Configuration Register tab in System Builder (**System Builder > Security > Configuration Register**) and the MSS Security Policies Configurator has been removed. Use the Configure Register Lock Bits tool from the Design Flow window to configure the register lock bits.

When a design is migrated from Libero 11.7 or earlier release to Libero 11.7 SP1, the register lock bit configuration is preserved. To change the register lock bit configuration, use the Register Configuration Lock Bit tool (**Design Flow Window > Configure Register Lock Bits**)

The Configure Register Lock Bits tool is not available for RTG4 devices in this release but is planned for a future release.

Software Enhancements

Unless otherwise noted, Software Enhancements apply to SmartFusion2, IGLOO2, RTG4, SmartFusion, Fusion, IGLOO, and ProAsic devices.

System Verilog Support

As part of an on-going roadmap to add System Verilog support in Libero, release v11.7 SP1 adds support for System Verilog constructs. Set explicitly the Verilog standard to System Verilog (**Project > Project Settings > Design Flow**) to allow Libero SoC to process System Verilog constructs. By default, Libero SoC supports the Verilog 2001 Standard.

When System Verilog is specified in the Project Settings, Verilog (*.v) files containing System Verilog RTL constructs can be imported into a Libero SoC project and processed without errors.

Limitations:

The support for System Verilog in this release has the following limitations:

- Import of System Verilog (*.sv) files is not supported in this release. Only *.v files can be imported.
- The System Verilog “package” construct is not supported in this release. If the design uses packages, follow the steps below:
    1. Create a standalone Synplify Pro Project.
    2. Set System Verilog as the Verilog Language.
    3. Set the Output File Options to Mapped Verilog Netlist.
    4. Import the System Verilog (*.sv) files, including the one containing the package construct into the standalone Synplify Pro Project.
    5. Run Synthesis in Synplify Pro.
    6. Create a Libero SoC project.
    7. Import the Verilog Netlist (*.vm) file from Synplify Pro into the Libero Project.
    8. In the Libero SoC Project Settings, select Design Flow (**Project > Project Settings > Design Flow**) and uncheck “Enable Synthesis” so that no synthesis is run on the *.vm netlist and the design flow begins from **Compile Netlist.**

    For details, please refer to the SmartFusion2/IGLOO2 Custom Flow User Guide.

HDL Language Mode Unification

HDL language mode selections are centralized in one place (**Project > Design Flow > Project Settings**). The language options set explicitly for Simulation (**Project > Project Settings > Simulation options**) and Synthesis (**Design Flow window** > **Synthesis > Configure options**) are removed. You can select System Verilog/Verilog 2001 or VHDL-2008/VHDL-93 as language options for Verilog and VHDL, respectively. Verilog 2001 and VHDL 2008 are the default language option on initial creation of a new project. These options are used by Simulation and Synthesis tools while parsing the HDL Source/Simulation files. Language options set (different from the default) in Project Settings are inherited by Synthesis and Simulation tools and do not need to be set separately.

Advanced Synthesis Scripting Options

Libero SoC v11.7 SP1 adds support for Synthesis power users for Synplify Pro synthesis. As part of the Libero SoC Synthesis Options dialog, you can now include advanced synthesis tool directives (either in a name-value pair format, or in a Synplify Pro-compatible Tcl script). This support enables you to leverage Synplify Pro-specific synthesis optimization options directly from the Libero SoC user interface. This enhancement is limited to SmartFusion2, IGLOO2, and RTG4 devices.

SmartFusion2/IGLOO2/RTG4 IBIS Model Selector

IBIS format provides for minimum, typical, and maximum corner data within each individual model. Additional variations are now supported through the model selector feature.

Enhanced Constraint Flow Improvements

The Enhanced Constraint Flow (for SmartFusion2, IGLOO2, and RTG4 devices only) has the following enhancements in Libero SoC v11.7 SP1:

- Improved timing closure for Microsemi IP – In Libero SoC v11.7, under rare circumstances, Microsemi IPs such as CoreConfigP encounter maximum or minimum delay violations. Libero SoC v11.7 SP1 enhances the handling of these IPs – they are automatically placed in fixed regions, assuring that Microsemi IPs do not cause timing violations.
- Derived constraints are now supported for RTG4 EPCS and XAUI IPs.
- Encrypted VHDL flow support is added.
- Constraint Coverage Reporting Enhancements – A Place-and-Route Constraint Coverage Report and a Timing Verification Constraint Coverage Report are available for generation from the Constraint Manager (**Constraint Manager > Timing > Constraint Coverage > Generate Place and Route Constraint Coverage/Generate Timing Verification Constraint Coverage**). The reports can be generated after the Synthesis step and without the need to complete the Place-and-Route step. The Constraint Coverage Reports are listed in the Reports window under the Place and Route node and under the Verify Timing node.

Secure Production Programming Solution (SPPS)

The Libero SoC v11.7 SP1 release contains bug fixes and improvements to the security of SPPS (for SmartFusion2 and IGLOO2 only).

SgCore and DirectCore Changes

The following SgCores and DirectCores are updated for Libero SoC v11.7 SP1:

Core	Device/Family	Libero SoC v11.7 SP1 - Compatible Core Version	Changes
CoreResetP	SmartFusion2/ IGLOO2	7.1.100	Add 060/090 label for target die.
CoreConfigP	SmartFusion2/ IGLOO2	7.1.100	Add 060/090 label for target die.

RTG4FCCC	RTG4	1.1.216	Dynamic CCC solution
RTG4CCCAPB_IF	RTG4	1.1.105	New for Dynamic CCC solution

Resolved Issues

Customer Reported SARs Resolved in Libero v11.7 SP1

Customer Case Number	Description
493642-2118984907	RTG4 : different timing values observed in SmartTime for the same cell
493642-2084369325	Runtime error upon opening Synplify Pro interactively in Libero 11.7
493642-2113974195	RTG4 SERDES Configurator missing data width selections
493642-2102704852	Libero 11.7 freezes
493642-2097588311	Libero 11.7 crashes due to Windows Defender
493642-2091217167	Export bitstream fails when I use network path
493642-2089949478	Different timing summary between "Verify Timing" and "Interactively"
493642-2082110374	Libero gives error when updating a design from Libero 11.6 SP1 to Libero 11.7
493642-2066358457	RTG4 CCC: negative value of programmable delay is not working as documented in simulation
493642-2053998309	IO Attribute Editor sets "Resistor Pull" as same polarity for Differential IOs
493642-2064400828	Parallel paths are not displayed in SmartTime v11.7
493642-2064890266	Invalid timing constraints generated by the tool
493642-2019039338	ModelSim simulation of SmartFusion2 and IGLOO2 PLL has output phase shifted when External feedback clock is enabled.
493642-2048678447	Update Table 10 in FP User guide
493642-2033734577	RTG4: APB: Simulation does not handle the APB macro used for dynamic simulation RTG4: APB: Need updated APB macro to connect two CCC for Dynamic configuration
493642-2038099819	passing script file for synthesis in "run_tool" is not working [tcl flow]
493642-2026162606	Libero 11.6 adds new line in modelsim.ini file
493642-2028845499	Need to update On-line Help, STAPL file is supported for SmartFusion2/IGLOO2
493642-2001670265	SmartFusion2/IGLOO2/RTG4: SERDES configurator is not updating register setting of PCI_MSI_0 if set for MSI8
493642-2007160699	Improve menu options under debug security policy (SmartFusion2)
493642-2006108279	HDLPlus: "create core from HDL" does not mention the reason for the error
493642-1957857941	Number of Differential pairs mentioned in datasheet, mismatch in reality (M2GL150T-FCV484)
493642-1956744000	Net delay is different for the same net in Required path and Arrival path
493642-1963390867,493642-2001772558	Tcl Doc missing the export_pin_reports but the command is in the Online help
493642-1971667927, 493642-2031527769	HDL_VERILOG_INCLUDE: Errors linking VERILOG Include files
493642-1956975334	Radiation parameter specified in Libero GUI is not transmitted to Designer In Libero 11.6 (RT ProASIC3L devices)
493642-1950495833	RTG4: Add enable/disable SET filter per individual Flip-Flop
493642-1894897370	Libero SoC Parser error
493642-1816901556,493642-	TCL_SYNTHESIS: FDC: TCL Command to set Synplify Pro options

1840050939,493642-1964918196	
493642-1798516219	with-select in process should error in Check HDL.
493642-1552594864	TCL_SYNTHESIS: FDC: provision to pass arguments that overrides .prj file
	SERDES AHB Interface simulation model different from behavior in silicon
	RTG4 LSRAM: Remove the Sync Reset from ECC Output Pipeline Registers in simulation models
	RTG4:IOPAD_VDD Timing Model Updates
	Add FDDR_POWER_DOWN_0/1 modules to the simulation library

Known Limitations, Issues and Workarounds

Note: Unless mentioned in the Resolved_Issues list above, Known Issues from Libero SoC v11.7 also apply to Libero SoC v11.7 SP1. Review the Libero SoC v11.7 Release Notes for Known Issues in Libero v11.7.

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

Antivirus Software Interaction

Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for any assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

RTG4

SmartTime Reports Incorrect Data Required Time for the IOINFF Macro

The timing model of input registers (IOINFF) is incorrect. The register data input is incorrectly modeled as sensitive to both the rising and falling edge of the clock. As a result the slack calculation for input to register paths uses half the clock period. This will be fixed in Libero 11.7 SP2.

Custom Flow with uPROM: uPROM content must be a single line file

If you are using the custom flow and are importing uPROM content using the import_component_data command, the uPROM memory file must not have any newlines.

Single Event Transient (SET) Mitigation ON may result in Hold Violations

Turning **SET Mitigation** ON may result in Hold time violations in some cases. Enable **Repair Minimum Delay Violations** in Place and Route Options to have the Place and Route tool mitigate these and other Hold time violations.

SmartDebug for RTG4: Device Resets during JTAG Operations with SmartDebug

After performing one or more JTAG operations, if a user closes and reopens SmartDebug (either standalone or within the Libero SoC software), the device resets itself.

Workaround:

The device reset problem can be avoided using FlashPro5 Programmer and by setting a value of "1" on the def variable "**SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET".**

- For Standalone SmartDebug
  - When invoking tool from command line, add the following argument:
    - Console >
      ./sdebug.exe SMARTDEBUG**_RTG4_FLASHPRO5_DISABLE_RESET**:1
  - When invoking from GUI:
    - Edit the sdebug.def file and change the value of def variable to '1' in the line below:
      data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
- For SmartDebug Invoked from Libero:
  - Edit the sdbg.def file and change the value of def variable to "1" in the line below:
    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
  - Add the following line in the libero.def file:
    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 1 OVERRIDE
- For Tcl script-driven batch mode operation, add the following def variable and the value in a Tcl script:
  defvar_set -name **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET** -value 1

Please note that when this def variable is set to 1, the LiveProbe set in a previous SmartDebug session is not retained when subsequent SmartDebug session is invoked.

SmartFusion2/IGLOO2 False Warning When Running Programming Actions

A warning message appears when running programming actions for SmartFusion2 or IGLOO2 devices:

"Warning: programmer 'E2005C4JN' : device 'Microsemi Device' : Device authentication failure: Failed to validate device certificate."

This warning message is invalid and can be ignored.

Libero crashes when Exporting FlashPro Express Job for UEK1 or UEK2 with eNVM

Libero crashes when Export FlashPro Express Job tool is invoked to generate a programming job encrypted using UEK1/UEK2 and eNVM is the only component selected. To work around this problem, select BOTH Fabric AND eNVM components for exporting programming job encrypted using UEK1 or UEK2.

SmartFusion2/IGLOO2 Device Speed Grade and SERDES Data Rate Limits

Libero 11.7 SP1 implements data rate upper limits for EPCS protocol as follows:

- STD Speed Grade device supports a maximum data rate of 2500 Mbps.
- -1 Speed Grade device supports a maximum data rate of 3200 Mbps.

After migrating a design project from 11.7 or earlier releases to Libero 11.7 SP1, open the SERDES configurator to review the data rate settings before you continue with the design process when all of the following are true:

- The device family is SmartFusion2 or IGLOO2.

- The design contains a SERDES core which is configured for the EPCS protocol.
- You are certain that the data rate for the EPCS is above the upper limit introduced in Libero 11.7 SP1 or you are not sure.

SmartFusion2, IGLOO2 and RTG4 - Chip Planner Displays Some Unplaced Macros after Layout in Enhanced Constraint Flow

This is a Chip Planner display issue. It can be ignored if layout is successful.

- If the “Repair Minimum Delay Violations” option is enabled in layout options and the layout tool adds buffers to do the repair, opening Chip Planner after layout may display the added buffers as unplaced macros.
- If nets on Row Globals or local asynchronous resets for RTG4 are constrained to a user-created exclusive region in Chip Planner before layout is run, re-opening Chip Planner may display the macros connected to those constrained nets as unplaced macros even though the layout process has successfully completed.

Extra Pop-Up Messages from SynplifyPro

When SynplifyPro Synthesis is invoked interactively, SynplifyPro pops up message windows about completion of Tcl script file execution, if and when prior to the interactive invocation of SynplifyPro:

- Additional user-specified Synthesis Options are configured in a Tcl script and passed by Libero to SynplifyPro.
- The Synthesis Option is entered in the Configure Synthesis Option dialog box as a command line entry and passed to SynplifyPro.

These pop-up messages can safely be ignored. Click **OK** to continue with the SynplifyPro synthesis.

Enhanced Constraint Flow

The following tools and flows are not supported in the Enhanced Constraint Flow in Libero SoC v11.7 SP1:

- Precision Synthesis
- IO Advisor
- Netlist Viewer
- Block Flow
- Design Separation Flow using MSVT

Programming

Programming Recovery Not Working After Programming Interruption

Exporting a SPI bitstream with Programming Recovery enabled with another programming file type (STAPL, DAT) will erase and reprogram the Programming Recovery setting. If a programming interruption occurs before the Programming Recovery setting is reprogrammed with the following programming method (Auto Update, Auto Programming, or IAP/ISP services), then Programming Recovery will not occur.

To workaround this issue, export SPI bitstream only without any other programming file type. This will be resolved in Libero v11.8.

SPPS Flow: export_hsmtask fails when set_security_overwrite is followed by set_envm_update

If the user Tcl script has the security overwrite command followed by the eNVM update command, the export of HSM job will fail. In other words, if set_security_overwrite is followed by set_envm_update, export_hsmtask fails.
Workaround:
If both the security overwrite command and the eNVM update command are needed, make sure the eNVM update command is executed before the security overwrite command. Put the set_envm_update Tcl command before the set_security_overwrite Tcl command in the Tcl script.

No Programming Support for Virtual Machines (VM)

Programming is supported for physical machines only. Programming is not supported on any Virtual Machine (VM).

Restricts ARM® Cortex®-M3 Debug with DPK (Debug Pass Key)

SoftConsole does not support this feature.

VALIDATE_USER_ENC_KEYS Not Shown in Drop-Down Menu in FlashPro Express

When an HSM task is loaded in FlashPro Express, the VALIDATE_USER_ENC_KEYS action is not available in the drop-down action menu.

Workaround:

Use the following Tcl script commands to run the action:

```
set_programming_action –name {dev_name} –action {VALIDATE_USER_ENC_KEYS}
run_selected_actions
```

Inspect Device Feature Disabled in FlashPro

The Inspect Device feature is disabled in FlashPro for SmartFusion2/IGLOO2 devices beginning with Libero 11.7 Release. Use Standalone SmartDebug instead.

Documentation

Web-based documentation

Starting with Libero SoC v11.7, most Users Guides for SmartFusion2, IGLOO2, and RTG4 are available on the Microsemi website. Libero and Programming/Debug tools will include links to the website.

If the machine on which you have installed Libero does not have access to the Internet, you (or a site administrator) can download all Libero SoC v11.7 Users Guides from Microsemi's Libero SoC documentation site.

Linux: Firefox requirement for Online Help and Users Guides

Libero SoC v11.7 SP1 requires the "Firefox" executable to be in your PATH variable on Linux. Alternatively, you can access the Reference Manuals on the Microsemi website, or by clicking **Help > Reference Manuals** in Libero. For the Libero SoC v11.7 SP1 release, the "Web Browser" selection in the Libero Preferences dialog is only used by Online Help and for some user guide links.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. A 64-bit OS is required for designing SmartFusion2, IGLOO2, and RTG4 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents web page.

Operating System Support

Supported

- Windows 7, Windows 8.1.
- RHEL 5* and RHEL 6, CentOS 5* and CentOS 6.
- SuSE 11 SP4 (Libero only; FlashPro Express, SmartDebug, and Job Manager are not supported)

** RHEL 5 and CentOS 5 do not support programming using FlashPro5.*

Discontinued

- 32-bit operating systems are no longer supported.
- Windows XP is no longer supported.
- Support for the following Operating Systems will cease in the first half of 2017:
  - Solaris Flexlm license daemon support; Libero SoC is already not supported on Solaris.
  - Libero SoC software support for RedHat Enterprise Linux 5, and CentOS 5.

Download Libero SoC v11.7 SP1

This Service Pack is an incremental updates and must be installed on top of the Libero SoC v11.7.

Installation requires Admin privileges.

Windows Download

Linux Download

SoftConsole 3.4/4.0

Libero SoC v11.7 SP1 is compatible with SoftConsole v3.4 SP1 and SoftConsole v4.0.

Download SoftConsole v4.0 for Windows

Download SoftConsole v4.0 for Linux

Download SoftConsole v3.4 SP1 for Windows

Installation Note:

After installation of Libero on Linux, the attempt to run the udev_install script for FlashPro setup fails with this message:

```
% ./udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:
The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, as such, is not a valid shell script.

Workaround:
Run the `dos2unix` command on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
%. /udev_install
```

If the `dos2unix` command is not available, install the command first, and then run `dos2unix, and udev_install`:

```
% sudo yum install dos2unix
% dos2unix udev_install
%. /udev_install
```

Revision History

Revision Number	Date	Author	Comment
1.0	6/3/2016	Microsemi	Initial Release
1.1	6/15/2016	Microsemi	Clarifications on System Verilog support and Updates to Software Enhancements.
1.2	7/12/2016	Microsemi	No Programming Support for VMs added. Workaround for RTG4 Device Reset Added
1.3	7/31/2016	Microsemi	Added to Known Issues: • Device Speed Grade and EPCS Data Rate • SmartFusion2/IGLOO2 Programming Action Warning • Synthesis Extra Pop-Up Warning Messages • Exporting FlashPro Express Job
	8/29/2016	Microsemi	Added to Known Issues • Chip Planner display issue • IOINFF Input-to-Reg slack calculation Issue
1.4	10/17/16	Microsemi	Added Programming Recovery to Known Issues

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Centre, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades; update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; Enterprise Storage and Communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 4,800 employees globally. Learn more at **www.microsemi.com.**

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