Libero IDE v9.2 SP3 Release Notes

Thank you for your interest in Microsemi's Libero Integrated Design Environment (IDE) v9.2 SP3.

These Release Notes are cumulative. In addition to new content, they include the complete Release Notes for the base release and all previous service packs.

Libero IDE v9.2 SP3 includes:

- The Global Set Fuse option is removed from the Generate Programming Files UI in this service pack, which eliminates the option to use internal power-on reset circuits to establish flip-flop states at power-up. To correctly establish the power-up states of flip-flops, Microsemi recommends the use of an external power-on reset circuit.
- Fixes for the SDF back annotated simulation

Libero IDE v9.2 SP2 includes:

- Use of the ProASIC®3 A3PE1500 for RT prototyping with the Free Gold license
- New MX packages for customers migrating from ACT1 and ACT2 devices.

Libero IDE v9.2 SP1 includes:

- Use of the ProASIC®3 A3PE3000 for RT prototyping with the Free Gold license
- Fixes a Designer runtime error introduced in v9.2
- Allows A3PE high-effort layout for RT prototyping

Libero IDE v9.2 includes timing enhancements for RTAX™-S/SL/DSP and Axcelerator FPGA families. This version also updates the routing of long delay lines in RTAX4000S/SL/DSP FPGAs and adds a new design rule check to RTAX-S/SL/DSP pipeline SRAM.

Device Support in Libero IDE

Axcelerator® (including RTAX™-S, RTAX-D)

SX/SX-A (including RTSX/-S/-SU)

ProASIC PLUS (aka APA)

eX

42MX

40MX

ACT1

ACT2/1200XL

ACT3

3200DX

ProASIC (aka 500K)

ProASIC®3E is available for RT prototyping only

Use Libero SoC for designing all other device families.

Contents

What's New in Libero IDE v9.2 SP3

Software Fixes and Enhancements

SAR	Customer Case	Summary
63404	493642-1764988552	pre synthesis simulation of Two Port RAM is not as expected
64022	493642-1800456531, 493642-1858459527	Designer Generate 0.00 as min time for RTSX-SU
68152	493642-1869957150	RTSX72SU simulation issue
68179	493642-1874661784	No ref clk available when create a generated clk
70060	493642-1911587871	Exporting SmartTime .sdc timing constraints after compile step gets appended with additional paths.
72907	493642-1743158292	RTAX/AX:Remove global set fuse selection option from Generate Programming Files UI
76090	493642-2053959082	RTSX-SU postlayout SDF shows 0 delay for all macros in best case?

Fixed in Libero IDE v9.2 SP2

ACT to MX Migration Table

A Tcl script is available to facilitate your design migration. Refer to Application Note AC399 and Application Note AC405 to download the Tcl script.

ACT1		40MX	
A1010B	84 CPGA	A40MX02	84 CPGA
A1020B	84 CPGA	A40MX04	84 CPGA
A1020B	84 CQFP	A40MX04	84 CQFP

ACT2		42MX	
A1240A	144 PQFP	A42MX09	144 PQFP
A1240A	132 CPGA	A42MX09	132 CPGA
A1280A	172 CQFP	A42MX16	172 CQFP
A1280A	176 CPGA	A42MX16	176 CPGA

Software Fixes in 9.2 SP2

SAR	Customer Case	Summary
59059	493642-1668140385	SXS SDC: TDPR crashes if length of clock constraint exceeds 100 chars
61015		incorrect SDC conversion
59397	493642-1676544432, 493642-1720933183	9.2 SDF does not match Tmin best number
58433	493642-1657158666	Timing report has incorrect External Setup with EMD
55484		SmartPower reports 1/2 power for RTAX LVDS I/Os
59880		Add A3PE1500 for RT Prototyping

Fixed in Libero IDE v9.2 SP1

57490 Fixes a v9.2 problem that prevents running high-effort layout for A3PE devices.

57773 Fixes runtime error when executing Designer in Libero IDE 9.2 using Gold license.

56282 Add A3PE3000 to the free Libero Gold license.

Introduced in Libero IDE v9.2

New Implementation of Min-Max Timing Analysis for RTAX™-S/SL/DSP FPGAs

Libero IDE v9.2 includes timing enhancements for Hold Check under Worst Case and Setup Check under Best Case timing analysis for RTAX™-S/SL/DSP and Axcelerator FPGAs. Please read Application Note AC395: RTAX-S/SL/DSP Timing Analysis Using Libero IDE v9.2 for details. This document describes a detailed max-min analysis of the external setup and hold time and clock-to-output time for a synchronous design implemented in Microsemi RTAX™- S/SL/DSP FPGAs. We recommend four-corner timing analysis on RTAX-S/SL/DSP and AX designs. See Customer Notification CN1410.

Routing change for RTAX4000S and RTAX4000D.

Libero IDE 9.2 implements a routing constraint on RTAX4000S and RTAX4000D designs. The router will not create connections using more than four unbuffered long lines. This change to routing behaviour is intended to avoid long propagation delays in RTAX4000S and RTAX4000D designs. For more information, refer to Customer Notification CN1412.

AX/RTAX-S/RTAX-D pipeline SRAM issue

Libero IDE v9.2 provides a new SRAM design rule check (DRC) put in place for RTAX and AX designs. This check will prevent the usage of a pipeline SRAM configuration which can result in a race condition in the SRAM. For more information, refer to Customer Notification CN1411.

Designer is no longer available from the Programs > Microsemi Libero IDE v9.2 list

Select Libero IDE v9.2.

Alternatively, you can double-click on <installation_path>\Microsemi\Libero_v9.2\Designer\bin\designer.exe.

Resolved Issues in the v9.2 Release

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

Table 1 Resolved SARs in Libero IDE v9.2 Release

SAR	Case Number	Product	Summary
25751	1-40412951	Synopsys	Need attribute to control AX DFM* macro inference.
27434	489394-107140793 489394-178835093 493642-30133523 493642-32925603 493642-559503196	VHDL Library	Inconsistent data in the DP RAM when the data is read back out.
28808	489394-198764592	SmartTime	Running datasheet report in SmartTime corrupts timing data in subsequent analysis.
30657	489394-399717782	Misc	RHEL6-Request for newer MOTIF Library Support in Libero Linux.
37665	493642-1028036568	Timing	RTAX-S/SL/DSP External Setup decreased when temperature increased
45569	493642-1063001761	Designer	Creating ANTIFUSESTATS report causes different AFM file.
44005	493642-1196381888	Compile	Libero v9.1 SP5 Designer crashes when an ADB created with Libero 9.1.3 is opened.
44457	493642-1215350914	Designer	Designer crash during layout stage.
45502	493642-1215350914	Designer	Excessively long instance names causes crash during layout.
44838	493642-1219970789	Designer	RTSX-SU Prototyping flow for CQ84 is not implemented.
45501	493642-1231776798	Timing	SXA/S Net delay no change between FF to Latch even place a new location
47801	493642-1296864192	Timing	Re-open a saved ADB does not keep the min delay analysis
48809	493642-1355056818	Timing	Tcl command: st_expand_path does not generate complete report in CSV format.
50919	493642-1412481392	Timing	RH1280 design has large delay on bi-directional bus.
51128	493642-1458982040	Timing	Best case analysis considers non-zero Krad (radiation).
52134	493642-1474493016	CAE	AX Vital lib has wrong if statement.
52150	493642-1494513598	Timing	Timing driven layout crashes in Libero 9.1 SP5.
52296	493642-1495486649	SmartGen	RTAX_COUNTER: Compact counter does not function correctly at 26th bit & onward.
52323	493642-1499505826	Layout	Prototyping file generation is crashing.
53518	493642-1503387344	Timing	RTAX4000D: EMD factors still in default values.
53517	493642-1503387344	Timing	RTAX4000S -1 speed grade factor on nets is not correct.
52388	493642-1503683041	Timing	Max/Min delay constraints enhancements.
53461	493642-1523263801	Timing	SmartTime issue with cross clock domain timing analysis.
53449	493642-1529815451	Timing	Incorrect clock constraint on inter-clock domain analysis.
53765	493642-1539844086	Timing	Timing difference between SmartTime GUI & timing report.
53961	493642-1552954572	VHDL Library	APA Dynamic PLL simulation model issue.
30870	493642-25401413	Synopsys	Netlist Implementation of 40 MX and 42MX.
36094	493642-553205603	SmartTime	Constraints coverage report fails to recognize constraints.
36750	493642-622346682	SmartTime	Enhance data sheet reporting functionality.
36746	493642-624269471	Synopsys	Using syn_maxfan & syn_noclockbuf but signals are still buffered.
37748	493642-744434833	Compile	Optimized netlist is dropping INV from the original netlist.
53444	493642-752234875, 493642-1510861284	Compile	Port missing after publishing the Designer block.
32724	493642-87097473	SmartTime	Constraint Coverage Report.
40282	93642-945599141	Synplify Pro	Post-synthesis simulation failed with Synplify Pro ME 2010.09A-1 & speed_grade=STD.

Synopsys and Mentor Graphics Tools

The following versions are included with Libero IDE v9.2. Future releases of Synopsys ME tools will be released standalone as they become available.

- Synplify Pro ME G-2012.09A SP4 - This version resolves the problems described in PCN 1209, 1309, and CN 1404
- Identify ME H-2013.03M SP1
- Synphony Model Compiler ME I-2013.09M-1
- ModelSim 10.2c ME

Prerequisite Software: To run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

OEM Release Notes and User Guides

Mentor Graphics ModelSim® ME
Synopsys Synplify Pro ME
Synopsys Identify ME
Synphony Model Compiler ME

Known Limitations, Issues and Workarounds

AX generated clocks issue with SP3

Users may see an issue (crash) with Timing-driven Place and Route or Timing analysis when an AX design has a PLL and the timing constraints file has a generated clock constraint (that is, 'create_generated_clock' constraint) on the PLL output clocks. To get around this issue, users can use create clock constraint (that is, 'create_clock') on the PLL output.

Repeated clock-to-out entries in SmartTime (RTAXS)

SmartTime clock-to-output incorrectly displays multiple repeated entries (i.e. fills to 'number of paths' limit with repeats). As a result, no other signals can be accessed from the summary level.

Workaround: The repetition is due to the generated clock on the output port. It is possible to see other paths in the same set by temporarily removing the generated clock or by explicitly looking for paths to a specific output.

Synplify Pro will not run in batch mode with a node-locked license

If you want to run Synplify Pro ME in batch mode you need a floating license. Floating licenses for Libero Gold are free. If you are purchasing Libero Platinum, request a floating license product. If have a Libero Platinum node-locked license and want to exchange it for floating, please contact customer.service@microsemi.com.

Unresponsive Buttons on Linux

Buttons (Close, Browse, OK, Cancel, Next, Back, etc.) in the configurators and dialog boxes may be unresponsive to mouse clicks when the window is first opened.

Workaround*:* Move the entire dialog box slightly. The buttons will then respond.

Also, some of the buttons must be double-clicked (such as Execute Script dialog buttons), which is not typical button behavior.

Drag and drop of Catalog components to SmartDesign Canvas may stop working when using VNC on Linux

Use one of the following workarounds to solve the issue:

- Right-click the selected core in the Catalog and choose **Instantiate in SmartDesign**.

- Exit Libero. Create a new VNC session and log back in to the machine. Start Libero. The drag and drop feature will be enabled.

JTAG Reset Option Description in the Online Help is Incorrect

RTAX-S enables you to program an internal pull-up resistor for the JTAG TRST pin. This option is available in the Programming dialog box. The help topic for this dialog box is INCORRECT. It says:

Use the JTAG reset pull-up resistor - Forces the JTAG circuitry to constantly be in RESET. Microsemi recommends that you use this option.

The correct statement is:

Use the JTAG reset pull-up resistor – Programs the pull-up and forces TRST to HIGH so that it will not reset the Tap controller.

FlashPro Issues Previously Reported in Libero IDE v9.0 SP3 Release Notes

23423 - Error when using Inspect Device if JTAG chain is constructed by performing Auto-Chain Construction.

If the JTAG chain is constructed automatically by selecting Construct Chain Automatically in the **Configuration** Menu, and you click the Inspect Device button, you will see the following error:

Error: Cannot initialize debug engine: Cannot initialize the programmer: No available Actel products found on USB port.

Workaround*:*

Option 1: Construct the device chain by manually specifying the list of devices in the chain using the **Add Actel Device** or **Add non-Actel Device** options, and save the FlashPro project.

Option 2: Manually resolve the device by selecting the Actel device that is in the chain, and save the FlashPro Project.

Option 3: Load the programming file for the devices in the chain; execute read_idcode action in the programming files, and save the FlashPro Project.

6871 - Cannot load the same PDB for multiple devices or copy and paste.

Workaround: Use STAPL files. Generate STAPL files from Libero IDE or FlashPro.

6859 - When using FlashPro programmer with Windows Vista operating system, the Refresh/Rescan may remove the programmer from the programmer list.

Workaround: Restart the FlashPro software. This action will refresh the list of programmers.

System Requirements

Refer to System Requirements on the web for more information regarding operating system support and minimum system requirements.

Libero IDE v9.2 and its service packs require runtime components of Microsoft Visual C++ libraries. If a Libero IDE application fails to start, download and install one of the following packages:

- For 32-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x86)
- For 64-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x86)

Setup Instructions for Red Hat Enterprise Linux OS can be found on the Libero IDE Documents webpage.

Download Libero IDE v9.2 SP3

Important Note: *Libero IDE v9.2 SP3 is an incremental service pack and must be installed over Libero IDE v9.2, Libero IDE v9.2 SP1, or Libero IDE v9.2 SP2.*

Download Libero IDE v9.2 SP3 here:

Windows

Linux

If you have not previously installed Libero IDE v9.2 you can download it from:

Libero IDE 9.2 for Windows

Libero IDE 9.2 for Linux

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.
The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; Enterprise Storage and Communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 4,800 employees globally. Learn more at **www.microsemi.com.**

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