Total Ionizing Dose - 00T-RT1460-UCK069

TR0024 Test Report

February 12, 2016

Microsemi

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I. Summary Table

Parameter	Tolerance
Gross Functionality	> 16 krad (Si), exact number depending on customers application
$I_{DDSTDBY}$	Passed 16 krad (Si) , <6mA after room temperature anneal
V_{IL}/V_{IH}	Passed 16 krad (Si)
V_{OL}/V_{OH}	Passed 16 krad (Si)
Propagation Delays	Passed 16 krad (Si)
Rising/Falling Edge Transient	Passed 16 krad (Si)
Power-up Transient Current	Passed 16 krad (Si)

II. Total Ionizing Dose Testing

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. DUT

Table 1 lists the DUT information.

Table 1 DUT Information

Part Number	RT1460A
Package	PG207
Foundry	MEC
Technology	0.8 μm CMOS
Die Lot Number	UCK069
Quantity Tested	4
Serial Number	LAN3501, LAN3502, LAN3503, LAN3504

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2 Irradiation Parameters

Facility	NASA
Radiation Source	Co-60
Dose Rate	6 krad (Si)/day (+-10%)
Final Total Dose	16 krad (Si)
Temperature	Room
Bias	5.0 V

C. Test Method

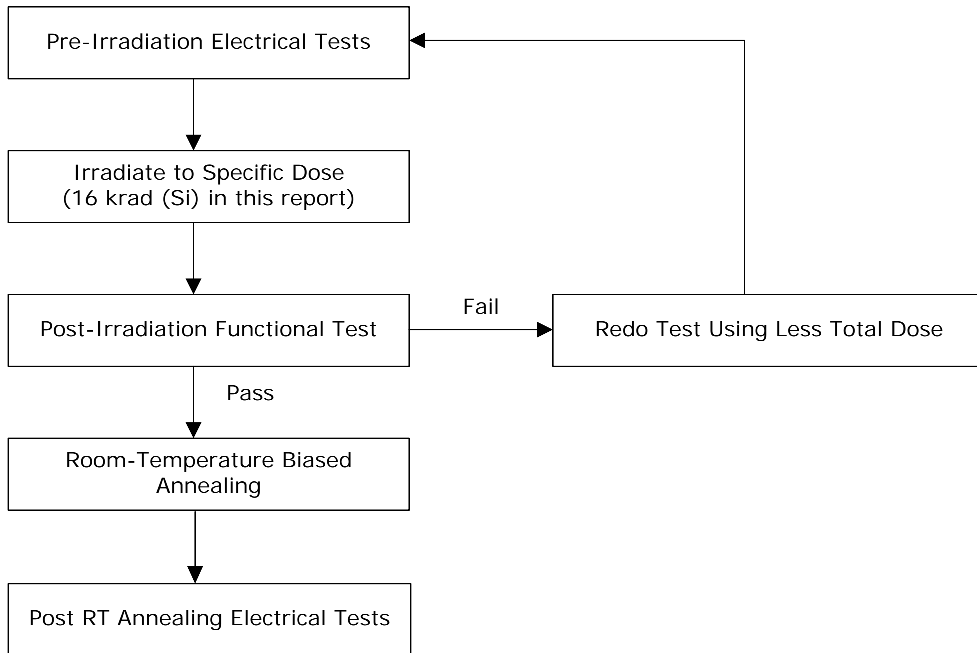

Figure 1 Parametric Test Flow Chart

In Microsemi Total Ionizing Dose (TID) testing, the following two methods are used:

- Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.
- Method two performs irradiation and then parametric test. Gross functional test is included in this method. This method is in compliance with TM1019. Biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results shows that antifuse field programmable gate arrays (FPGAs) fabricated in the MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, the bench setup has less noise but can only sample a few pins (due to logistics, not inability). However, since the $I_{DDstandby}$ always determines the tolerance, sampling a few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDstandby}$ and functionality (of selected pins) during irradiation. This isn't logistically possible for an automatic tester. Also, an important but non-standard parameter, power-up transient current, can only be measured on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3 Logic Design for Each Measured Parametric

Parameters	Logic Design
Functionality	All key architectural functions
$I_{DDSTDBY}$	DUT power supply
V_{IL}/V_{IH}	TTL compatible input buffer
V_{OL}/V_{OH}	TTL compatible output buffer
Propagation Delays	String of inverters
Rising/Falling Edge	D flip-flop output
Power-up Transient Current	DUT power supply

III. Test Result Reports

Test result reports can be generated in the following two methods:

- Irradiate to Gross Functional Failure
- Irradiation and Parametric Test

A. Irradiate to Gross Functional Failure

This test was not performed in this report.

B. Irradiation and Parametric Test

This section presents the parametric test results for pre-irradiation and post room temperature annealing tests. The only post-irradiation test is the gross functional test, as shown in Figure 1.

1. Functional Test

Table 4 lists the functional test results.

Table 4 Functional Test Results

	Pre-Irradiation	Post-Irradiation	Post-Annealing
LAN3501	passed	passed	passed
LAN3502	passed	passed	passed
LAN3503	passed	passed	passed
LAN3504	passed	passed	passed

2. $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ is monitored during the irradiation and room-temperature annealing. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation/annealing effect. Compared to the spec of 25 mA, the small (<1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25 mA and used to determine tolerance.

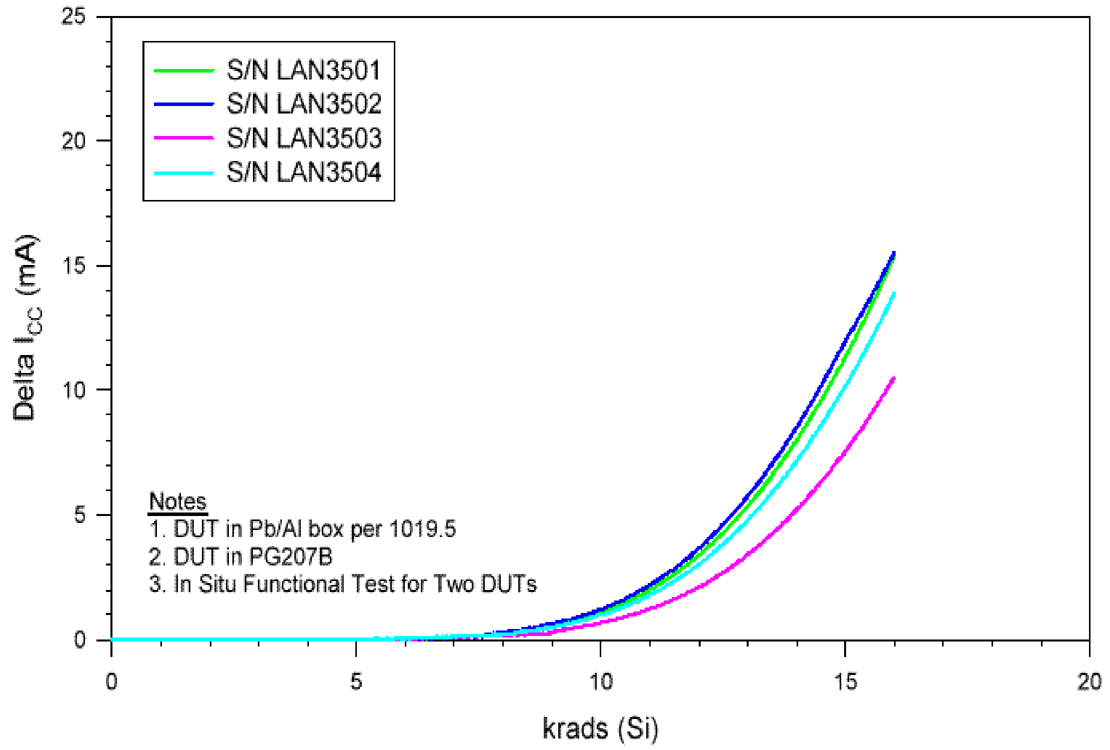

Figure 2 Delta $I_{DDstandby}$ Versus Total Dose

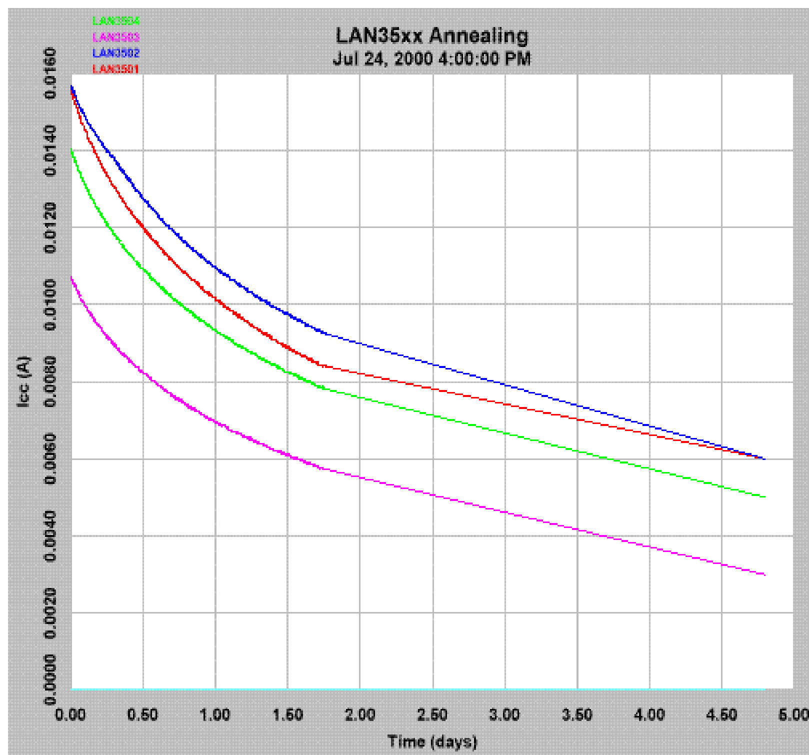

Figure 3 Delta $I_{DDstandby}$ Annealing Curves

As shown in Figure 2, DUT serialized LAN3501, LAN3502, LAN3503 and LAN3504 were irradiated to 16 krad (Si). Every DUT has $I_{DDstandby}$ below 25 mA (the spec) after irradiation. Figure 3 shows the annealing curves. This biased annealing at room temperature is used to reduce the static leakage and power-up transient current.

3. Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-room-temperature annealing. The irradiated-and-annealed DUT is within the spec and the change for each DUT is less than 10%.

Table 5 Input Logic Threshold (V_{IL}/V_{IH}) Results

	Pre-Irradiation	Post-Annealing
LAN3501	1.27 V	1.27 V
LAN3502	1.27 V	1.27 V
LAN3503	1.27 V	1.27 V
LAN3504	1.27 V	1.27 V

4. Output Characteristic

Figure 4 and Figure 5 show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUT. All irradiated-and-annealed DUT are within the spec and no significant radiation effect can be identified. The spec is, at I_{OL} = 6 mA, V_{OL} cannot exceed 0.4 V.

Figure 6 and Figure 7 show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUT. All DUT passed the spec and the radiation effect is negligible. The spec is, at I_{OH} = 4 mA, V_{OH} cannot be lower than 3.7 V.

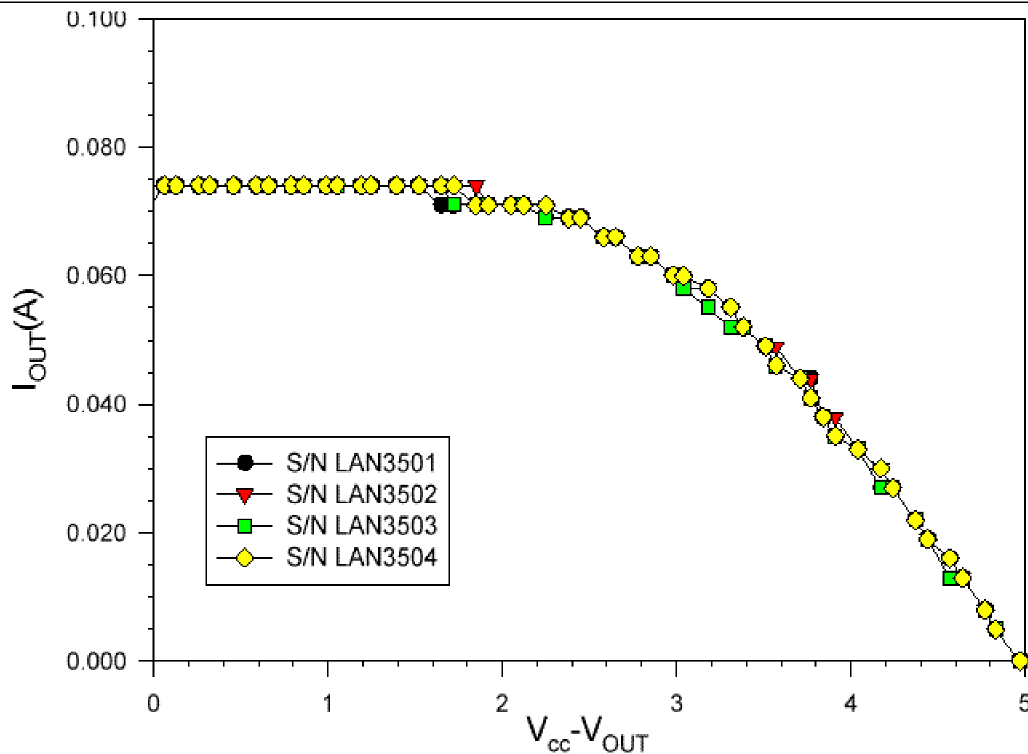

Figure 4 Pre-irradiation V_{OL} Characteristic Curves

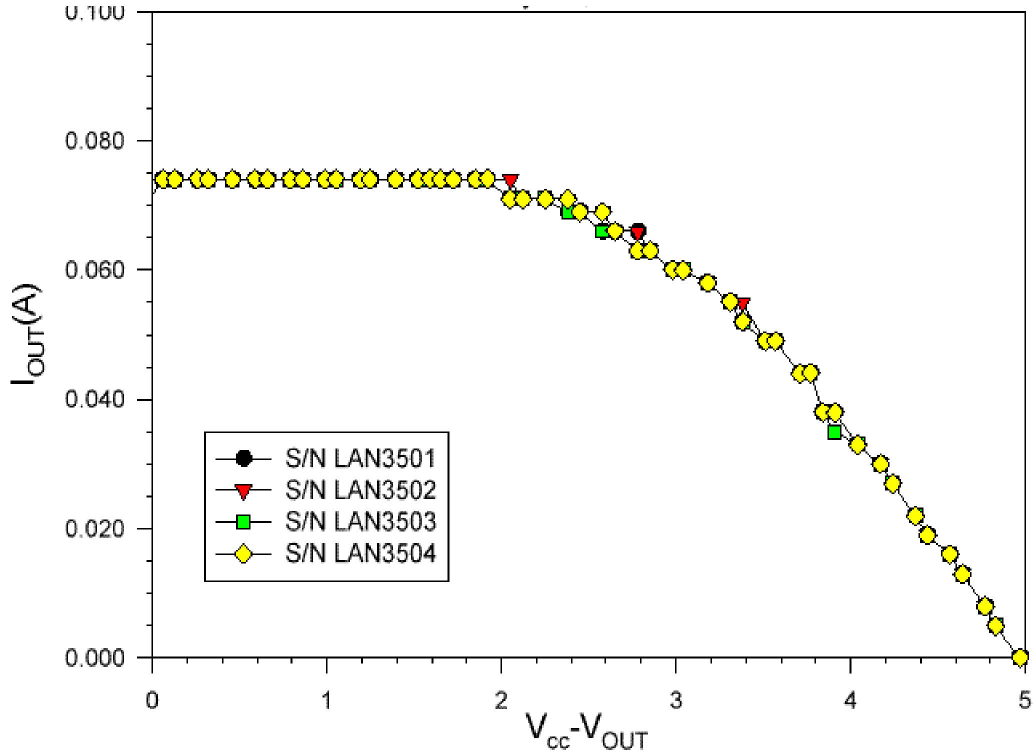

Figure 5 Post-annealing V_{OL} Characteristic Curves

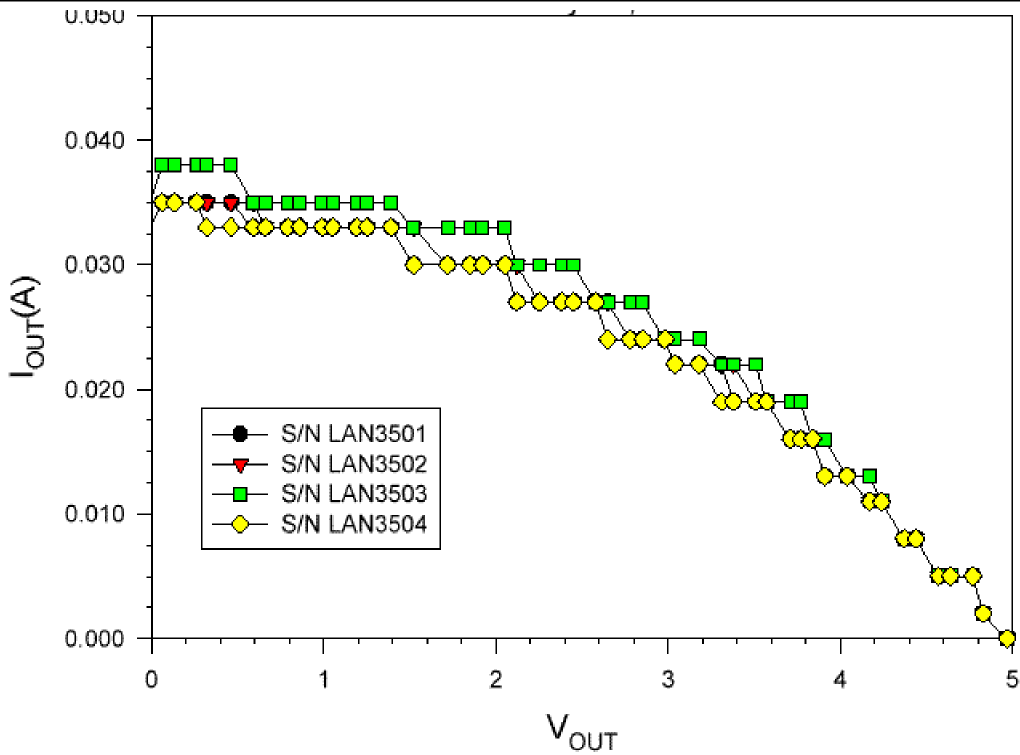

Figure 6 Pre-irradiation V_{OH} Characteristic Curves

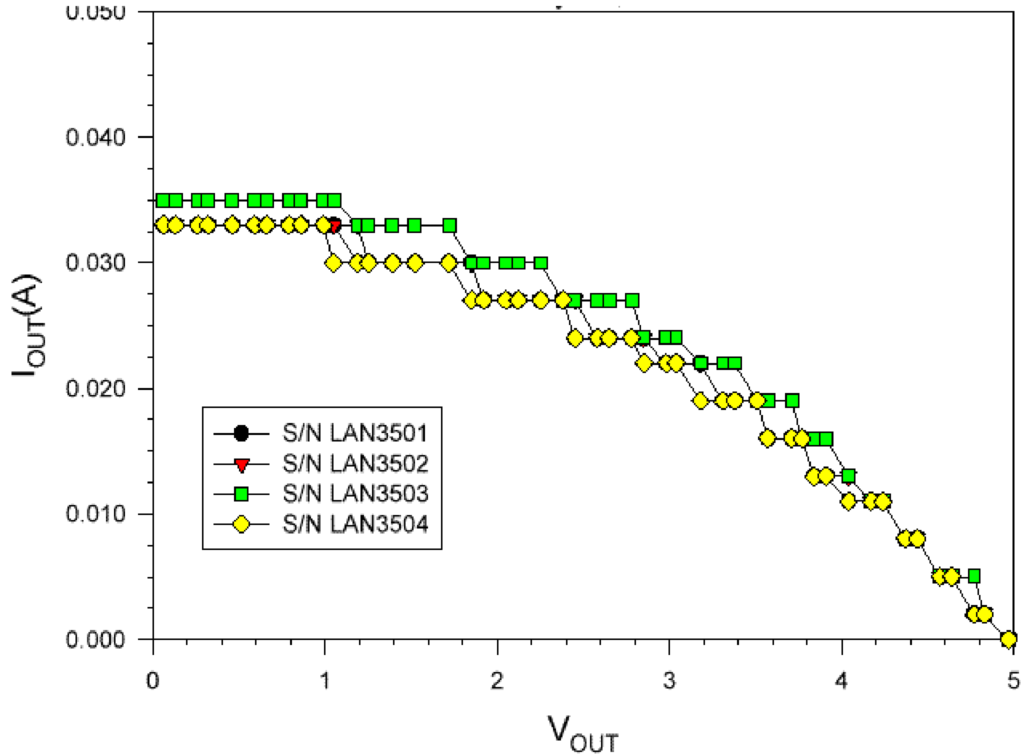

Figure 7 Post-annealing V_{OH} Characteristic Curves

5. Propagation Delays

The propagation delays were measured on three paths, including a combinational path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, Table 7, and Table 8 list the results. The variation due to radiation effect is always within 10%.

Table 6 Propagation Delays of Combinational Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	**Post-Annealing**	**Pre-Irradiation**	**Post-Annealing**
LAN3501	562	575	560	578
LAN3502	531	542	529	545
LAN3503	521	530	520	534
LAN3504	540	552	538	555

Table 7 Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	**Post-Annealing**	**Pre-Irradiation**	**Post-Annealing**
LAN3501	9.7	9.6	8.8	8.9
LAN3502	9.3	9.1	8.5	8.4
LAN3503	9.4	9.2	8.7	8.6
LAN3504	9.6	9.5	8.7	8.7

Table 8 Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN3501	7.2	7.3	6.1	6.0
LAN3502	6.7	7.0	5.8	5.7
LAN3503	6.5	6.6	5.8	5.5
LAN3504	6.8	6.9	5.9	5.7

6. Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figure 8 and Figure 9 show the rising edge transients of LAN3504. Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, and Figure 17 show the falling edge transient of LAN3501, LAN3502, LAN3503, and LAN3504. The radiation effect is basically negligible.

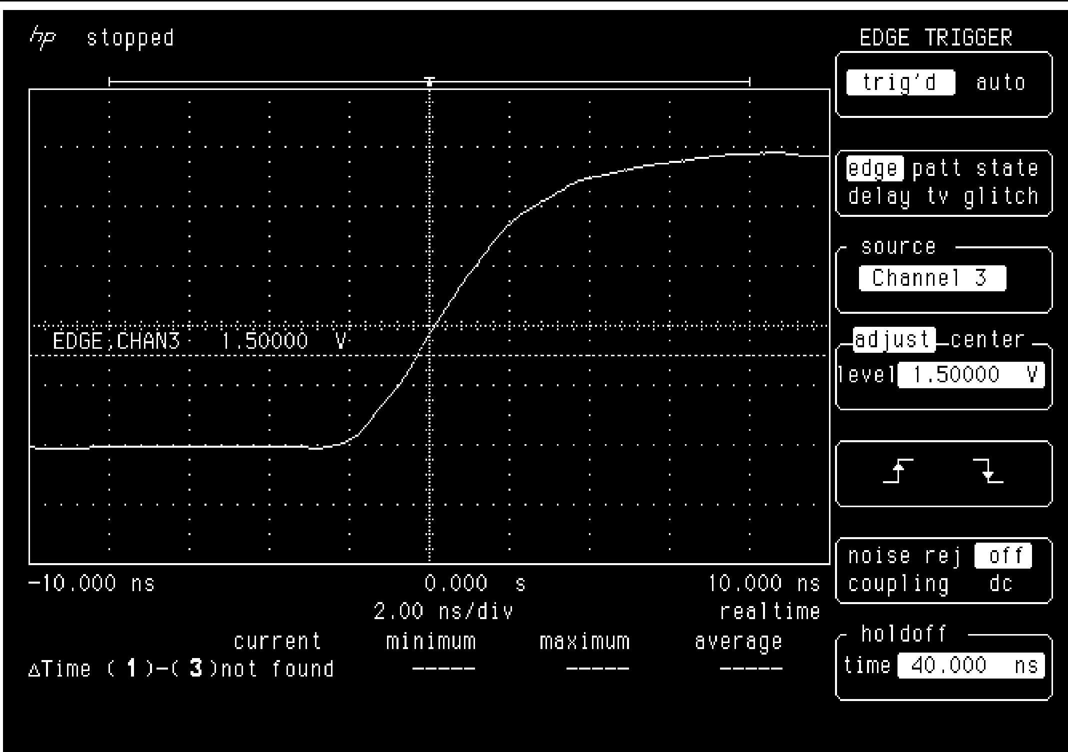

Figure 8 Rising Edge of LAN3504 Pre-irradiation

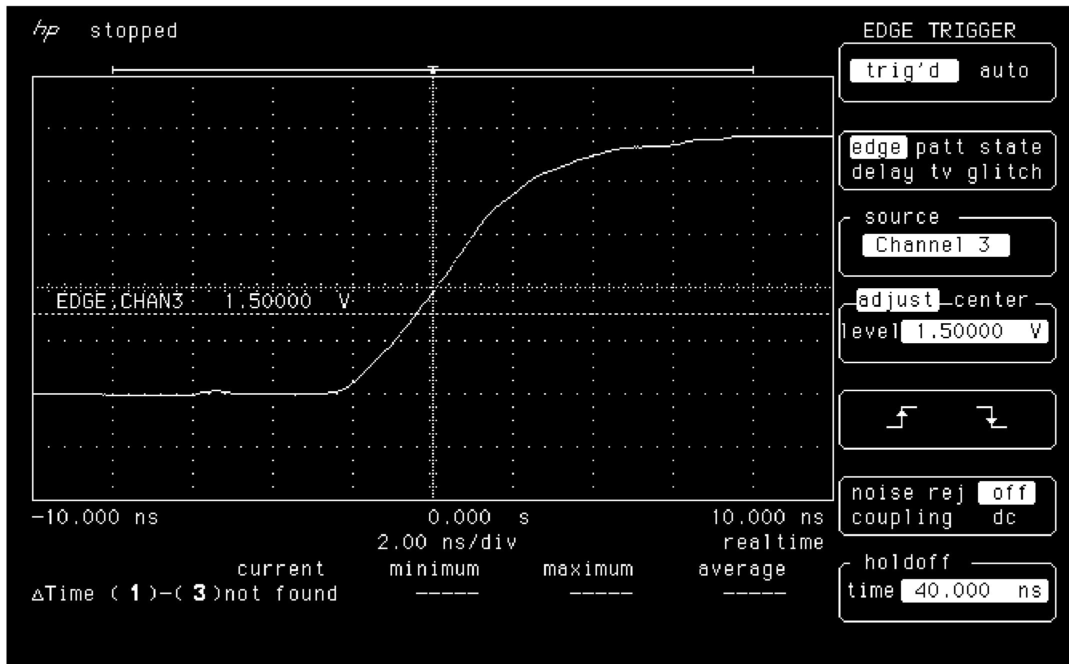

Figure 9 Rising Edge of LAN3504 Post-annealing

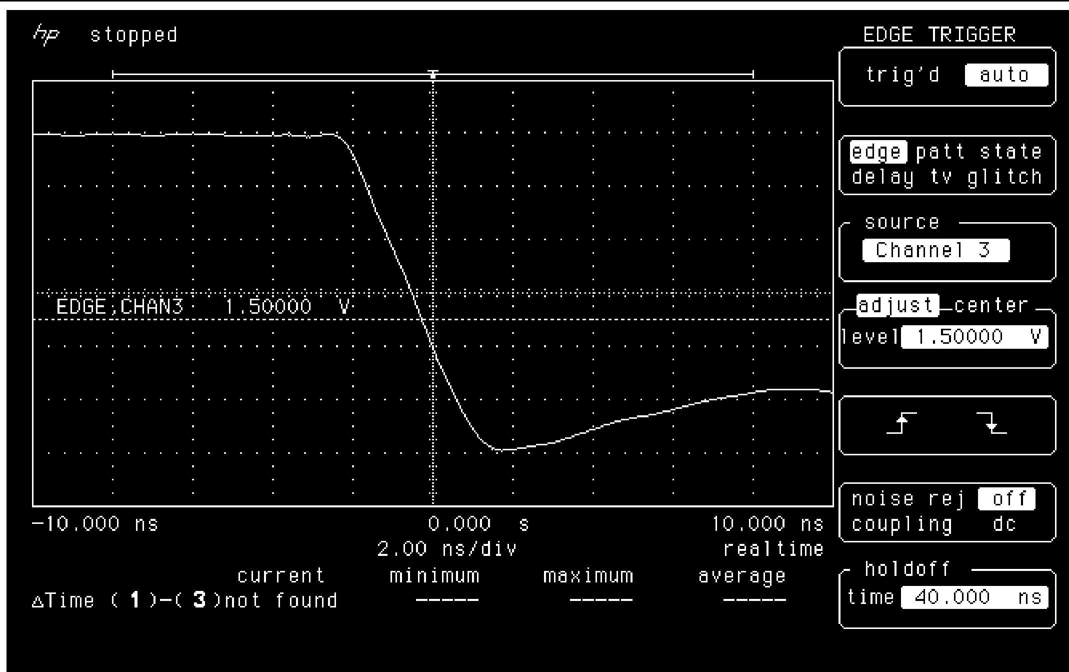

Figure 10 Falling Edge of LAN3501 Pre-irradiation

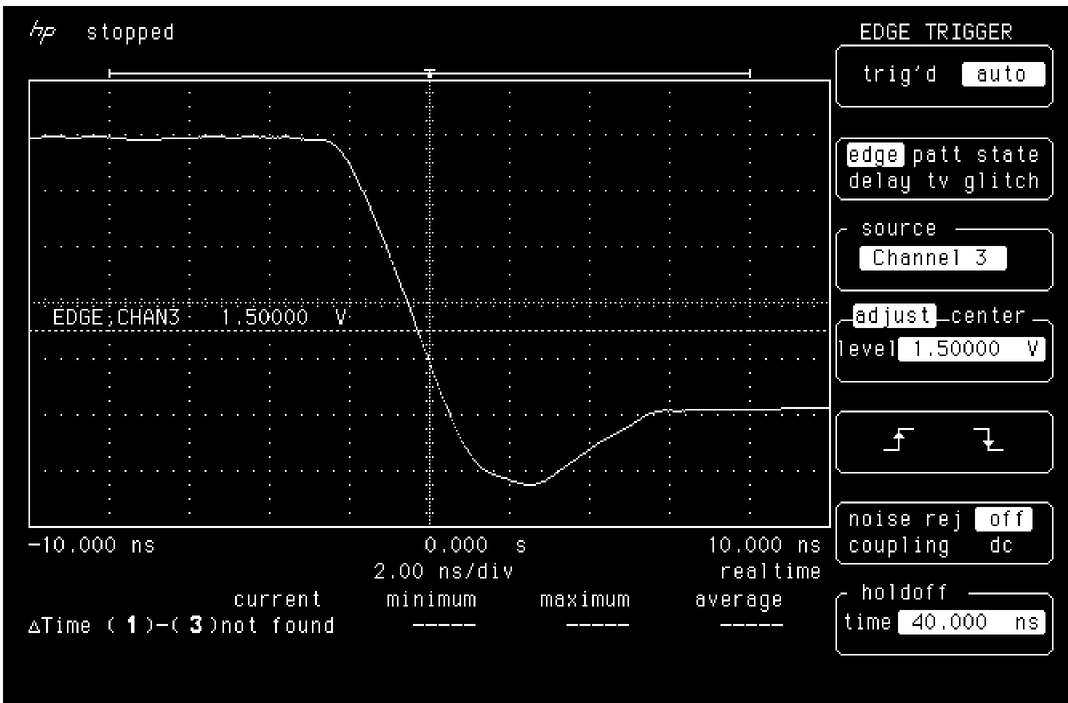

Figure 11 Falling Edge of LAN3501 Post-anneal

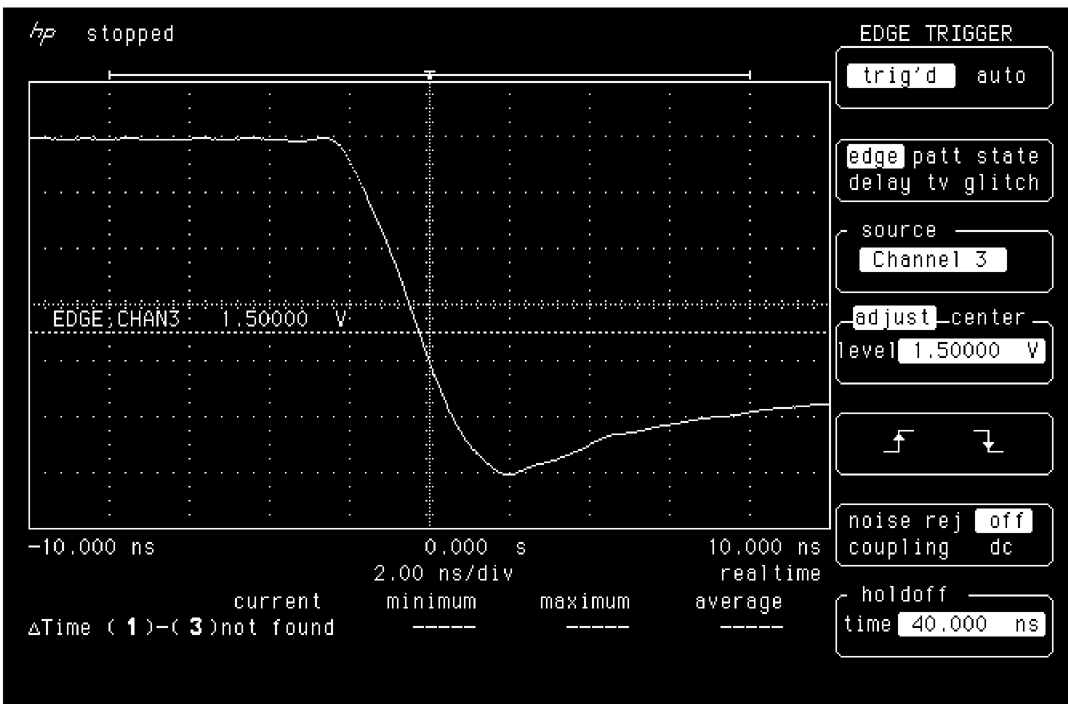

Figure 12 Falling Edge of LAN3502 Pre-irradiation

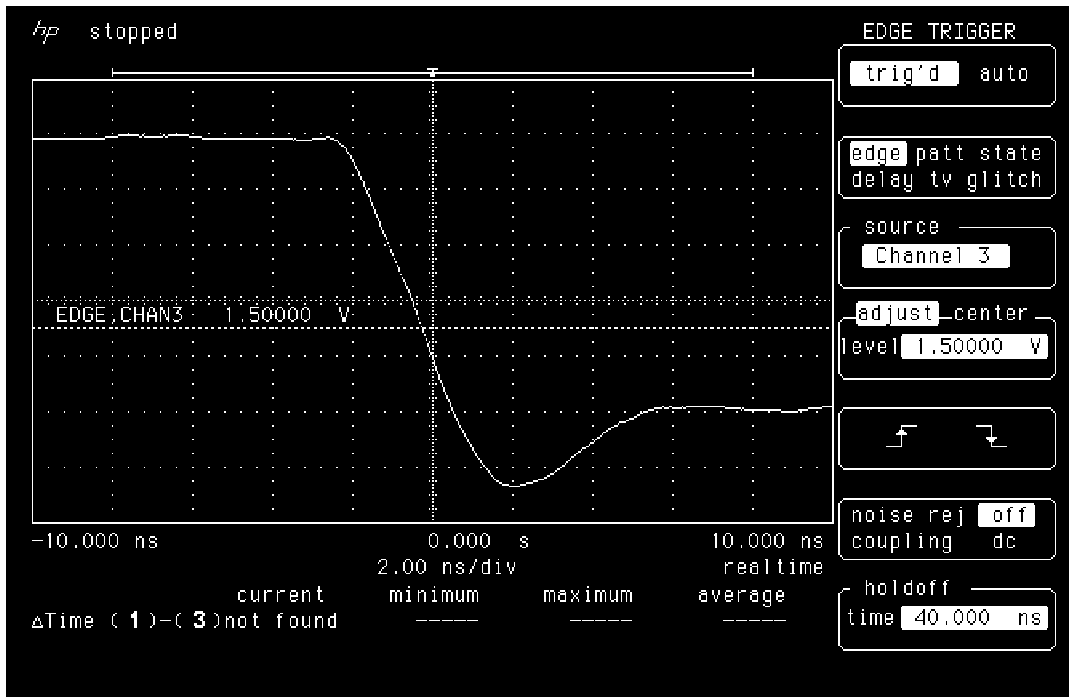

Figure 13 Falling Edge of LAN3502 Post-annealing

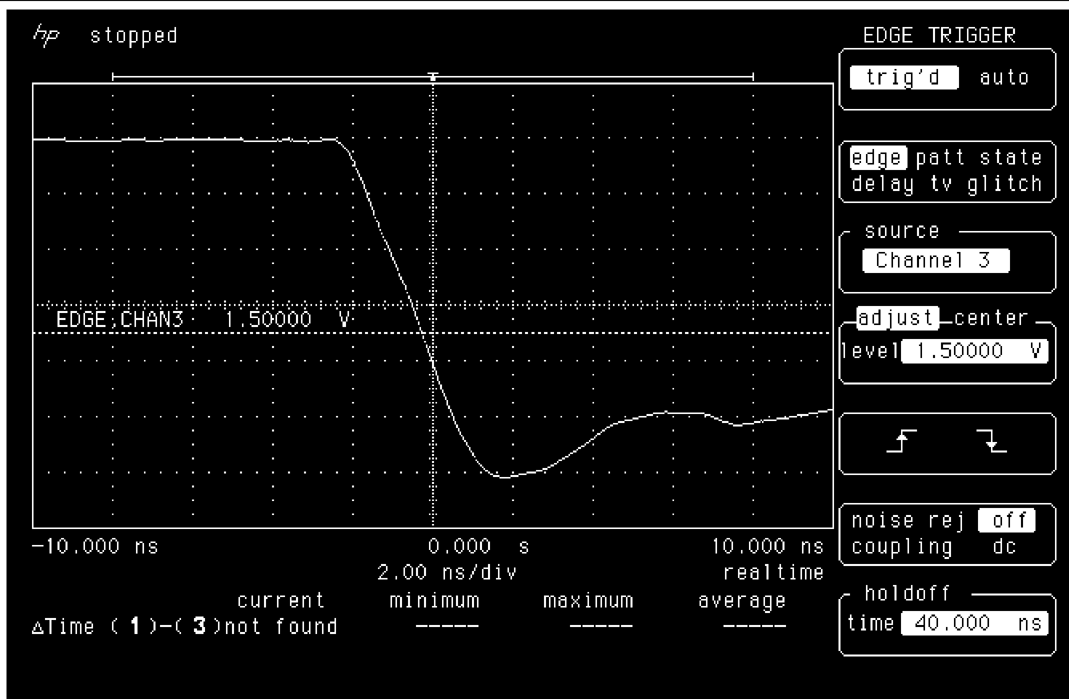

Figure 14 Falling Edge of LAN3503 Pre-irradiation

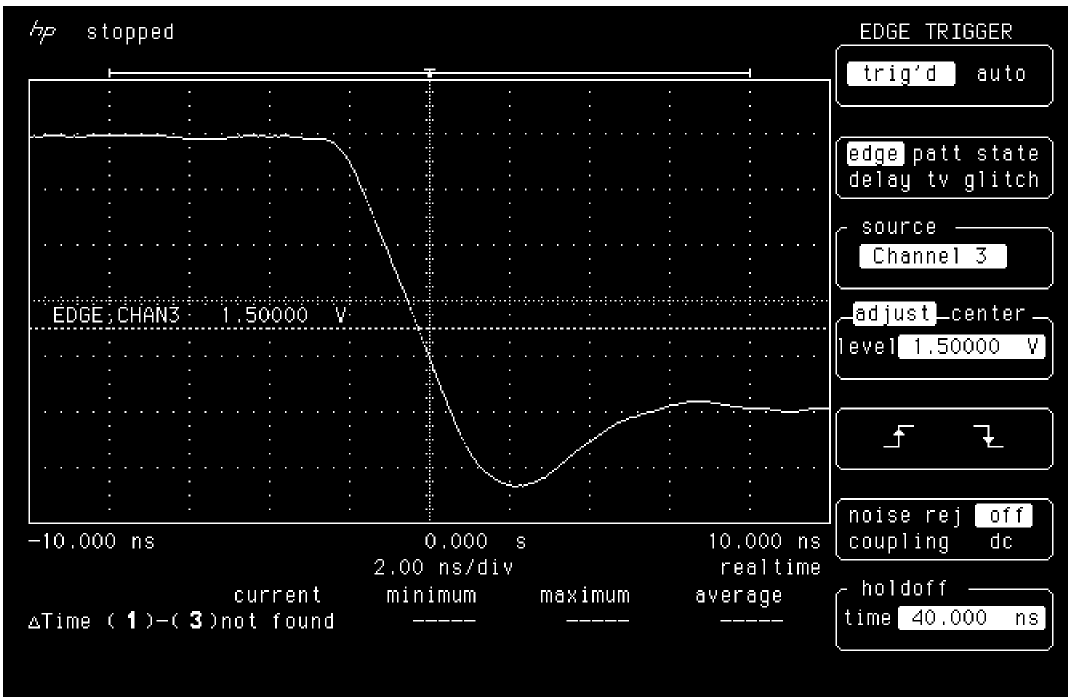

Figure 15 Falling Edge of LAN3503 Post-annealing

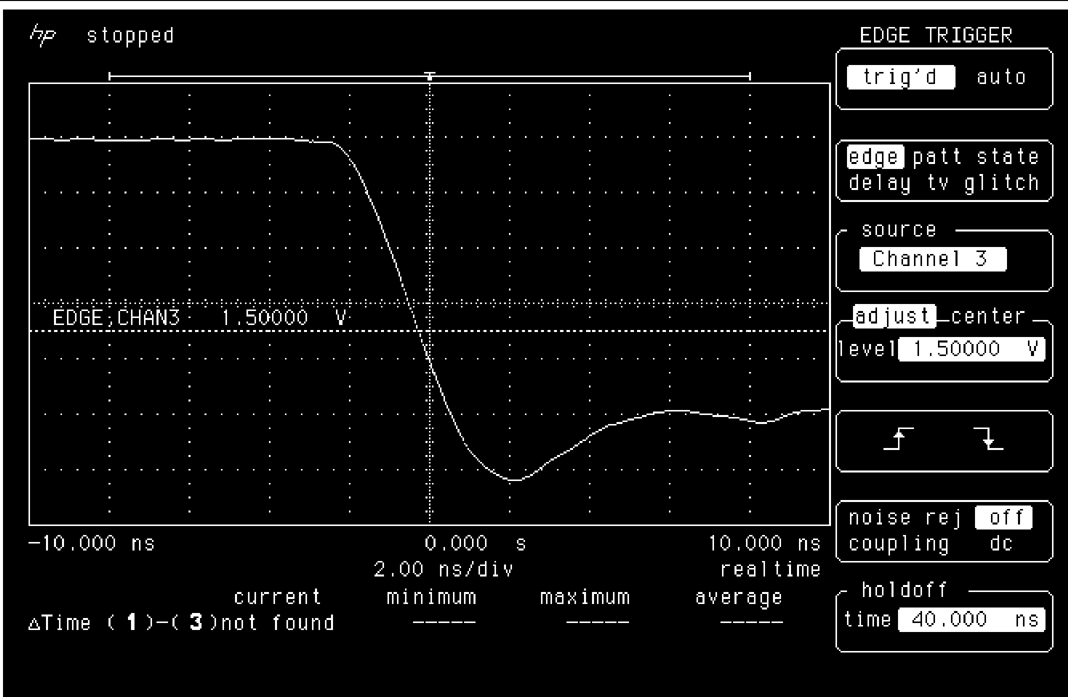

Figure 16 Falling Edge of LAN3504 Pre-irradiation

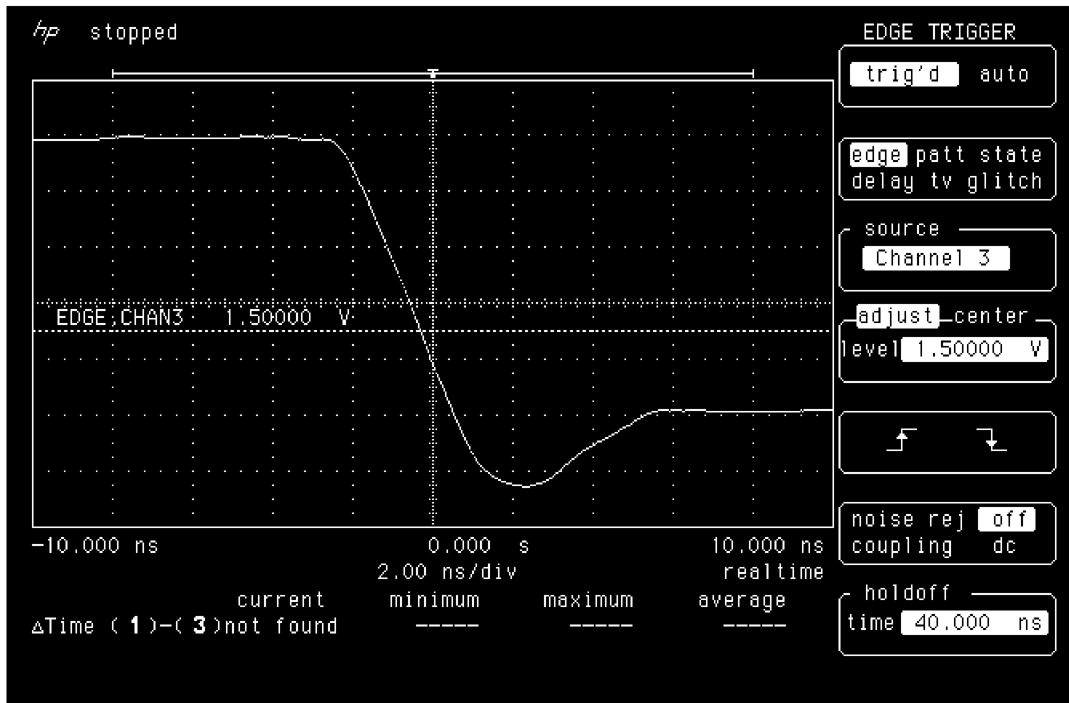

Figure 17 Falling Edge of LAN3504 Post-annealing

7. Power-Up Transient

In each measurement, the rising time of the power supply voltage (V_{CC}) was set at 1.2 ms. The board housing the DUT has a minimum capacitance, so that the transient current comes only from the DUT. Figure 18, Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, and Figure 25 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 5.0 V, and another curve showing I_{CC}. The scale is 1 V per division for V_{CC} and 100 mA per division for I_{CC}. These pictures show that 16 krad (Si) of irradiation basically has no impact on the power up.

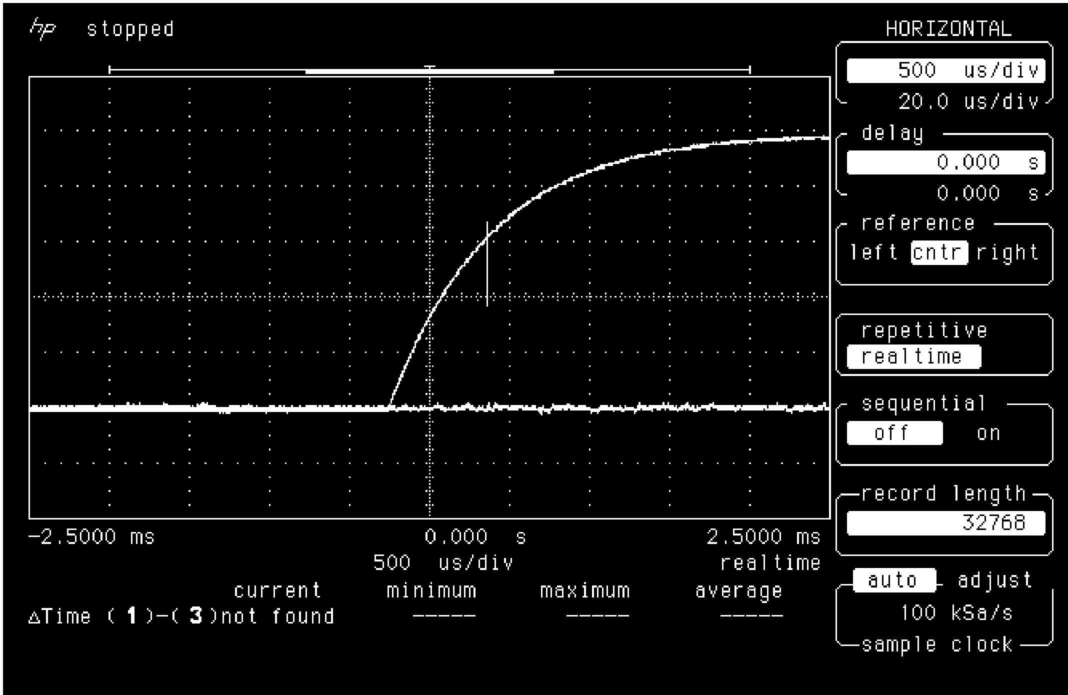

Figure 18 Power-up Transient of LAN3501 Pre-irradiation

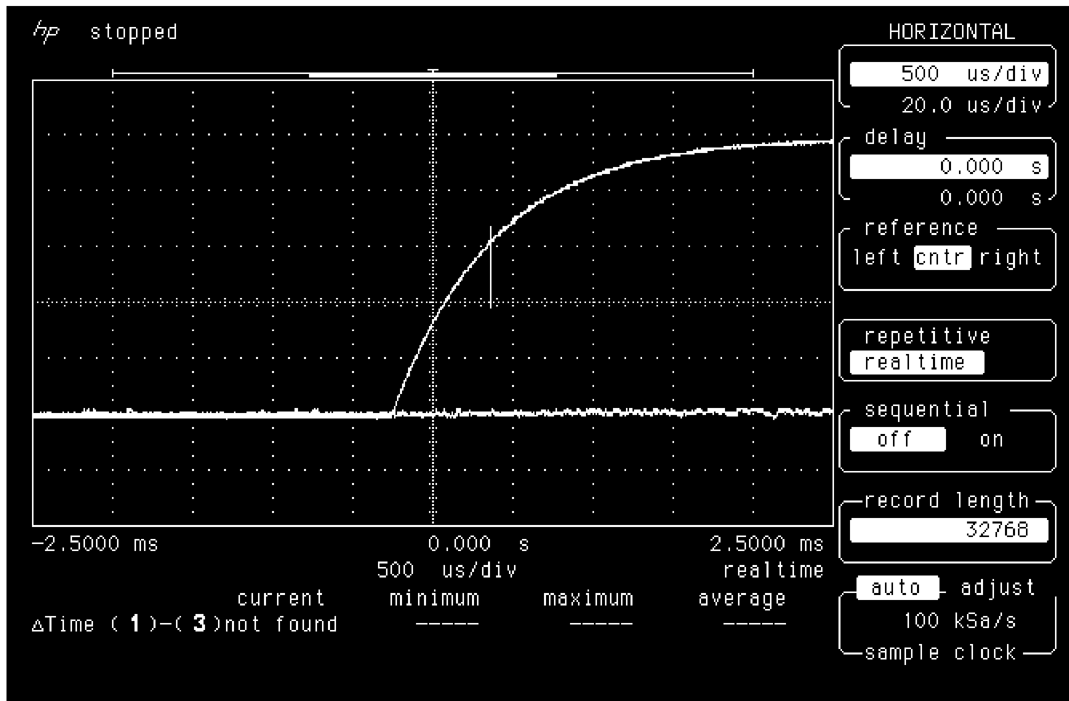

Figure 19 Power-up Transient of LAN3501 Post-annealing

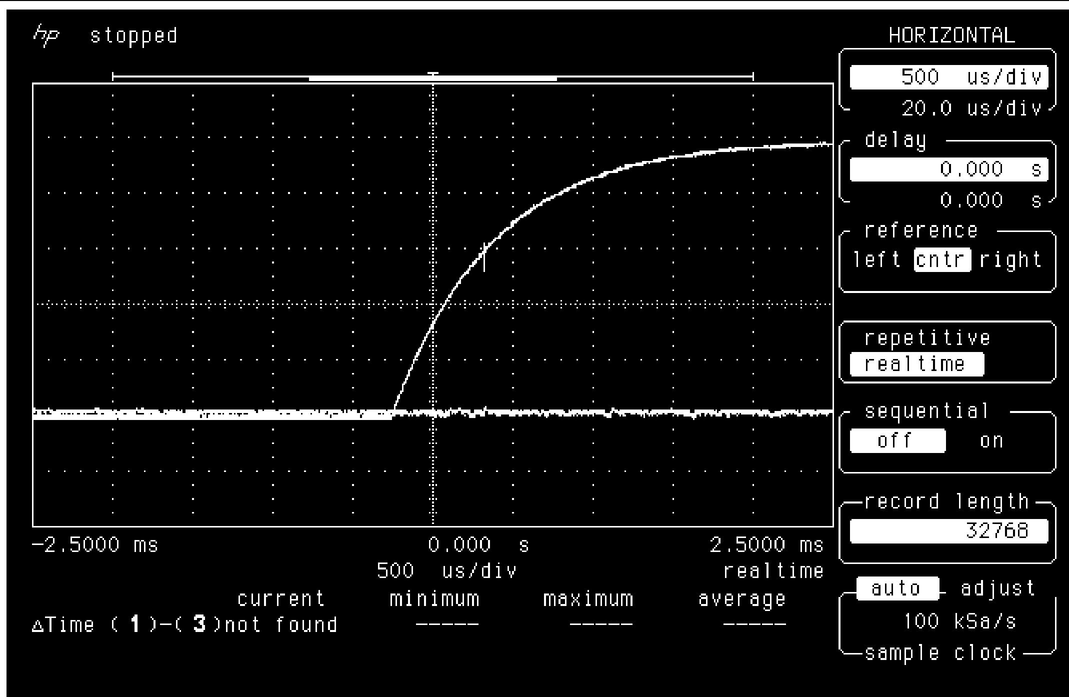

Figure 20 Power-up Transient of LAN3502 Pre-irradiation

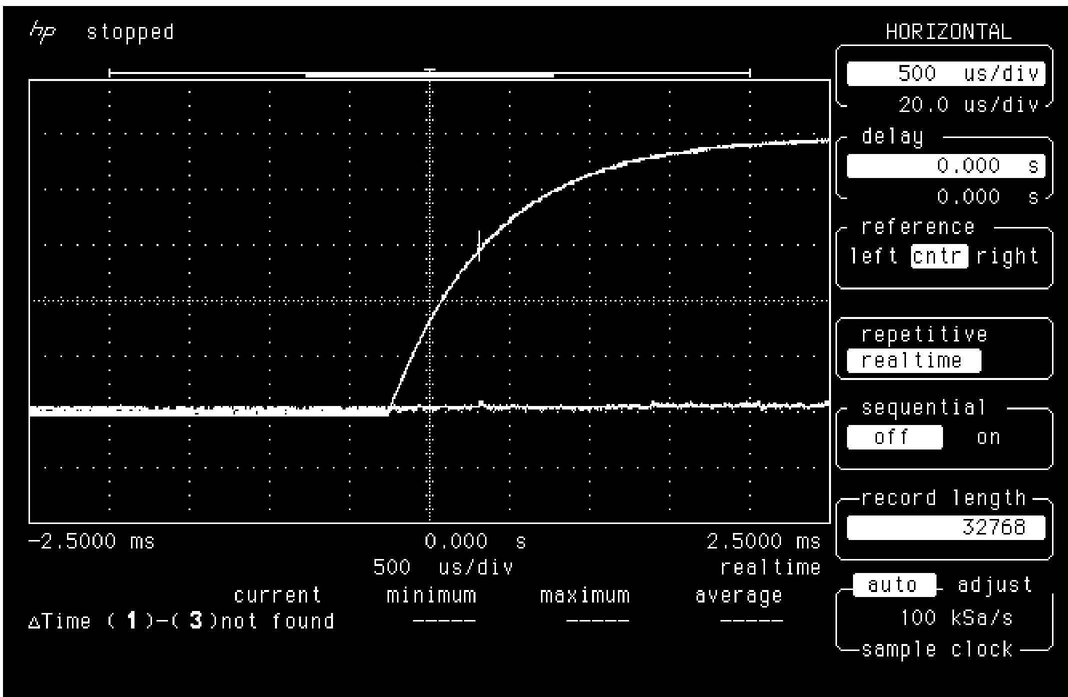

Figure 21 Power-up Transient of LAN3502 Post-annealing

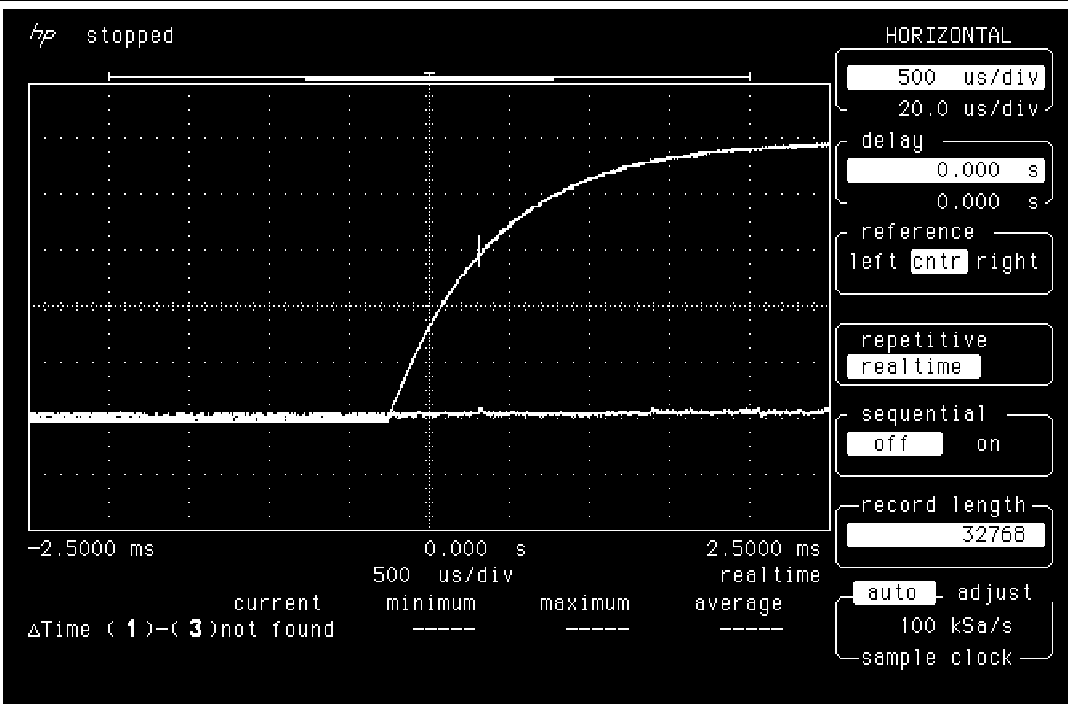

Figure 22 Power-up Transient of LAN3503 Pre-irradiation

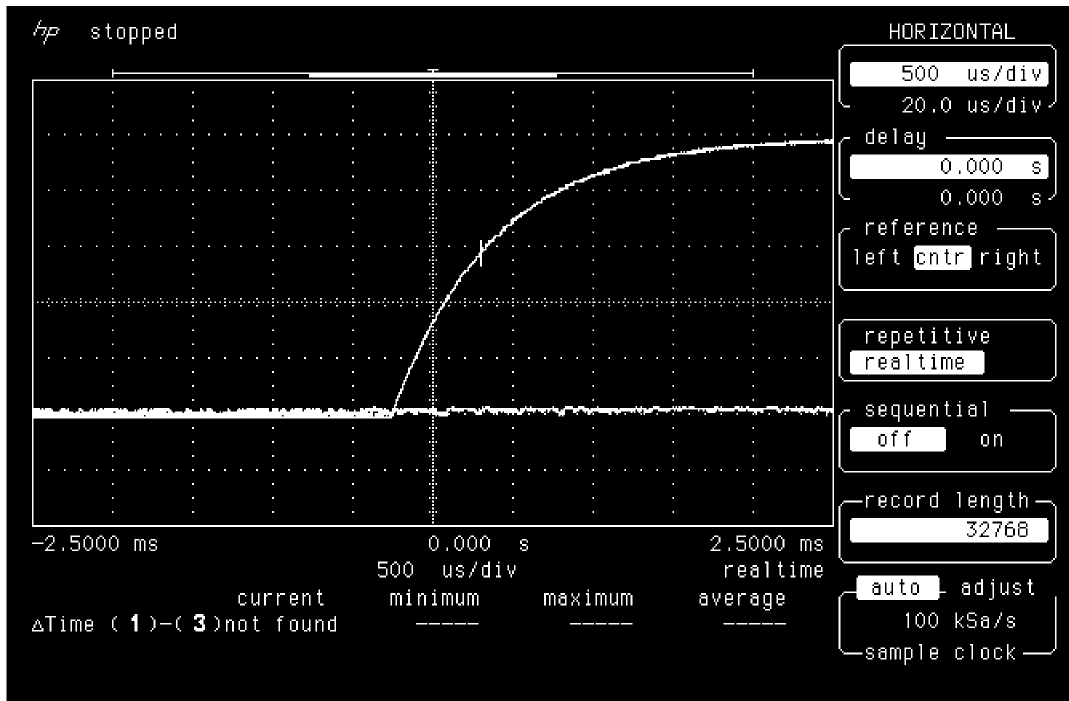

Figure 23 Power-up Transient of LAN3503 Post-annealing

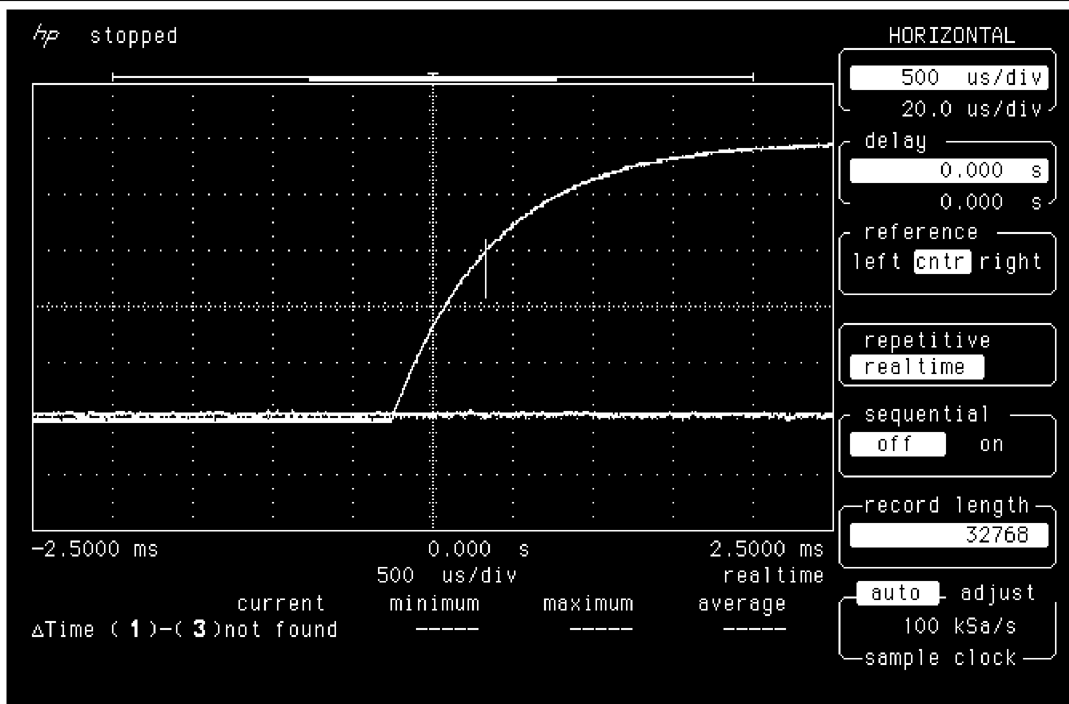

Figure 24 Power-up Transient of LAN3504 Pre-irradiation

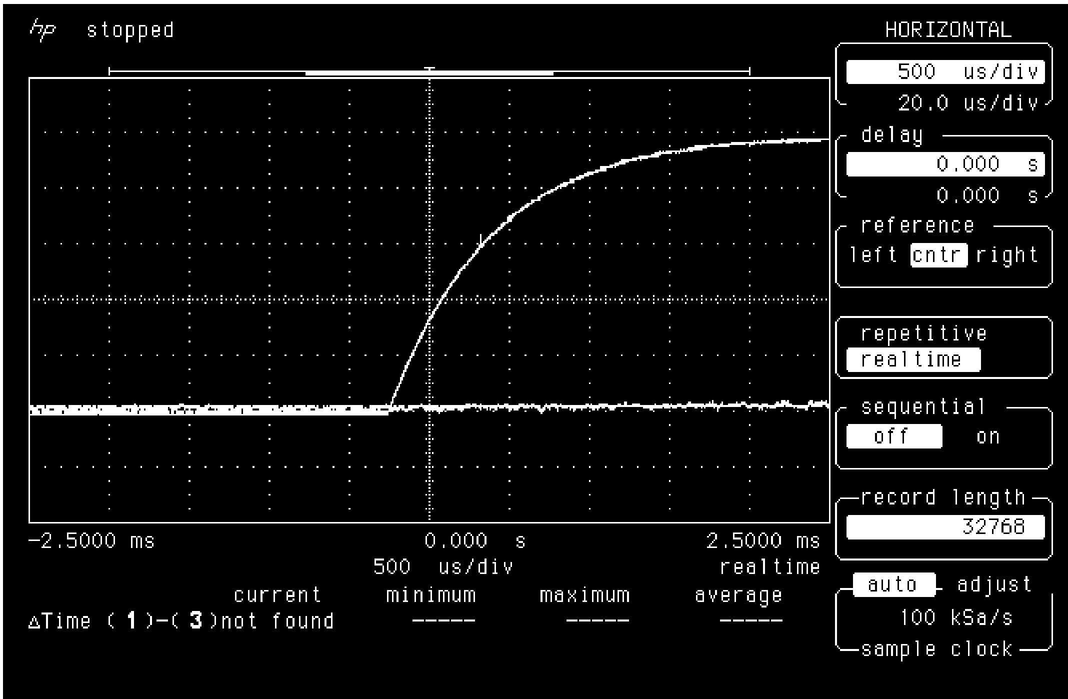

Figure 25 Power-up Transient of LAN3504 Post-annealing

IV. List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 1 (February 2016)	Non-technical updates.	N/A
Revision 0 (October 2000)	Initial release.	N/A

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