Libero SoC v11.7 Release Notes

Libero® System-on-Chip (SoC) is comprehensive and powerful FPGA design and development software available from Microsemi, providing start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such EDA powerhouses as Synplify Pro® and Model*Sim*®.

Libero SoC v11.7 is the premier production release for the new RTG4 Radiation Tolerant 65nm process silicon family.

Libero SoC v11.7 contains critical timing data updates for SmartFusion2 and IGLOO2 families. We highly recommend that customers with SmartFusion2 and IGLOO2 designs created with Libero SoC v11.5 SP3 or earlier open their design in Libero SoC v11.7, update cores as necessary, and rerun the Verify Timing step.

Use Libero SoC v11.7 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3, and Fusion FPGA families.

To access Datasheets and Silicon User Guides, visit www.microsemi.com, select your Product, then click the Documents tab. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the Design Resources tab.

Refer to the Online Help in Libero SoC for details about new software features and enhancements.

Contents

What's New in Libero SoC v11.7

Silicon Feature Support

RTG4 Multiple Asynchronous Resets

RTG4 production devices now support multiple asynchronous resets in the same design. This is an architecture enhancement over the chipwide single asynchronous reset that was available in the RTG4 Engineering Sample devices. Libero SoC v11.7 enables you to create designs and generate programming files for RT4G150 production designs containing multiple asynchronous resets.

RTG4 Improved Timing Data

Libero SoC v11.7 introduces enhancements to RTG4 timing data. Data state still remains "Advanced"; however, the quality and accuracy of the RTG4 timing models has been improved over previous releases.

RTG4150 Programming and Debug Support

Libero SoC v11.7 enables Programming and Debug support for the RTG4150 production device. SmartDebug support for SERDES is also available in this release.

RTG4150 Power Enhancements

In Libero SoC v11.7, SmartPower now supports the RTG4 uPROM. In addition, starting with Libero SoC v11.7, unused FDDR and SERDES blocks are “tied off” in a low power state. Libero SoC v11.7 also enhances the accuracy of the static power estimation in SmartPower.

RTG4 Tie-off of Unused FDDR Blocks

If FDDR is not used, the Libero SoC v11.7 software will tie off the unused FDDR blocks by adding CFG0 instances and nets to the user netlist. The following restrictions apply:

- AL2, AE1, AE41, and AL40 pins cannot be used with DDR_OUT. Registers cannot be combined on the output and enable pins.
- Tie-off will always be done if the FFDR block is not used, and compile or layout will fail if you try to use these pins with these features.

Software Enhancements

Unless otherwise noted, Software Enhancements apply to all SmartFusion2, IGLOO2, and RTG4 Devices.

Enhanced Constraint Flow

Libero SoC v11.7 introduces an enhanced constraint flow that simplifies the management of all constraints for your design.

I/O, timing, floorplanning, and netlist optimization constraints can be created, imported, edited, checked, and organized in a single view. Timing constraints need only be entered once, and can be automatically applied to Synplify synthesis, Timing-Driven Place and Route and Timing Verification. Constraint checkers are available to validate constraints before each of the above three design flow steps.

Timing constraints for known hardware blocks and IPs (CCC, Oscillator, MSS/HPMS, FDDR, SERDES, CoreConfigP, and CoreResetP), can also be derived automatically. Constraints for these blocks are derived based on the selected block configuration, and can easily be applied to Synthesis, Place and Route, or Timing Verification.

The Enhanced Constraint Flow is available as an option for new projects created with Libero SoC v11.7.

Chip Planner

Libero SoC v11.7 introduces a full overhaul of the Chip Planner floorplanning tool. Chip Planner now provides a more responsive user interface, with a contemporary look and feel. Significant runtime enhancements compared to earlier versions of the same tool provide a smoother user experience on large, high-utilization designs. Navigate through your design with ease using the revamped design hierarchy browser, with advanced search and filtering support. Chip Planner also introduces usability enhancements, with easy access to design and resource properties, and a highly customizable display interface for enhanced productivity. Cross-probing from SmartTime to Chip Planner is also supported in Libero SoC v11.7

SmartDebug

SmartDebug in Libero SoC v11.7 introduces a redesigned Debug FPGA Array probe management User Interface. A new netlist hierarchy browser helps you navigate through your design to manage Live Probes, Active Probes, and Probe Insertion. Active Probes can be also organized using the new Probe Grouping feature. New for v11.7 are Device Status Report, eNVM Page Status enhancements for SmartFusion2 and IGLOO2 devices, and SERDES Debug enhancements for SmartFusion2, IGLOO2, and RTG4 devices. Also included in this release are run time improvements.

Starting in v11.7, SmartDebug can be run in as a standalone tool for SmartFusion2, IGLOO2, and RTG4 devices. SmartDebug in standalone mode is launched outside of the Libero Design Flow. It is intended to

be used in debug environments – lab setups, for example – where the full Libero SoC tools suite may not be installed. The SmartDebug standalone tool can be installed using the new Program and Debug Tools installer, which also contains FlashPRO, FlashPRO Express, and Job Manager.

Microsemi's Secure Production Programming Solution (SPPS)

SPPS enables you to prevent overbuilding of your Microsemi FPGA's, using Thales e-Security FIPS140-2 level 3 certified hardware security modules (HSMs), custom firmware, and the state-of-the-art security protocols built into every Microsemi SmartFusion2 SoC FPGA and IGLOO2 FPGA. See the SPPS User Guide for details.

M2S010 (FG484) and M2S050 (FG896) – Simultaneous Switching Noise (SSN) Analysis

New in Libero SoC v11.7 is the Simultaneous Switching Noise Analyzer tool. The SSN Analyzer helps achieve the desired voltage noise margin for I/Os. It analyzes various parameters (for example, switching frequency of neighboring I/Os, I/O drive strength, etc.) and estimates the noise margin available for each I/O in a design.

SmartFusion2: Enhanced SoftConsole 4.0 Integration

You can now use Libero SoC v11.7 to export System Configuration files compatible with SoftConsole 4.0. Unlike earlier releases, no manual editing of these files is required.

Synplify Pro Enhancements

Synplify Pro J2015-03MSP1-2, packaged with Libero SoC v11.7, includes general enhancements to improve Quality of Results (QoR).

For RTG4 devices, Synplify Pro is now able to infer LSRAMs and URAMs with ECC mode enabled.

Place and Route Tool Enhancements

CCC Input Pin Swapping

Enhancements have been made to how hardwired CCC clock pad input pins can be routed, resulting in a quadrupling of the available solution space for placing global nets. This enhancement can result in increased routability for designs with multiple CCCs using hardwired clock input pads.

Changes to Timing Optimization

In previous versions of Libero SoC, the Layout tools considered all clocks to be asynchronous to one another for purposes of optimization. Timing paths with different launch and latch clocks were never explicitly optimized unless a "max_delay" constraint was employed.

In Libero SoC v11.7, this same behavior is preserved for: (1) pre-existing projects, and (2) new projects created in Libero SoC v11.7 with the "Classic Constraint Flow" option. However, for new projects created with the "Enhanced Constraint Flow" option, the Layout tools will treat all clocks as if they are synchronous to one another. That is, they will optimize all inter-clock paths unless explicitly prohibited.

There are several reasons for introducing this change:

1. More designs use multiple clock domains -- including phase-shifted outputs from CCCs -- and inter-clock timing optimization is a necessary technique for closing timing.
2. Across the industry, most CAD tools assume that clocks are synchronous to one another unless otherwise specified.
3. The "Clock group" constraint, which is introduced in Libero SoC v11.7, can be used to quickly and easily specify asynchronous relationships between clocks. (The "False Path" constraints can also be used.)

Users of the "Enhanced Constraint Flow" will need to pay careful attention to the timing constraints in the "TDPR Scenario". The Layout tools will optimize all launch and latch clocks unless otherwise prohibited.

It is important to note that inter-clock paths often have stricter required times than their base clock domains. This can render the inter-clock paths more timing-critical. The Layout tools will optimize every path in the "TDPR Scenario" set of timing constraints. The most critical of these paths will receive the

greatest "attention" during optimization, possibly to the detriment of other paths. Designers need to carefully evaluate all paths in the "TDPR Scenario" to prevent unnecessary inter-clock timing paths from dominating the optimization. For example, if there are two clock domains in your design, one at 125 MHz and the other at 100 MHz, all paths from the 125 MHz clock domain into the 100 MHz clock domain will be timed at 2 ns. Because this is a tight timing constraint, you must add an exception if the paths are actually false.

Clocks can be marked as asynchronous to one another in several different ways:

1. "Clock group" constraints can be used to mark asynchronous clocks.
2. "False path" constraints can also be used, but they are less efficient than "Clock group" constraints.
3. After the first successful Layout, the SmartTime GUI can be opened, the "Inter-clock analysis" option can be de-selected from within the GUI, the changes Saved, and the Layout re-run, and both Inter-clock optimization and analysis will be disabled.

Timing Verification Enhancements

Four-Corner Timing Analysis:

Libero SoC v11.7 introduces Four-Corner Timing Analysis, which increases the completeness of your timing analysis by generating reports across multiple scenarios of operating conditions. The Verify Timing step can now generate the following four types of timing and violation reports:

- Slow MAX: high temperature, low voltage, slow process, max delay timing and violation reports
- Fast MAX: low temperature, high voltage, fast process, max delay timing and violation reports
- Slow MIN: high temperature, low voltage, slow process, min delay timing and violation reports
- Fast MIN: low temperature, high voltage, fast process, min delay timing and violation reports

Note that enabling multiple types of timing and violation reports may highlight latent issues in your design, necessitating additional steps to achieve timing closure. You can filter the types of reports generated using the Verify Timing options dialog.

Clock Groups: Libero SoC v11.7 introduces clock groups, an SDC command to specify related and unrelated clocks. Typically, clocks from the same source (e.g. Oscillator, CCC) must be in the same group. Design paths crossing between clocks in the same group are analyzed by SmartTime. Note that the clock groups command is only valid for SDC files managed as part of the Enhanced Constraint Flow.

Libero Project Manager Enhancements

HDL folder Import: With Libero SoC v11.7, you can now import and link entire HDL folders into your project. Once part of your project, Project Manager audits and manages HDL files in the HDL folders, just as if you had imported the files individually.

Hierarchical Resource Report: Libero SoC v11.7 includes a Hierarchical Resource Usage Report. This report can be found in the Reports Window after the Compile step is run, and enables you to analyze the resource usage of different blocks in your design hierarchy.

SgCore Enhancements

The following SgCores have been updated for Libero SoC v11.7:

Core	Device/Family	Libero SoC v11.7-compatible version	Changes
Chip Oscillator	SmartFusion2/IGLOO2	2.0.101	Modified to support Enhanced Constraint Flow.
High Speed Serial Interface	SmartFusion2/IGLOO2	1.2.210	SAR53964 (see Resolved Issues) Added Signal Integrity changes.

High Speed Serial Interface 2	M2S/M2GL090T/TS	1.2.212	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
High Speed Serial Interface 3	M2S/M2GL090T/TS	1.2.211	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
Clock Conditioning Circuitry	RTG4	1.1.208	PLL Lock Window Default setting changed from 3000 to 6000 ppm
Two-Port RAM	RTG4	1.1.105	Changed handling of ECC flags. Prior to this update, seperate sets of ports for ECC flags were exposed. With this update, only one set is exposed for both Port A and Port B.
Microcontroller Subsystem	SmartFusion A2F200/500	2.5.200	Enhanced system boot operation.
High Speed Serial Interface (EPCS, and XAUI)	RTG4	1.1.220	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
High Speed Serial Interface (PCIe, EPCS, and XAUI)	RTG4	1.1.220	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
High Speed Serial Interface (EPCS, and XAUI), with Initialization	RTG4	1.0.110	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
High Speed Serial Interface (PCIe, EPCS, and XAUI), with Initialization	RTG4	1.0.110	SAR53964 (see Resolved Issues) Added Signal Integrity changes.
Generic DDR Memory Simulation Model	SmartFusion2/IGLOO2/ RTG4	1.0.102	Fixed issue with VCS VHDL Simulations.

Signal Integrity Changes in High Speed Serial Interface Configurators

You can select “Receive CTL Equalization” from one of the “Pre-Defined” settings in the GUI. For each Pre-Defined setting selected, the ‘Low Frequency Amplitude’ and the ‘Cut-Off Frequency’ are fixed and shown in the GUI. The corresponding registers are programmed with appropriate values by software.

Runtime Improvements

Libero SoC v11.7 includes runtime improvements to Power report generation. In addition, the Project Manager has been enhanced from a runtime perspective; Design Hierarchy construction is significantly faster, and other menu interactions have also been sped up.

Resolved Issues

Issues Resolved in Libero v11.7

SAR53964: SERDES EPCS: Proper port width calculation

In earlier releases, SERDES EPCS ports of widths less than 20 needed to be manually tied off. Libero SoC addresses this issue, always exposing the correct number of ports to the top level.

SAR69162: VERIFY_DIGEST always fails in master file/job when external digest check is restricted

This issue has been resolved in Libero SoC v11.7; the VERIFY_DIGEST action now succeeds in the case where the external digested check is restricted.

Customer Reported SARs Resolved in Libero v11.7

Customer Case Number	Description
	RTG4: "The placer was unable to find a solution which satisfied architectural placement of global nets."
	Unable to change PMA settings directly from GUI
	Add BER(bit-error rate) status to SERDES SmartDebug GUI
493642-2016646691	CCC PREADY signal shows high-z causing APB transaction to hang
493642-2010248422	RTG4 CCC generated RTL is not showing the correct width of INIT STRING
493642-1893623058,493642-1895523156	Missing Min-period timing arcs in the simulation model of UFROM and UFROMH
493642-1963000720	Error occurred while generating Programming file after Layout completed
	Design with Routing Region constraints after successful "Place and Route" step fails in "Generate Biststream" with open nets.
493642-1829929008	Logic cone does not retain logic added to a net
493642-1972801421	Confusing Error message (SF2 programming failure)
493642-1827819781	SVF export with customize TCK - FlashPro only
	SPPS: Allow user to overwrite security policy in Job Manager
493642-1966630751	To open Synplify in Linux, setenv LM_LICENSE_FILE should be port@hostname
493642-1917238998	eNVM AHB access is cycle inaccurate
493642-1958954082	CORE AXI simulation fails after 200000(dec) read transactions with message # MONAXI1: ERROR Non mat
493642-1941178061	eNVM hard-coded paths don't retain the relative path to the .hex files
493642-1926640908	Libero won't invalidate the bitstream even eNVM mem content updated
	Libero 11.6 crashes with design. Duplicate modules get generated on second run.
493642-1982329807	Libero 11.6 crashes when generating Smart Design Component from design hierarchy
493642-1968324433, 493642-1964389284	Libero 11.6 prints warning messages on terminal from HDL design but there is no warning on Libero GUI
493642-1885746150	In Linux, Libero regenerates the IP RTL files even if the configuration is not changed
493642-1898026386, 493642-1973446060	Libero loses track of RTL updates when using HDL+ if Libero was closed
493642-1808806782 , 493642-1821688701, 493642-1772302804, 493642-1818096627, 493642-1865263914, 493642-2027106509	smarttime.exe/Libero.exe is in Processes Tab even after Libero 11.5 is closed

493642-1722648844	"check hdl file" errors out on the wrong file
493642-1404235599,493642-1946519426	Importing FDC file option in Libero project is not available
	Introduce RTG4 and G4M MDDR/FDDR register read/write commands (TCL only)
	Implement G4M SERDES read/write TCL commands
	Probe point selection GUI and TCL should support wild card search.
	11.6 Alpha: Issue with upgrading core version of a DirectCore instantiated to multiple SD components
493642-2010248422	RTG4 CCC generated RTL is not showing the correct width of INIT
	Relative paths in script for SF2 CFG file script to update the ENVM
	Design with ROM construct crashes in SynplifyPro
493642-1595471765	Synplify doesn't Infer multiply and accumulate when enable is used for input and output registers
	ODT setting in FDDR/MDDR configurator in Libero is incorrect for LPDDR interface when migrating from previous release to 11.6
493642-1964879861	SmartTime is not calculating the clock generation correctly
	Need cross-probing between SmartTime and Chip Planner
493642-1913483321	IGLOO2 RAM false setup/hold violations in PR simulation
	G4Placer: Improve print-out in the event of illegally-placed cells
493642-1870660106	BLOCK: exporting cxz file with a different filename does not allow to import in a different project
493642-1857320475	PDB file generated from Libero is not updating the PDB file from previous run if the PDB file is opened in Flashpro.
493642-1970291559, 493642-1973073993	RTG4 Placer error message need to be improved
493642-1772077521	FlashPro Software Creates not standard STAPL function INT (hex number) when exporting
493642-1930722571	ProASIC3: Export BSDL option is not listed in the Design Flow window
	SPPS: Enforce the overbuild protection by making a tcl parameter as required
493642-1771657311	The data storage client of the eNVM is not accepting relative paths.
	Compile error from customer design. Message needs update
493642-1987117613	Need to display the proper ThetaJA values in the smartpower for the Smartfusion2 TQ144 package
	From within Libero, allow choosing different programmer if more than one programmer is connected
493642-1977246176	Check HDL error message points to wrong file
493642-1953826240	Enhancement: shortcut keyword for Libero complete run.
493642-1887808755	SDC checking should happen before compilation
493642-1849382710	Export option in constraint editor
493642-1709713206, 493642-1782280067	FIRMWARE_EXPORT: SC: A Java Runtime Environment (JRE) or Java Development Kit (JDK) must be available in order to run Eclipse
	Give user the option of using multiple IO Constraints pdc at the same time

493642-1435744139	Libero Enhancement-Treemap format to track memory usage through the design Hierarchy
493642-1558734186	Enhance View device Status report content
493642-1662897931,493642-1692283632, 493642-1722796823	SYSRESET macro is missing the timing models
493642-1637762925	syn_ramstyle attribute declaration issue
493642-1874702581	set_clock_groups command not supported in Libero
	Top bar should show directory path
493642-2039633013	eNVM-only programming requires 11.7 generated bitstream

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** and the installation will complete successfully.

Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider if you need assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. We are aware of issues when using Symantec, McAfee, Avira, Sophos and Avast tools. The combination of operating system, antivirus tool version and security settings all contribute to the end result. Depending on your environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

RTG4

Custom Flow with uPROM: uPROM content must be a single line file

If you are using custom flow and are importing uPROM content using the import_component_data command, the uPROM memory file must not have any newlines.

SET Mitigation ON may result in Hold Violations

Turning ON SET Mitigation may result in Hold time violations in some cases. Enable Min Delay Repair in Place and Route Options to have the Place and Route tool mitigate these, and other Hold time violations.

Enhanced Constraint Flow

Tool/Flow Limitations

The following tools and flows are not supported in the Enhanced Constraint Flow in Libero SoC v11.7:

- Precision Synthesis
- IO Advisor

- Netlist Viewer
- Block Flow
- Design Separation Flow using MSVT
- Secure IP (IEEE 1735) Flow

Explicit and potential clocks cannot be found for Enhanced Constraint Flow designs started from EDIF

If you are using the Enhanced Constraint Flow, and you are not running Synthesis (i.e., you import an EDIF netlist), the Constraints Editor is not able to find the names of explicit and potential clocks in your design.

Multiple-line False Path Constraints are not taken into account by Timing Verification

With false path constraints of the type

```
set_false_path -ignore_errors -through [ get_nets {
test_sb_0/CORERESETP_0/*sdif*_phr/hot_reset_n
test_sb_0/CORERESETP_0/*sdif*_phr/sdif_core_reset_n_0 } ]
```

the second false path may be ignored by the Place and Route and Timing Verification tools. To work around the issue, split up the get_nets directive in separate false path constraints:

```
set_false_path -ignore_errors -through [ get_nets {
test_sb_0/CORERESETP_0/*sdif*_phr/hot_reset_n ]
set_false_path -ignore_errors -through [ get_nets {
test_sb_0/CORERESETP_0/*sdif*_phr/sdif_core_reset_n_0 } ]
```

Derived Constraints Limitations

The Derived Constraints Feature of the Enhanced Constraint Flow has the following known limitations. If your design is impacted by these limitations, you will need to review and manually add the appropriate constraints:

XAUI mode: Clock constraints are not generated on clocks XAUI_TX_CLK_OUT and XAUI_RX_CLK_OUT

CoreRSDEC: If your design contains a CoreRSDEC IP, Derive Constraints will throw an error of the format:

```
RSDEC_KITDELAY_RAM.vhd(54): ERROR: expression has 8 elements ;
formal wd expects 9 (VHDL-1549)
```

The above error message is benign and can be ignored.

CoreConfigP

In some isolated test cases, you may see max delay violations in paths containing the CoreConfigP. You must correct these violations, either by floorplanning, or by running multi seed layout.

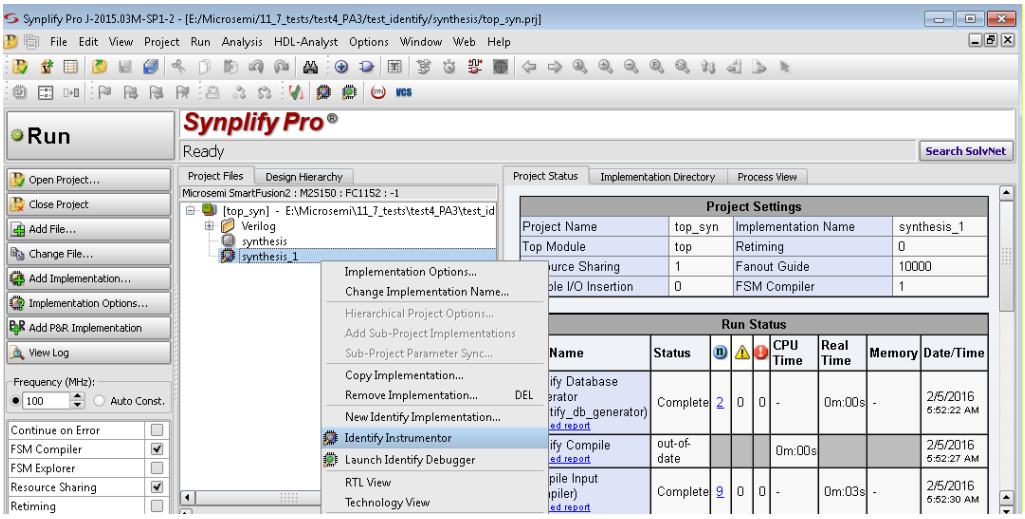
Identify and Synphony-generated constraints files cause errors

If you want to use constraints files generated by Identify or Synphony or SynplifyPro for Identify Implementation in the Enhanced Constraint Flow, you must do the following:

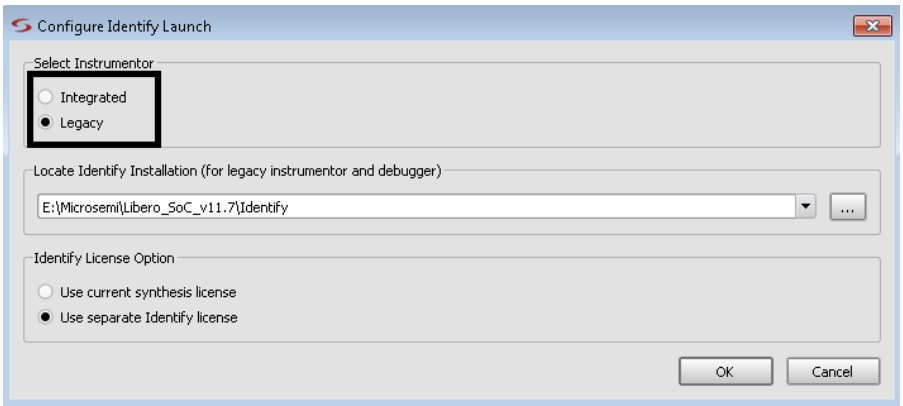
- Collect any timing constraints present in the SDC file generated by Synphony and translate these constraints to the standard SDC format into a new SDC file.
- Collect any netlist attributes present in the SDC file generated by Synphony and copy them into a new FDC file.
- Import the new SDC and FDC files into your Libero SoC project using the Manage Constraints User Interface, and associate these files with the Synthesis step before running Synthesis.

Limitations on Identify Instrumentor Modes

You must invoke Identify Instrumentor from Synplify Pro in “Legacy Mode” to ensure seamless integration between Libero, Synplify Pro, and Identify. Doing this will ensure that the Identify Implementation is located in the correct directory. Right-click the synthesis implementation which you want to instrument and click “Identify Instrumentor” (see screenshot below). Do not click “New Identify Implementation”.



If you have used Identify in Integrated mode on your machine, you may need to readjust the Identify Launch option. Open the “Configure Identify Launch” dialog; in the Synplify Pro main window, click “Options”, then click “Configure Identify Launch”. Ensure that the “Legacy” radio button is selected, then click “OK” to exit the dialog.



Synthesis

Libero does not directly support SystemVerilog in v11.7.

Workaround: Invoke SynplifyPro in standalone mode, import all HDL files, and run synthesis. The output of SynplifyPro (*.edn or *.vm) can then be incorporated into the Libero project.

Programming

Generate Bitstream crashes in Libero flow for designs in chain mode

For Libero projects which involve a chain of SmartFusion2/IGLOO2/RTG4 and older Flash devices (SmartFusion, IGLOO, ProASIC3, and Fusion) in which the older Flash device is added using PDB, the following tools will not work in Libero:

Generate Bitstream
Export Bitstream
Export FlashPro Express Job

Workaround: Use STAPL instead of PDB when adding an older Flash device to a SmartFusion2/IGLOO2/RTG4 chain.

Generate Bitstream fails when serialization memory file is copied to project directory

For SmartFusion2 and IGLOO2 devices, in the eNVM configurator, do not select the "Copy Memory File to Project Path" option on a serialization client's memory file. If you do so, bitstream generation will fail in Libero SoC v11.7.

Generate Bitstream fails with "Contents filled with 0s" option

For RTG4 devices, in the uPROM configurator, if the "Contents filled with 0s" option is selected, bitstream generation will fail. As a workaround, use a .mem file, filled with '0''s.

Job file (.job) created is missing the programming bitstream

When creating a new programming job for the IHP job type, the job file (.job) created is missing the programming bitstream. This issue will be resolved in 11.7 SP1.

Programming – Programming Recovery Not Working After Programming Interruption

Exporting a SPI bitstream with Programming Recovery enabled with another programming file type (STAPL, DAT) will erase and reprogram the Programming Recovery setting. If a programming interruption occurs before the Programming Recovery setting is reprogrammed with the following programming method (Auto Update, Auto Programming, or IAP/ISP services), Programming Recovery will not occur.

Workaround: Export the SPI bitstream only without any other programming file type. This will be resolved in Libero v11.8.

Documentation

Web-based documentation

Starting with Libero SoC v11.7, most Users Guides for SmartFusion2, IGLOO2, and RTG4 will be published on the Microsemi website. Libero and Programming/Debug tools will include links to the website.

If the machine on which you have installed Libero does not have access to the Internet, you (or a site administrator) can download all Libero SoC v11.7 Users Guides from Microsemi's Libero SoC documentation site.

Linux: Firefox requirement for Online Help and Users Guides

Libero SoC v11.7 requires the "Firefox" executable to be in your PATH variable on Linux. Alternatively, you can access the Reference Manuals on the Microsemi website, or by clicking "Help -> Reference Manuals" in Libero. For the Libero SoC v11.7 release, the "Web Browser" selection in the Libero Preferences dialog is only used by Online Help and for some user guide links

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. A 64-bit OS is required for designing SmartFusion2, IGLOO2 and RTG4 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents web page.

OS Support

Supported

Windows 7, Windows 8.1

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6
SuSE 11 SP4 (Libero only; FlashPro Express, SmartDebug, and Job Manager are not supported)

** RHEL 5 and CentOS 5 do not support programming using FlashPro5.*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.7 installation:

- Synplify Pro ME J2015.03MSP1-2
- ModelSim ME 10.4c
- Identify ME J2015.03MSP1-2
- Synphony Model Compiler J2015.03M

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.7

Installation requires Admin privileges.

Windows download

Linux download

SoftConsole v3.4 SP1 should be installed over SoftConsole v3.4 for use with Libero SoC v11.7.

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.7.

Download SoftConsole 3.4 SP1

Installation Note:

After installation of Libero on Linux, any attempt to run the udev_install script for FlashPro setup will fail.

When running the script, users will see the following:

```
% ./udev_install

/bin/sh^M: bad interpreter: No such file or directory
```

Problem:

The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, as such, is not a valid shell script.

Workaround:

Users must run dos2unix on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
% ./udev_install
```

If dos2unix is not available, users might need to run the following command, and then run dos2unix:

```
% sudo yum install dos2unix
```

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; Enterprise Storage and Communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 4,800 employees globally. Learn more at **www.microsemi.com.**