Libero SoC v11.6 SP1 Release Notes

Libero® System-on-Chip (SoC) is comprehensive and powerful FPGA design and development software available from Microsemi, providing start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such EDA powerhouses as Synplify Pro® and Model*Sim*®.

Libero SoC v11.6 SP1 introduces support for the Tgrade1 and Tgrade2 Automotive operating ranges for the IGLOO2 and SmartFusion2 device families. Libero SoC v11.6 SP1 also introduces silicon-characterized Timing and Power data for the M2S/M2GL 060 devices.

Libero SoC v11.6 SP1 adds the capability to generate reports that detail register configuration data for some components (INIT String Reports).

Use Libero SoC v11.6 SP1 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3, and Fusion FPGA families.

To access Datasheets and Silicon User Guides, visit www.microsemi.com, select your Product, then click the Documents tab. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the Design Resources tab.

Refer to the Online Help in Libero SoC for details about new software features and enhancements.

Contents

What's New in Libero SoC v11.6 SP1

SmartFusion2 and IGLOO2: New Device Operating Condition Support

Libero SoC v11.6 SP1 adds support for the Automotive Tgrade1 and Tgrade 2 operating conditions. The following tables provide details about device and package support.

SmartFusion2

Die	Packages	Speed Grade	Temp Ranges	Free Libero Gold
M2S005S	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	Yes
M2S010TS	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	Yes
M2S025TS	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	No
M2S060TS	400 VF, 484 FBGA, 676 FBGA	-1	Tgrade2	No
M2S090TS	484 FBGA, 676 FBGA	-1	Tgrade2	No

Table 1: New SmartFusion2 device operating condition support in Libero SoC v11.6 SP1

IGLOO2

Die	Packages	Speed Grade	Temp Ranges	Free Libero Gold
M2GL005S	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	Yes
M2GL010TS	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	Yes
M2GL025TS	256 VF, 400 VF, 484 FBGA	-1	Tgrade2	No
M2GL060TS	400 VF, 484 FBGA, 676 FBGA	-1	Tgrade2	No
M2GL090TS	484 FBGA, 676 FBGA	-1	Tgrade2	No
M2GL005	484 FBGA	-1	Tgrade1	Yes
M2GL010	484 FBGA	-1	Tgrade1	Yes
M2GL025	484 FBGA	-1	Tgrade1	Yes
M2GL060	484 FBGA	-1	Tgrade1	Yes
M2GL090	484 FBGA	-1	Tgrade1	Yes

Table 2: New IGLOO2 device operating condition support in Libero SoC v11.6 SP1

SmartFusion2 and IGLOO2 – Production Data

Production (post-silicon) Timing and Power analysis is available for M2S060/M2GL060 devices.

SmartFusion2	IGLOO2	Timing	Power
M2S005	M2GL005	Production	Production
M2S010	M2GL010	Production	Production
M2S025	M2GL010	Production	Production
M2S050	M2GL050	Production	Production
M2S060	M2GL060	Production	Production
M2S090	M2GL090	Production	Production
M2S150	M2GL150	Production	Production

Table 3: Summary of Timing and Power Data Status for SmartFusion2 and IGLOO2 devices

MSS SPI0 enhancement to support Auto Update while sharing SPI0 pin with Fabric Controller

When Auto-update is enabled, the SmartFusion2 MSS SPI0 can now be configured to share the SPI0 pin with a SPI Controller implemented in the FPGA Fabric. To share the SPI0 port, you must implement a multiplexer in the FPGA fabric to switch the SPI0 pins between MSS-SPI0 and the Fabric SPI Controller.

INIT String Reports

Libero SoC v11.6 SP1 provides an enhanced usability feature that improves reporting support for the MSS, High Speed Serial Interfaces, Fabric DDR, and Fabric CCC(s). This new report is generated during bitstream generation, and provides, for each MSS, High Speed Serial Interface, Fabric DDR (FDDR), and Fabric CCC block used in the design, the final INIT string that is programmed in the device for that block. The report is available in .xml and .txt formats.

Resolved Issues

Issues Resolved in Libero SoC v11.6 SP1

69998 - Design hierarchy issue when instantiating design entities across libraries

In VHDL designs, if an entity is instantiated using the „<instance> : entity <library>.<entity name>(<architecture>)" syntax, the Libero Design Hierarchy is not fully resolved if there is not a „use <library>.all" clause defined for that library. This issue has been fixed in Libero SoC v11.6 SP1; the „use <library>.all" clause is no longer required.

72083 – High Utilization Designs no longer successfully complete Layout

Libero SoC v11.6 included Quality of Results improvements for SmartFusion2 and IGLOO2 designs. A side effect of these improvements was that certain extremely high utilization designs could no longer be successfully placed. In Libero SoC v11.6 SP1, this issue has been addressed in High-effort Place and Route. If the design is very difficult to place, a force-fit algorithm is automatically invoked. This may lead to increased layout runtime and diminished timing performance. Regular-effort Place and Route is unchanged. There is a strong possibility that reducing the size of the design, or relaxing region and floorplanning constraints will help to improve timing closure and runtime.

71639 – VHDL design fails Multipass Place and Route with error: "set_root failed"

Some VHDL projects may fail multiple pass Place and Route with the above error. This happens when the post-synthesis EDIF netlist's root module does not belong to the "work" library. This has been addressed in Libero SoC v11.6 SP1 – Multiple pass Place and Route proceeds using the currently selected project root.

71638 – Block Flow: Routed nets are dropped with Min Delay Repair

In Libero SoC v11.6, under a particular set of circumstances, Layout appears to pass but in actuality, no nets were routed. The symptom of this issue is an error message of the type "Error during net delay calculation of net <net name> .... Delay set to 0". This issue occurs in the following scenario:

1. Publish a block with routing (i.e., the block contains routing information).
2. Instantiate the block in a top-level design.
3. Run Place and Route.

   The above steps may have been performed in Libero SoC v11.5 or 11.6.

4. Subsequently, in Libero SoC v11.6, rerun Place and Route, with Repair Min Delay Violations enabled.

This issue has been fixed in Libero SoC v11.6 SP1.

Customer Reported SARs Resolved in Libero SoC v11.6 SP1

SAR #	Product	Case Number	Summary
72265	Designer	493642-1753784552	Layout is crashing during routing in 11.6

72335	Designer		Compile run time is too high
72407	Enhancement	493642-1976254548	M2S060 silicon is not matching the timing from v11.6
71441	Timing	493642-1963054036	v11.6 timing report shows incorrect data status
71602	Project_Manager	493642-1963956663	HDLPLus: Bus Interface is removed on updating the HDLPlus instance on project close and reopen
73215	Timing	493642-1998448846	SmartTime does not do reg-reg analysis even the clk constrain exists
71715	Project_Manager	493642-1971546966	HDL_VERILOG_INCLUDE: Verilog 'include' problem with Libero 11.6
71216	Designer	493642-1955483733	Block: The software freezes upon compile
73216	Timing	493642-1998448846	SmartTime does not reports all the edges for the path to serdes ref clock
73634	Project_Manager	493642-2008273623	Libero 11.6 crashes when clicked on generate component
72241	Designer	493642-1978306551	Libero 11.6 Crash during PnR which uses Repair Min Delay Violation selected
73259	Designer		Repair min-delay inserts buffer on hardwired net inside BIBUF I/O
71869	SmartGen	493642-1584599779, 493642-1586678760, 493642-1827873760	INIT string reports (INIT to register for MSS, SERDES, FDDR)
70276	Enhancement		Provide ability for customers to use Auto Update without MSS SPI
71867	Micro_Controller_Subsystem		SF2 MSS_CCC: Expose MCCC_GLMUX_SEL signal
69905	Help	493642-1931095761	Remove set and get_defvar from Online Help

Known Limitations, Issues, and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** and the installation will complete successfully.

Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider if you need assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on your environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

SmartTime

SAR74310: SmartTime is unable to report paths though registers in user sets

In user sets, SmartTime will not report any paths crossing sequential elements (through clock-to-q) unless the start point is a clock pin of a register (or other sequential element). Paths reported in other areas are not affected by this issue.

System Requirements

Refer to System Requirements on the Microsemi website for more information about operating systems support and minimum system requirements. A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents web page.

OS Support

Supported

Windows 7, Windows 8.1

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6

** RHEL 5 and CentOS 5 do not support programming using FlashPro5.*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

No third-party tools are included with the Libero SoC v11.6 SP1 release. You can continue using the third-party tools that were included with the baseline Libero SoC v11.6 release:

- Synplify Pro ME J2015.03M-3
- ModelSim ME 10.3c
- Identify ME J2015.03M-1
- Synphony Model Compiler 2015.03M

Download Libero SoC v11.6 SP1

Installation requires Admin privileges, and a pre-existing install of Libero SoC v11.6.

Download Libero SoC v11.6 SP1 for Windows

Download Libero SoC v11.6 SP1 for Linux

Libero SoC v11.6

Refer to the Libero SoC v11.6 Release Notes for information about features, bug fixes, and known issues pertaining to the Libero SoC v11.6 baseline release, and for Libero SoC v11.6 download links.

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,600 employees globally. Learn more at **www.microsemi.com**.

51300137-0/12.15