Total Ionizing Dose - 15T-RTAX250S-CQ352-D8KNM1

TR0023 Test Report

December 17, 2015

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I. Summary Table

Parameter	Tolerance
Gross Functionality	Passed 300 krad (SiO_2)
Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO_2)
Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database at *http://www.klabs.org* and *http://www.microsemi.com/soc)* accumulated from the TID testing of many generations of antifuse-based FPGAs. (For example, TID data of antifuse-based field programmable gate array (FPGA)

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation and annealing, each input or output is tied either to the ground or VCCI with a jumper.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX250S
Package	CQ352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	TOP_AX250S_TID
Die Lot Number	D8KNM1
Quantity Tested	6
Serial Number	300 krad(SiO2): 5429, 5432 200 krad(SiO2): 5481, 5492 100 krad(SiO2): 5526, 5616
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (± 5%)	7.5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

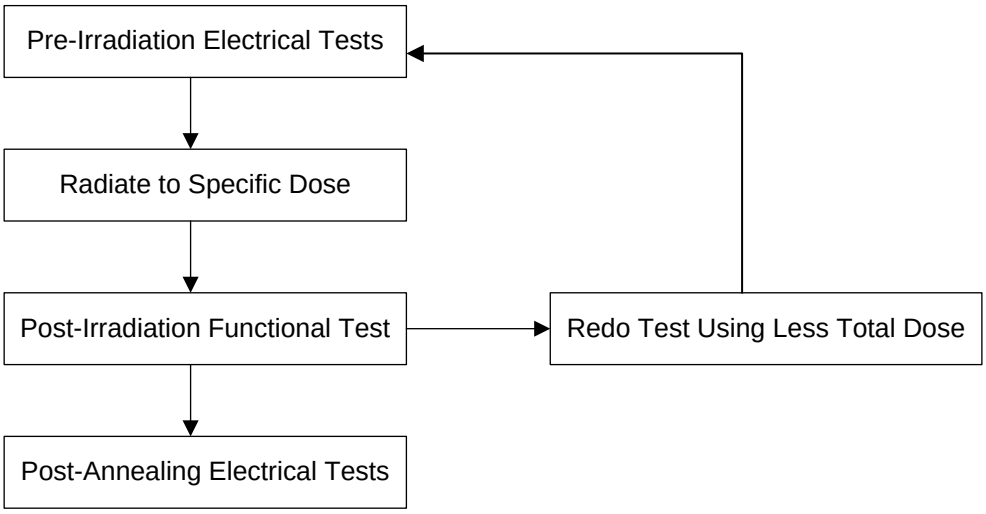

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 (Parametric test flow chart) shows the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi System-on-Chip (SoC) Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX250S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

Each DUT uses a high utilization generic design (RTAX250S_TID) to test the total dose effects in typical space applications.

Table 2 lists each electrical parameter to be measured and the corresponding logic design. The functionality is measured on the output pin (O_BS) of a combinational buffer-string with 2,300 buffers, output pins (O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA) of four (4) shift registers with 1,312 bits total, and half of the output pins (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6, and OUTX7) of the embedded RAM configured as 2048x6.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
Functionality	All key logic functions (O_BS, O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA), and outputs of embedded RAM (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6 and OUTX7)
ICC (ICCA/ICCI)	DUT power supply
Input Threshold (VIL/VIH)	Single ended inputs (EN8/YQ0, DA/QA0, IO_I_0/IO_O_0, IO_I_1/IO_O_1, IO_I_2/IO_O_2, IO_I_3/IO_O_3, IO_I_4/IO_O_4, IO_I_5/IO_O_5), and differential inputs (Din_P_0/Dout_0, Din_P_1/Dout_1, Din_P_2/Dout_2, Din_P_3/Dout_3, Din_P_4/Dout_4, Din_P_5/Dout_5, Din_P_6/Dout_6)
Output Drive (VOL/VOH)	Output buffer (DA/QA_0)
Propagation Delay	String of buffers (CLOCK to O_BS)
Transition Characteristic	D flip-flop output (O_BS)

ICC is measured at the power supply of the logic-array (ICCA) and I/O (ICCI), respectively. The input logic threshold (VIL/VIH) is measured at single-ended inputs EN8, DA, IO_I_0, IO_I_1, IO_I_2, IO_I_3, IO_I_4, and IO_I_5, and also at differential inputs Din_P_0, Din_P_1, Din_P_2, Din_P_3, Din_P_4, Din_P_5, and Din_P_6. The differential inputs are configured as LVPECL instead of LVDS. Because LVPECL uses 3.3 V DC, higher than 2.5 VDC used by LVDS, it is the worst case among the differential pairs. During the measurement at the differential inputs, the N (negative) side of the differential pair is biased at 1.8 V. The output-drive voltage (VOL/VOH) is measured at QA_0. The propagation delay is measured at the output (O_BS) of the buffer string. The definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output O_BS. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured at the output O_BS, are shown as oscilloscope snapshots.

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests. The as-irradiated DUT is functionally tested at the output (O_FF_HCLKA) of the largest shift register.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation, and post-annealing ICC. The post-annealing ICC for four different bit patterns (all 0, all 1, checkerboard, and inverted-checkerboard) in the RAM are the same.

Table 3 Pre-irradiation, Post Irradiation, and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
5429	300 krad	5	3.71	3	42	27.61	59
5432	300 krad	9	6.09	7	64	26.99	62
5481	200 krad	4	2.33	5	52	25.52	65
5492	200 krad	4	5.41	7	22	24.31	51
5526	100 krad	2	3.76	5	19	25.62	46
5616	100 krad	1	1.66	1	22	26.53	17

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA, and ICCDIFFA values in Table 2-4 of the RTAX-S/SL/DSP datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 250 mA; the PIPL of ICCI equals 20 + 10 + 3.13 x 7 = 51.91 (mA). There are 7 pairs of differential LVPECL inputs in each DUT. Based on these PIPL, each post-annealed DUT passes both the ICCA and ICCI spec for 300 krad (SiO_2).

Figure 2 through Figure 7 show the influx standby ICCA and ICCI versus total dose for each DUT.

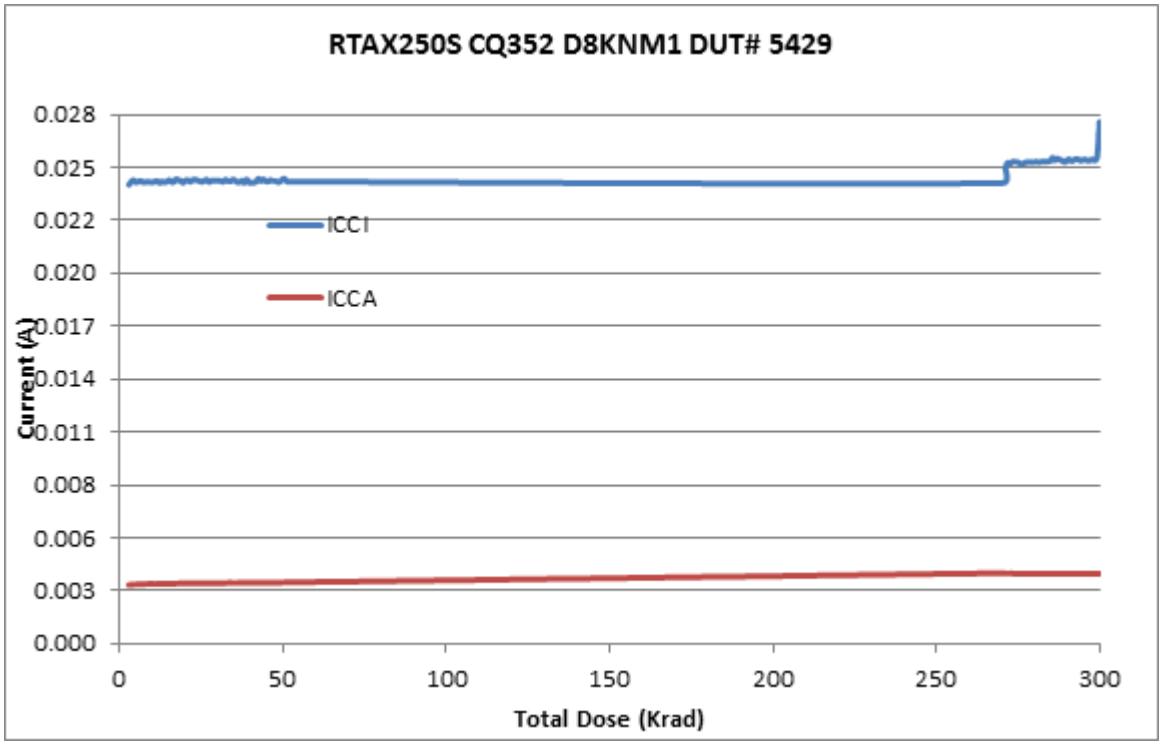

Figure 2 DUT 5429 Influx ICCI and ICCA

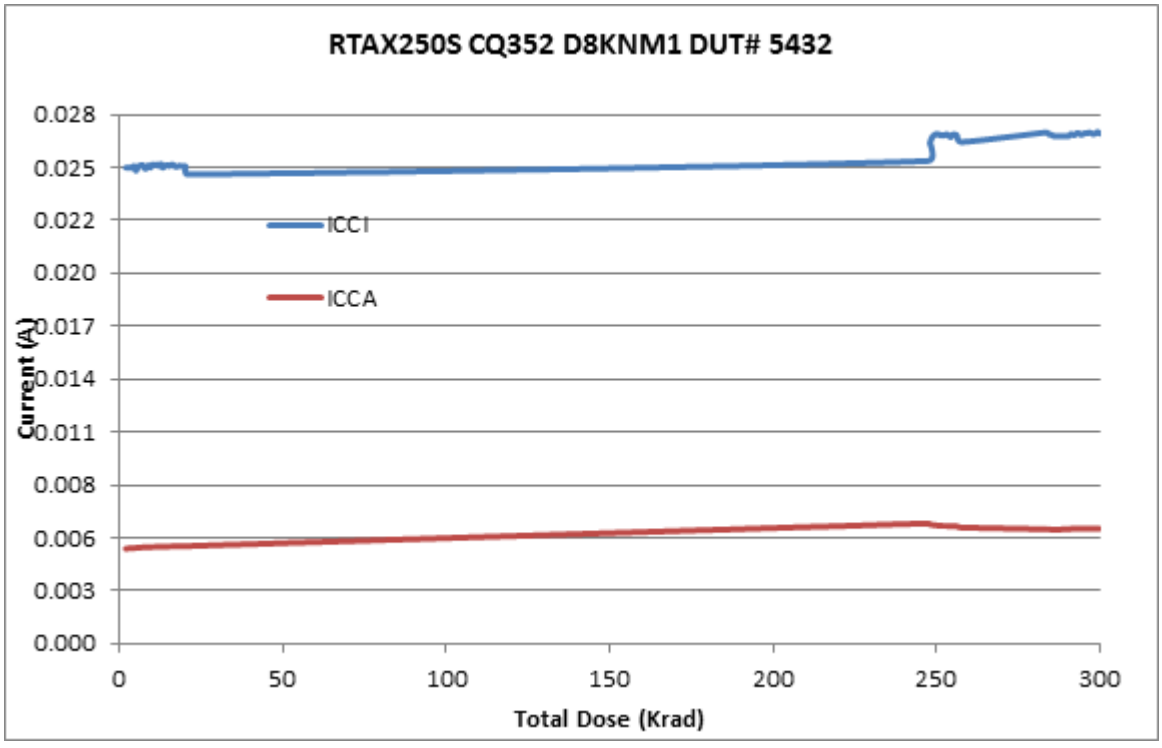

Figure 3 DUT 5432 Influx ICCI and ICCA

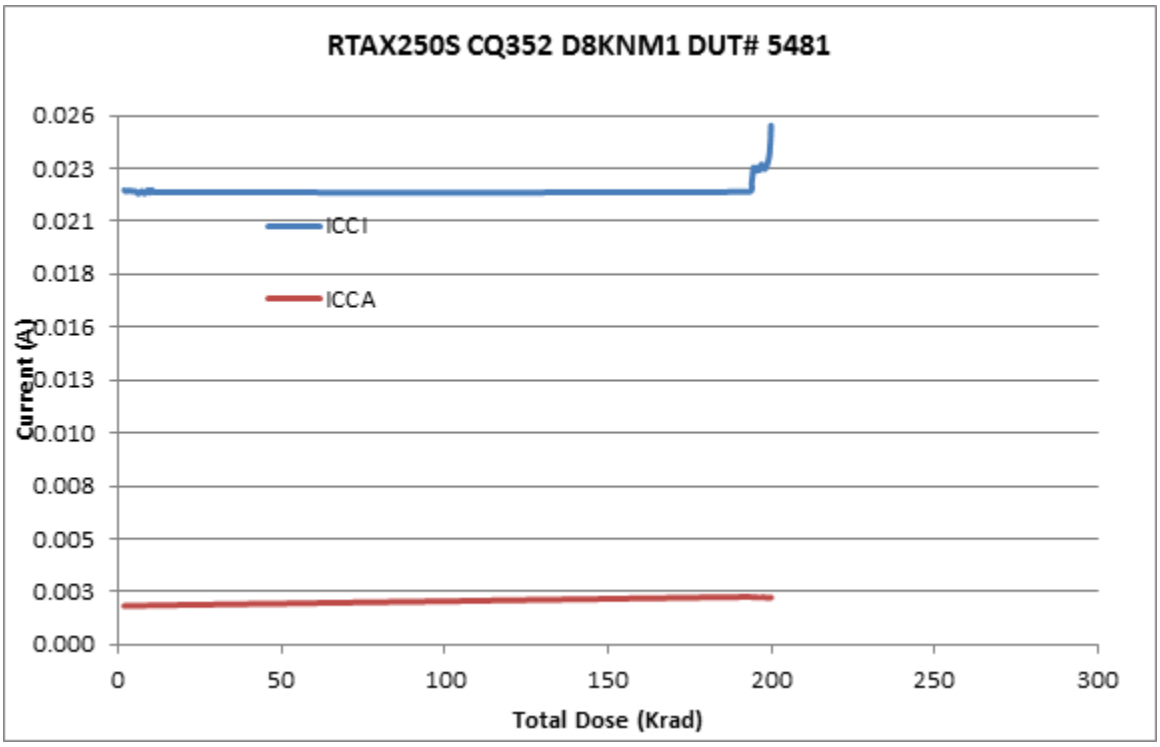

Figure 4 DUT 5481 Influx ICCI and ICCA

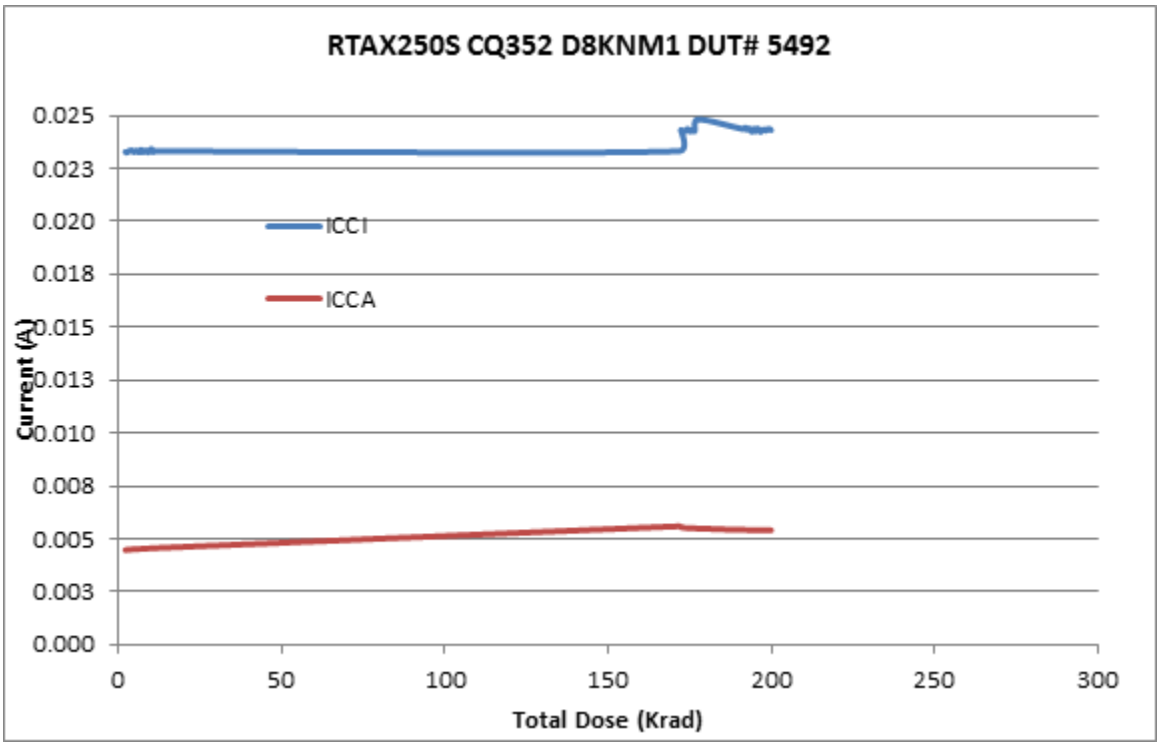

Figure 5 DUT 5492 Influx ICCI and ICCA

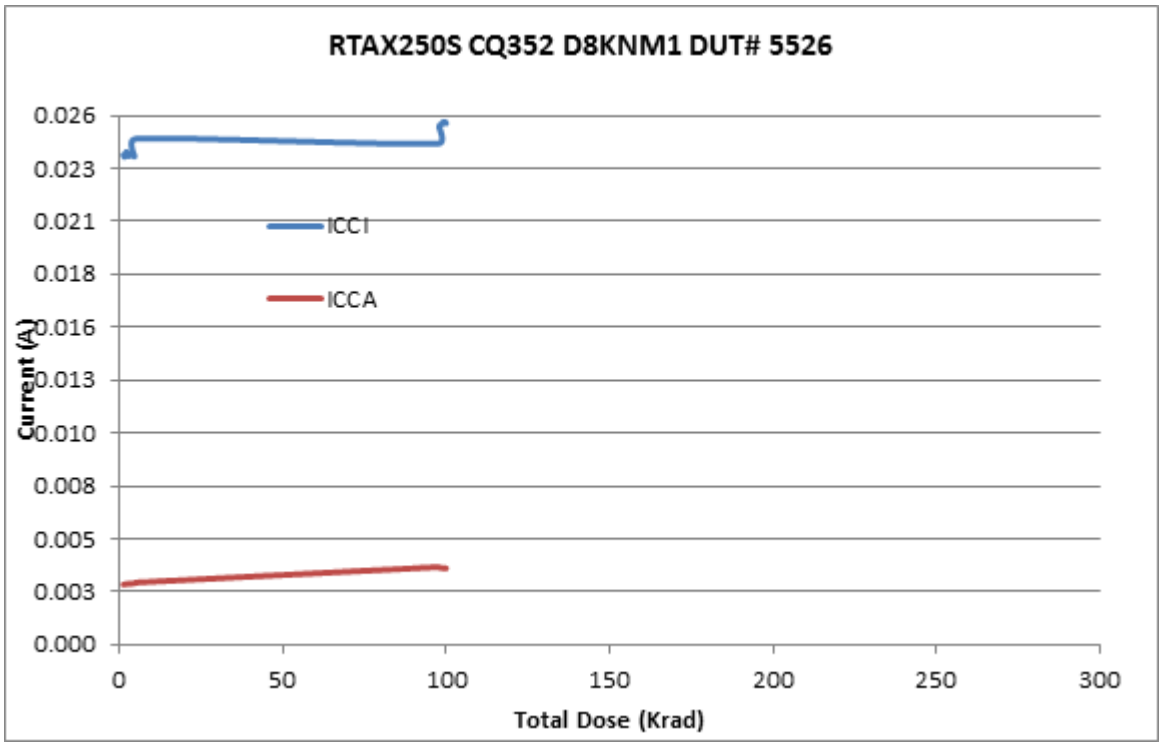

Figure 6 DUT 5526 Influx ICCI and ICCA

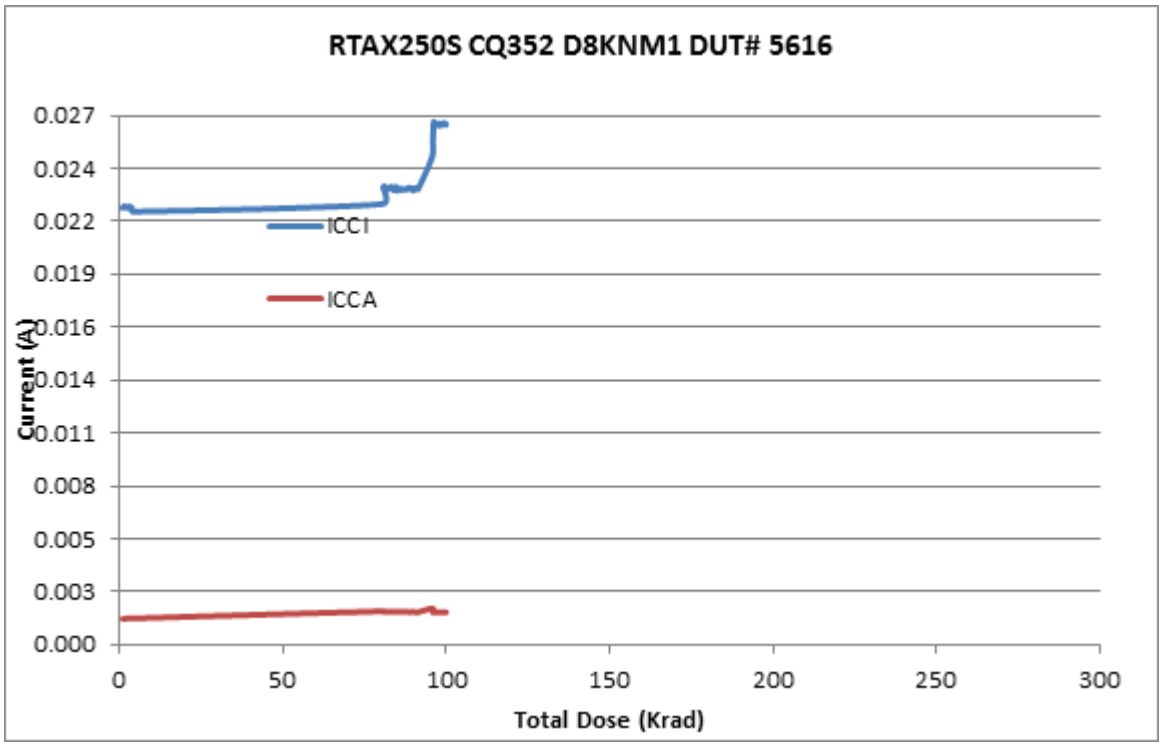

Figure 7 DUT 5616 Influx ICCI and ICCA

C. Single-Ended Input Logic Threshold (VIL/VIH)

Table 4 through Table 7 list the pre-irradiation and post-annealing single-ended input logic threshold. All data are within the specification limits, and the post-annealing shift in every case is less than 10%.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin		IO_I_0/IO_O_0				IO_I_1/IO_O_1			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.485	1.490	1.495	1.495	1.490	1.505	1.505	1.505
5432	300 krad	1.500	1.485	1.505	1.490	1.510	1.510	1.520	1.500
5481	200 krad	1.495	1.490	1.525	1.500	1.505	1.505	1.525	1.505
5492	200 krad	1.495	1.480	1.500	1.485	1.505	1.485	1.515	1.435
5526	100 krad	1.495	1.475	1.495	1.490	1.495	1.505	1.515	1.500
5616	100 krad	1.505	1.485	1.525	1.485	1.525	1.485	1.525	1.485

Table 5 Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin		IO_I_2/IO_O_2				IO_I_3/IO_O_3			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.500	1.440	1.430	1.465	1.495	1.455	1.500	1.500
5432	300 krad	1.520	1.445	1.520	1.435	1.445	1.500	1.510	1.500
5481	200 krad	1.535	1.440	1.520	1.480	1.470	1.500	1.515	1.500
5492	200 krad	1.445	1.490	1.510	1.435	1.480	1.450	1.515	1.495
5526	100 krad	1.495	1.430	1.510	1.430	1.495	1.440	1.505	1.495
5616	100 krad	1.530	1.490	1.550	1.485	1.470	1.485	1.485	1.485

Table 6 Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin		IO_I_4/IO_O_4				IO_I_5/IO_O_5			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.485	1.490	1.500	1.465	1.455	1.450	1.505	1.500
5432	300 krad	1.520	1.500	1.485	1.505	1.455	1.470	1.485	1.495
5481	200 krad	1.500	1.500	1.500	1.470	1.525	1.480	1.535	1.505
5492	200 krad	1.495	1.490	1.480	1.475	1.475	1.450	1.505	1.460
5526	100 krad	1.510	1.485	1.465	1.465	1.450	1.460	1.540	1.500
5616	100 krad	1.520	1.495	1.480	1.520	1.495	1.500	1.530	1.465

Table 7 Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin		DA/QA0				EN8/YQ0			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.490	1.505	1.500	1.515	1.470	1.490	1.510	1.520
5432	300 krad	1.510	1.505	1.520	1.515	1.490	1.490	1.530	1.520
5481	200 krad	1.510	1.495	1.520	1.515	1.495	1.480	1.530	1.520
5492	200 krad	1.500	1.505	1.510	1.515	1.480	1.490	1.515	1.520
5526	100 krad	1.500	1.500	1.510	1.510	1.480	1.485	1.520	1.515
5616	100 krad	1.510	1.465	1.520	1.515	1.490	1.455	1.530	1.545

D. Differential Input (LVPECL) Threshold Voltage (VIL/VIH)

Table 8 through Table 11 show the LVPECL differential input threshold voltage changes due to irradiations. All pins show negligible changes, and all the data are within the specification.

Table 8 Pre-Irradiation and Post-Annealing Differential Input Thresholds

In/Out Pin		Din_P_0/Dout_0				Din_P_1/Dout_1			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.775	1.770	1.805	1.805	1.785	1.785	1.785	1.785
5432	300 krad	1.775	1.775	1.800	1.810	1.785	1.790	1.780	1.780
5481	200 krad	1.770	1.785	1.810	1.805	1.785	1.785	1.780	1.780
5492	200 krad	1.780	1.775	1.820	1.805	1.795	1.790	1.790	1.785
5526	100 krad	1.765	1.780	1.755	1.810	1.785	1.785	1.785	1.780
5616	100 krad	1.770	1.785	1.810	1.780	1.790	1.790	1.790	1.785

Table 9 Pre-Irradiation and Post-Annealing Differential Input Thresholds

In/Out Pin		Din_P_2/Dout_2				Din_P_3/Dout_3			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.780	1.790	1.780	1.785	1.810	1.785	1.800	1.785
5432	300 krad	1.780	1.785	1.785	1.785	1.775	1.795	1.760	1.805
5481	200 krad	1.785	1.785	1.780	1.780	1.800	1.790	1.780	1.760
5492	200 krad	1.785	1.785	1.780	1.780	1.805	1.790	1.795	1.785
5526	100 krad	1.785	1.780	1.785	1.780	1.815	1.810	1.805	1.800
5616	100 krad	1.785	1.790	1.785	1.790	1.805	1.795	1.800	1.790

Table 10 Pre-Irradiation and Post-Annealing Differential Input Thresholds

In/Out Pin		Din_P_4/Dout_4				Din_P_5/Dout_5			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)		VIL (V)		VIH (V)	
5429	300 krad	1.790	1.790	1.800	1.800	1.795	1.785	1.755	1.780
5432	300 krad	1.785	1.790	1.800	1.800	1.765	1.810	1.830	1.760
5481	200 krad	1.795	1.800	1.800	1.775	1.725	1.575	1.765	1.770
5492	200 krad	1.790	1.785	1.800	1.795	1.730	1.775	1.850	1.785
5526	100 krad	1.790	1.790	1.800	1.800	1.795	1.745	1.760	1.855
5616	100 krad	1.790	1.795	1.800	1.790	1.805	1.795	1.775	1.795

Table 11 Pre-Irradiation and Post-Annealing Differential Input Thresholds

In/Out Pin		Din_P_6/Dout_6			
DUT	Total Dose	Pre-Irrad.	Post-Ann.	Pre-Irrad.	Post-Ann.
		VIL (V)		VIH (V)	
5429	300 krad	1.780	1.785	1.770	1.785
5432	300 krad	1.775	1.780	1.775	1.780
5481	200 krad	1.795	1.800	1.775	1.790
5492	200 krad	1.790	1.790	1.775	1.770
5526	100 krad	1.795	1.805	1.790	1.775
5616	100 krad	1.790	1.800	1.785	1.800

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Table 12 and Table 13. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 12 Pre-Irradiation and Post-Annealing VOL (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
5429	300 krad	0.010	0.010	0.106	0.108	0.176	0.180	0.442	0.451	0.916	0.931
5432	300 krad	0.010	0.010	0.107	0.108	0.178	0.179	0.449	0.451	0.930	0.931
5481	200 krad	0.010	0.010	0.108	0.109	0.180	0.182	0.455	0.457	0.944	0.941
5492	200 krad	0.010	0.010	0.108	0.108	0.180	0.180	0.452	0.454	0.937	0.937
5526	100 krad	0.010	0.010	0.104	0.110	0.174	0.183	0.437	0.461	0.907	0.952
5616	100 krad	0.011	0.008	0.110	0.089	0.183	0.147	0.462	0.372	0.958	0.780

Table 13 Pre-Irradiation and Post-Annealing VOH (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
5429	300 krad	3.288	3.283	3.211	3.204	3.076	3.066	2.724	2.708	2.049	2.029
5432	300 krad	3.288	3.283	3.211	3.204	3.078	3.066	2.728	2.706	2.062	2.023
5481	200 krad	3.288	3.284	3.211	3.203	3.076	3.064	2.724	2.701	2.048	2.011
5492	200 krad	3.288	3.285	3.210	3.206	3.074	3.067	2.719	2.707	2.039	2.023
5526	100 krad	3.288	3.285	3.212	3.204	3.080	3.063	2.734	2.698	2.068	2.003
5616	100 krad	3.288	3.289	3.210	3.222	3.073	3.105	2.717	2.797	2.033	2.191

F. Propagation Delay

Table 14 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is below 10%.

Table 14 Radiation-Induced Propagation Delay Degradations

Delay (ns)				
DUT	**Total Dose**	**Pre-rad**	**Post-rad**	**Post-ann**
5429	300 krad	611.5	626.05	605.71
5432	300 krad	602.5	614.91	594.63
5481	200 krad	633.5	643.3	630.15
5492	200 krad	605	616.6	603.33
5526	100 krad	617.5	602.3	615.15
5616	100 krad	640	603.2	636.4
Radiation Δ (%)				
DUT	**Total Dose**	**Pre-rad**	**Post-rad**	**Post-ann**
5429	300 krad	–	2.38 %	-0.94 %
5432	300 krad	–	2.06 %	-1.3 %
5481	200 krad	–	1.55 %	-0.52 %
5492	200 krad	–	1.92 %	-0.27 %
5526	100 krad	–	-1.46%	-0.38 %
5616	100 krad	–	-1.41%	-0.56 %

G. Transition Time

Figure 8 through Figure 31 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

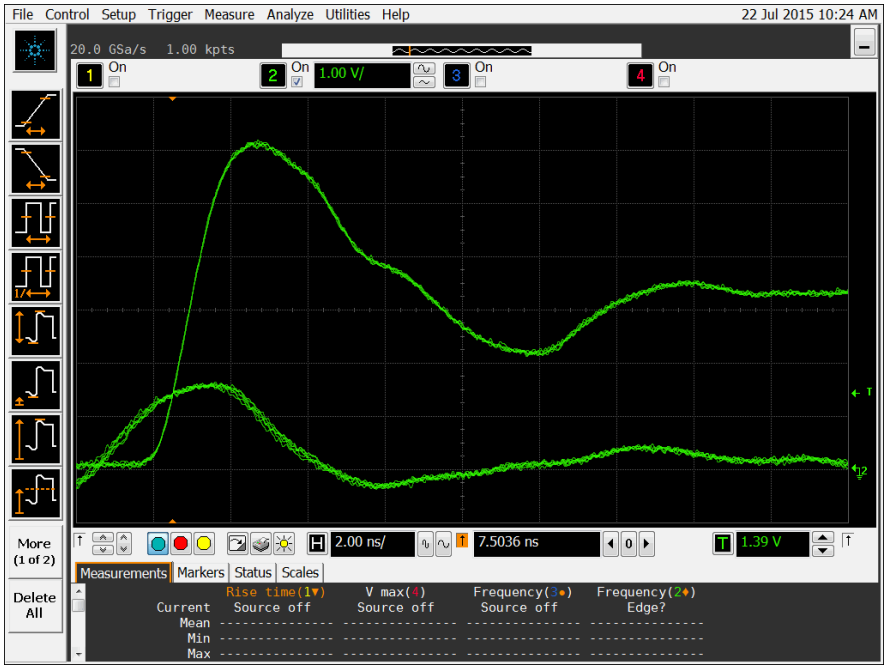

Figure 8 DUT 5429 Pre-Irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

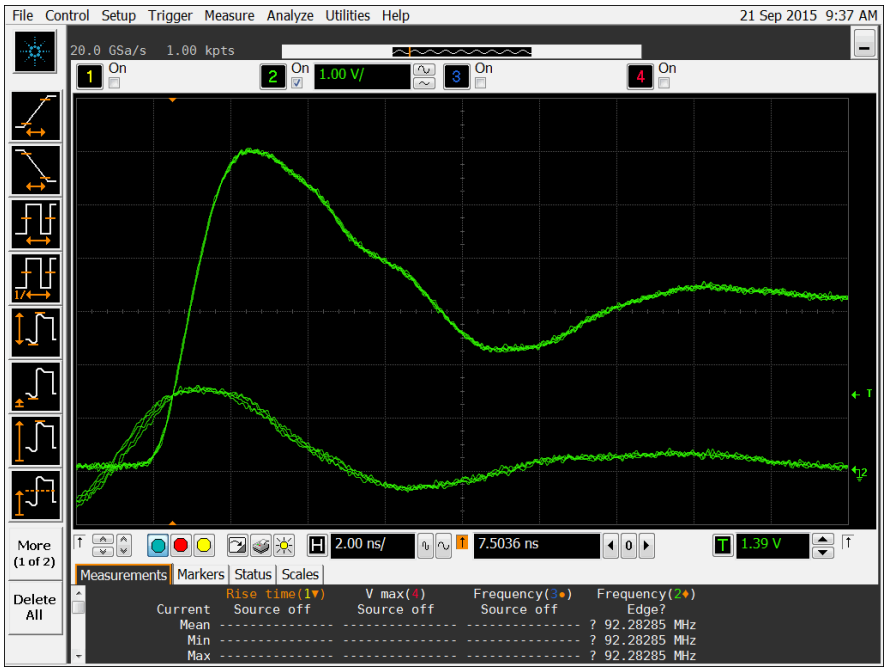

Figure 9 DUT 5429 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

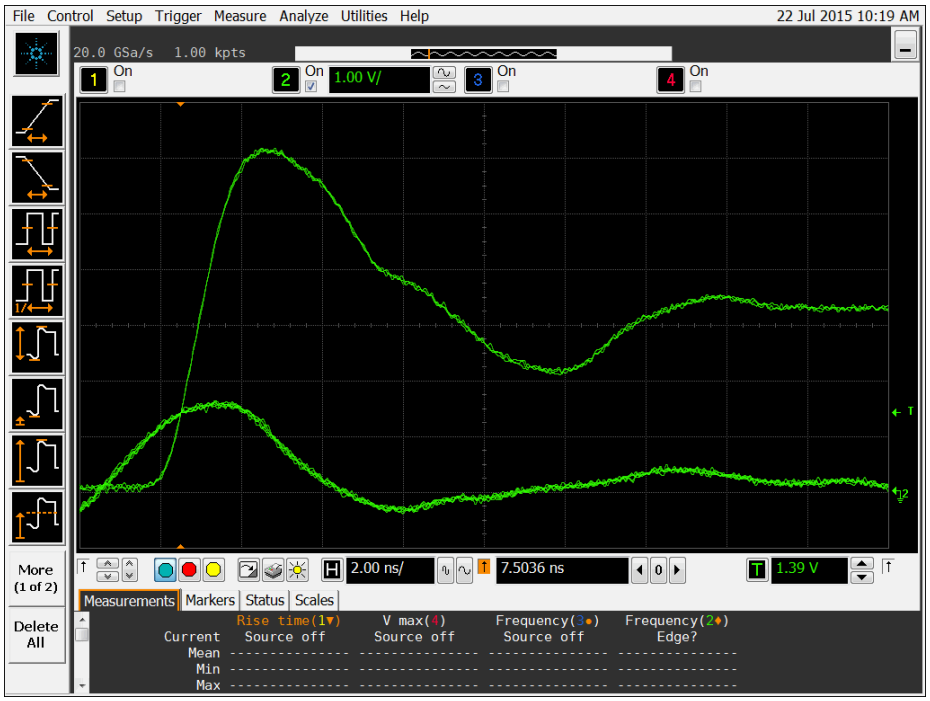

Figure 10 DUT 5432 Pre-irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

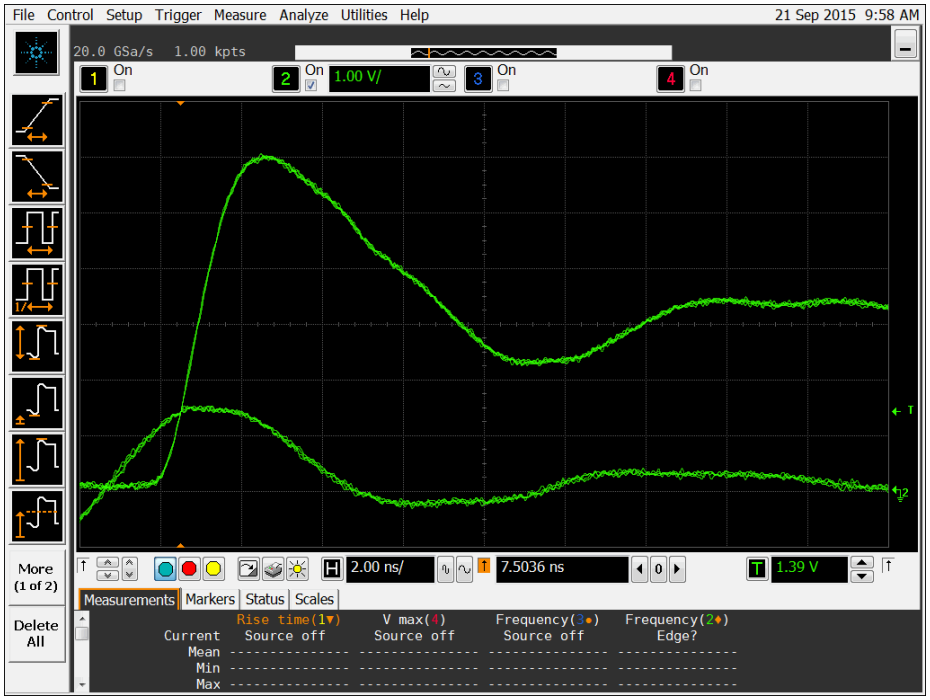

Figure 11 DUT 5432 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

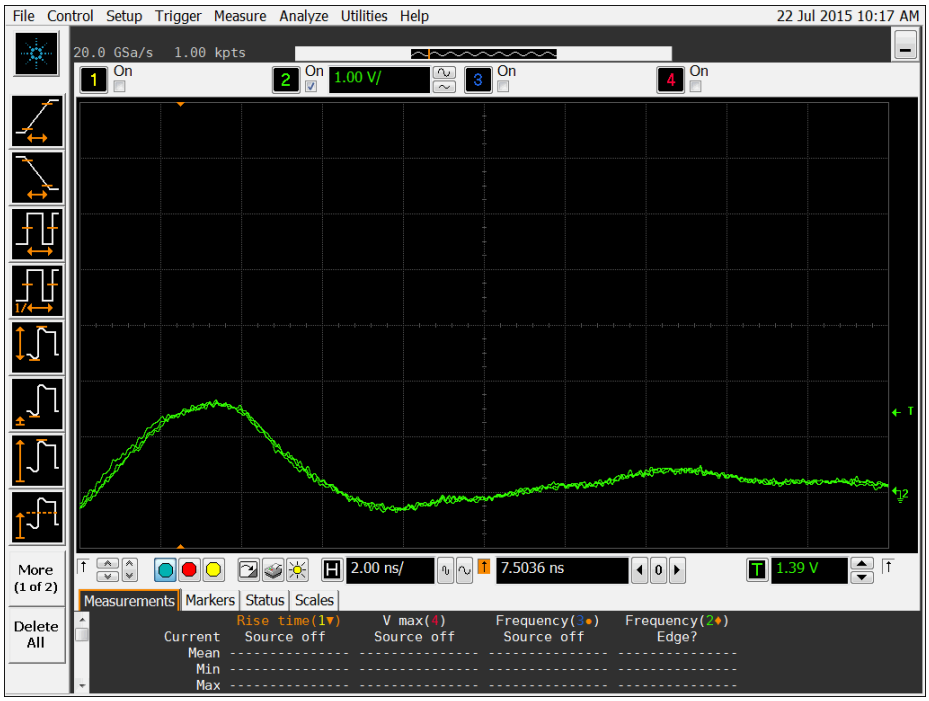

Figure 12 DUT 5481 Pre-Irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

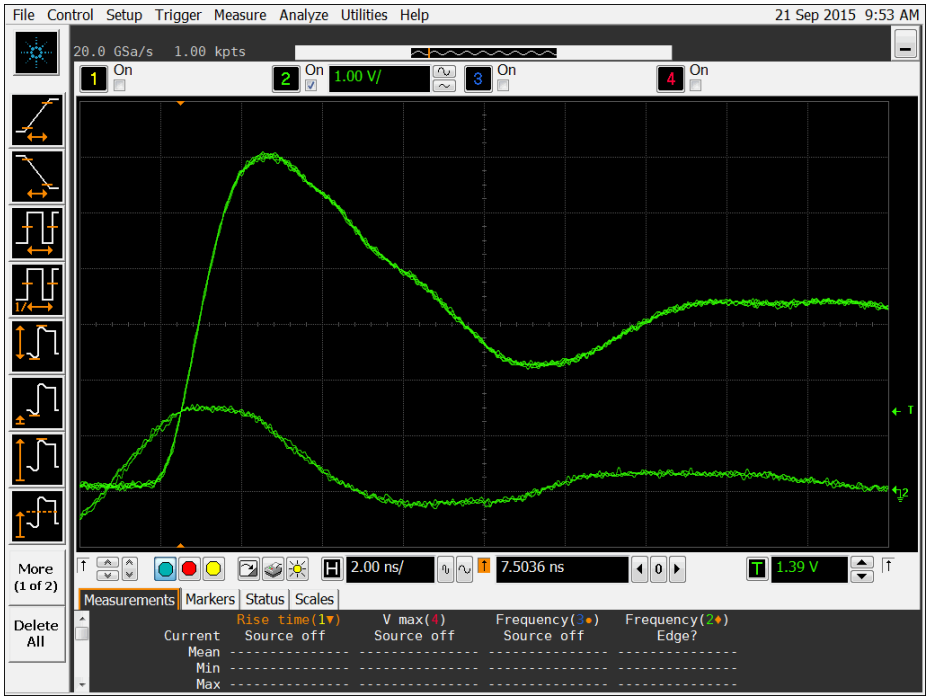

Figure 13 DUT 5481 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

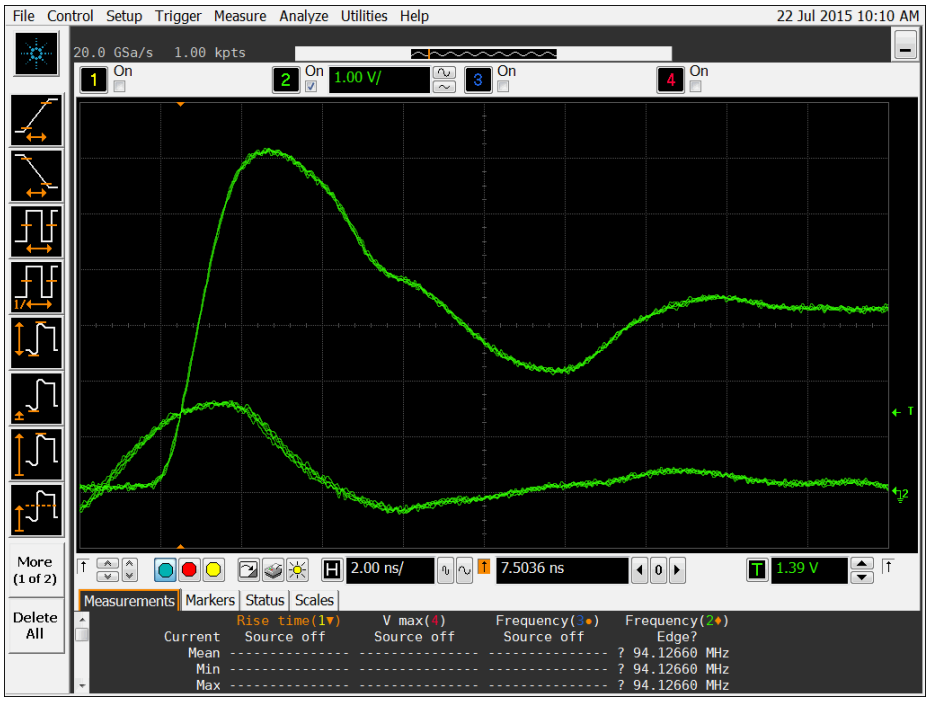

Figure 14 DUT 5492 Pre-Irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

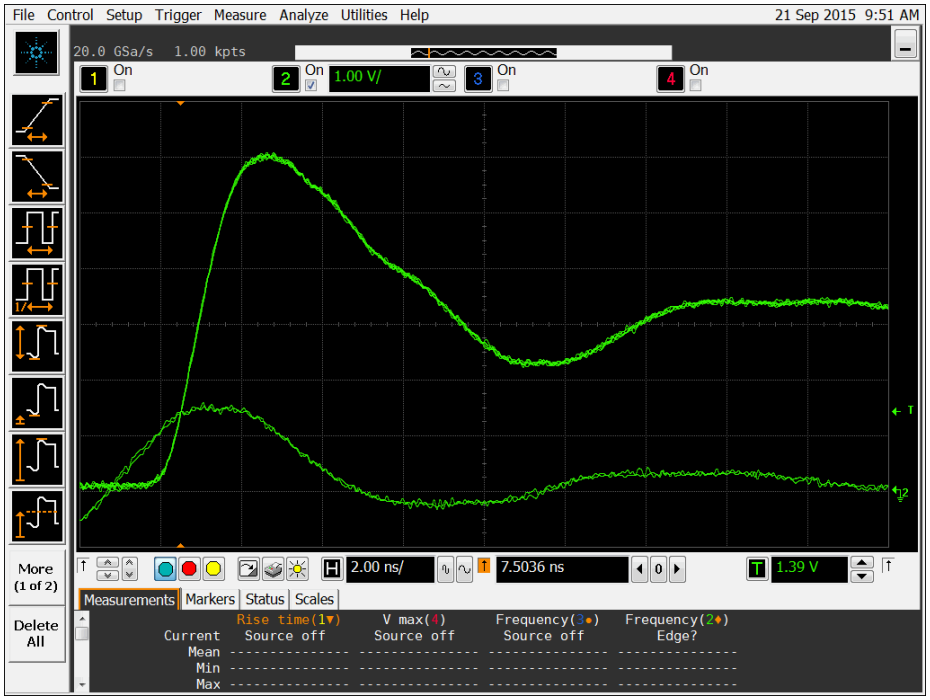

Figure 15 DUT 5492 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

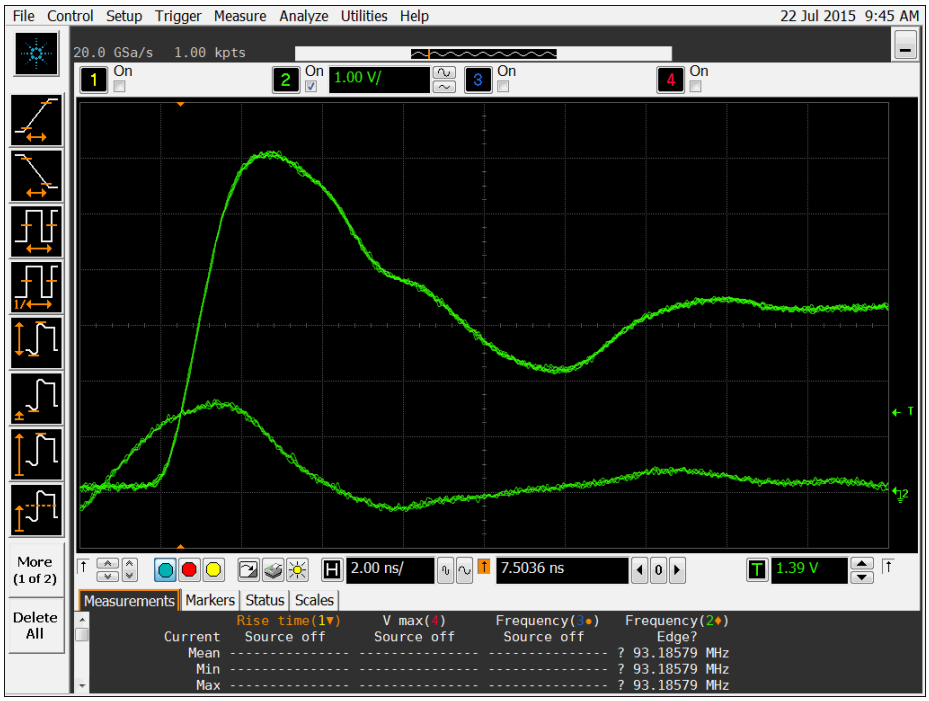

Figure 16 DUT 5526 Pre-Irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

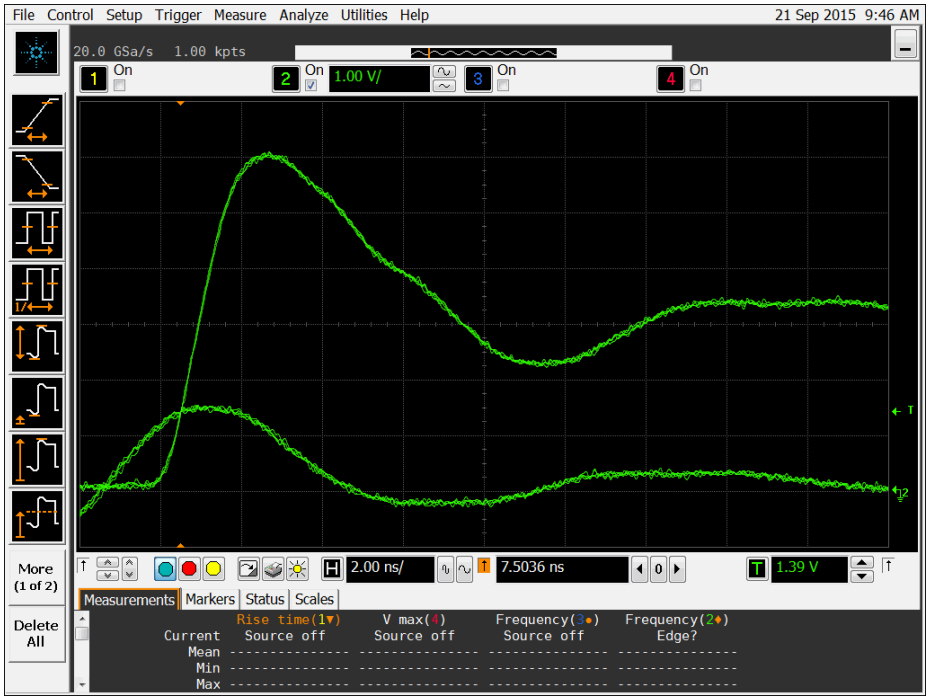

Figure 17 DUT 5526 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

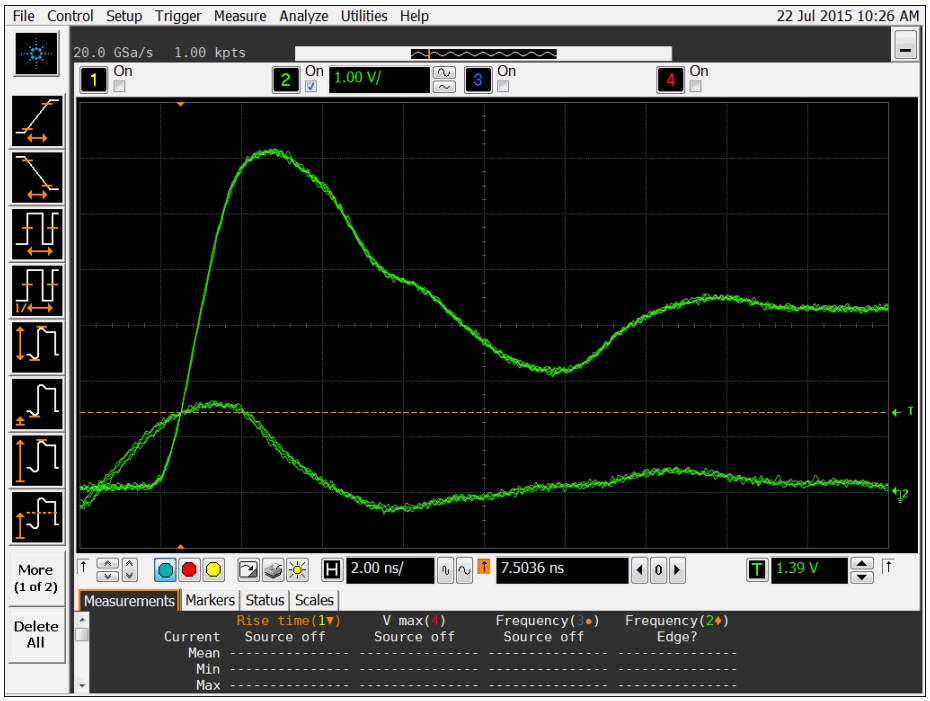

Figure 18 DUT 5616 Pre-Irradiation Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

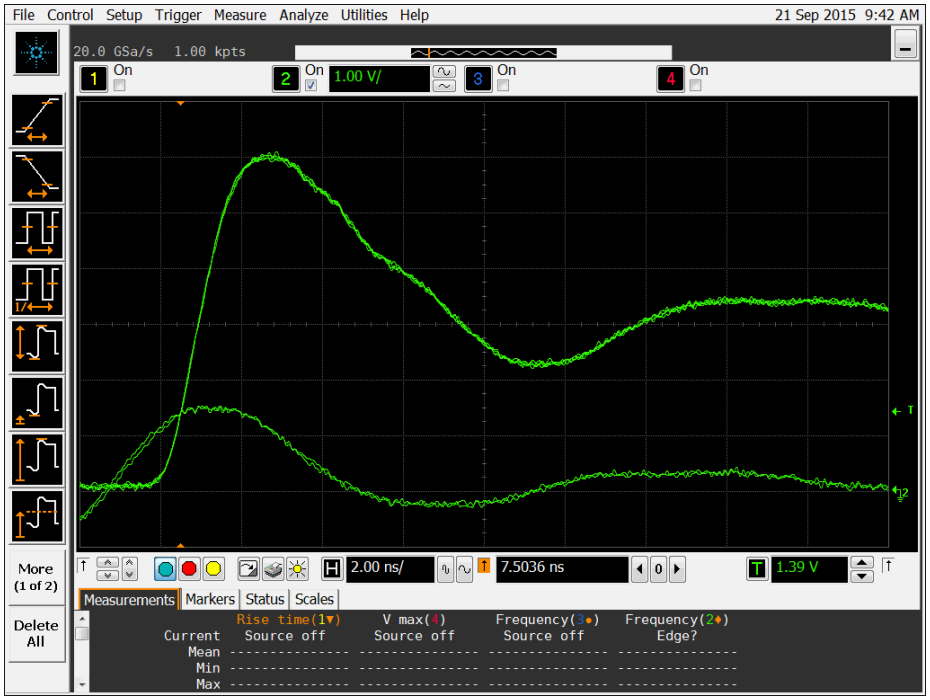

Figure 19 DUT 5616 Post-Annealing Rising Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

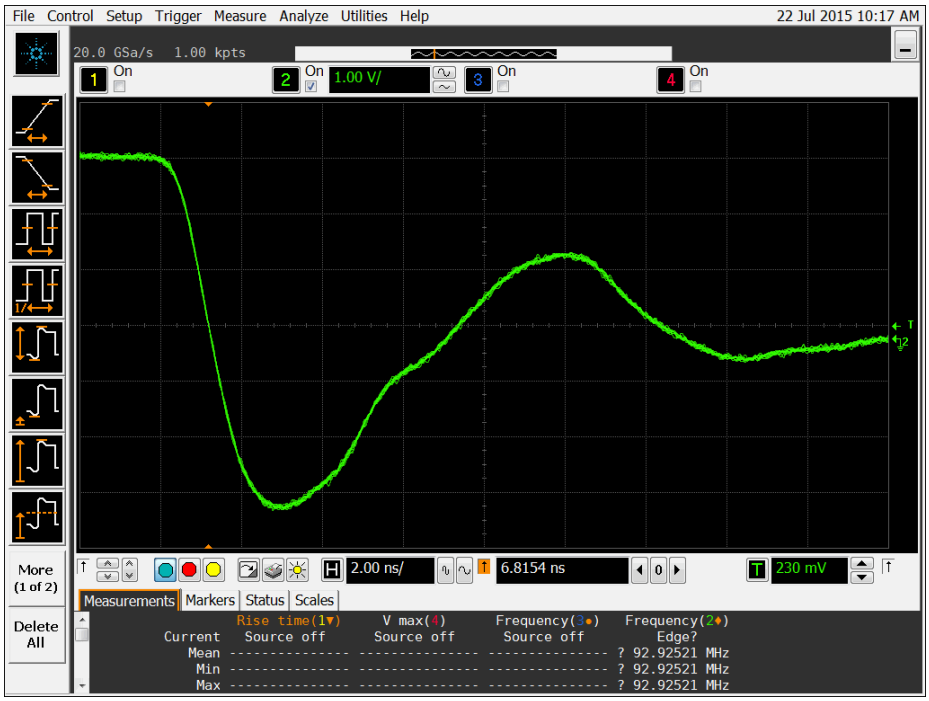

Figure 20 DUT 5481 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

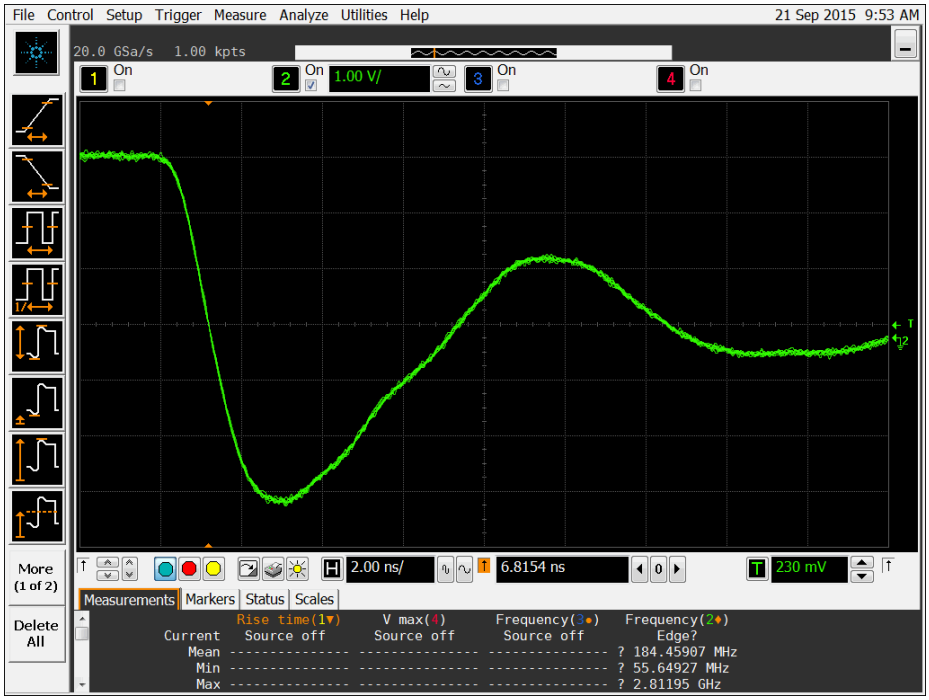

Figure 21 DUT 5481 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

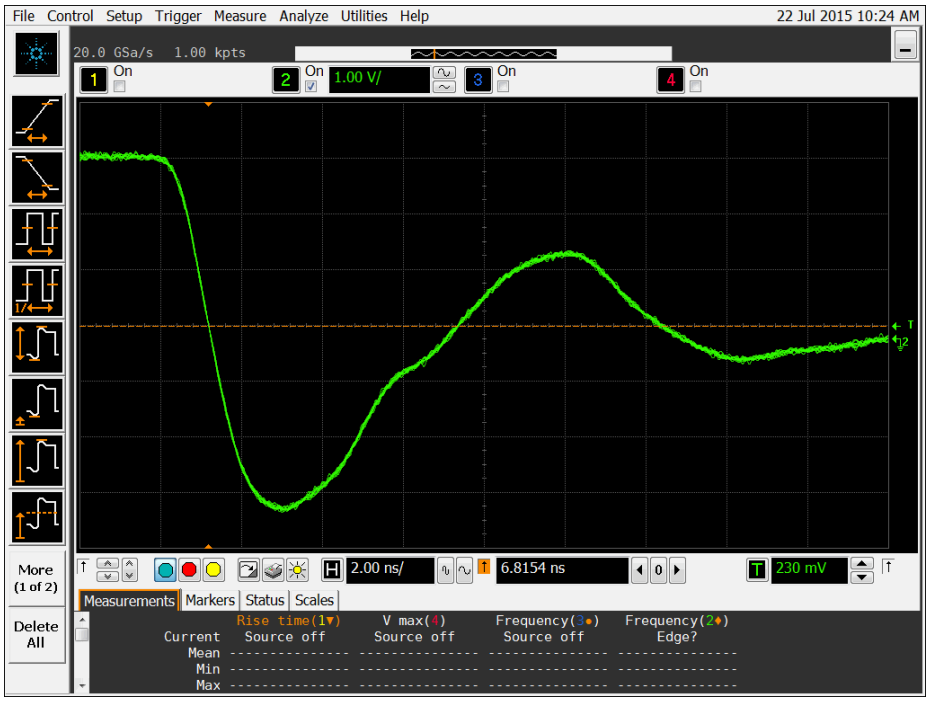

Figure 22 DUT 5429 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

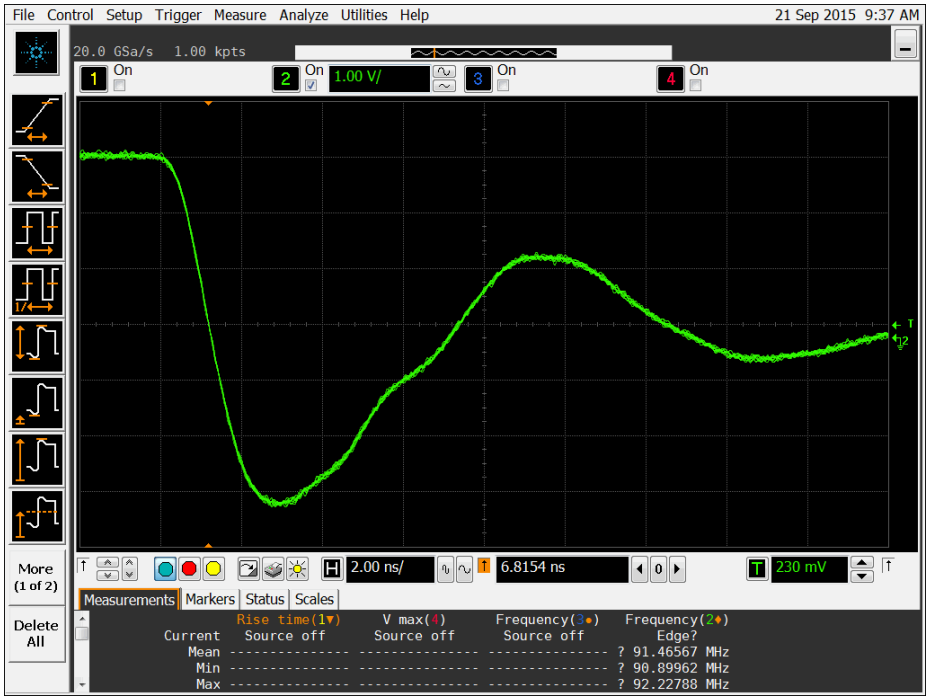

Figure 23 DUT 5429 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

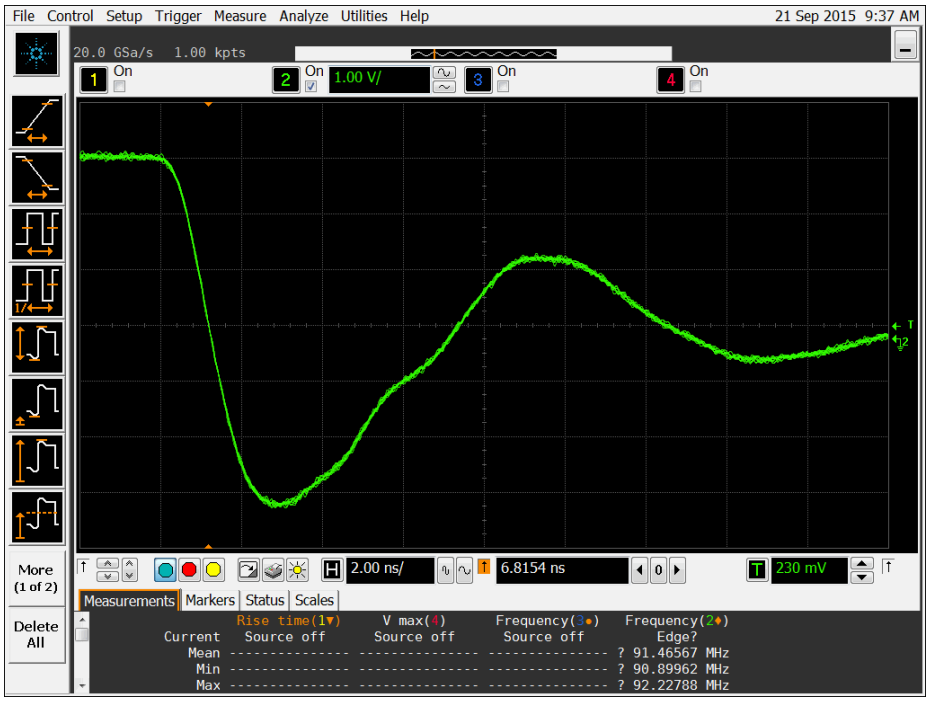

Figure 24 DUT 5432 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

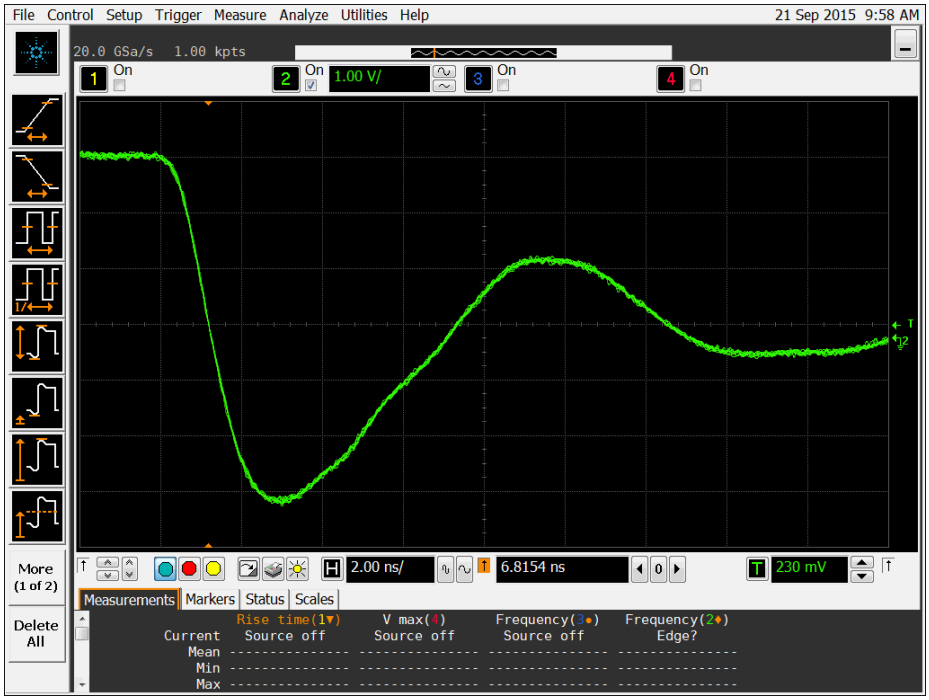

Figure 25 DUT 5432 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

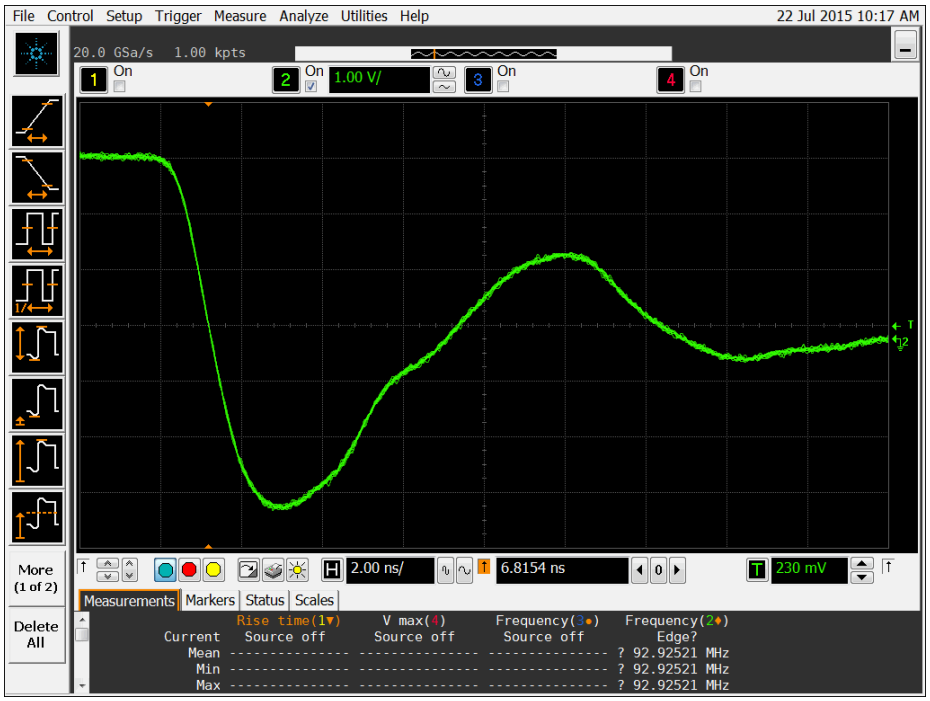

Figure 26 DUT 5481 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

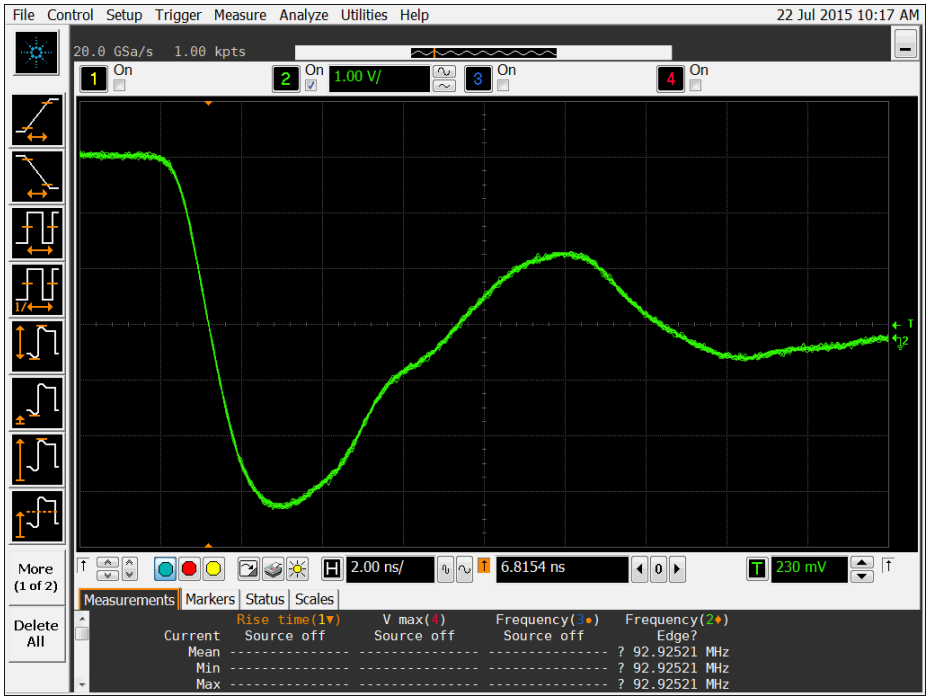

Figure 27 DUT 5481 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

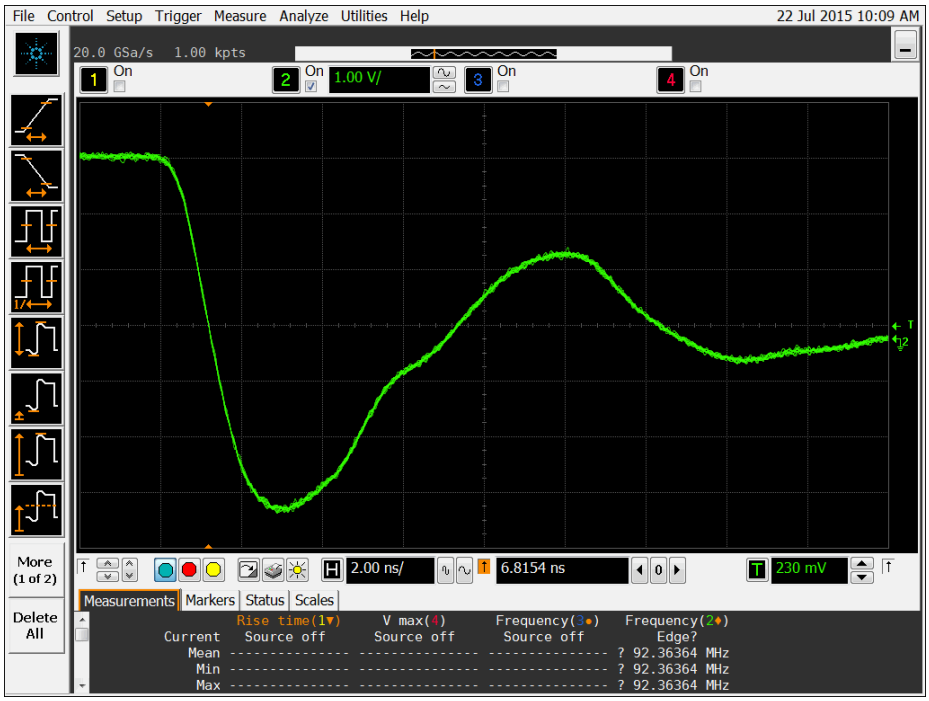

Figure 28 DUT 5492 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

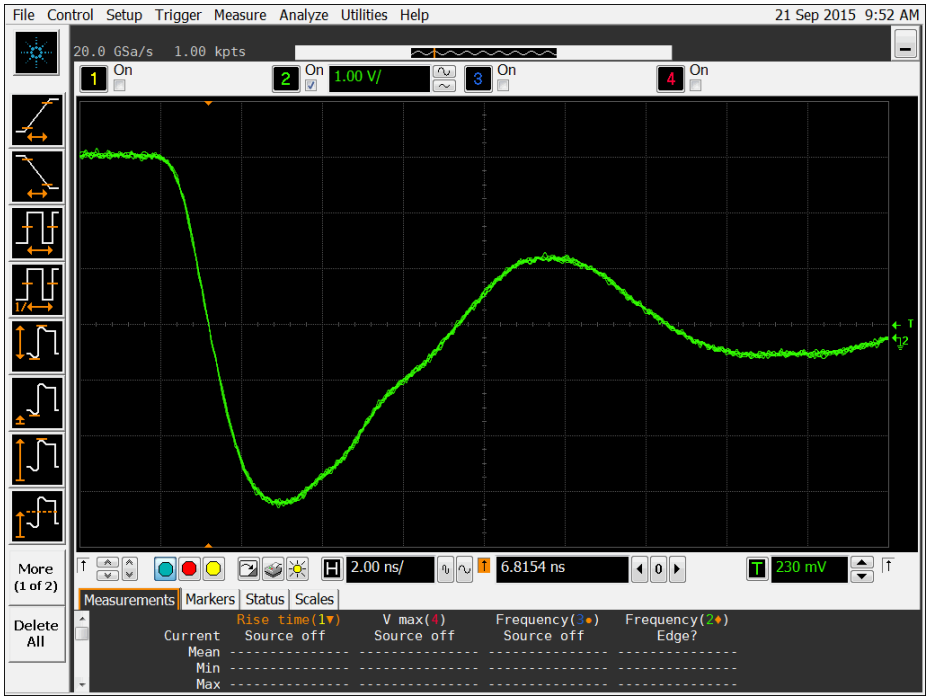

Figure 29 DUT 5492 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

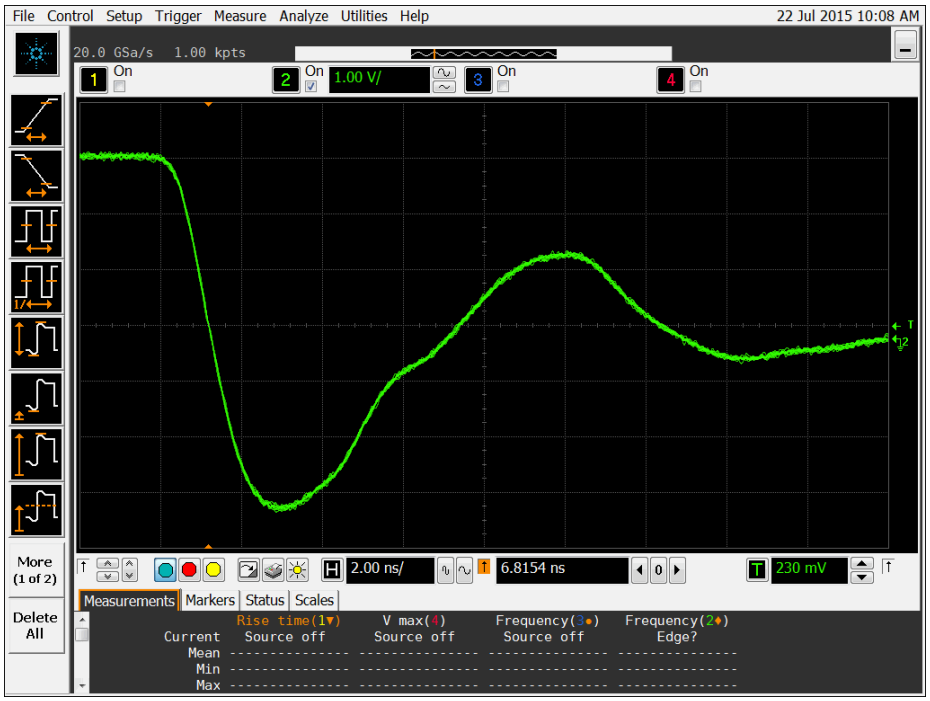

Figure 30 DUT 5526 Pre-Irradiation Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

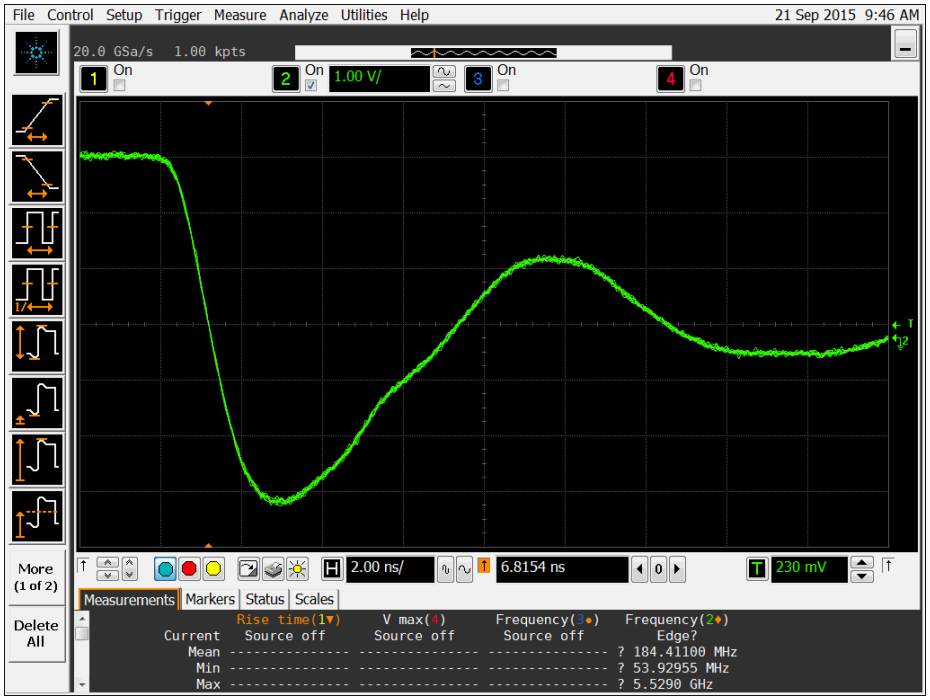

Figure 31 DUT 5526 Post-Annealing Falling Edge, Abscissa Scale is 1 V/div and Ordinate Scale is 2 ns/div

Note: For more information on DUT design schematics or the Verilog code, refer to *RTAX250S-D1H381 TID Reports* or *07T-RTAX250S-D1M6K1 TID Reports*.

IV. List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 1 (December 2015)	Initial revision	N/A

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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