Designing a PD69208AH PoE System 802.3af/802.3at Compliant

Application Note

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 12-ports of 4-pairs Power over Ethernet (PoE) system, based on three Microsemi™ PD69208AH 8-channel PoE managers. A layout guideline for PoE system based on PD69208AH is also included in this document.

This document enables designers to integrate PoE capabilities, as specified in IEEE802.3af and IEEE802.3at , into an Ethernet switch.

PD69208AH 8-ports PoE manager implements real time functions as specified in the standards, including detection, classification and port-status monitoring. The PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection methods, as specified in the standards.

The PD69208AH provides PD real time protection through the following mechanisms: overload, under load, over voltage and short-circuit.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69208AH datasheet catalogue number DS_PD69208AH

Features

- IEEE 802.3af-2003 standard compliant
- IEEE802.3at-2009 standard compliant
- Configurable AT/AF modes
- Supports 4-pair connection
- Two fingers classification
- Supports RPD/MRPD mechanism.
- Supports pre-standard PD detection
- Single DC voltage input (32 – 57V_{DC})
- Low power dissipation
- Built in 3.3V_{DC} and 5V_{DC} regulators
- Internal sense resistor (0.1Ω)
- Internal MOSFET with Low R_{DS_ON} (~0.24Ω)
- Internal power on reset
- Includes Reset input from hosting system
- Four direct I^2C address configuration pins
- Continuous port monitoring and system data
- Voltage monitoring/protection
- On-chip thermal protection
- Only one external front end component per port
- Wide temperature range: -40° to +85°C
- MSL1,RoHS compliant

Integration

The system described is designed for a 12-port switch feeding power over 4-pair for each port. (24 physical ports that are combined to 12 ports of 4-pair by three ICs of PD69208AH).

PoE system board can be easily integrated on top of a switch, providing the capability to add any PoE application while using different daughter applications (refer to Figure 1).

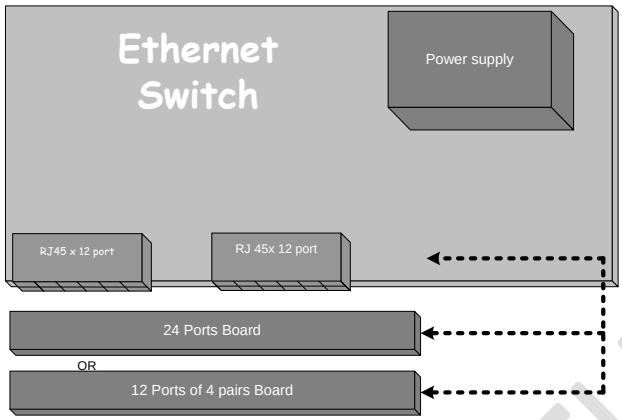


Figure 1: PoE Daughter Board Integration

Overall Description

A typical application includes the following blocks (Figure 2):

- PoE circuit for 12 ports (4 pairs) based on 3 PD69208AH.
- Host CPU Controller circuit, used to initialize, control and monitor each of the PD69208AH via an I^2C bus. The PD69208AH communicates with the Host CPU via an isolated I^2C interface.

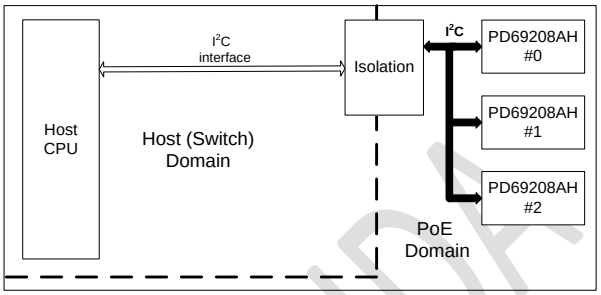


Figure 2: 12-port Configuration block diagram

General Circuit Description

The 12-port configuration for a PoE system shown in Figure 2, comprises three PoE manager circuits (PD69208AH) controlled by a Host CPU controller. PoE operations are automatically performed by PoE manager circuits, while Host Controller performs power management and other tasks. A configuration of 64 ports over two pairs of wires per port using 8 PoE managers or 64 ports over four pairs of wires per port is also possible using 16 PoE manager circuits (PD69208AH).

Communication Interfaces

Communication between Host CPU and PD69208AH via an I^2C interface. For more information, refer to the *User Guide reg map PD69208AH , catalogue number PD69208AH_UG_REG_MAP*.

Control

- An RESET_N control signal driven by Host CPU is used to reset the PoE system.

Indications

- An INT_OUT interrupt signal, utilized to indicate PoE events.

Main Supply

PoE system operates within a range of $32V_{DC}$ to $57V_{DC}$ (802.3at port's range is $50V_{DC}$ to $57V_{DC}$). To comply with UL SELV regulations, maximum output voltage **should not** exceed $60V_{DC}$.

Grounds

Several grounds are utilized in the system.

- PoE Domain Analog
- PoE Domain Digital
- Chassis
- Host Domain Floating

Digital and analog grounds are electrically the same ground. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

Chassis ground is connected to switch's chassis ground. This ground plane should be $1500V_{rms}$ isolated from PoE circuitry.

Host domain floating ground is isolated from PoE domain grounds.

Detailed Circuit Description

Block Diagram/Main

Refer to Figure 5.

Communication Interfaces/Isolation

There is one communication interface in this circuitry:

- An interface between the Ethernet switch and the PD69208AH; this interface is an I^2C interface and has 1500Vrms isolation.

Isolation circuit comprises a digital isolator (U1 on Figure 7). Note that each side of the isolator circuitry is fed by a separate power supply.

I^2C communication:

PD69208AH uses I^2C communication in order to communicate with host.

I^2C acts as an I^2C slave mode only and supports Standard mode (100KHz), Fast-mode (400KHz), Fast-Mode Plus (1MHz) frequencies.

Each PD69208AH has an address determined by ADDR0-ADDR3 pins. Up to 16 ICs can be supported for 4-pairs configuration or eight ICs in 2-pair configuration.

Clock: PD69208AH has an internal CLK of 8 MHz and 31MHz clock oscillators.

$5V_{DC}$ and 3.3 V_{DC} Regulators

Each PD69208A utilizes two power sources. One of $5V_{DC}$ and the other one $3.3V_{DC}$.

There are three options to supply these sources and it's up to the designer to choose the best option for the design.

- Option 1: PD69208AH internal regulators—since the PD69208AH consumes 35mA typically the power dissipation that will be imposed on the PD69208AH internal regulator is 35mA multiplied by Vmain (about 35mA x 55V = ~2W). This option can be used where proper ventilation or heat sink is used.
- Option 2: external linear regulator based on NPN transistor controlled by PD69208AH—in this option the power dissipation on the external linear regulator will still be about 2W, however it is possible to locate this NPN transistor away from the PD69208AH and have better thermal design of the system. When using this option, add 4.7uF capacitor on pin DRV_VAUX5.
- Option 3: external step down regulator utilizing external 5V source if available or adding a step down regulator. In this case the regulator power dissipation will be about 0.2W (taking into consideration 90% efficiency). This option is suitable for crowded, small or unventilated design. See Figure 3.

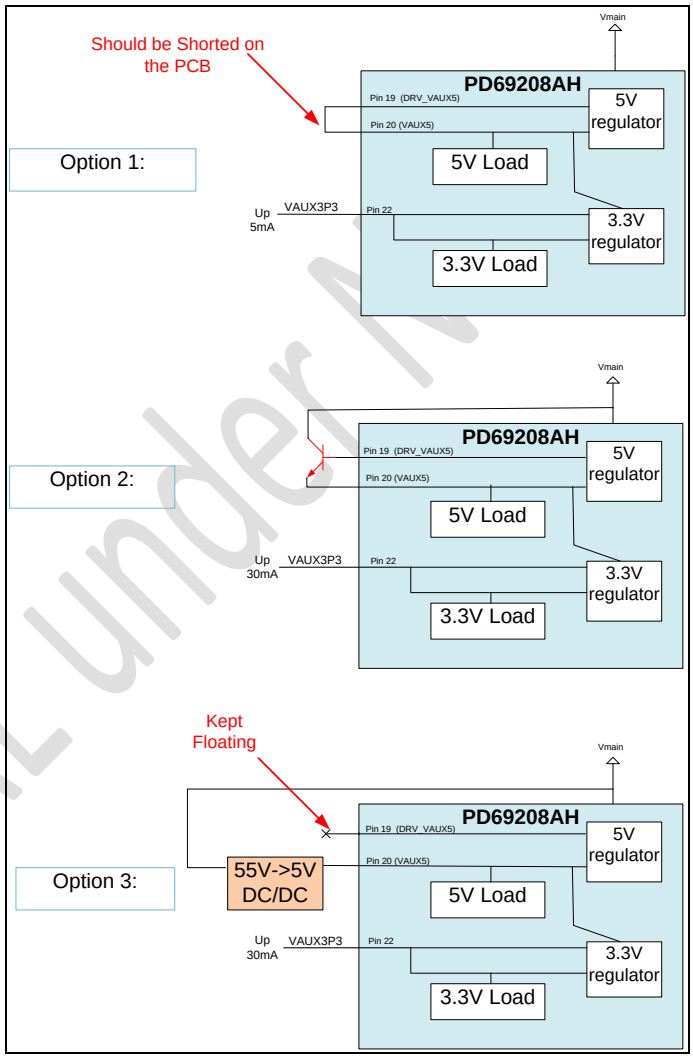
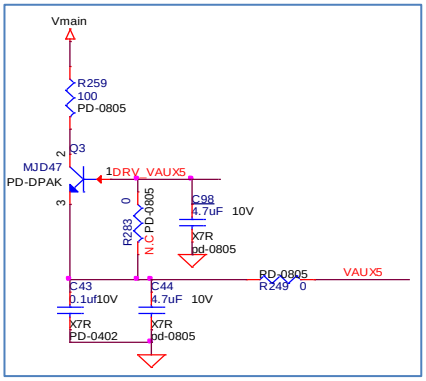


Figure 3: Three options for 5V design

- when using external PS for the 5V the sequence must be:

1. Turn on Vmain (above 32V).
2. Turn on External 5V.



Option 2 details.

PoE Manager Circuitry

PD69208AH performs a variety of internal operations and PoE functions, requiring a minimum of external components. Each PD69208AH handles up to eight ports.

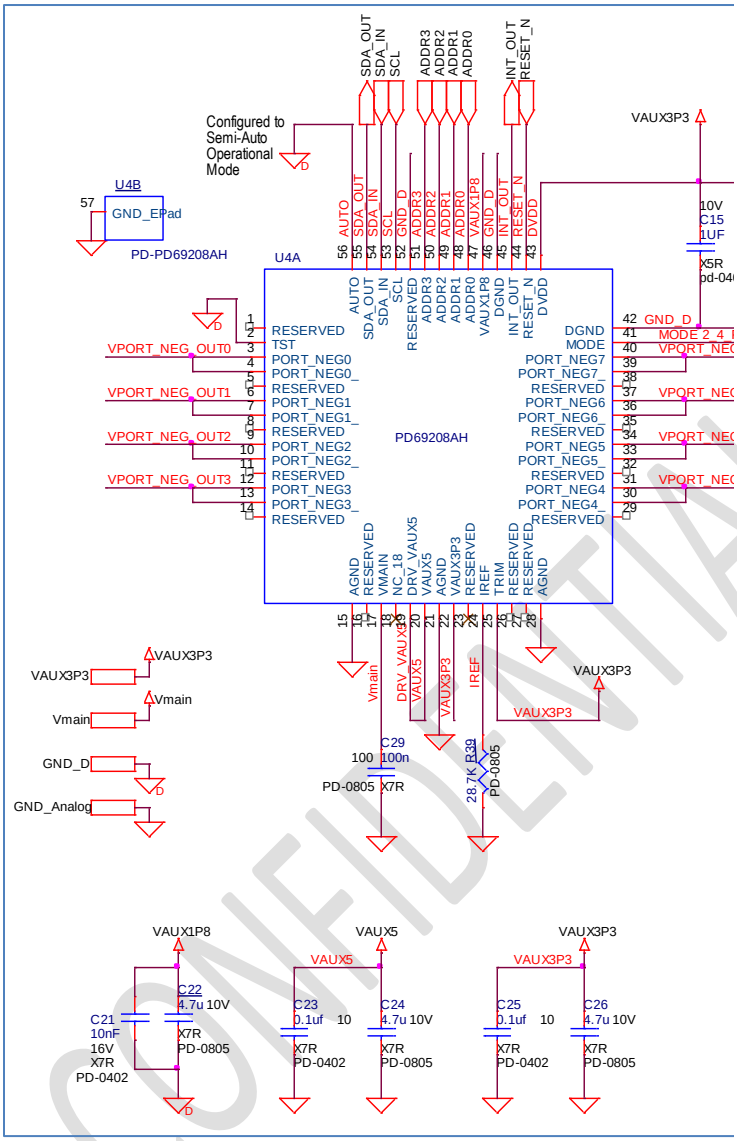


Figure 6 shows PoE Manager #0 with its related components for an 8-port configuration. Figure 5 presents a duplication of three PoE Managers for 12 ports of 4 pairs.

Reference Current Source

Reference for internal voltages within PD69208AH is set by a precision 28.7KΩ resistor (R39).

Sense Resistors

PD69208AH is providing an internal sense resistor of 100mΩ to each port. This resistor is utilized to measure port currents.

Front End components

A single capacitor per port is the only external front end component being used.

All other components such as reverse diode, port protection, sense resistor and switching MOSFET are internal.

Fuses per port are not required in circuits with total power level of up to 3kW as the PD69208AH is designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1.

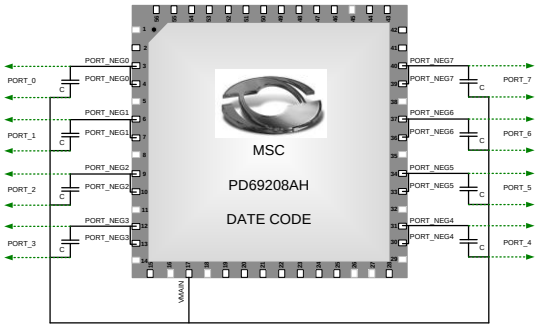


Figure 4: 8-ports Front End components

Line transformer

The designer should use a line transformer that is dedicated to PoE. Moreover, special care should be taken in order to choose a line transformer with the application desired PoE current.

Operation mode:

There are two operation modes for the PD69208AH

- Auto mode

- Semi Auto mode

These two options can be configured by pin #56
Called AUTO before chip power up.
GND = Semi Auto Mode
3.3V = Auto Mode

I^2C address in 2-pairs mode:

In 2-pairs mode the IC keeps the PoETeC 4-ports architecture and addresses each 4-port portion in a different address by changing the ADDR0 bit internally.
When the IC is in 2-pairs mode it will have 2 I^2C addresses ('010',A3,A2,A1,'0'b) and ('010',A3,A2,A1,'1'b).
For example: if the IC ADDR3,ADDR2,ADDR1,ADDR0 are '0000' then the IC will response to I^2C addresses 0100000b and 0100001b while the 0100000b will refer to ports 1-4 and 0100001b will refer to ports 5-8.

I^2C address in 4-pairs mode:

In 4-pairs mode the register map will refer to the 4-pairs ports only.
When the IC is 4 pairs then it will have one I^2C address ('010',A3,A2,A1,A0 b).
Maximum number of ports will be 16x4=64.

4-pairs / 2-pairs MODE

MODE pin set the PD69208AH operational mode between eight 2-pairs ports or four 4-pairs ports.
The pin must be set before chip power up.
The PD69208AH do not support mix of 2-pairs and 4-pairs.

4-Pair Connectivity

In order to have the ability to deliver to the PD more than 30W, 4-pairs powering is used.
4-pairs powering utilizes all eight RJ45 wires for delivering the power.
Four pairs of wires is quite easy using PD69208AH in pin #41 to 4-pair mode.
It is implemented by utilizing two physical ports (1 logical port) of PD69208AH with two separate front-ends, each delivers maximum AT power, enabling delivery of 60W over 4-pairs.
The 2-ports drive separates 2-pairs and connects together inside the PD after the serial diodes.
4-pairs port can be mixed between each two ports in the same IC.
For example: port 1 with port 7, etc.

I^2C lines

An SDA_IN signal should be connected to pin #54 of PD69208AH.

An SDA_OUT signal should be connected to pin #55 of PD69208AH.

An SCL signal should be connected to pin #53 of PD69208AH.

A pull-up resistor is required on the I^2C communication line (pins 53,54 and 55).

Ground Interface Connection (AGND)

Power supplies ground connector enables the current path back to power supply. Ground connection should be capable of carrying all strings current back to power supplies.

Thermal Design

The design should take into account power dissipation of PoE manager and associated circuitry and the maximum ambient operating temperature of the switch. Adequate ventilation and airflow should be part of the design to avoid thermal over-stress. The power dissipation over the PoE manager can be calculated as follows:

$I_{port}^2 \times R_{CH\_ON} \times 8 + P_{Regulator} = P_{PoE\_manager}$

Were:

I_{port} – is the port maximum output current

R_{CH_ON} – is the total PoE manager internal channel resistance *

8 – indicates eight ports

$P_{Regulator}$ – is the internal regulator losses if it has been used (See PoE manager regulators section on page 4 above).

* Pay attention that R_{CH_ON} can get 50% higher than typical in a hot environment as the Mosfet R_{DS_ON} is temperature dependent.

Ambient Temperature

Application's thermal design should take into account the temperature derived from Switch's power dissipation and from PoE daughter board powered at maximum load.

PD69208AH

PoE design should ensure that PD69208AH maximum operating junction temperature (150°C) is not exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at the maximum load according to the design, and all other product units functions and fully operational (such as the Ethernet Switch phy, power supply, LED drivers etc.). *PD69208AH datasheet, catalogue number DS_69208AH contains* additional thermal characteristics details.

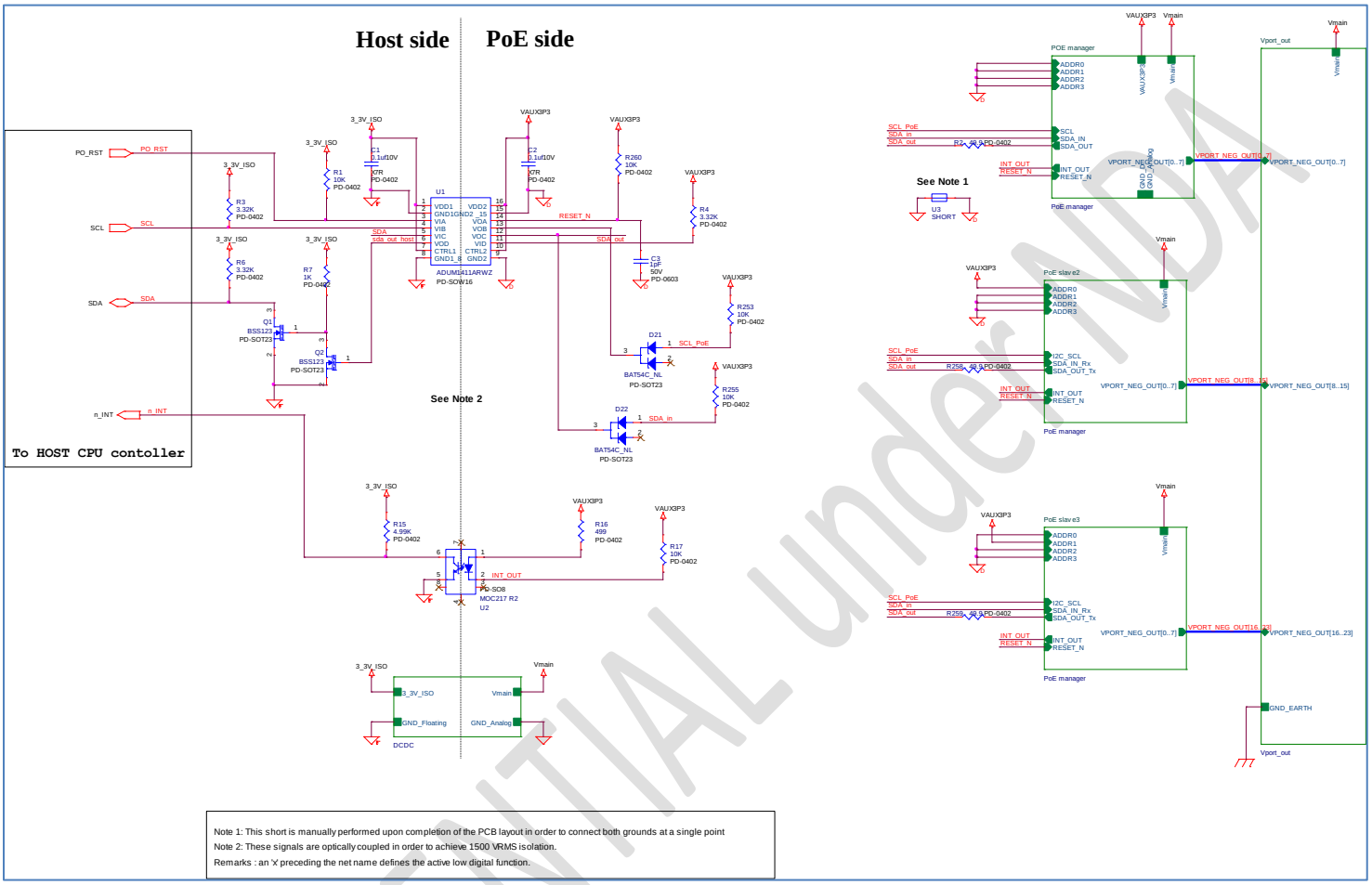


Figure 5 : 12-ports System main blocks

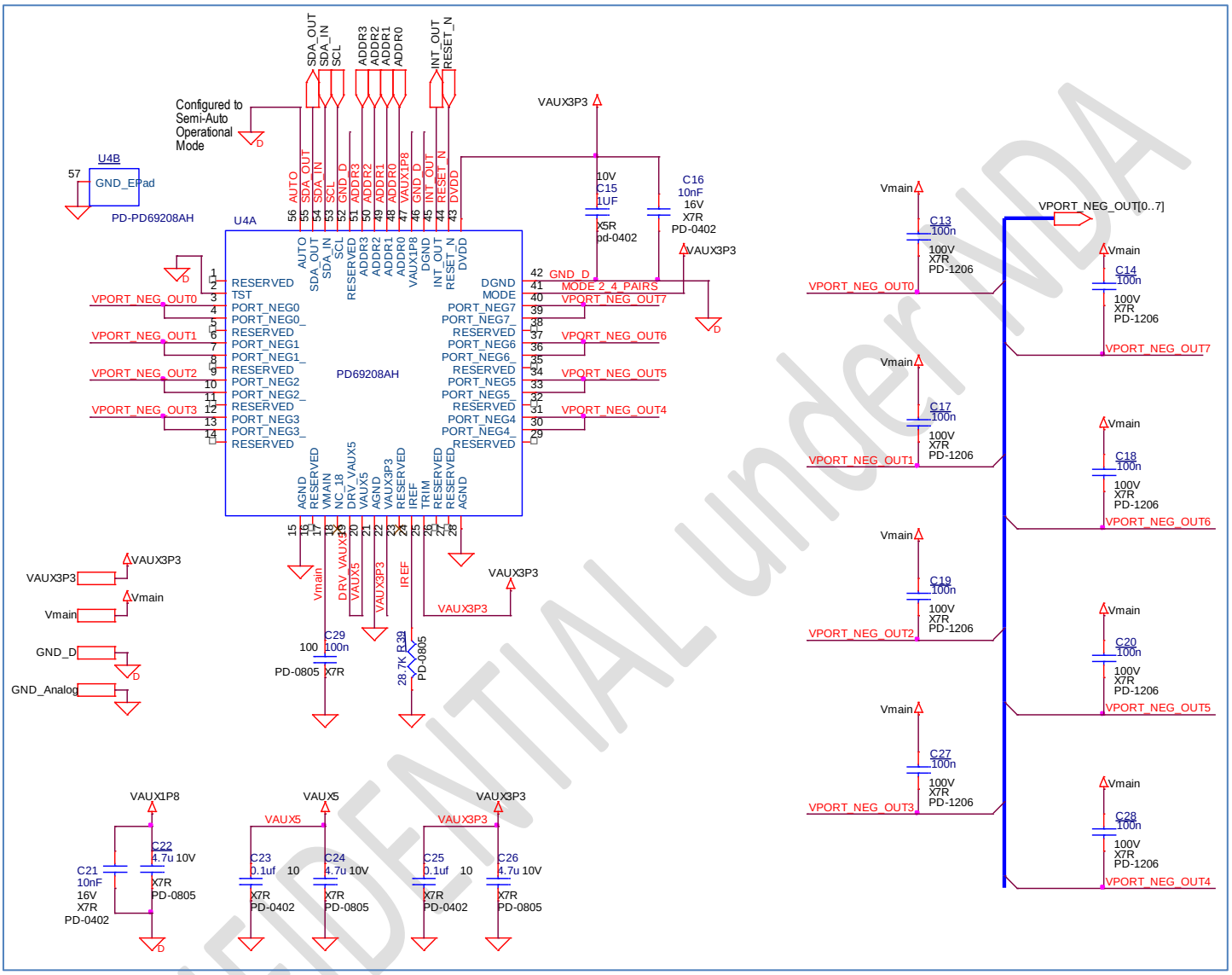


Figure 6: PD69208AH Circuitry for PoE Manager #0 (6 PL)

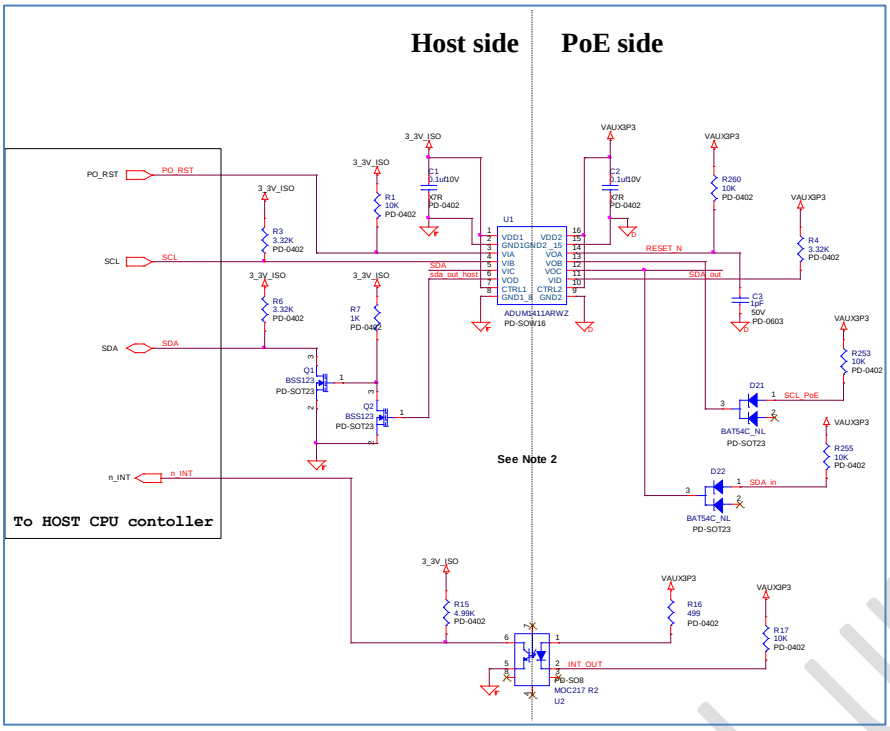


Figure 7: Digital Isolator + interrupt isolator

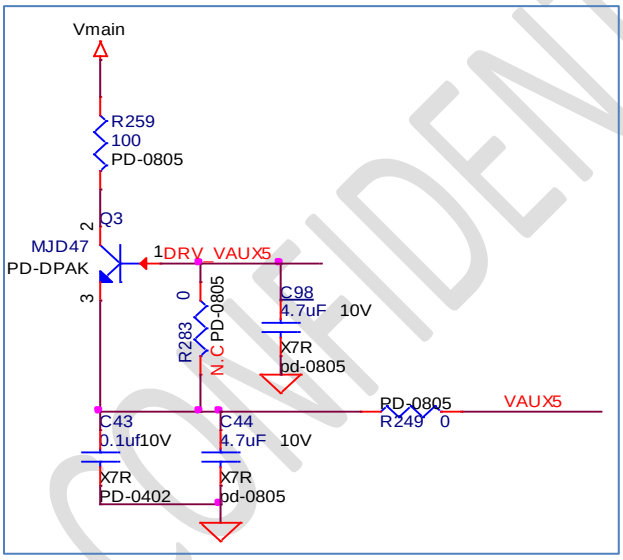


Figure 8: Boost Transistor to the 5VDC Regulator

Bill of Materials for a PoE System

Table 1: Main Block Components

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
MAIN	2	C1,C2	CAP CER 0.1uF 10V X7R 10% ^^0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	C3	Capacitor, COG, 1pF, 50V 0603 ±0.25pF	PD-0603	AVX	06035A1R0CAT2A
	2	D21,D22	DIO 30V 200mA COM.CATHODE SOT 23 DOUBLE	PD-SOT23	Fairchild	BAT54C
	2	Q1,Q2	FET NCH 100V 0.15A 6RLogic Level SOT23	PD-SOT23	Infineon	BSS123
	5	R1,R17,R253,R255,R260	RES TCK FLM 10K 1% 62.5mW ^^0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	3	R2,R258,R259	RES TCK FLM 49.9R 1% 62.5mW ^^0402 SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	3	R3,R4,R6	RES TCK FLM 3.32K 1% 62.5mW ++0402 SMT	PD-0402	Bourns	CR0402-FX-3321-ELF
	1	R7	RES TCK FLM 1K 1% 62.5mW ^^0402 SMT 100 PPM	PD-0402	Panasonic	ERJ2RKF1001X
	1	R15	Resistor, 4.99K, 1%, 1/16W 0402	PD-0402	Panasonic	ERJ-2RKF4991X
	1	R16	RES TCK FLM 499R 1% 62.5mW ^^0402 SMT	PD-0402	Bourns	CR0402-FX-4990-ELF
	1	U1	IC Dig.Isol VDD1-3ch/VDD2-1ch 1Mbps 3.3/5V SO16^	PD-SOW16	Analog Devices	AD80273ARWZ-RL **
	1	U2	IC OPTOISOLATOR MOC217^^	PD-SO8	Fairchild	MOC217 R2

Table 2: PoE Manager Components

Block	Qty*	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Manager	8	C13,C14,C17-C20,C27,C28	CAP CRM 100nF 100V 10%X7R 1206 SMT	PD-1206	Murata	GRM319R72A104KA01D
	2	C22,C24,C26	CAP CRM 4.7uF 10V 10%^^X5R 0805 SMT	PD-0805	Murata	GRM219R61A475KE19D
	1	C29	Capacitor, X7R, 100nF 100V 10% 0805	PD-0805	AVX	08051C104KAT2A
	2	C23,C25	CAP CER 0.1uF 10V X7R 10% ^^0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	C15	CAP CER 1.0UF 10V X5R 10% 0402	PD-0402	Panasonic	ECJ-0EB1A105M
	1	R39	RES 28.7K 125mW 1%0805 SMT MTL FLM	PD-0805	Vishay	CRCW080528K7FKEA
	1	C16,C21	Capacitor, CER, X7R, 10nF 16V 10% 0402 SMT	PD-0402	Murata	GRM155R71C103KA01D
	1	U4	IC 8 Port PSE PoE Manager SMT	PD-MLF56-HS	Microsemi	PD69208AH

*These quantities should be multiplied by the number of PD69208AH (three managers in this paper)

**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.
***Fuses per port are not required for use in circuits with a total power level of up to 3kW. That's because PD69208AH is a UL 2367 (category QVRQ2) recognized component and fulfills limited power source (LPS) requirements of latest editions of IEC60950-1 and EN60950-1.

Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a 8-port Power over Ethernet (PoE) system, based on Microsemi's™ 8-channel PoE Manager—the PD69208AH.

Isolation and Termination

According to the IEEE 802.3af and the IEEE802.3at standard, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.

These requirements are taken into account by PoE switch vendors, while designing the switch circuitry. However, when a PoE Manager is integrated into a switch, special design considerations must be met, due to the unique combination of data and power circuitries.

The following paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating the Microsemi's PoE Chip Set and the daughter boards.

Isolation

As specified in the IEEE PoE standards, 1500 Vac rms isolation is required between the switch's main board circuitry including protective and frame ground and the Media Dependent Interface (MDI). Figure 9 illustrates the overall isolation requirements.

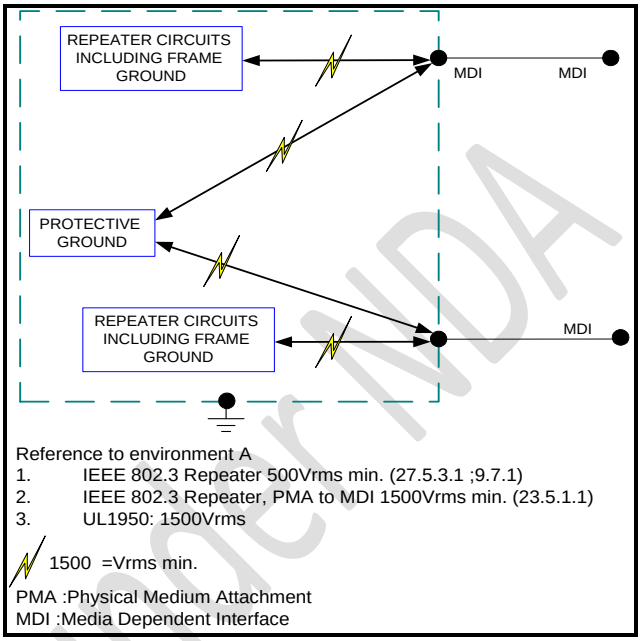


Figure 9: Isolation Requirements

High Voltage Isolation

- For a switch with no PoE circuitry: isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers (see Figure 9).
- When integrating a PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry/ground.

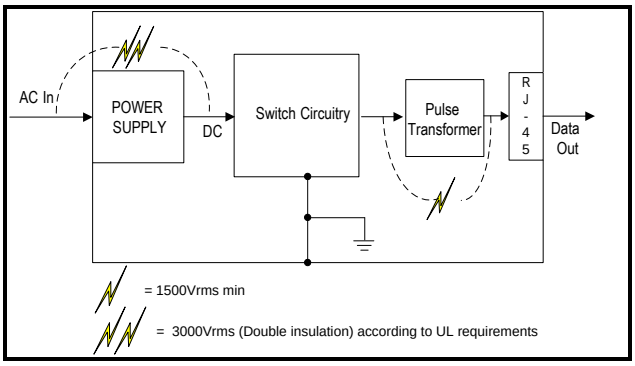


Figure 10: Standard Switch Circuitry

To comply with the above isolation requirements, the PoE managers must be isolated in regards to all other switch circuitries. Use one of the following methods:

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 10).
- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 11).

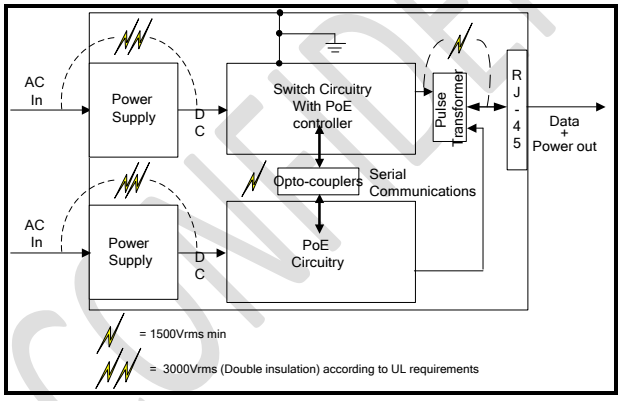


Figure 11: Switch Circuitry with Two DC Source

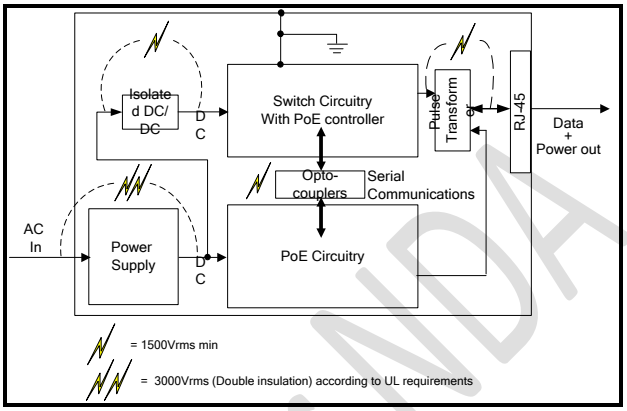


Figure 12: Switch Circuitry with a Single DC Source

To maintain 1500 Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended, to provide a safe margin for hi-pot requirements.

PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry (see Figure 13). Note that in most PoE systems, it is recommended to use 0 Ω resistors for R1 and R2. However, certain systems may benefit from 75 Ω resistors. Filtering provisions should be made. Note that in quiet PoE systems the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both methods are detailed in Figure 14 which illustrates an MDI-X (or Auto MDI-X) connection associated with the switch.

Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 Vrms isolation between PoE voltages and frame ground (EGND). Notice that RJ-45 jack assemblies have a metal cover of 80 mils that almost reaches to the PCB surface.

Maintain an 80 mils traces clearance between EGND traces for the RJ-45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 Vrms isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as VDC. Thus, plan adjacent traces for 100 VDC operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

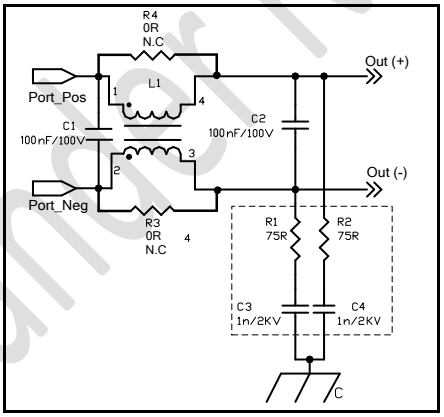


Figure 13: Recommended EMI Filter

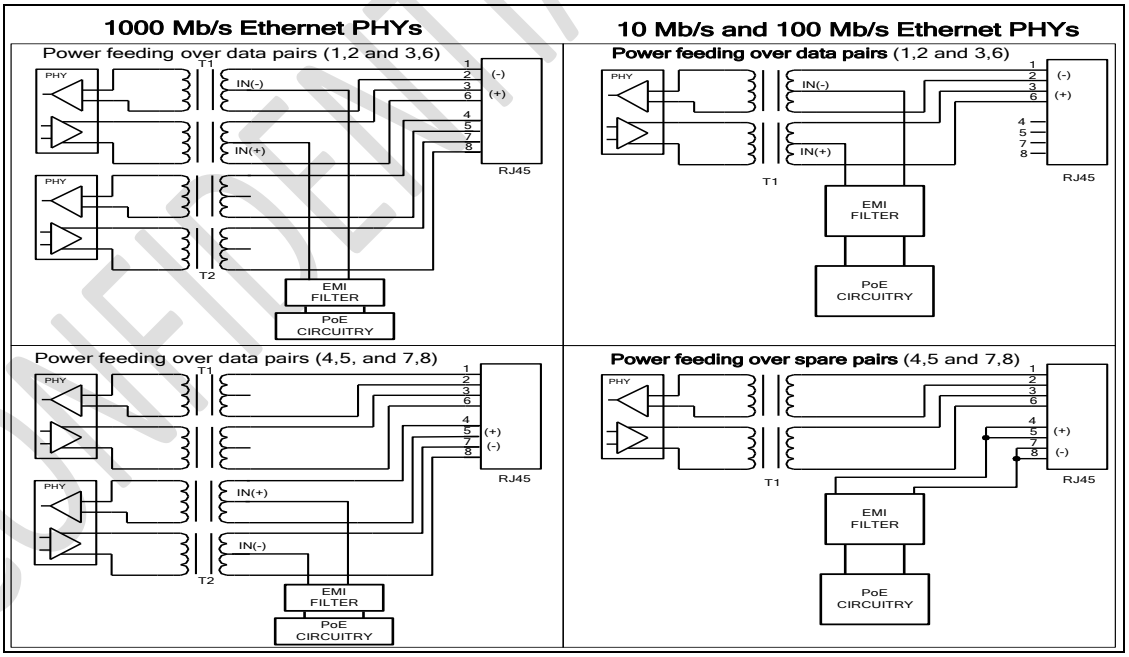


Figure 14: Output Ports Design Details

Layout Guidelines

Microsemi's PD69208AH PoE Manager is designed to simplify the integration of PoE-circuitry, based on the IEEE PoE standards, into switches. The pin-out arrangement has been configured for optimal PCB routing.

Figure 15 describes the various circuits and elements surrounding the PD69208AH PoE Manager in the block diagram. This block diagram includes the following peripheral elements, identified by numbers:

- 5 V Voltage source (VAUX5) (1)
- 3.3 V Voltage source (VAUX3P3) (2)
- Output capacitor used for filtering (4)
- I^2C Bus, I^2C Address Lines (5)
- 1.8 V Voltage source (VAUX1P8) (6)

Note The VAUX5 supply may include an external transistor connected to pin 20, designed to increase current drive for external circuitry. To prevent heat from being transferred to the PD69208AH, place this transistor away from the PoE Managers.

Locating PoE Circuitry in a Switch

To minimize the length of high current traces, as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. The circuit can be fully integrated into the switch PCB, or can be easily placed on top of the switch PCB as a daughter board. Typical integration of PoE modules inside a switch is shown in Figure 17 and Figure 18 .

Ground and Power Planes

Since the PoE solution is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines.

The reference design assumes a four layer board: top, mid1, mid2, bottom. The main planes are Vmain/AGND, DGND.

Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines, as illustrated in Figure 19:

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69208AH (see Figure 20) Thermal Pad Definition and Design).
- The AGND should be located on an external layer.
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds as shown in Figure 20.
- To connect various DGND points and to enable stable impedance to the I^2C bus traces, extend the digital ground (DGND) surface under pins 41 – 56 of the PD69208AH Managers.
- A focal interconnection point for the digital and analog grounds should be located at about the middle of the overlapping section.
- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inversed Schottky diodes near each PoE Manager (Figure 20) between the analog and digital layers. The capacitors form low impedance paths for digital driving signals.
- The power and return (ground) planes for the 48V supply must be designed to carry

the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using a wide copper lands. When implementing the PoE circuitry on a daughter board, the high current does not have to be routed through the daughter board but only the return path as can be seen in Figure 16.

Current Flow through the PoE application

See Figure 16.

The port's DC current flows in an application utilizing a PoE daughter board (DB) as follow:

1. Coming from the switch's power supply positive to the center taps of the line transformer via a mother board wide trace (not through the DB).

2. From the center tap of the line transformer via the switch's RJ45 to the PD side.

3. The return current from the PD flows via the RJ45 and the line transformer to the DB PoE circuitry.

4. From the DB analog ground (AGND) the current flows back to the switch's power supply negative via harness.

Note The positive port's heavy current flows directly to the PD side without going through the PoE Managers on the DB.

Specific Component Placement

Peripheral Components

To minimize heat transfer among various components a gap between them should be maintained. The following are suggested gaps. However, any gap can be used as long as the designer monitors the thermal performance during the design and follows the maximum temperatures allowed at the various components.

- Minimum gap between PD69208AH ICs should be 50mm.
- Minimum gap between PD69208AH to PoE controller should be 30mm.
- Minimum gap between PD69208AH to NPN transistor regulator (if used) should be 50mm.

PD69208AH PoE Manager and Peripherals

- The side of the PoE Manager that includes pins 41 to 56 should face the digital ground (DGND plane). The pins function as communication and control pins for the Manager (connect between the PoE Manager and the PoE controller via isolation circuitry).
- Locate the bypass capacitors for the PoE Manager supply input close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower value capacitor closer to the pin on the same layer and place the higher value capacitor at a more distant location.
- Locate VAUX5 and VAUX3P3 0.1 µF and 4.7 µF filtering capacitors as close as possible to the PoE Manager pins 20 and 22 respectively.

Vmain Capacitors

It's good design to have 3 x 47uF capacitors over Vmain in order to prevent noise and spike events to penetrate into Vmain rail. (Figure 19).

Conductor Routing

General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in general layout guidelines, specifically:

- Conductors that deliver a digital signal are to be routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

Specific Requirements for Clock and Sensitive Signals

Issues that require special design considerations:

- The IREF resistor (connects to pin 24), used for current reference, is directly connected to AGND and pin 24 using the shortest path.
- Carefully route the I^2C communication clock (SCL) line coming from the Host Controller so that it will not disturb other lines. Two ground lines (connected to DGND) could be routed alongside the clock line to isolate it from the rest of the lines.

Port Outputs

For robust design, the ports output traces are to be 45-mil wide so as to handle maximum current and port power.

- However, to obtain a 10° C (maximum) copper rise under 0.6A per port, set the minimum width for traces in accordance with the layer location and copper thickness:
- For two ounce copper, external layer: 15 mils
- For two ounce copper, internal layer: 20 mils
- For one ounce copper, external layer: 25 mils
- For one ounce copper, internal layer: 30 mils
- For 1/2 ounce copper, external layer: 30 mils
- For 1/2 ounce copper, internal layer: 55 mils (20° C copper rise)
- The ports output traces must be short and parallel to each other, to reduce RFI pickup and to keep the series resistance low.
- The PoE ports outputs must be connected to the switch's pulse transformers as shown in Figure 14. The common mode choke and 'Bob-Smith' termination (resistor-capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is to be located as close as possible to the pulse transformer.

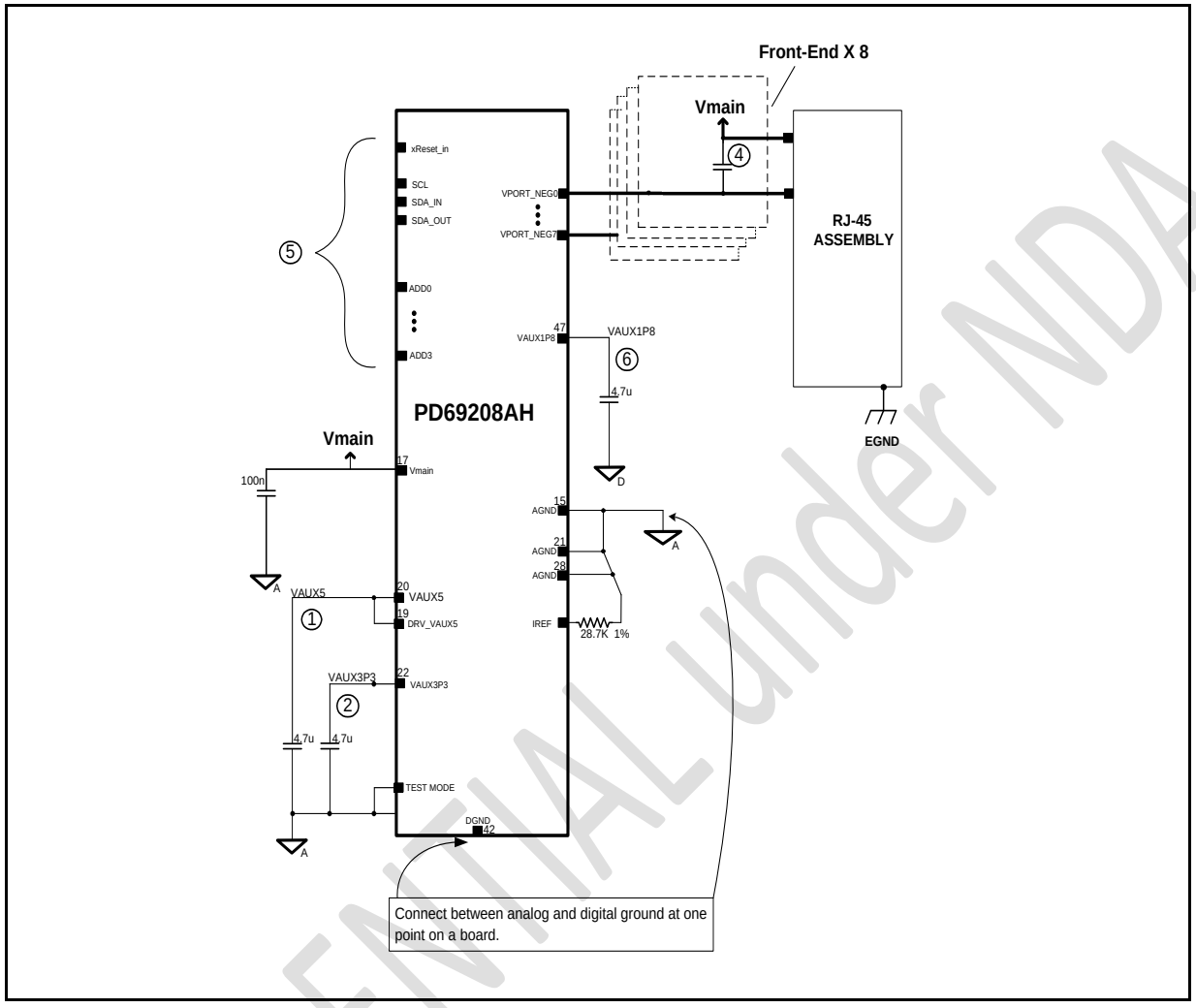


Figure 15: Component Identification for PD69208AH Circuitry

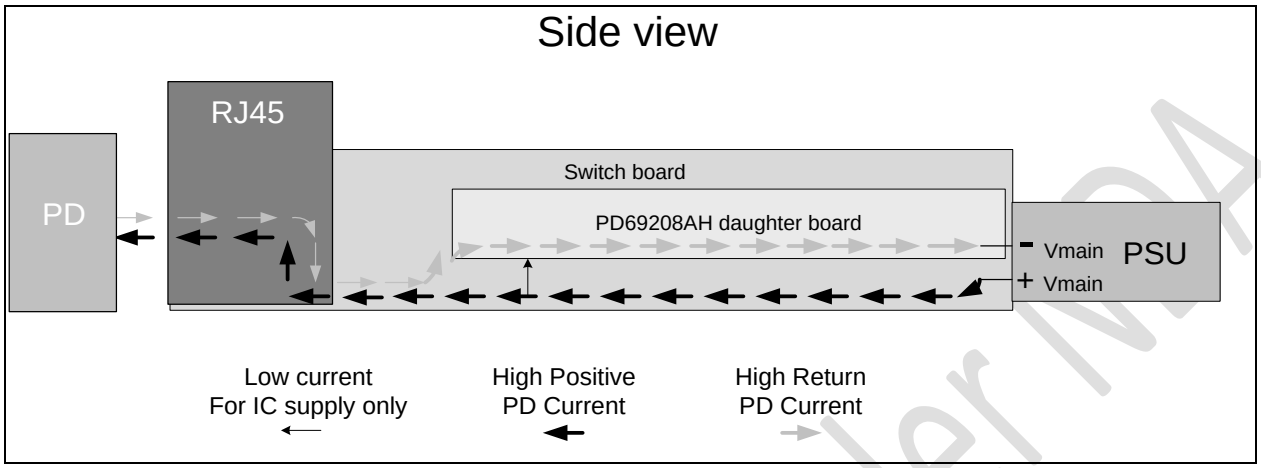


Figure 16: Component Identification for PD69208AH Circuitry

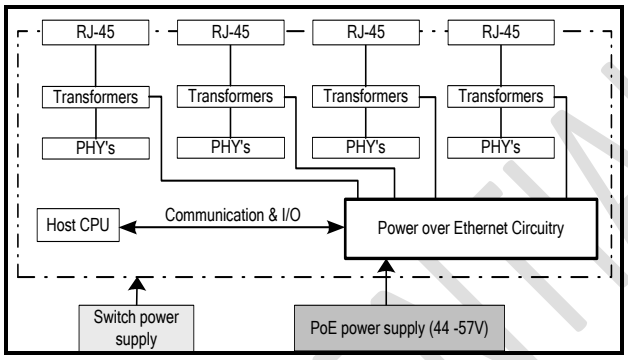


Figure 17: Block Diagram - PoE Circuitry Inside the Switch

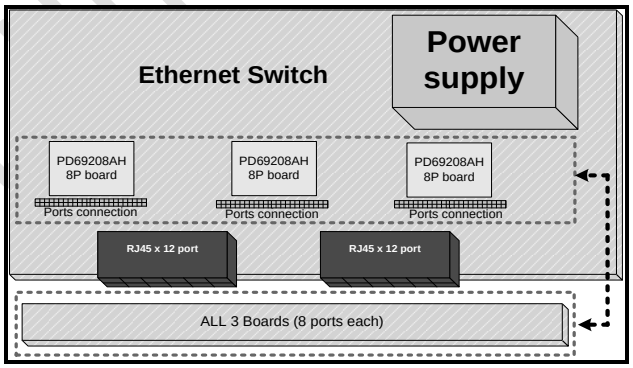


Figure 18: PoE DB Circuitry Inside the Switch

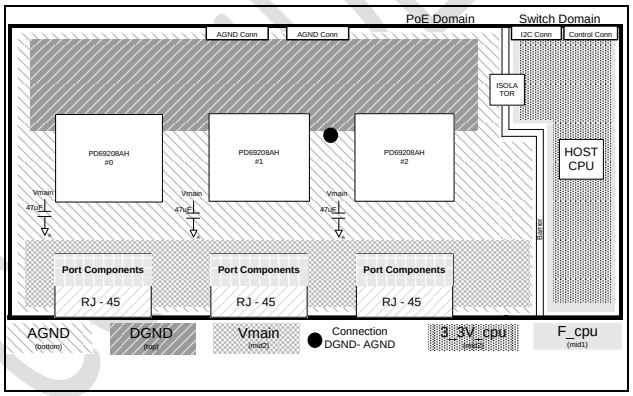


Figure 19: Ground and Power Planes

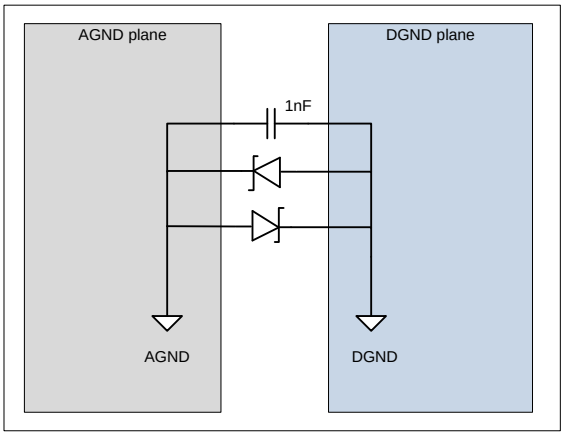


Figure 20: Grounding scheme

Thermal Pad Definition and Design

The PD69208AH utilizes a thermal dissipation exposed pad in a 56-pin 8 x 8 mm QFN package. The package is molded in such a way that the lead frame is exposed at the bottom surface of the package.

Direct soldering of the exposed pad to a copper land provides an efficient thermal path. In multilayer board designs, a matrix of 6x6 vias thermally connects the exposed pad to the AGND copper planes.

Requirements

The PCB design should consider the exposed pad of the PD69208AH. This pad is used for thermal cooling of the package. Basically, the PCB should be designed as shown in Figure 22 - Figure 25.

In these figures the PD69208AH pad is soldered to a dedicated area on the PCB. This contact area is composed of a 36 vias array, each penetrating and thermally connecting to large ground areas in the PCB at various planes, providing efficient heat dissipation.

To ensure optimum thermal transfer through the thermal vias to internal planes or to the bottom side of the PCB, the vias system **should not be used** as used in web construction techniques. Web construction for PCB vias is a standard technique used to facilitate soldering, by designing the via to achieve high thermal resistance. This is not desirable for heat dissipation from the PD69208AH package. It is recommended that vias used under the PD69208AH package be internally connected to the planes, using continuous connection surrounding the whole diameter.

Thermal Pad Design

The PD69208AH exposed pad is a metal substrate on the bottom of the package. The attachment process for the exposed pad package is equivalent to standard surface mount packages.

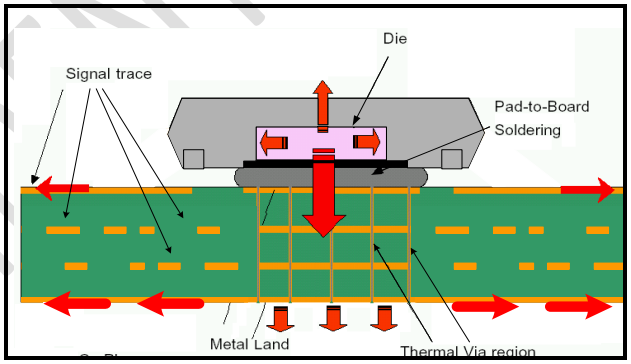


Figure 21: Heat Dissipation in PC

See Figure 22 and Figure 23 (CS & PS) for a design layout of the recommended contact pad.

For proper heat dissipation, the following footprint / layout guidelines must be followed:

- All thermal vias are to be connected to the AGND area under the PD69208AH

- Via diameter should be approximately 0.3 mm with one ounce copper barrel plating. Solder flow into the vias from the component side can result in voids during the solder process and this must be avoided.
- If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste, filling those vias to avoid the above mentioned voids. Figure 24 and Figure 25 show the associated, solder printing masks (CS & PS). The solder mask openings are lined-up in respect to the 6 x 6 thermal via array. Since large solder printing mask openings may result in poor release, the opening should be subdivided as shown in these figures.
- For a nominal package standoff of 0.1 mm, a solder mask stencil thickness of 5 mils should be considered.

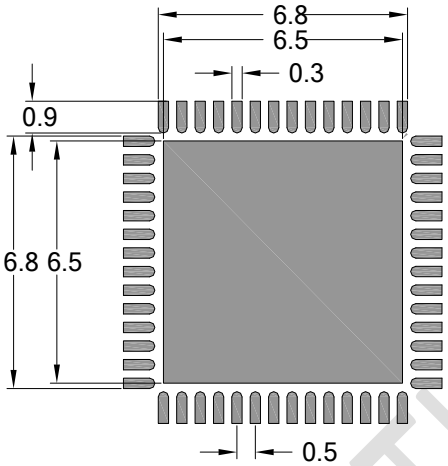


Figure 22: Thermal Pad Array Footprint (CS)

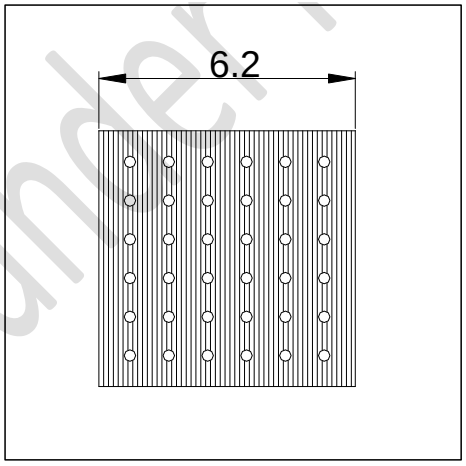


Figure 23: Thermal Pad Array Footprint (PS)

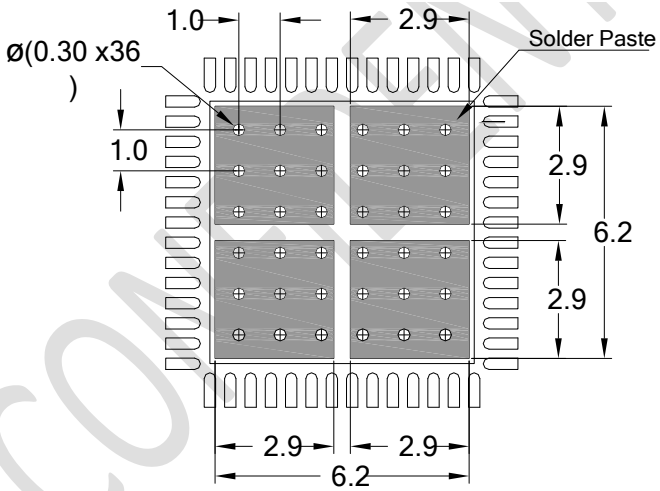


Figure 24: Top Solder Printing Mask (CS)

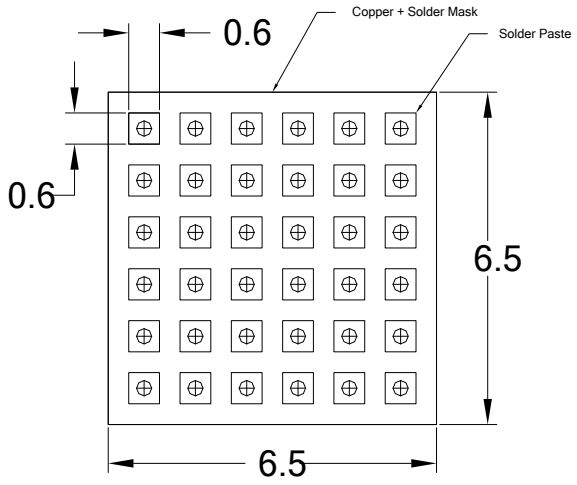
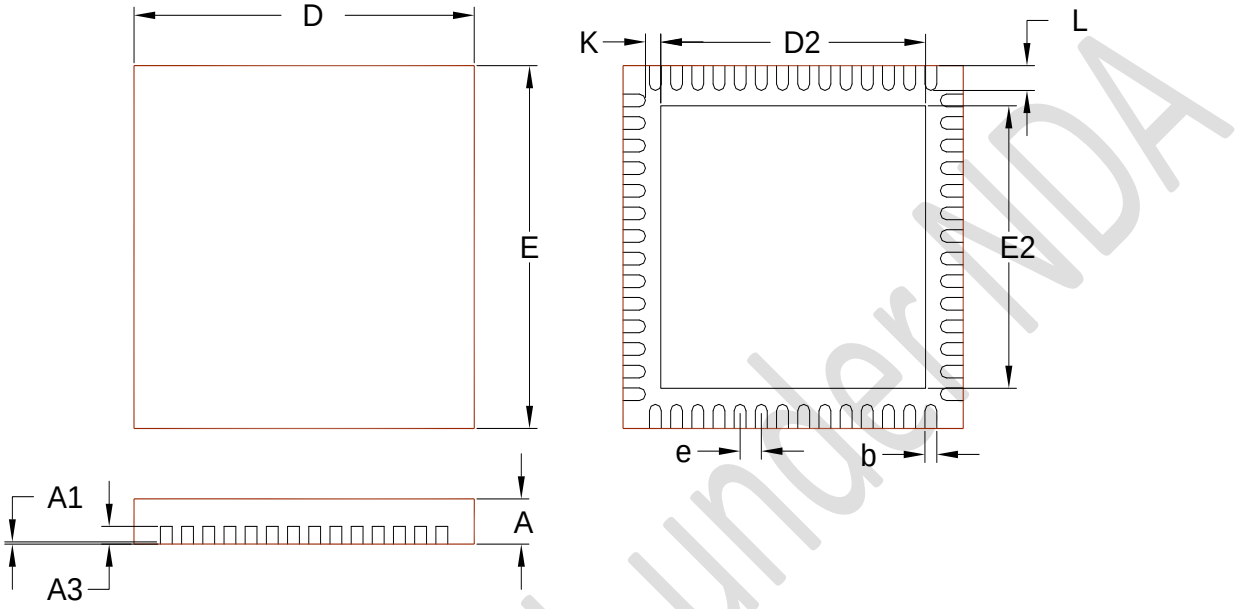


Figure 25: Bottom Solder Printing Mask (PS)

All dimensions are in mm.



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Figure 26: Package Outline Drawing 56 Pin QFN 8x8 mm

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

Revision History

Revision Level / Date	Para. Affected	Description
0.1 5 Jun 2014	-	Initial Release
0.2 25 July 2015	-	Adding notes for 5V regulator and thermal effects.
0.3 10 Nov 2015	-	Update figure 3 for internal connection, using only pin 22.

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