

**UG0678**  
**User Guide**  
**Sequence Controller v4.1**



**Power Matters.™**

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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Added the IP version to the document title.
- Removed g\_STD\_IO\_WIDTH configuration parameter from section [Configuration Parameters](#), page 5.

## 1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

## 2 Introduction

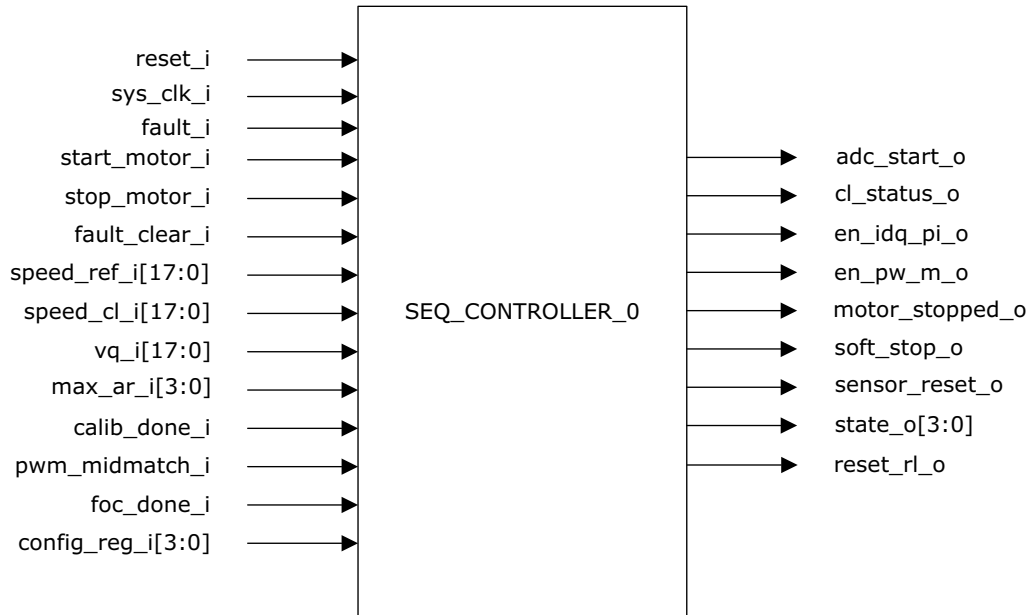
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Implementation of field oriented control (FOC) of AC motor needs an intelligent state machine (FSM) apart from the transformations and closed loop control. It is useful to have all the state transitions managed in a single IP module. The Sequence Controller IP manages the starting, stopping, fault, and fault clear operations through FSM. It also manages the transition from closed loop to open loop and vice versa. It acts as a master block that controls all other IPs involved in FOC. The sequence controller triggers the ADC sampling and conversion, enables and disables the PWM based on the motor operating state and also enables and disables current and speed PI controllers.

## 3 Hardware Implementation

The following figure shows the block diagram of sequence controller.

**Figure 1 • System-Level Block Diagram of Sequence Controller**



The `start_motor_i` and `stop_motor_i` signals are used to trigger motor starting and stopping operations. The `speed_ref_i` input is the motor reference speed, while the `speed_cl_i` input is the threshold motor speed at which the `cl_status_o` is asserted. This signal is asserted, as long as the reference speed is equal to or above the threshold speed. The `vq_i` input is the  $I_q$  PI output and is used in checking for rotor lock condition. If a rotor lock is detected, the motor is restarted from zero speed. The number of times the motor is restarted before entering FAULT state is specified by the `max_ar_i` state. The `calib_done_i` signal must be asserted (level high), when predetermined ADC samples have been accumulated for offset computation.

The `pwm_midmatch_i` signal is an active high pulse of one system clock cycle width which is asserted periodically at the rate of the PWM frequency. The `foc_done_i` signal must be asserted (active high pulse with one system clock cycle delay) when all the FOC loop computations are complete. The `adc_start_o` provides the start conversion pulse (rising edge) for an ADC interface block. The `en_idq_pi_o` signal is used to enable the current PI controller(s). The `en_pwm_o` is used to enable the PWM generation block. The `motor_stopped_o` signal (level high) can be used to clear accumulators or buffers in the design. The `sensor_reset_o` signal is used to reset and initiate sensor calibration.



## 3.1 Inputs and Outputs

The following table lists the input and output ports of sequence controller.

**Table 1 • Inputs and Outputs of Sequence Controller**

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design.
sys_clk_i	Input	System clock.
fault_i	Input	Active high level indicates fault occurrence and forces the FSM to Fault state where motor is stopped. It remains in Fault state unless cleared through fault_clear.
start_motor_i	Input	Rising edge on the signal triggers the FSM to start the motor.
stop_motor_i	Input	Active high level on the signal triggers the FSM to go to Stop state and the motor is stopped.
fault_clear_i	Input	Rising edge in this signal clears fault if fault_i is 0 and FSM is released from Fault state to Idle state.
calib_done_i	Input	Active high level triggered signal to indicate ADC offset calculation done.
pwm_midmatch_i	Input	Periodic active high pulse (1 clock cycle width) that are used to trigger ADC and FOC loop.
foc_done_i	Input	Active high pulse (1 clock cycle width) indicating completion of FOC loop computations.
speed_ref_i	Input	Motor speed reference input.
speed_cl_i	Input	Threshold speed value above which the motor operates in closed loop. Open loop angle is used if speed is below threshold.
vq_i	Input	Q-axis voltage (IQ PI Output).
max_ar_i	Input	Maximum number of auto-restarts before fault condition is asserted.
config_reg_i	Input	Configuration register. config_reg_i(3): Soft Stop – When 1, enabled; When 0, disabled. config_reg_i(2): Startup Mode – When 1, C/f; When 0, V/f. config_reg_i(1): Sensor calibration (calibrates sensor to angle 0). config_reg_i(0): Auto restart (when rotor slips) - When 1, enabled; When 0, disabled.
adc_start_o	Output	ADC start signal (active high pulse).
cl_status_o	Output	Indicates if motor is in closed loop (active high level) or open loop.
en_idq_pi_o	Output	Enable signal for current PI controllers.
en_pwm_o	Output	Enable signal for 3 phase PWM block.
motor_stopped_o	Output	Indicates motor stopped/not running (Active high level).
soft_stop_o	Output	Soft Stop signal (Active high level) to rate limiter block.

**Table 1 • Inputs and Outputs of Sequence Controller (continued)**

Signal Name	Direction	Description
sensor_reset_o	Output	Sensor reset signal (active low level) activates sensor calibration.
reset_rl_o	Output	Reset rate limiter signal (active high level).
state_o	Output	Debug signal indicates the FSM state of the sequence controller.

## 3.2 Configuration Parameters

The following table shows the description of the configuration parameter used in the hardware implementation of sequence controller. This is generic parameter and can be varied as per the requirement of the application.

**Table 2 • Configuration Parameters**

Signal Name	Description
g_DEBUG	When 0, supports synthesis When 1, supports simulation

## 3.3 Resource Utilization

Sequence controller is implemented on the SmartFusion<sup>®</sup>2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO<sup>®</sup>2 devices. The following table lists the resource utilization report after synthesis.

**Table 3 • Resource Utilization Report of Sequence Controller Block**

Cell Usage	Count
Sequential elements	50
Combinational logic	197
MACC	0
RAM1kx18	0
RAM64x18	0