TID and SEE characterization of Microsemi's 4th generation radiation tolerant RTG4 flash-based FPGA

Nadia Rezzak, *Member, IEEE*, Jih-Jong Wang, *Member, IEEE*, Durwyn Dsilva, *Member, IEEE*, Narayan Jat

***Abstract*—TID and SEE characterization of Microsemi's 4th generation RTG4 flash-based FPGA is presented. The radiation performance of RTG4 is compared to SmartFusion2, Microsemi's 4th generation commercial flash-based FPGA.**

I. INTRODUCTION

RTG4 is Microsemi's 4th generation family of radiation tolerant flash-based field programmable gate arrays (FPGAs). RTG4 FPGAs are fabricated in UMC 65 nm technology, featuring a non-volatile, reprogrammable flash-based FPGA fabric with proven high reliability. Compared to the commercial SmartFusion2 SoC FPGA family, RTG4 FPGAs comprise multiple functional blocks with radiation hardening by design, such as radiation hardened PLLs, DSP blocks, fabric SRAM with optional error detection and correction (EDAC) encoding, self-corrected triple module redundant (STMR) flip-flops, and many other hardened functional blocks, as shown in Fig. 1.

Flash based FPGAs are known to be sensitive to Total Ionizing Dose (TID) [1-3]. The charge pump circuit is one of the most TID-sensitive blocks because it's high voltage operation requires the use of thick oxide MOS devices, which are sensitive to charge trapping. Also, Floating Gate (FG) cells can be affected by TID [4], resulting in threshold voltage shift and consequently bit errors [3]. To address these TID issues Microsemi introduced RTG4 a new radiation tolerant flash-based FPGA, that uses new radiation tolerant thick oxide devices and Push-Pull configuration flash bit cell, while maintaining the flash-based FPGA SEE reliability superiority at the same time [5]. This work covers the TID and SEE performance of the radiation tolerant 65 nm flash-based RTG4 FPGA. The TID and SEE results are presented and compared to SmartFusion2, Microsemi's 4th generation (65 nm) commercial part.

Manuscript received July 10, 2015.

Nadia Rezzak is with Microsemi SoC, 3850 N. 1st Street, San Jose, CA, 95134, USA (phone: 408-643-6063, e-mail: nadia.rezzak@microsemi.con).

Jih-Jong Wang, Durwyn Dsilva and Narayan Jat are with Microsemi SoC, 3850 N. 1st Street, San Jose, CA, 95134, USA.

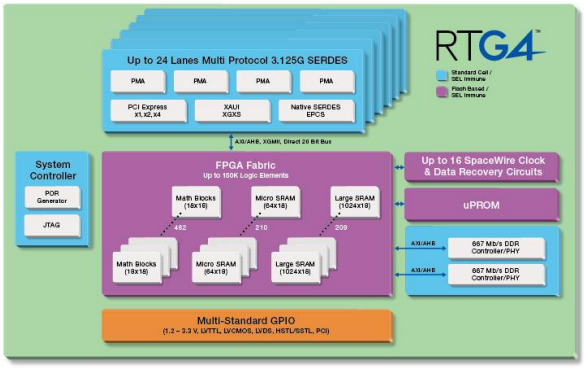


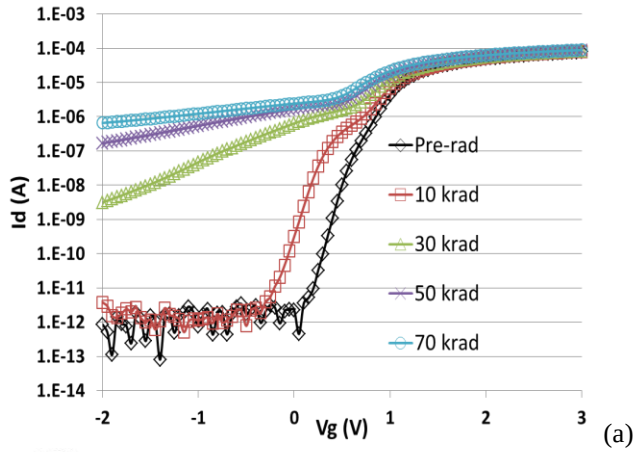
Fig. 1. RTG4 device block diagram.

II. TID RESULTS

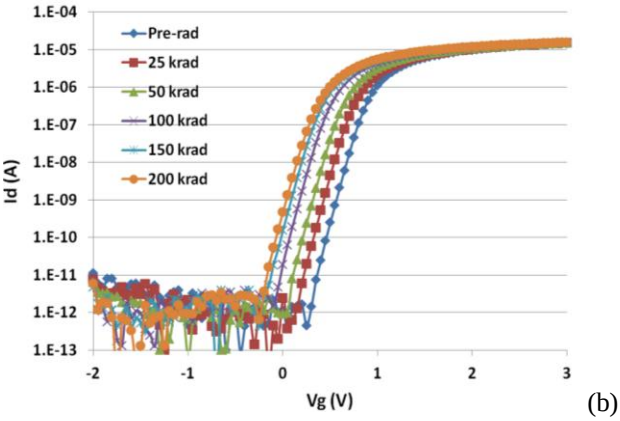
The tested device is the RT4G150 from the RTG4 family. TID testing is performed at three facilities, the Air Force Research Laboratory (AFRL) in Albuquerque, NM, NASA Goddard Space Flight Center in Greenbelt, MD, and Vanderbilt University in Nashville, TN, using both gamma ray and x-ray.

The TID effects in the flash-based FPGAs were shown first as radiation-induced charge loss in the floating gate [1-4] and second as radiation induced leakage currents and shifts in the threshold voltage of the thick oxide devices (HV/MV CMOS transistors) [3], used in the programming control circuits.

The high voltage and medium voltage NMOS thick oxide devices have been shown to contribute to the increase in the power supply current and propagation delay in SmartFusion2 and previous generation flash-based FPGAs [3]. To address this issue new radiation hardened NMOS high voltage and medium voltage devices are introduced in RTG4, and show negligible radiation induced drain to source leakage current compared to the devices used in SmartFusion2. The I_dV_g characteristics of a high voltage NMOS devices with an effective gate oxide thickness of 290 Å for SmartFusion2 and RTG4 are shown in Figs. 2 (a) and (b), respectively. Similarly the I_dV_g characteristics of a medium voltage NMOS devices with an effective gate oxide thickness of 290 Å for SmartFusion2 and RTG4 are shown in Figs. 3 (a) and (b), respectively.

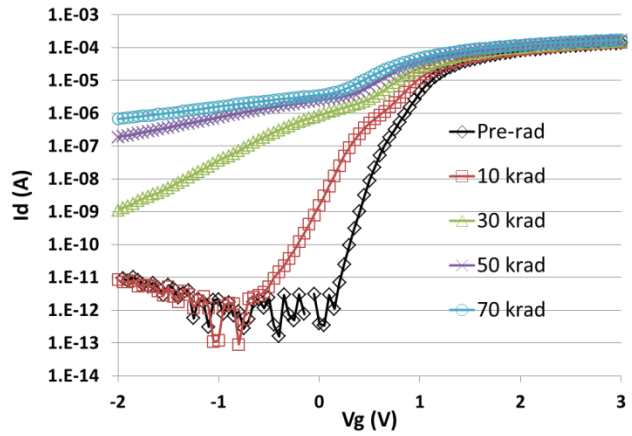


(a)

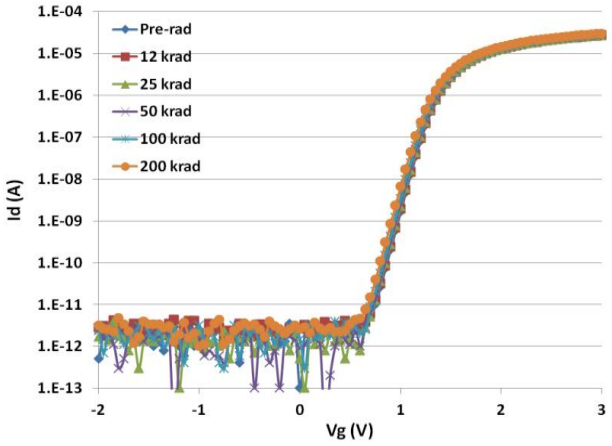


(b)

Fig. 2 (a). The pre and post-irradiation I_dV_g characteristics of a high voltage NMOS device in (a) SmartFusion2 and (b) RTG4.



(a)



(b)

Fig. 3 (a). The pre and post-irradiation I_dV_g characteristics of a medium voltage NMOS device in (a) SmartFusion2 and (b) RTG4.

In addition to the thick gate oxide devices, the sense-switch flash configuration cell used in SmartFusion2, also contributes to the propagation delay degradation [3]. In the sense-switch flash cell configuration, since the switch transistor in the data path is directly coupled to the floating gate, as shown in Fig. 4, TID induced charge accumulation in the floating gate causes the threshold voltage of the pass (switch) transistor to change. To mitigate this problem a new Push-Pull configuration flash cell is introduced in RTG4, where the data signal doesn't pass directly through the flash transistor. The pass (switch) transistor is held in the "on/off" by a pair of flash transistors in Push-Pull configuration as shown in Fig. 4.

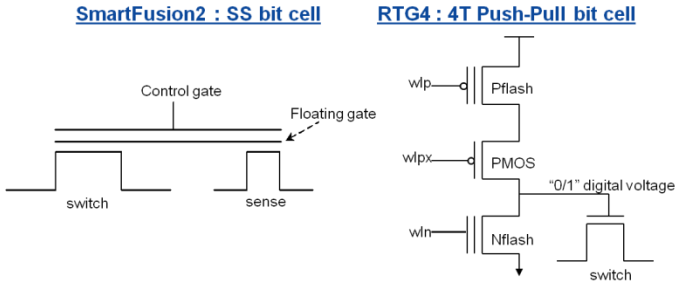


Fig. 4. RTG4 4T Push-Pull bit cell comparison with SmartFusion2 sense-switch bit cell.

The RTG4 Push-Pull cell is significantly more radiation tolerant, any change in the threshold voltage of the Nflash and Pflash transistors caused by accumulation of charge in their floating gates, does not result in a change in the state of the Push-Pull pair (and consequently the state of the switch device) until the threshold voltage degrades past the switching threshold of the transistors, which is at a TID level considerably higher than 100 krad. Fig. 5 shows the I_dV_g characteristics of a Nflash device in programmed state, where the V_T shifts with total dose and negligible drain to source leakage current is observed. The V_T shift versus dose of both Nflash and Pflash devices in programmed and erase sates are summarized in Fig. 6, along with the analytical model fitting to the experimental data. The model predicts the immediate TID effects on the threshold voltage of floating gate devices. The fit curves in Fig. 6 are obtained using the following radiation model [3], [6]:

$$V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)] \cdot \mathrm{Exp}(-A\,\gamma)$$

Where γ is the total ionizing dose, $V_T(0)$ is the pre-irradiation V_T, $V_T(\infty)$ is the saturation V_T, and A is a physical constant [3], [6].

Using the Push-Pull cell and the radiation hardened thick gate oxide devices result in negligible propagation delay degradation in RTG4. Fig. 7 (a) shows less than 1% degradation of the propagation delay in RTG4 after ~160 krad, whereas in SmartFusion2, the propagation delay reaches 10% degradation after ~25 krad as shown in Fig. 7 (b).

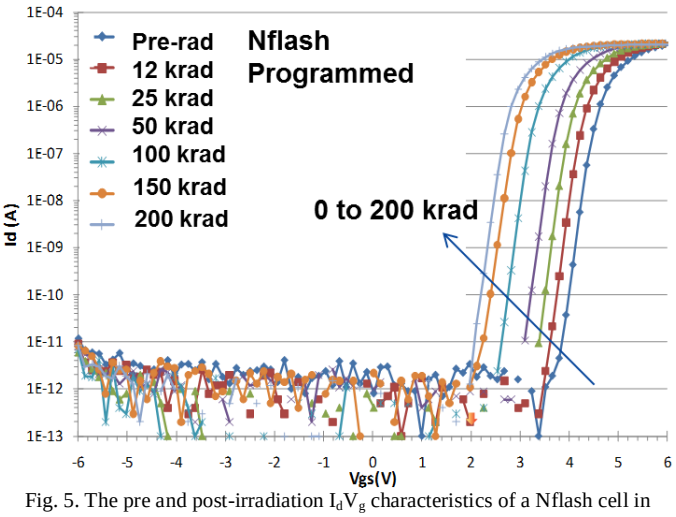


Fig. 5. The pre and post-irradiation I_dV_g characteristics of a Nflash cell in programmed state.

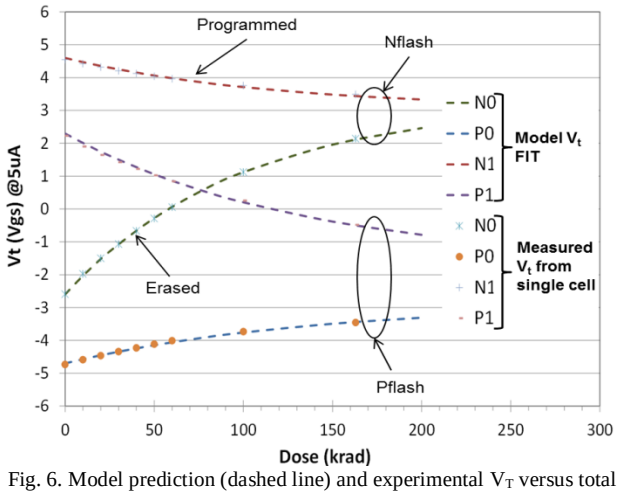
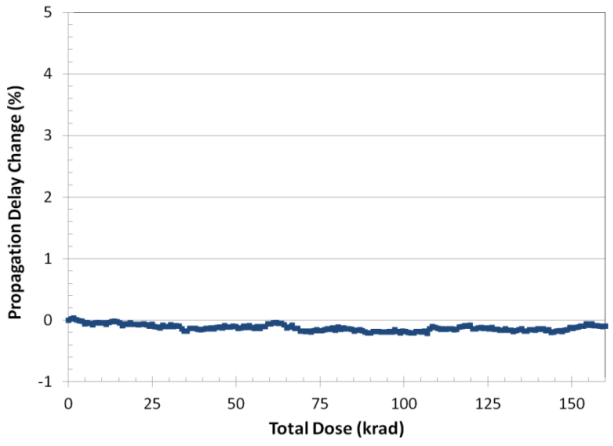
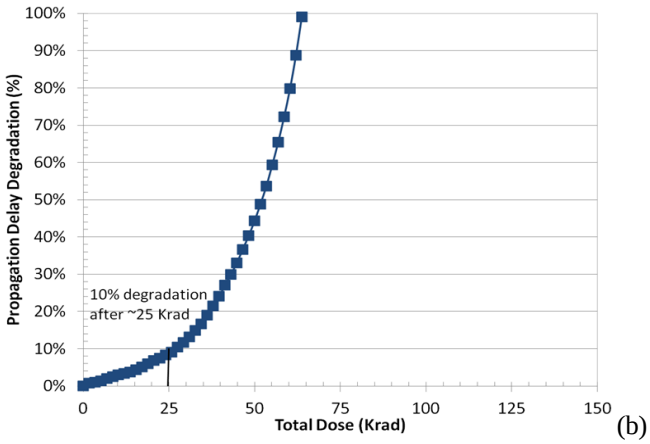


Fig. 6. Model prediction (dashed line) and experimental V_T versus total dose for Nflash and Pflash cells in erased and programmed states.



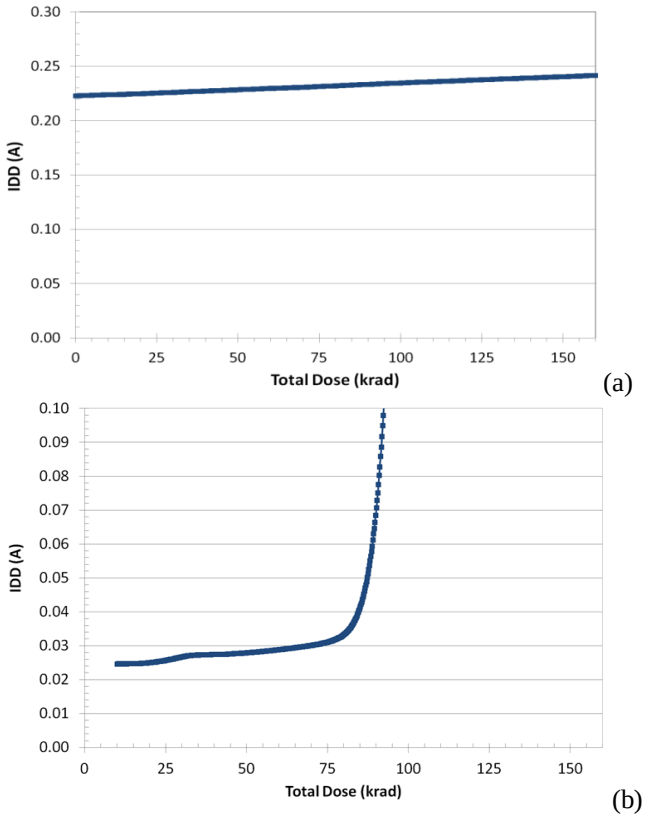
(a)



(b)

Fig. 7. Percentage of propagation delay degradation versus TID in (a) RTG4 and (b) SmartFusion2.

The core power supply current is monitored during irradiation, and a 10% increase in the RTG4 core power supply current after ~160 krad is observed, whereas for SmartFusion2 the core power current significantly increases after ~80 krad as shown in Fig. 8. The PLL, I/O bank and charge pump (programming circuit) power supply currents are also monitored and a negligible increase in the current is observed as shown in Fig. 9.



(a)

(b)

Fig. 8. The core power supply current (IDD) versus TID in (a) RTG4 and (b) SmartFusion2.

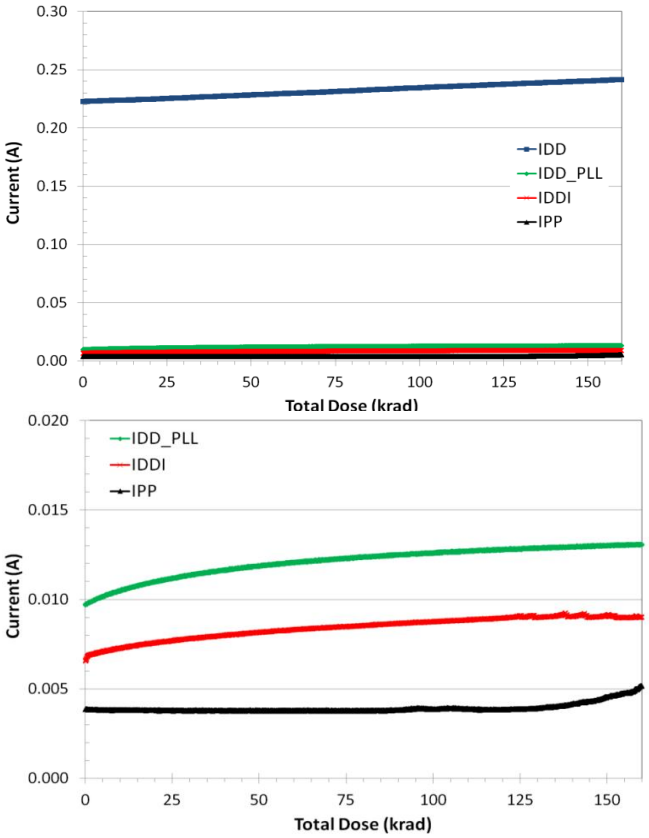


Fig. 9. (a) The core (IDD), PLL (IDD_PLL), I/O bank (IDDI) and charge pump (IPP) power supply currents versus TID in RTG4 and (b) zoomed in view of the RTG4 PLL, I/O bank and charge pump power supply currents.

III. SEE RESULTS

The heavy ion testing of the RT4G150 is conducted at Lawrence Berkley National Laboratory (LBNL) in Berkeley, CA, using their 16 MeV/nucleon cocktail and Texas A&M University (TAMU) in College Station, TX, using their 15 MeV beam.

1. Configuration Upset and SEL

Functionality of the FPGA was continuously monitored during radiation exposure and no configuration upsets were detected in the 10 parts tested at LBNL and TAMU up to LET = 103 MeV.cm^2/mg, as shown in Table 1. Therefore RTG4 flash configuration cell is SEU immune. Two parameters contribute to the RTG4 Push-Pull cell SEU immunity; first, Microsemi's FPGA flash cells are larger than standard commercial flash memory cells, which makes Microsemi's FPGA inherently SEU immune [5]. Second, compared to SmartFusion2, the switch transistor in the RTG4 Push-Pull data path is indirectly coupled to the floating gate as shown in Fig. 4. Therefore for a heavy ion to cause a configuration upset, it would need to charge or discharge the floating gate in one of the two flash transistors significantly to change the state of the switch control gate.

LET (MeV.cm^2/mg)	Configuration Upset	Total fluence (ions/cm^2)
1.16 to 103	0	$5.02\text{x}10^8$

Table 1. RTG4 Flash Configuration Cell Upset

Single Event Latchup testing is performed at room temperature and 100 ºC, with nominal+5% bias. The results show no SEL and are summarized in Table 2.

Temperature	LET	SEL	Fluence
Room Temp	9.8	0	$2.00\text{x}10^7$
	13.74	0	$2.00\text{x}10^7$
	26.9	0	$6.51\text{x}10^7$
	31.06	0	$5.00\text{x}10^7$
	89	0	$5.00\text{x}10^6$
	103	0	$2.60\text{x}10^7$
100 ºC	58	0	$4.00\text{x}10^7$
	89	0	$1.43\text{x}10^7$
	103	0	$7.58\text{x}10^7$

Table 2. SEL summary results at room temperature and 100 ºC.

2. STMR FF results

The Flip-flop in RTG4 is a self-corrected triple module redundant FF (STMR FF). The operation conditions under test are checkerboard data-pattern running at a clock of 1 and 10 MHz, and static all "1" and "0" patterns. Preliminary results show an upset rate $<1\times10^{-10}$ upset/bit-day versus 1.76×10^{-7} upset/bit-day for SmartFusion2 [5], proving the efficacy of the radiation hardened by design RTG4 STMRFF. The STMRFF shows an error rate at least 3 orders of magnitude better than SmartFusion2 FF's error rate.

3. Fabric SBU SRAM results

RTG4 devices consist of rows of SRAM blocks embedded in the RTG4's FPGA fabric for use in the customers' designs. There are two types of SRAMs in the fabric, the Large SRAM (LSRAM) and micro SRAM (µSRAM). Both have built-in EDAC with Single Error Correction Double Error Detection (SECDED) code. For this test EDAC is not enabled to compare the results with SmartFusion2. The LSRAM can store up to 24.5 Kbit versus 1.5 Kbit for the µSRAM; however the LSRAM bit cell area is about half the size of the bit cell area of the µSRAM. The bit cell areas are 4.07 um^2 and 7.74 um^2 for the LSRAM and µSRAM respectively.

Figs. 10 and 11 show the heavy ion single bit upset (SBU) cross section and weibull fitting curve of the µSRAM and LSRAM respectively. Both SRAM cells have similar LET threshold of 0.85 MeV.cm^2/mg. The saturated cross section is 4.5×10^{-9} cm^2/bit for the LSRAM and 8.0×10^{-9} cm^2/bit for the µSRAM. The µSRAM cross section is almost twice the LSRAM cross section, due the µSRAM bit cell area being approximately twice the size of the LSRAM bit cell area. Using the weibull fitting parameters and Crème 96, the upset rate is calculated, for solar minimum condition (cosmic ray maximum) and geosynchronous orbit with 100 mils aluminum shielding. The upset rates are 3.33×10^{-8} upset/bit-day and 4.03×10^{-8} upset/bit-day for the RTG4 µSRAM and LSRAM respectively. The upset rates are close to the SmartFusion2 upset rate reported in [5], since the fabric SRAM bit cells are the same in RTG4 and SmartFusion2.

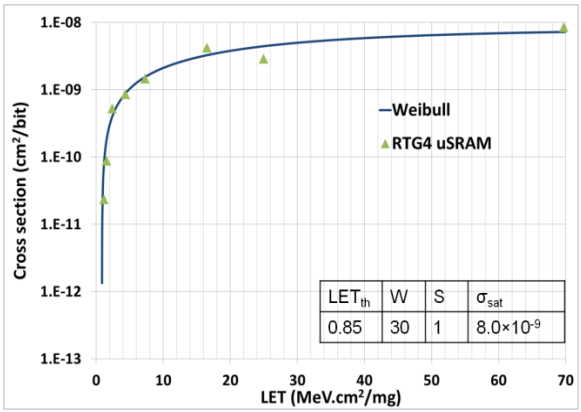


Fig. 10. The µSRAM heavy ion SEU cross section as a function of LET, and the weibull fitting curve.

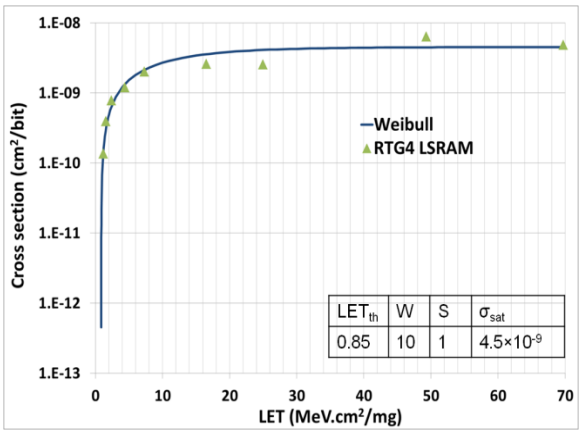


Fig. 11. The LSRAM heavy ion SEU cross section as a function of LET, and the weibull fitting curve.

4. SEU LSRAM 3D-TCAD simulation

3D TCAD simulations of the LSRAM using RCI tools are performed to compare and calibrate with beam test results. The 3D structure shown in Fig. 12 includes three LSRAM cells and "source-ties" to account for the SRAM's neighboring cells present in the real layout. The "source-ties" are additional junctions tied to V_{dd} and ground, to accurately simulate charge collection. The dashed lines represent the targeted LSRAM cell boundary.

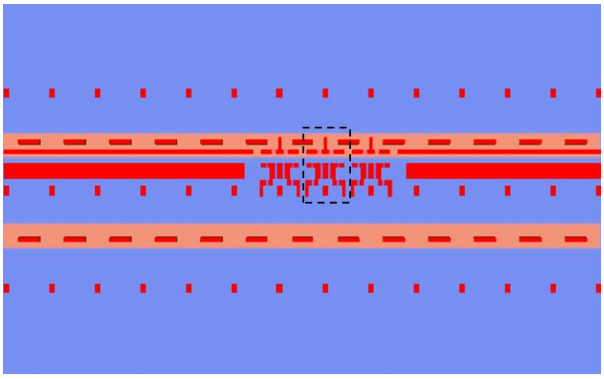


Fig. 12. The simulated 3D TCAD structure including three LSRAM cells and a simplification of the SRAMs surrounding cells (represented by added "source-ties") to emulate the effect of the SRAM's surrounding cells present in the real layout; the dashed lines represent the targeted LSRAM cell boundary.

The results show that the SEU rate of "1", "0" or checkerboard pattern is the same because of the SRAM circuit design. The two cross-coupled inverters in the SRAM cell are totally symmetrical. Since these two nodes are physically equivalent, the critical energy deposition for switching the bit is the same for both states.

The simulation results show a good correlation with beam test data especially at lower LET (<20 MeV.cm^2/mg) as shown in Fig. 13, at higher LETs the simulations deviate from testing data (results under investigation). Although the cross sections deviate at higher LET, it doesn't affect error rate prediction, because the LET spectrum in space is dominated by low LET ions. The upset rates using the simulated cross section and beam test data are very close; the beam test data upset rate is 4.03×10^{-8} upset/bit-day versus 4.67×10^{-8} upset/bit-day for the simulations.

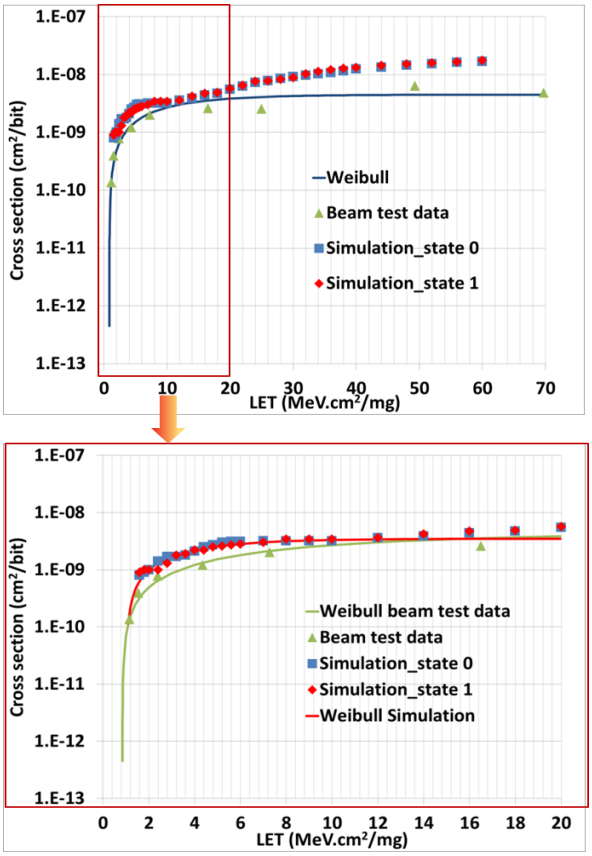


Fig. 13. The heavy ion SEU cross section as a function of LET, comparing beam test data to the simulation results (for state "0" and "1"). The bottom figure is a zoomed in view of the top figure for LET<20 MeV.cm^2/mg.

5. MBU and MCU results

Multiple bit upset (MBU) are mitigated by the interleaving of logical bits in the physical memory blocks in RTG4. Logically adjacent bits are separated by 9 physical bits as shown in Fig. 14, corresponding to a distance of ~16 µm for the LSRAM.

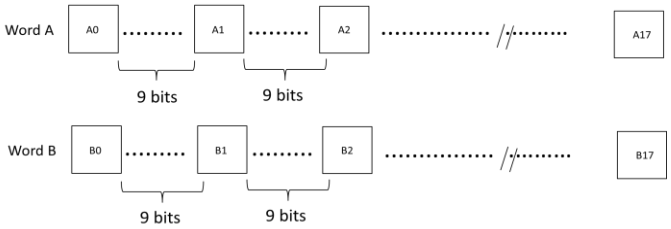


Fig. 14. Logically adjacent bits (bits belonging to the same word) are separated by 9 physical bits in RTG4.

The post-irradiation state of the SRAMs is compared to the "golden" SRAMs pre-irradiation state, where a read back of the SRAM is executed and processed to determine the number of SBU, MBU and multiple cell upset (MCU) count as shown in Fig. 15. The testing is performed at low flux and the refresh period is optimized to allow full read of the memory, therefore the probability of multiple ion strikes in the time it takes to read the memory is negligible.

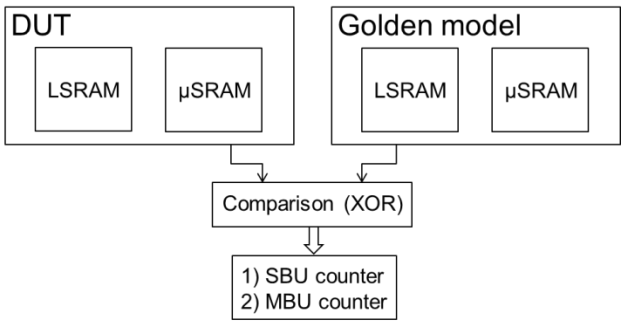


Fig. 15. The fabric SRAM (LSRAM and µSRAM) MBU, SBU and MCU detection.

Zero MBU (multiple bit upset that belong to the same word) are observed with RTG4 built-in interleaving as shown in Table 3. Multiple cell upset (MCU) size 2 to 8, which represent SBU that belong to different words are observed and shown in Figs. 16 and 17, for the LSRAM and µSRAM respectively. Although MCU are observed, they can be corrected with EDAC.

LET (MeV.cm^2/mg)	Total Fluence (ions/cm^2)	Flux (ions/cm^2/s)	MBU
9.8 to 103	1.72x10^8	1x10^4 to 5x10^4	0

Table 3. RTG4 Multi bit Upset summary

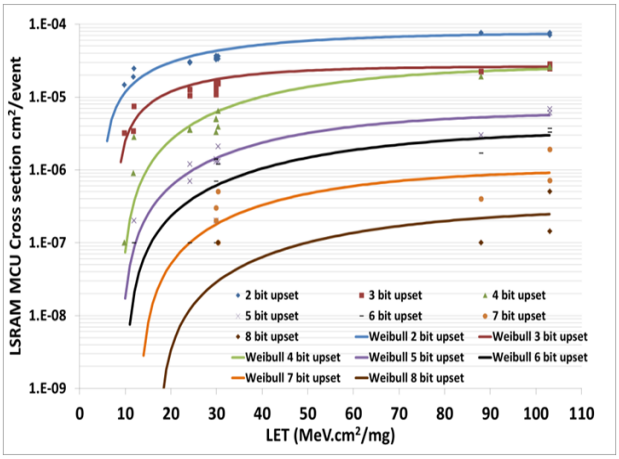


Fig. 16. The LSRAM heavy ion MCU cross section as a function of LET.

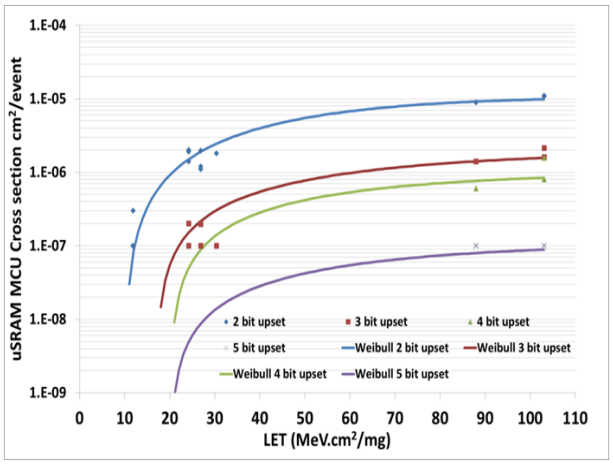


Fig. 17. The µSRAM heavy ion MCU cross section as a function of LET.

IV. CONCLUSION

TID and SEE testing of RTG4 (RT4G150) has been performed. The TID performance of RTG4 shows significant improvement compared to SmartFusion2 and shows a TID tolerance up to 160 krad. RTG4 Push-Pull flash configuration cell is SEU immune, and no SEL is observed at 100 ºC, and LET of 103 MeV.cm^2/mg. STMR FF error rate is at least three orders of magnitude better than SmartFusion2 FF error rate. 3D TCAD simulations allow good error rate prediction. Zero MBU are observed for LSRAM or µSRAM, and MCU are observed but can be corrected with EDAC.

V. REFERENCES

[1] J. J. Wang, S. Samiee, H. S. Chen, C. K. Huang, M. Cheung, J. Borillo, S. N. Sun, B. Cronquist, and J. McCollum, "Total Ionizing Dose Effects on Flash-Based Field Programmable Gate Array," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3759-3766, Dec. 2004.

[2] J. J. Wang, N. Charest, G. Kuganesan, C. K. Huang, M. Yip, H. S. H. Chen, J. Borillo, S. Samiee, F. Dhaoui, A. Khandelwal, J. Sun, S. Rezgui, J. McCollum, and B. Cronquist, "Investigating and modeling total ionizing dose and heavy ion effects in flash-based field programmable gate array," in *Proc. Radiation Effects on Components and Systems Workshop*, Athens, Greece, 2006.

[3] N. Rezzak, J. J. Wang, C. -K Huang, V. Nguyen and G. Bakker, "Total Ionizing Dose Characterization of 65 nm Flash-Based FPGA" *Radiation Effects Data Workshop (REDW), 2014 IEEE*, pp.1-5, 2014.

[4] J. J. Wang et al, "Biased-irradiation characteristics of the floating gate switch in FPGA," in *Proc. IEEE Nuclear and Space Radiation Effects Conf.*, Ponte Vedra, FL, 2006.

[5] N. Rezzak, J. J. Wang, D. Dsilva, C. K. Huang, and S. Varela, "Single Event Effects Characterization in 65 nm Flash-Based FPGA-SOC," *SEE Symposium 2014 Proceedings*.

[6] E. S. Snyder, P. J. McWhorter, T. A. Dellin, and J. D. Sweetman, "Radiation response of floating gate EEPROM memory cells," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2131–2139, Dec. 1989.