Power Matters

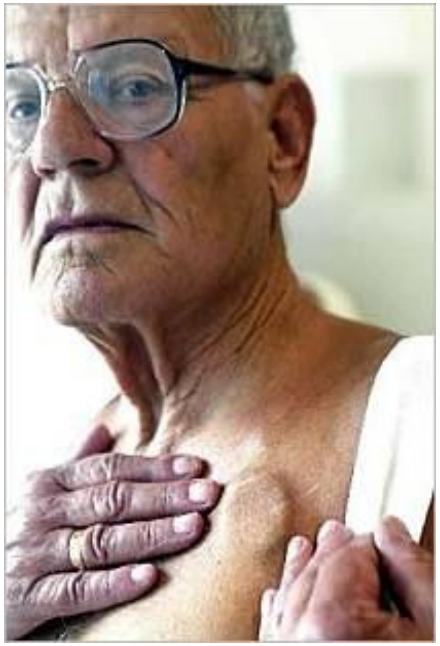
Microsemi

Advanced Packaging for Implantable Devices

Introduction

- Market drivers and the emergence of “hidden” devices
- Technology options
- Getting access to smart phone packaging technology
- Emergence of “hidden” die technology
- Case studies and where next

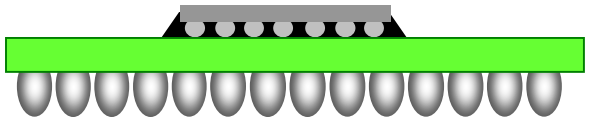
Market Drivers for “Hidden” Devices

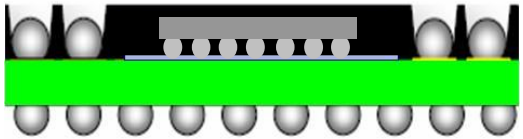


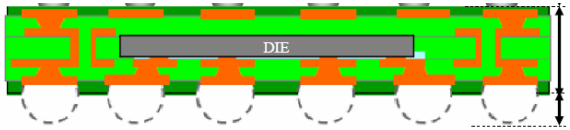
- Miniaturization
  - Patient comfort, aesthetics and wound healing
- Wireless telemetry
  - Remote monitoring and communication
- Low power
  - Additional functions limited by battery life
- Lower cost
  - Needed to increase sales
  - Simplified electronics assembly
  - Only 1 in 9 patients in emerging markets requiring pacemakers receive one
- These drivers are very similar to mobile phones

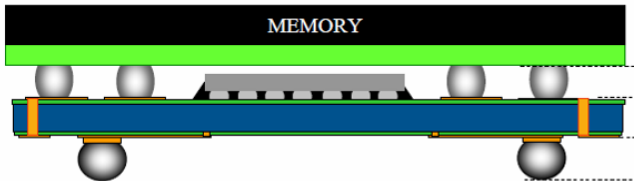
Packaging Technology Options

- Bare die package on package (PoP)
- Molded laser via PoP
- Embedded die in laminate
- FO waver level package (WLP)
- Silicon interposer/substrate
- Through-silicon Vias (TSVs)







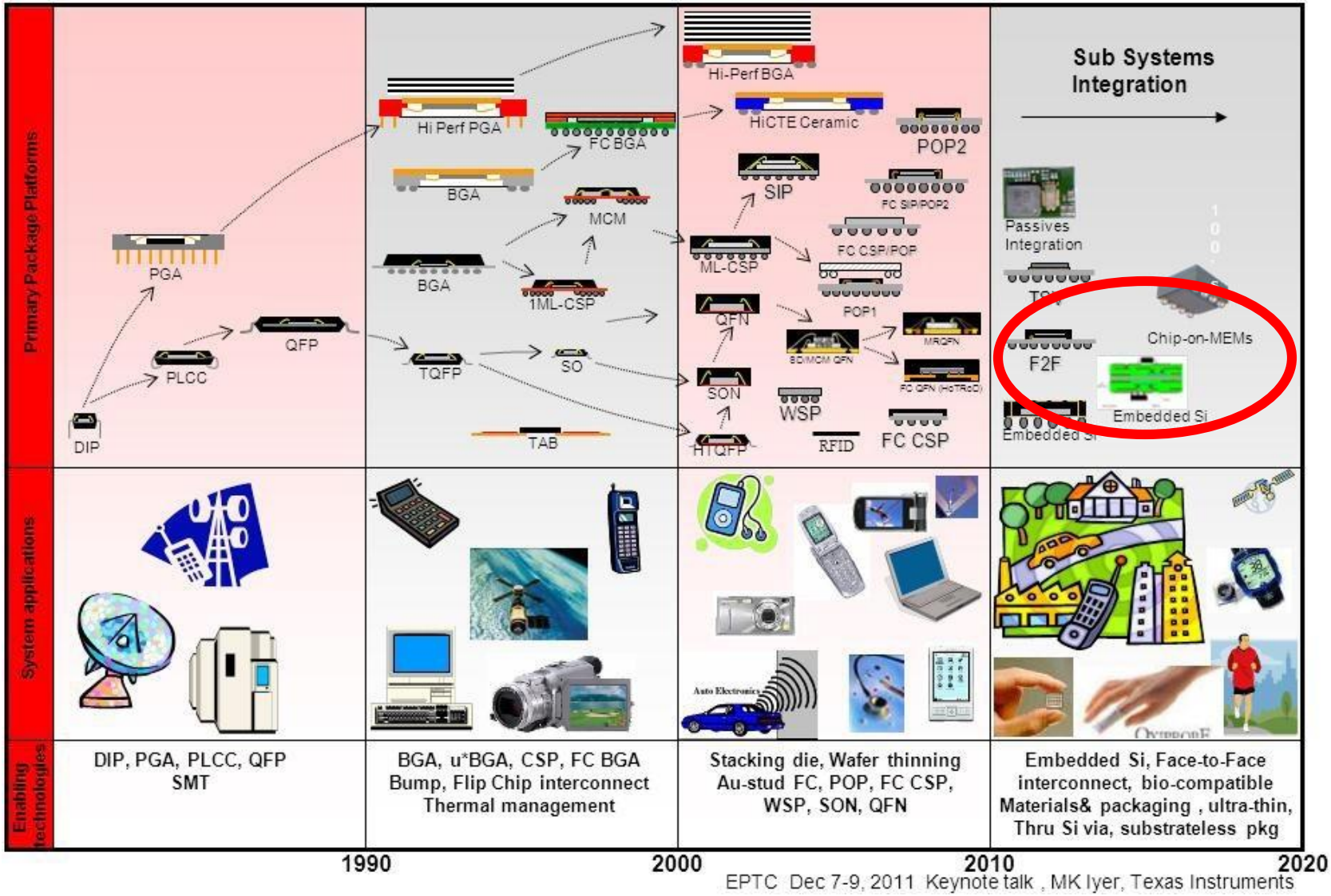


Images courtesy of STC

Getting Access to High Density Die Packaging

- Packaging needs are very similar to mobile phones
  - Mobile market is many times larger
  - Expensive tooling costs and dedicated chip designs are easily justified
- WFO
  - Dedicated designs and volume
- TSVs
  - Requires dedicated chip designs
  - May not be easy to justify in a mid-volume market
- 2.5 and 3D packaging
  - Requires high volume to get access to suppliers
  - Requires dedicated chip designs
  - Not all players want to supply the medical markets
- Getting access to right technology can be difficult

Emergence of Embedded Die Technology

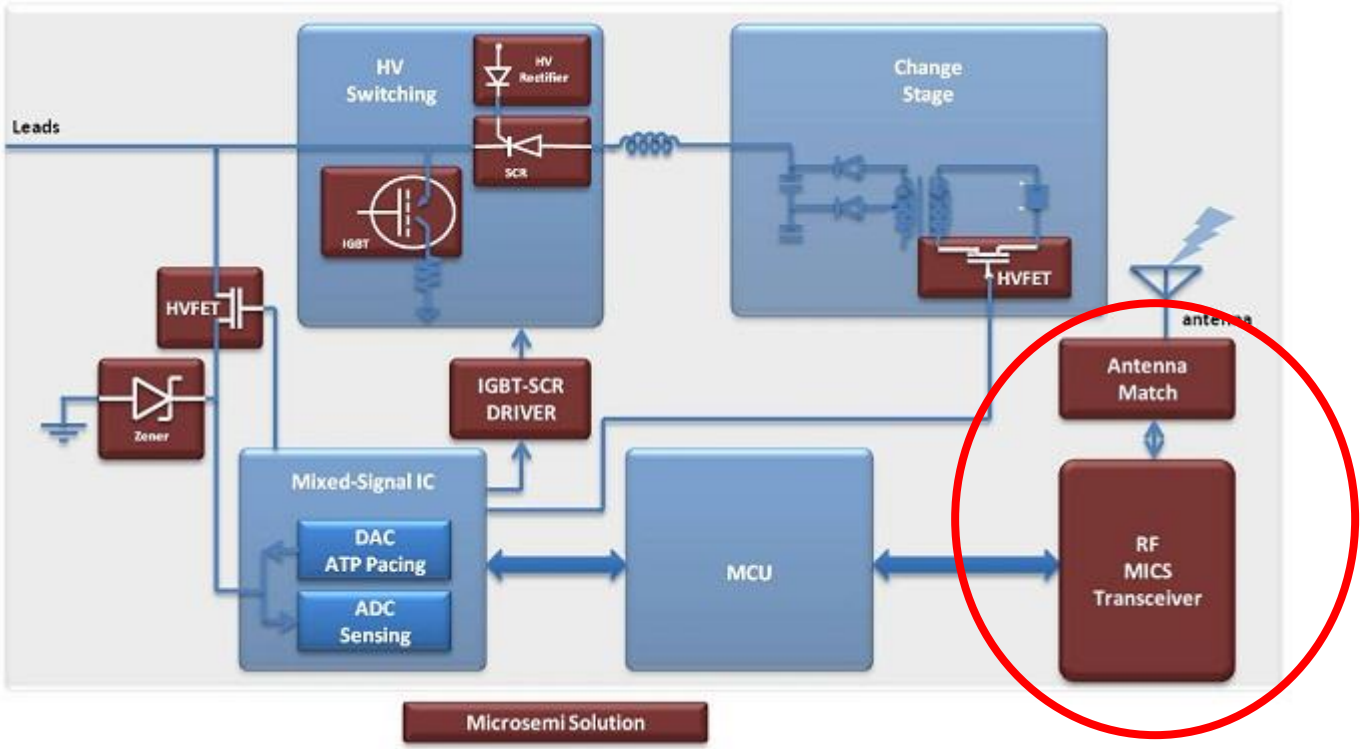


EPTC Dec 7-9, 2011 Keynote talk , MK Iyer, Texas Instruments

Case Study: Radio Module

Case Study: Radio Module

Typical Implantable Cardiac Defibrillator (ICD) Block Diagram

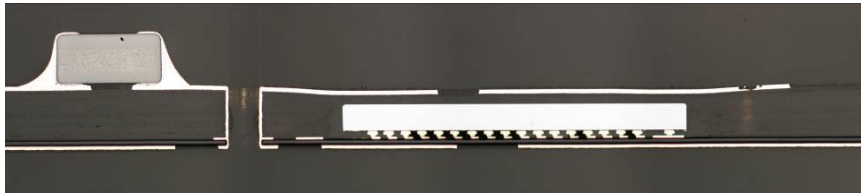


Area of focus – MICS Transceiver Circuit

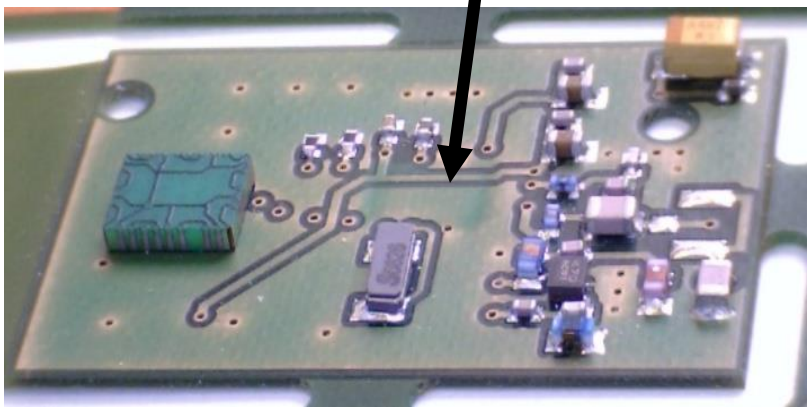
Case Study: Radio Module

- SHIFT – industrial/academic pioneering collaboration for embedded die

- Demonstrated
  - Reliability of embedded die
  - Potential for miniaturization
  - Design rules

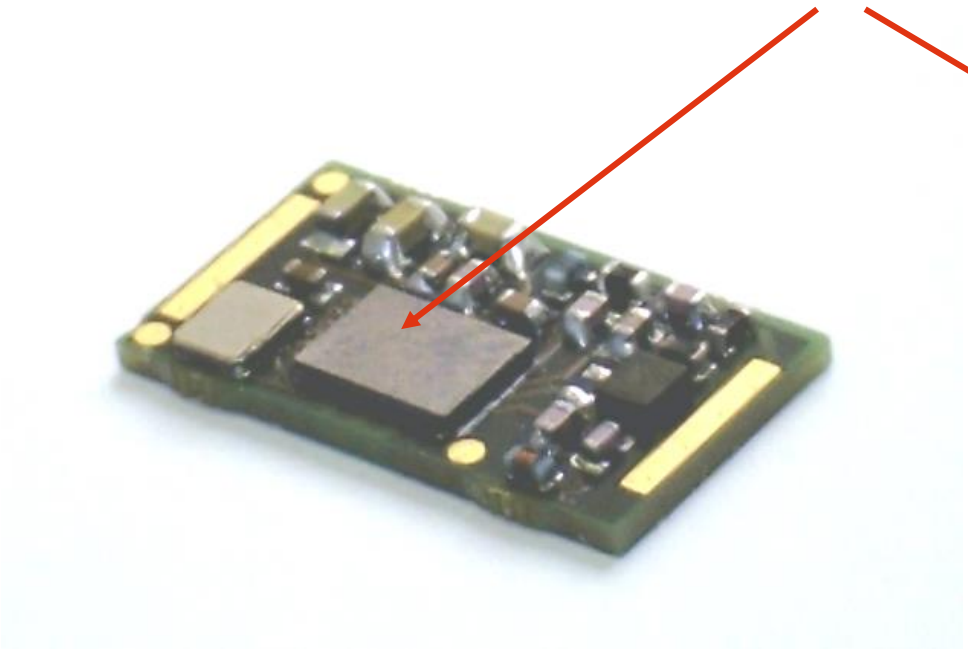


Test platform with die embedded here

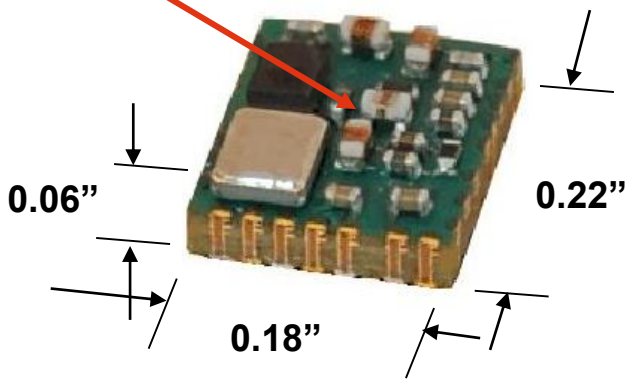


Case Study: Radio Module

Die hidden in the PCB



0.50” X 0.32” X 0.06”

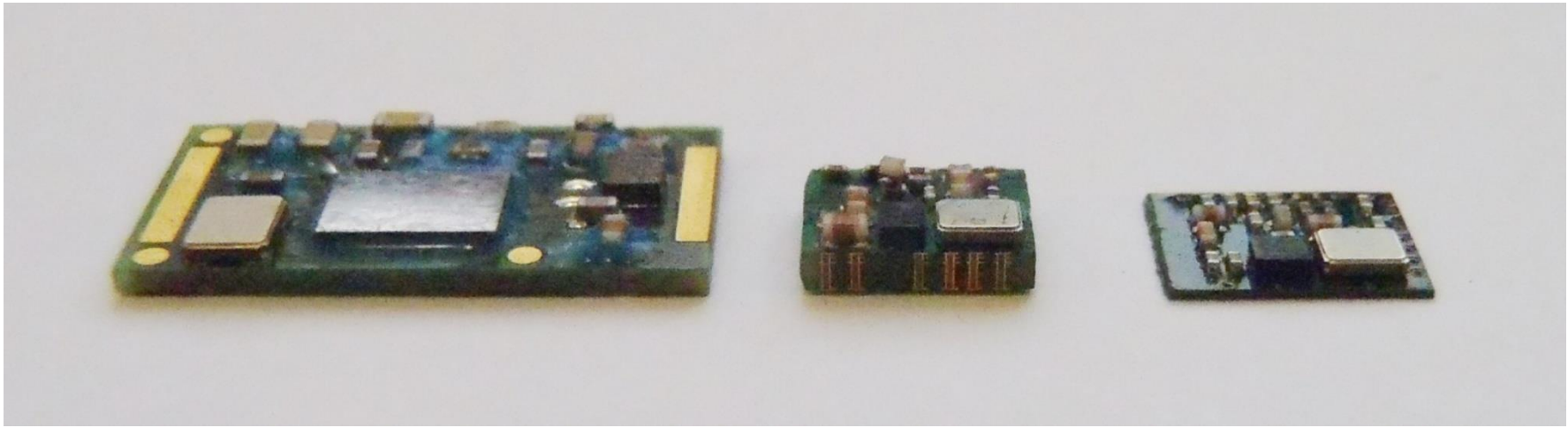


400% reduction in area

Radio Module Qualification

Microsemi	MiniMICS Technology Qualification Regime	
Test Group	**Test Standard**	**Result**
Moisture Sensitivity Preconditioning: Temperature Cycling Bake Moisture Soak 3x Reflow	JESD22-A113F, IPC/JEDEC J-STD-020 Level 2a -40°C to 60°C, 5 cycles 125°C for 24hrs 120hrs, 60°C/60%RH JESD22-A113F, 260°C	Pass
Thermal Stress: Low Temperature Storage High Temperature Storage Temperature Cycling	 -40°C, 72hrs 125°C, 72 hrs MIL-STD-883 Method 1010, Condition B, -55°C to 125°C, 20 cycles	Pass
Mechanical Stress: Mechanical Shock Mechanical Vibration Constant Acceleration	 MIL-STD-883 Method 2002, Condition B, 5 shocks, 1500g MIL-STD-883 Method 2007, Condition A, 20-2000Hz, 20G MIL-STD-883 Method 2001, 10,000G	Pass
Steady State Life Testing: Low and High Temperature Testing HTOL	 0°C, 55°C 125°C, 1000hrs	Pass
Exposure: Resistance to Solvents ESD	 MIL-STD-883 Method 2016 MIL-883 Method 3015, 1000V HBM	Pass
Assembly: Component Shear External physical dimensions Solderability Ionic Cleanliness	 MIL-STD-883 Method 2019/2011 MIL-883 Method 2016 MIL-STD-883 Method 2003.8/2022.2 IPC-TM-650	Pass

Case Study: Radio Module

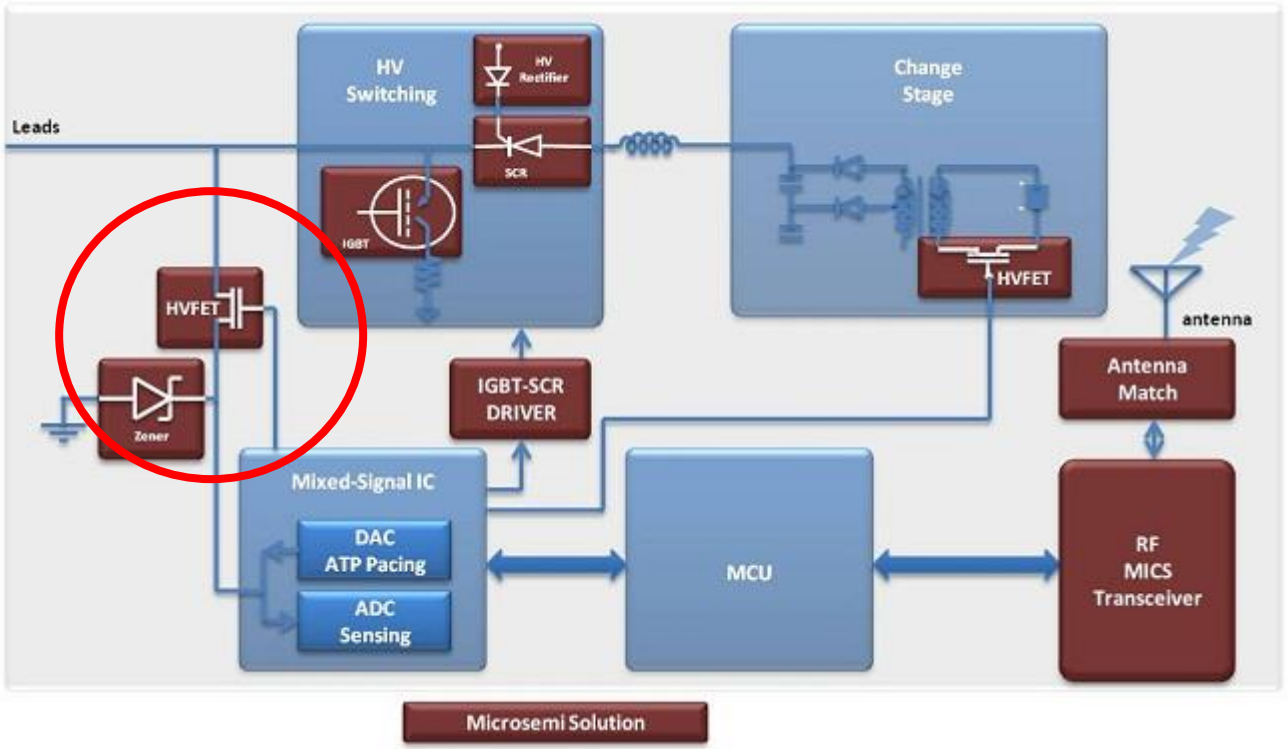


- Evolution is towards ultra-thin embedded die
- Die (50 to 80um) enables ultra-thin Z axis lamination 0.5mm
- Module height typically 1.0mm (discrete component limit)

Case Study
Stacked Die Module

Case Study: Stacked Die Module

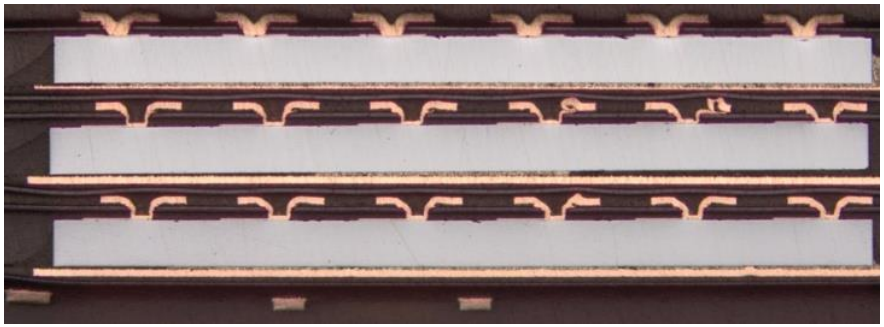
Typical Implantable Cardiac Defibrillator (ICD) Block Diagram

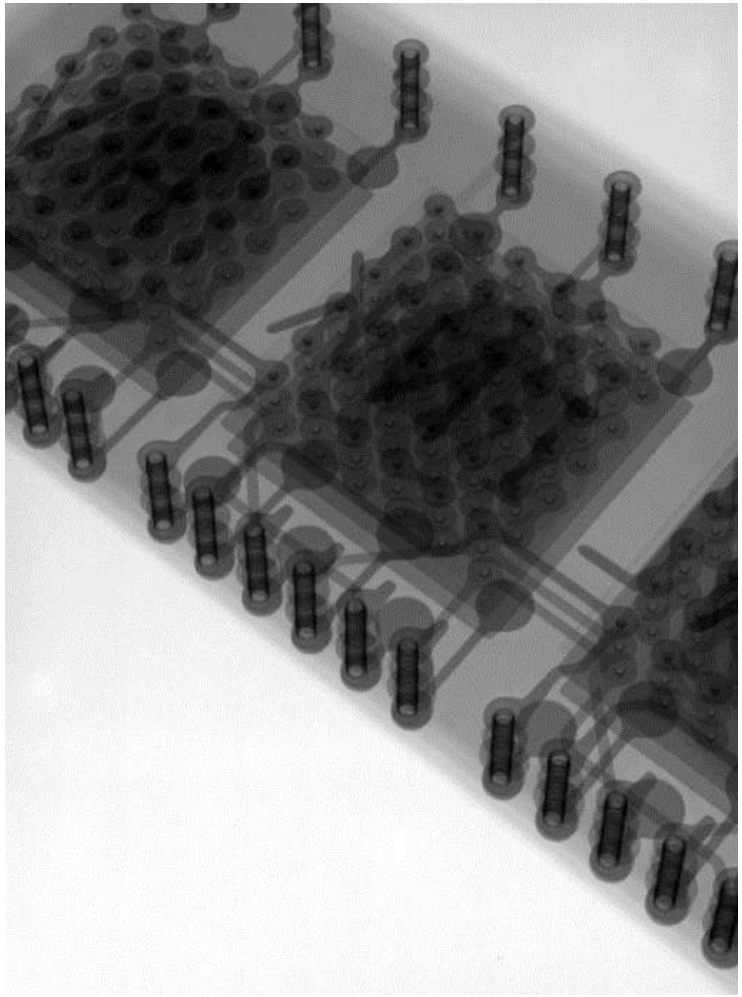


Area of focus – HVFET Circuit

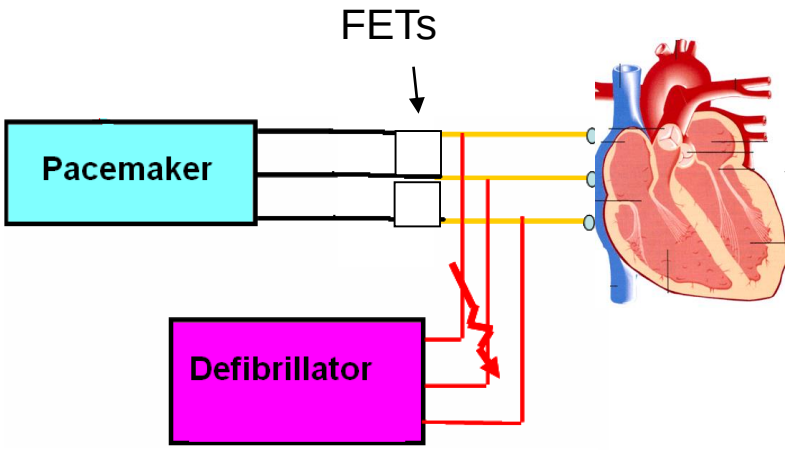
Case Study: Stacked Die Module

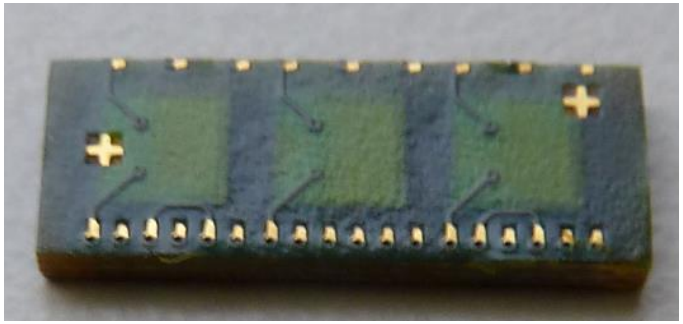
- Stacking embedded die layers
  - To enable further miniaturization
- Working on volume rather than planar surfaces of PCB
  - Volume is becoming more critical to device companies than area





Case Study: Stacked Die Module

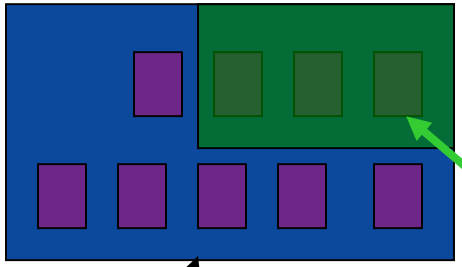




- Stack of pacemaker protection FETs
  - Large area consumed by the FETs – 10% of ICD PCB
  - Low-power, low-heat
  - High KGD yield
  - But challenging HV barrier requirements

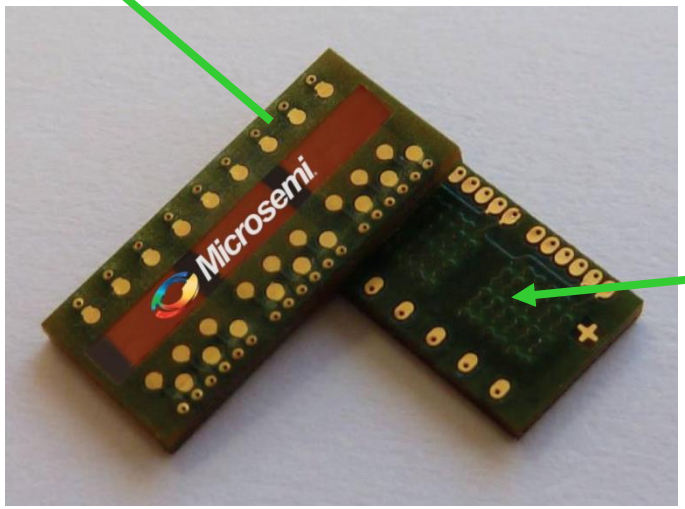
Case Study: Stacked Die Module

- 60% space-saving demonstrated by stacked die module

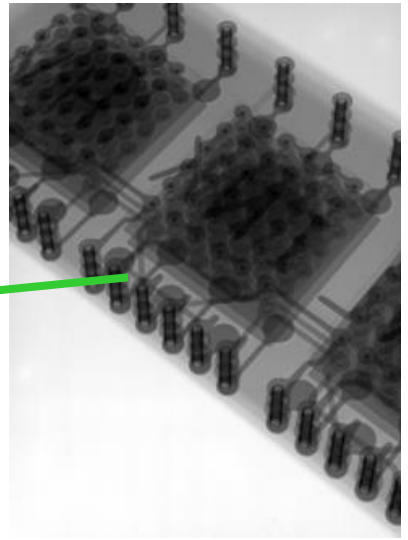


module area usage

FET area usage



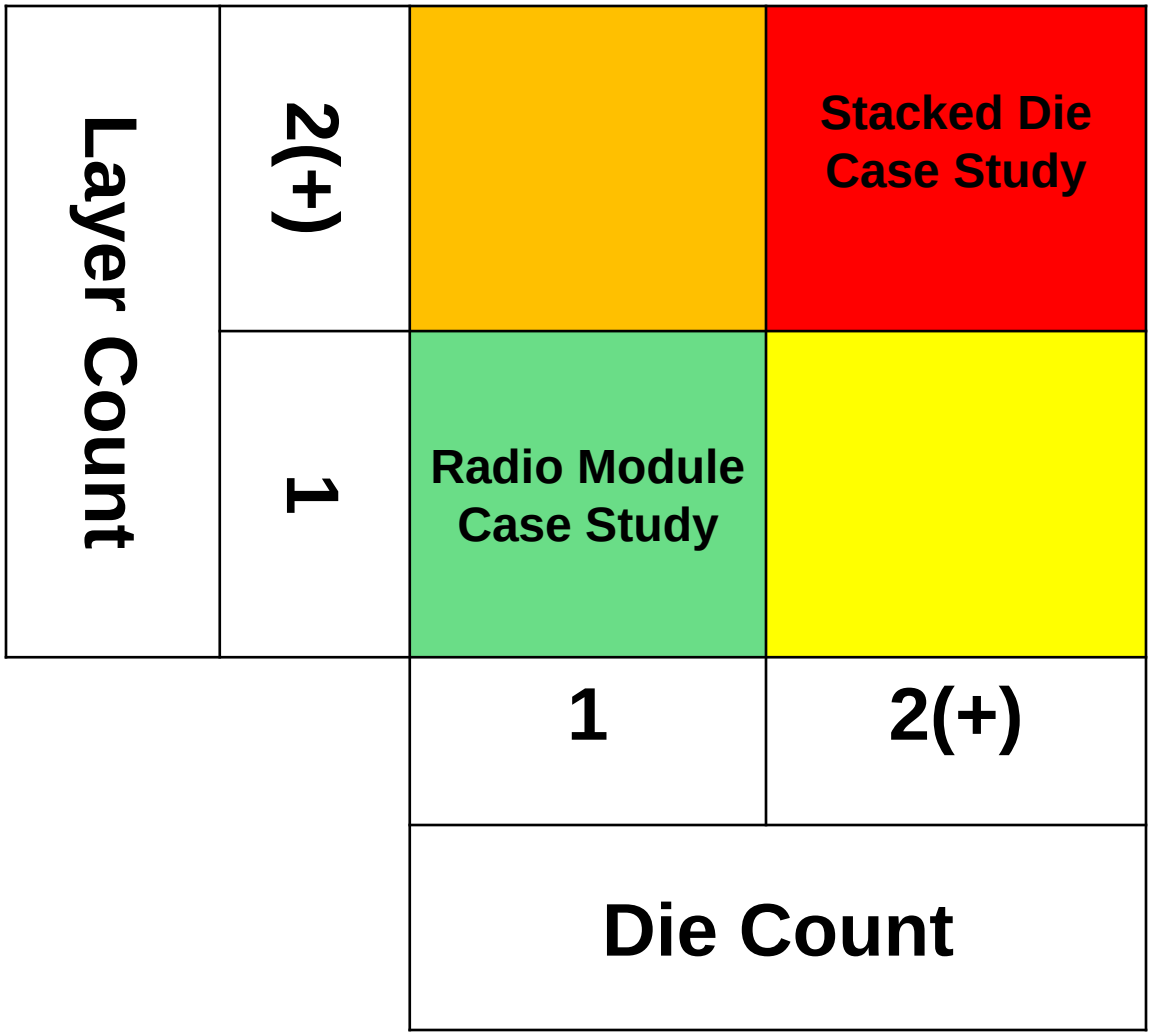
X-ray of test module



Observations for Both Technologies

- Single die single layer (SDSL) embedded die technology is established and gaining greater acceptance in products
- Stacked die technology gaining “interest” traction - currently better suited to low count I/O
- Stacked die technology typically working with stacks of 3 or 4 – some research institutes have discussed at 8 or 10
- Yields can be a limiting factor as die number and stack number increases complexity (MDML)

Embedded Die Complexity Matrix

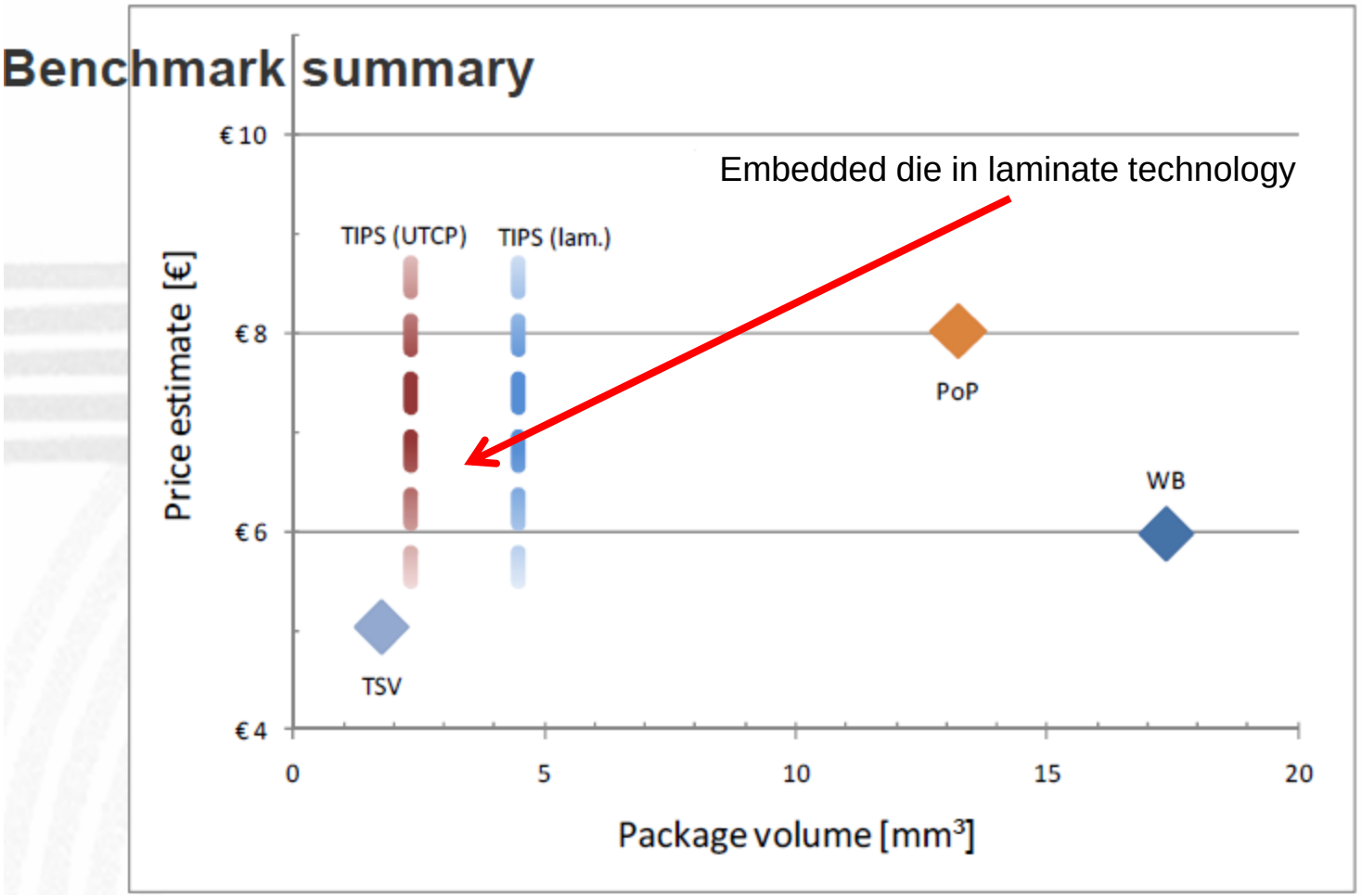


Greatest Area and Volume Saving

Advantages of Embedded Die Packages

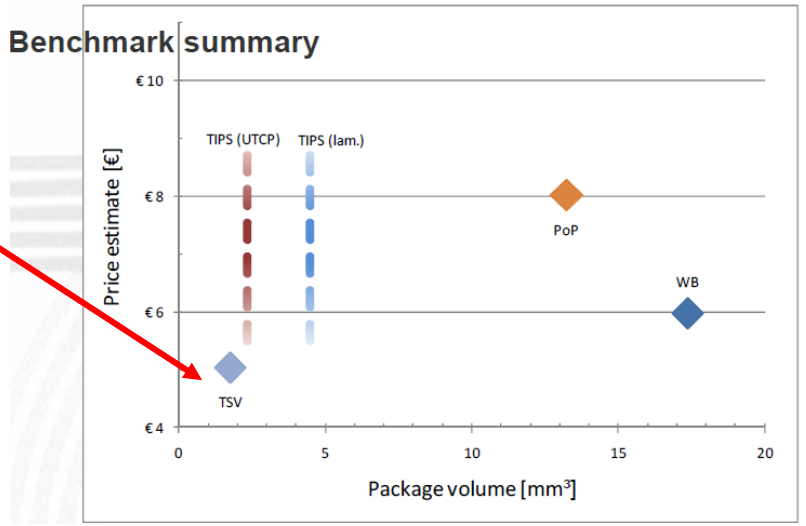
- Good scale of miniaturization
  - Especially height
  - Die becomes a near zero area occupancy
- More flexible package design
  - Package design and footprint can be adapted to meet the system
  - Standard die more easily integrated in to system – take a system approach for solution not an accept what is available
- Potentially low cost for low volumes
  - Large area mass production PCB panel process
  - Low tooling costs
  - Faster time-to-market

Where Does the Technology Fit?



Comparison with TSV

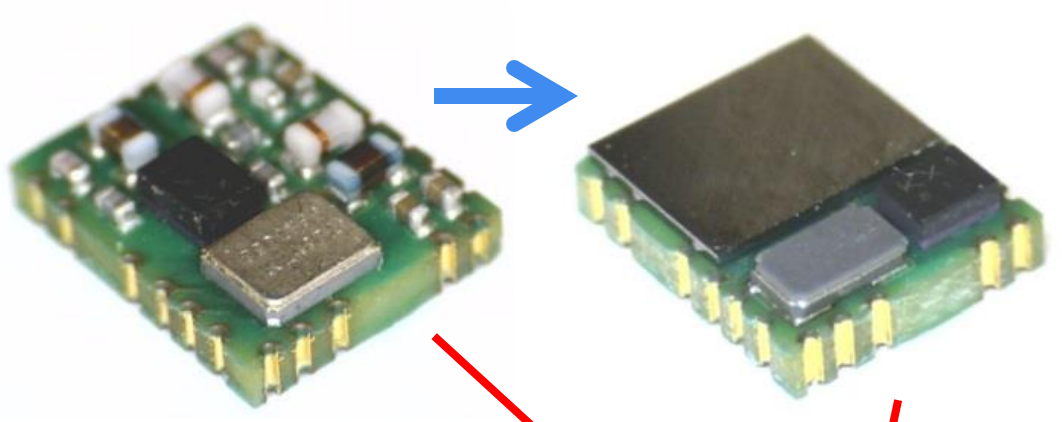
- TSV
  - Lower cost and smaller size



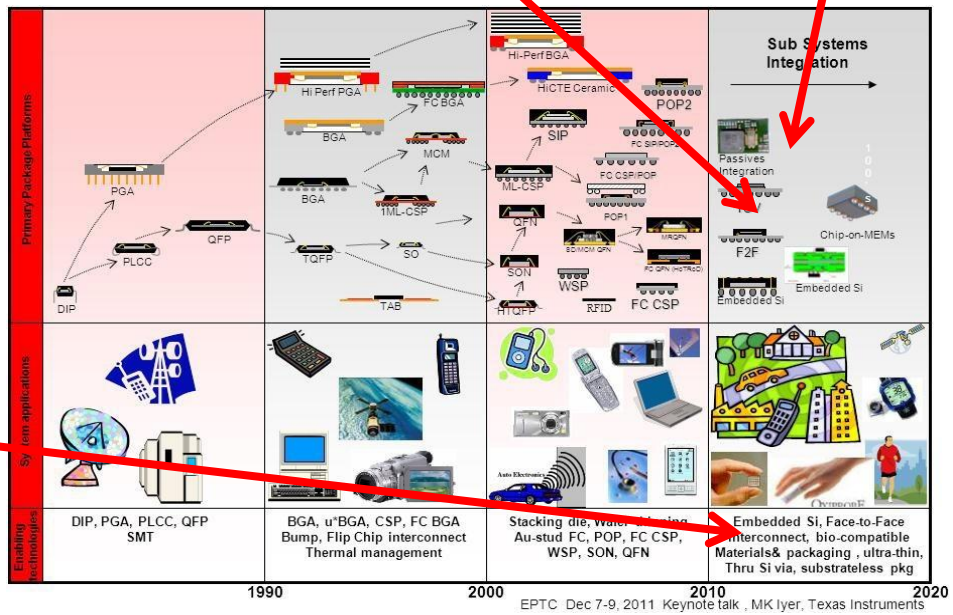
- However!
  - Silicon needs to be designed for TSV
  - TSV can consume chip real estate
  - Wafer-level processing as opposed to chip processing
  - TSV insulating liner integrity/leakage – at medical standards?
  - TSV are not available yet for reasonable commercial terms
  - Embedded die in laminate technology suits the lower to medium volumes of the medical market

On the Horizon

- Integrated Passives
  - Simplified assembly
  - Medical grade
  - Supports the ultra thin modu concepts



- Chip Scale Modules
  - Substrate less modules
  - Incorporating discrete devices



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Conclusions

- Advanced packaging technology can deliver substantial space and volume savings for electronic medical devices
- Embedded die technology suits medical applications
  - Low tooling costs for low to mid volumes
  - Extreme miniaturization in all three axis
- Stacked embedded die is a low cost credible alternative to TSV
  - No need for dedicated chip designs, uses available bare die
- Chip scale as opposed to wafer scale
  - More accessible for medium volume applications wanting to use existing semiconductor solutions

Thank you!

For more information: www.microsemi.com/design-support/package-miniaturization-services