UG0658
User Guide
Open-Loop Manager v4.1

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Added the IP version to the document title.
- Removed Configuration Parameter section from Hardware Implementation, page 3.

1.2 Revision 2.0

Updated the chapter title from Hardware Implementation to Open-Loop Manager (SAR 79511).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The rotor speed and position estimation is not reliable when the motor is running at low speeds. Hence, this information cannot be used to control the motor at start up and low speeds in sensor-less mode. The motor needs to be started with a forced angle (open loop angle) instead of estimated angle. The open loop angle along with current reference generation is managed by open-loop manager. The open-loop manager performs the following functions:

- Generates open loop angle based on the following equation:

$$\theta = ((\omega^* \times \theta_{factor}) + (\theta_{buffer} \times 2^{scale}))/2^{scale}$$

  where,

  θ is the angle generated

  ω^* is the speed reference input

  θ_{buffer} is the previous theta (generated angle) value

  θ_{factor} is a constant

  scale is a scaling value
- Switches the angle between open loop angle and estimated angle based on closed loop status
- Generates init values for speed and Iq PI controllers based on direction.

$$Speed\ \ PI\ \ init = iq\_ref\_in\_i$$

$$Iq\ \ PI\ \ init = speed\_ref\_i + dv\_i$$

Note: Theta factor is computed as:

$$\frac{67}{120} \times \frac{N_{rpm} \times N_{pp}}{f_{sw}}$$

where,

N_{rpm} is rated motor speed in RPM

N_{pp} is number of pole pairs

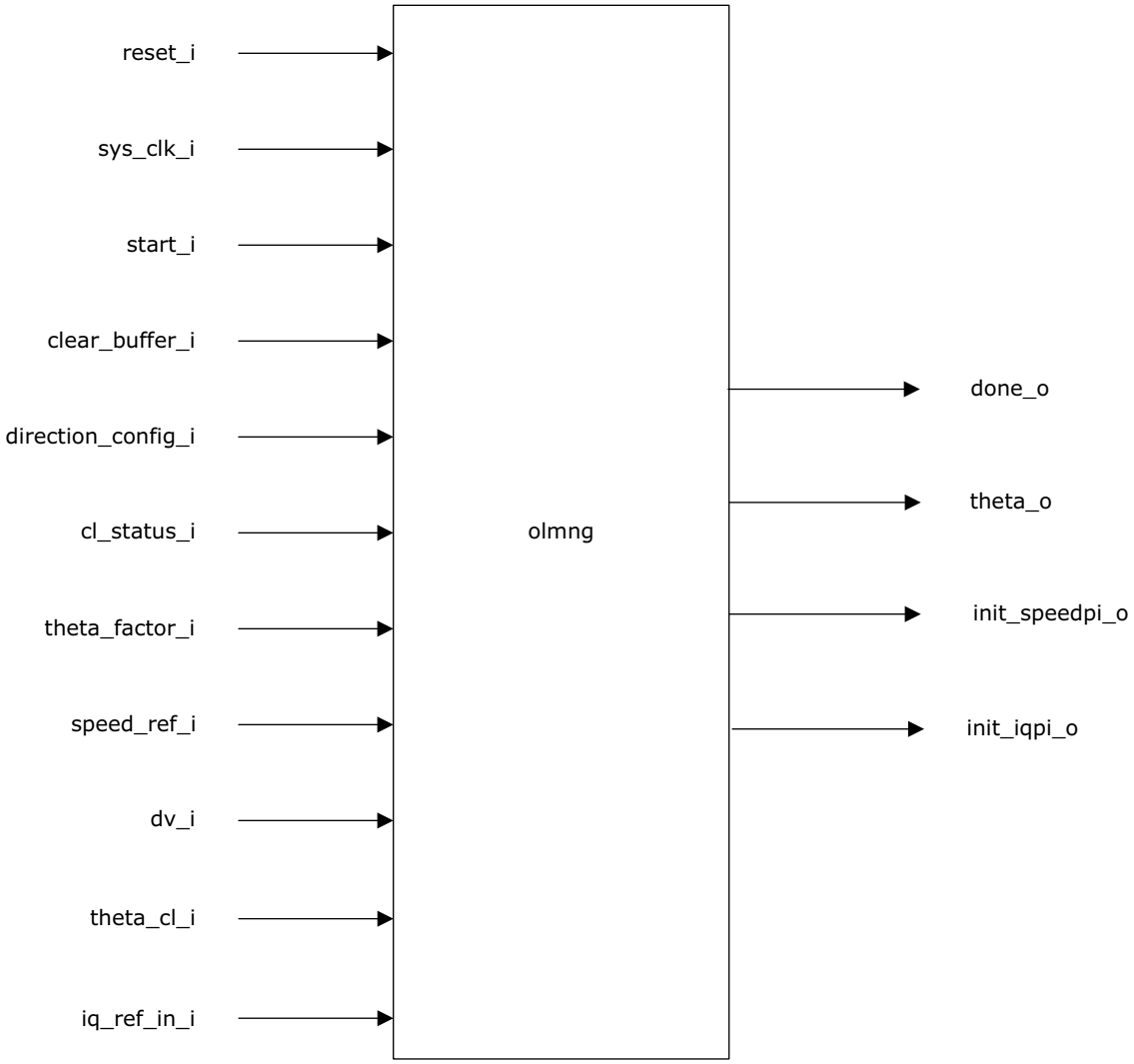
f_{sw} is switching frequency

3 Hardware Implementation

This section describes the implementation details of the open-loop manager block.

The following figure shows the block diagram of open-loop manager.

Figure 1 • **System-level Block Diagram of Open-Loop Manager**



3.1 Inputs and Outputs

The following table lists the input and output ports of open-loop manager.

Table 1 • **Inputs and Outputs of Open-Loop Manager**

Signal Name	Direction	Description
reset_i	Input	Asynchronous active low reset signal
sys_clk_i	Input	System Clock
start_i	Input	Start signal to start module computation - should be high for one system clock cycle
clear_buffer_i	Input	When high, internal buffers are set to zero
direction_config_i	Input	Motor Direction input
cl_status_i	Input	Closed loop status
theta_factor_i	Input	Theta factor (constant) input
speed_ref_i	Input	Motor speed reference input
dv_i	Input	Delta Voltage to add to Vq (through init value of IQ PI controller)
theta_cl_i	Input	Closed loop angle value
iq_ref_in_i	Input	Iq Current Reference value
done_o	Output	Indicates completion of module computations – high for one clock cycle
theta_o	Output	Angle output: When cl_status_i is 0, output is open loop angle (computed internally) When cl_status_i is 1, output is closed loop angle (from theta_cl_i input)
init_speedpi_o	Output	init value for speed PI controller
init_iqpi_o	Output	init value for Iq PI controller

3.2 Configuration Parameters

The following table shows the description of the configuration parameter used in the hardware implementation of open-loop manager. This is a generic parameter and can be varied as per the requirement of the application.

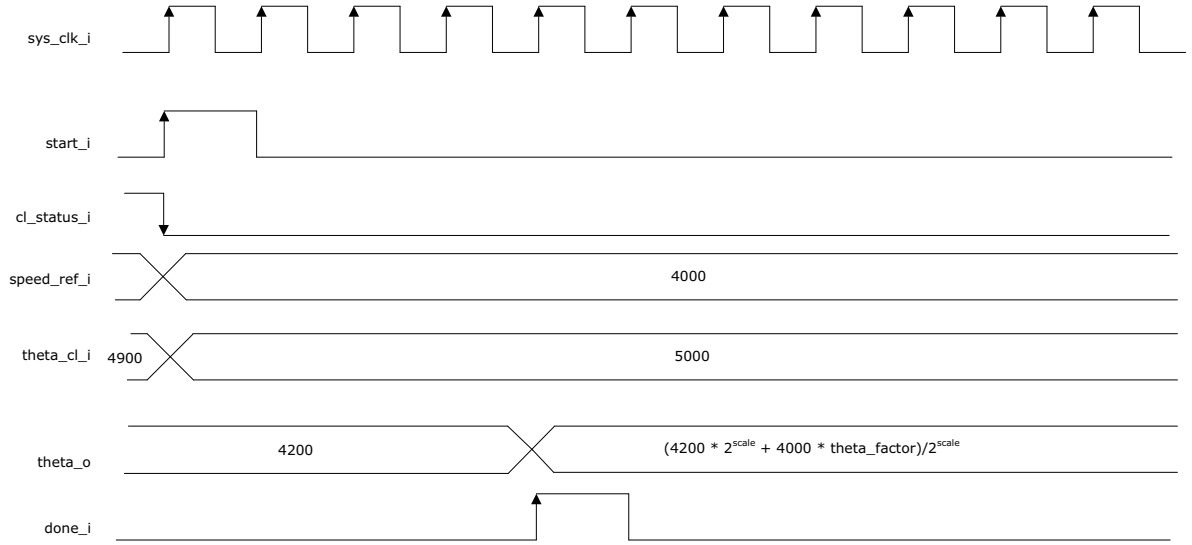
Table 2 • **Configuration Parameters**

Signal Name	Description
g_NO_MCYCLE_PATH	Defines the number of clock delays required before asserting the multiplier done signal.

3.3 Timing Diagrams

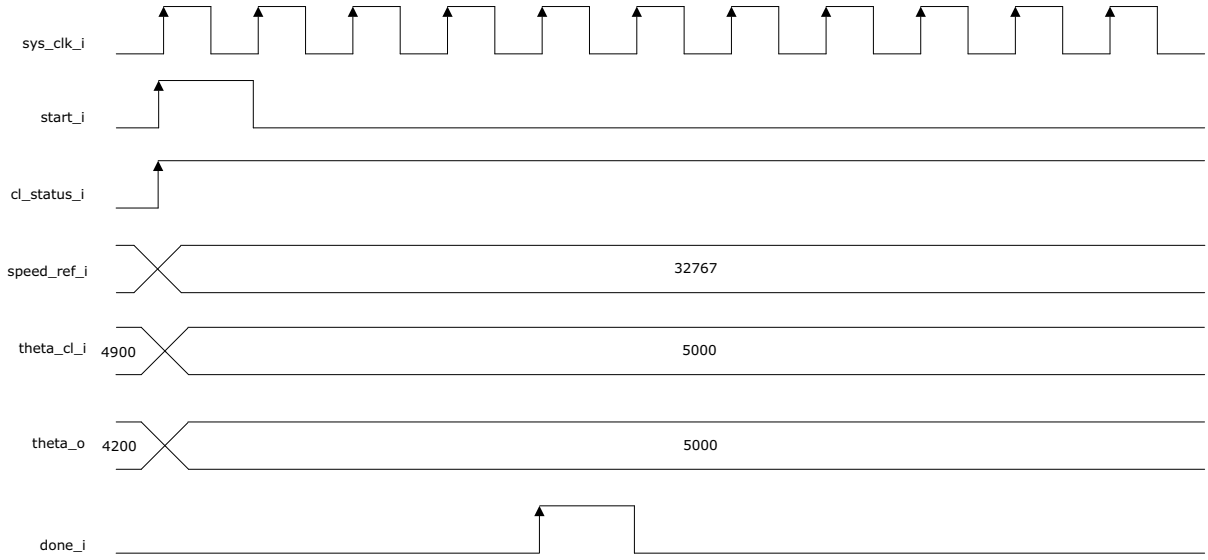
The following figure shows the timing waveform of the open-loop manager. A minimum of 5 x g_NO_MCYCLE_WIDTH clock cycles are required between successive start signals.

Figure 2 • **Timing Diagram of Open-Loop Manager in Open-Loop**



The following figure shows the timing waveform of the closed-loop.

Figure 3 • **Timing Diagram of Open-Loop Manager in Closed-Loop**



3.4 Resource Utilization

Open-loop manager is implemented on SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 devices. The following table shows the resource utilization report after synthesis.

Table 3 • **Resource Utilization Report of Open-Loop Manager**

Cell Usage	Count
Sequential elements	120
Combinational logic	90
MACC	1
RAM1kx18	0
RAM64x18	0