UG0657
User Guide
ADC Scaling v4.2

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of changes made in this revision:

- Updated the adc scaling version from v4.1 to v4.2 in the document title.
- Added the g_SIGNED signal name in the Configuration Parameter table (see Table 2, page 4).
- Updated the Scales raw ADC data into phase currents formula (see Introduction, page 2).
- Updated the count values for Sequential elements and Combinational logic in the Resource Utilization Report of PWM Scaling table (see Table 3, page 5).

1.2 Revision 2.0

This document was published in October 2016. The following was a summary of the changes in revision 2.0 of this document.

- Added the IP version to the document title.
- Removed g_STD_IO_WIDTH configuration parameter from sections Configuration Parameters, page 4 and Resource Utilization, page 5.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

An analog to digital converter (ADC) converts a voltage signal as input to a digital signal in a number of bits that depends on ADC resolution. Signals that are not available in voltage form, such as currents, are converted to a voltage signal before conversion to digital data. The digital signal output of the ADC that is relative to its bit width must be scaled to a value that can be properly interpreted by the system that processes the signal. The digital output of ADC can have an unintended DC offset that could be generated by the signal processing circuit before ADC input or the ADC itself. The offset value in signal measurement must be removed before using it in digital algorithm. The ADC scaling block performs the following functions:

- Performs auto offset computation initially:
  Involves disabling PWM and triggering the ADC by a pre-determined number of times (8192) to determine ADC offset.

$$ChX\_offset = adc\_result\_chX\_i + ChX\_offset$$

- Scales raw ADC data into phase currents:

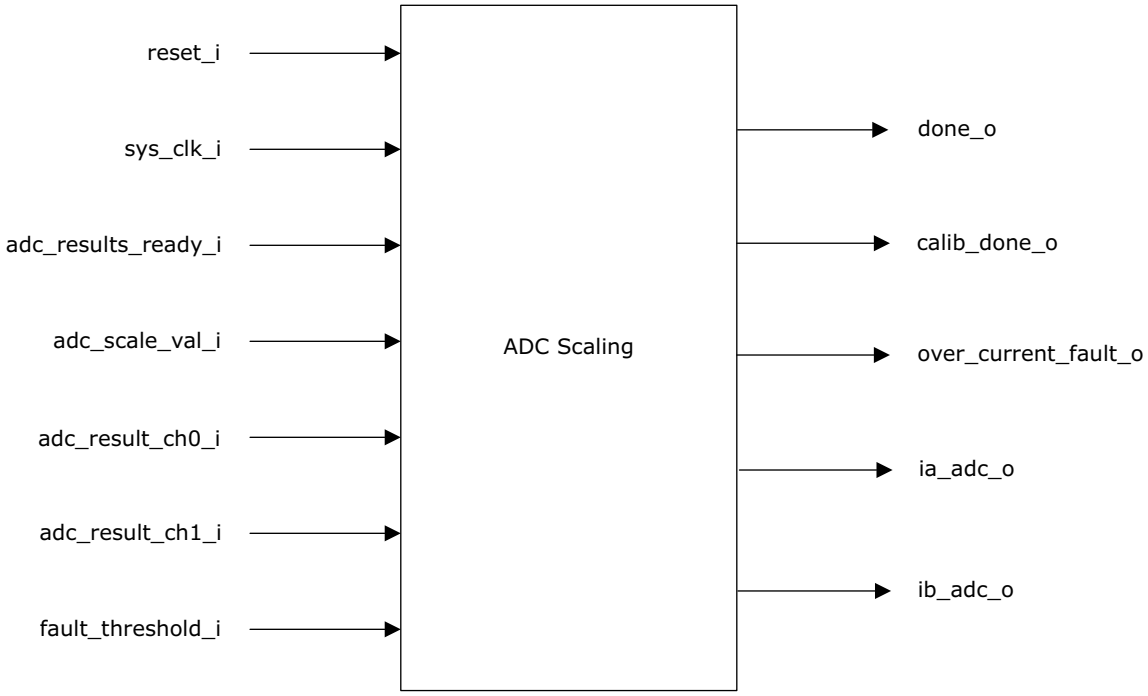
$$I_{ph} = \left(adc\_result\_chX\_i - \left(\frac{ChX\_offset}{8192}\right)\right) \times \left(\frac{adc\_scale\_val\_i}{256}\right)$$

- Detects over current fault after phase current computation, which can be used to stop the motors immediately.

3 Hardware Implementation

The following figure shows the block diagram of ADC scaling.

Figure 1 • **System-Level Block Diagram of ADC Scaling**



The ADC scaling accumulates the first 8,192 samples of adc_result_ch0_i and adc_result_ch1_i. The calib_done_o signal is asserted after 8,192 samples are accumulated. The accumulated data is averaged and subtracted from each sample thereafter. This value is multiplied with adc_scale_val_i to give the actual ADC result. The block also asserts the over_current_fault_o when the scaled currents are more than the fault_threshold_i value.

During simulation, the block need not accumulate a large number of samples. The g_DEBUG parameter can be set to 1 to reduce the number of samples that are accumulated to 5, while setting it to 0 accumulates 8,192 samples.

3.1 Inputs and Outputs

The following table lists the input and output ports of ADC scaling.

Table 1 • **Inputs and Outputs of ADC Scaling**

Signal Name	Direction	Description
reset_i	Input	Asynchronous active low reset signal to design.
sys_clk_i	Input	System clock.
adc_results_rdy_i	Input	Trigger indicating ADC inputs are available.
adc_scale_val_i	Input	Scaling value for currents.
adc_result_ch0_i	Input	Channel 0 result from ADC.
adc_result_ch1_i	Input	Channel 1 result from ADC.
fault_threshold_i	Input	Threshold value of current above which a fault is indicated.
done_o	Output	Indicates completion of scaling operations – high for one clock cycle.
calib_done_o	Output	A constant high signal indicates offset calibration is complete.
over_current_fault_o	Output	Indicates that at least one of the currents have exceeded the fault_threshold_i input value. The signal goes back to zero (not latched) when all the currents are less than fault_threshold_i.
ia_adc_o	Output	Scaled current value for phase a (from Channel 0).
ib_adc_o	Output	Scaled current value for phase b (from Channel 1).

3.2 Configuration Parameters

The following table lists the description of the configuration parameters used in the hardware implementation of ADC scaling. These are generic parameters and can be varied as per the requirement of the application.

Table 2 • **Configuration Parameters**

Signal Name	Description
g_DEBUG	When 0, supports Synthesis. When 1, supports Simulation.
g_SIGNED	When 0, supports signed inputs from the ADC interface block. When 1, supports unsigned inputs from the ADC interface block.
g_ADC_RESULTS_WIDTH	Defines the width of the inputs from ADC Measurements block.
g_NO_MCYCLE_PATH	Defines the number of clock delays required before asserting the multiplier done signal.

3.3 Resource Utilization

ADC scaling is implemented on the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 devices. The following table lists the resource utilization report after synthesis.

Table 3 • **Resource Utilization Report of PWM Scaling**

Cell Usage	Count
Sequential elements	200
Combinational logic	140
MACC	1
RAM1kx18	0
RAM64x18	0