PCI Express Refclk Jitter Compliance

1. *PCI Express Overview*

In the late 1990s the computing industry had taken the original parallel-data PCI bus to its practical throughput limits. The multi-drop PCI data bus was 64 bits wide, and the clock frequency had been pushed up to as high as 533MHz for the server-oriented variant called PCI-X. Physically, the large number of pins required to interface to a 64-bit PCI bus had a detrimental effect on component cost. At the system level, managing the timing skews between data lines at high clock rates was a significant challenge.

By this time, however, the communications equipment industry had become increasingly comfortable with gigabit per second (Gbps) *serial* interfaces using differential signaling. For any communication system with 2.5Gbps or 10Gbps interfaces, the core of the system had multi-Gbps electrical signals carrying data between cards.

In this industry context the PCI SIG (PCI Special Interest Group) adopted a revolutionary electrical layer for its new PCI Express specification. The foundation of the PCI Express (PCIe) electrical layer is point-to-point, bidirectional, high-speed serial *lanes*. This foundation eliminates many of the problems associated with the old parallel PCI bus. With the new PCIe paradigm, timing skews between wires are not an issue because data is sent serially rather than in parallel. Also, interface pin counts are greatly reduced, lowering component costs. In addition, system designers no longer have to be concerned with the variable transmission distances that were present in the multi-drop PCI bus because PCIe is point-to-point not multi-drop. Also data-to-clock timing is made simple because each serial lane is self-clocked. This is accomplished using line coding that provides a high-enough ones density to ensure that the receiver can recover the clock along with the data.

2. *Links and Speeds*

The other great benefit of PCIe is much higher data throughput. Devices communicate using a PCIe *link* that bundles together 1, 2, 4, 8, 12, 16 or 32 lanes (Figure 1), with each lane being a transmit differential pair and a receive differential pair. The original release--called PCIe 1.0 and later incremented to 1.1—specified a 2.5Gbps bit rate per lane in each direction and 8B/10B encoding. PCIe 2.0 (later incremented to 2.1) doubled the throughput by doubling the lane rate to 5.0Gbps. PCIe 3.0 roughly doubled throughput again with an 8Gbps lane rate and more-efficient 128B/130B encoding. Figure 2 shows the actual *per lane* data throughput, not counting the 8B/10B or 128B/130B encoding overhead. Note that a PCIe 3.0 link with 32 lanes has total throughput of 64 gigabytes per second (GB/s).

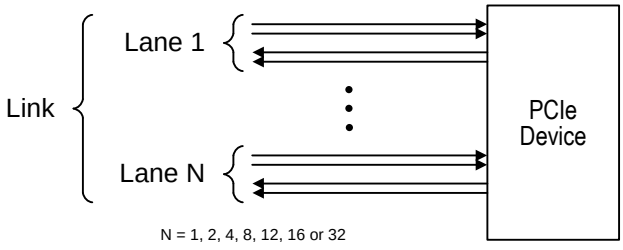


Figure 1 PCI Express Lanes and Links

PCIe Version	Lane Bitrate (a)	Directions (Tx & Rx) (b)	Encoding Bits Per Byte (c)	Throughput Per Lane = a x b ÷ c
1.1	2.5G	2	10	0.5GB/s
2.1	5.0G	2	10	1GB/s
3.0	8.0G	2	130÷16	~2GB/s (1.969)

Figure 2 PCI Express Per-Lane Throughput

3. *Refclk Signal Format*

To standardize the Refclk signal used between system boards and add-in cards from multiple vendors, the PCIe Card Electromechanical Specification Revision 2.0 specifies a differential signal format with a common-mode voltage in the 250 to 550mV range and a differential swing (Refclk+ minus Refclk-) of at least 150mV. This signal format is commonly called HCSL. It is considered to have a 0 to 700mV single-ended swing and is source terminated.

For systems where all components are on the same card or systems where all cards are made by one vendor, HCSL signal format is not required. Refclk can be another signal format such as LVDS, LVPECL or CML.

4. *Typical Application*

Figure 3 shows a typical PCI Express application using the Common Refclk Rx architecture. A central PCIe clock generator on the motherboard (compute application) or central processing/switching board (telecom application) creates the original 100MHz Refclk. This clock generator can be configured for spread-spectrum clocking to be on or off as needed by the system. The Refclk signal is then replicated by one or more fanout buffers to provide Refclk to all other PCIe devices in the system.

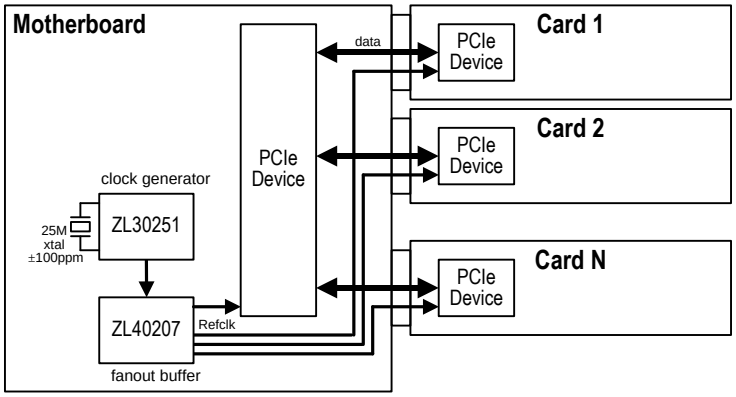


Figure 3 Typical PCI Express Application

5. *Refclk and Refclk Clocking Architectures*

The PCIe 3.0 Base Specification, in sections 4.3.7 (for 5GT/s lanes) and 4.3.8 (for 8GT/s lanes), describes the three Refclk architectures listed in Figure 4. It also specifies that Refclk frequency must be 100MHz ± 300ppm and that spread spectrum clocking (SSC) may be used for EMI reduction. The SSC parameters are -0.5% down-spread with 30kHz to 33kHz modulation rate. See Microsemi's Spread Spectrum Whitepaper for more details about SSC.

Architecture	Description	Spread Spectrum Modulation
Common Refclk Rx	Same 100MHz±300ppm Refclk to transmitter and receiver. Most widely used architecture.	Yes
Data Clocked Rx	100MHz±300ppm Refclk to transmitter only. Receiver recovers clock from incoming serial data. More difficult jitter requirements than Common Refclk Rx.	Yes
Separate Refclk	Separate 100MHz±300ppm Refclks to Tx and Rx. Much tighter jitter requirements. Not as thoroughly specified as other architectures. Not covered further in this document.	No

Figure 4 PCI Express Refclk Architectures

The Common Refclk Rx architecture is the easiest and most commonly used method for clock distribution among PCIe devices. Although the Data Clocked Rx architecture has a simpler block diagram, its jitter requirements are more difficult to meet because less filtering is applied. The Common Refclk Rx architecture has the filtering of the receiver clock multiplier PLL (Rx PLL in Figure 4-89 of PCIe 3.0), but the Data Clocked Rx architecture does not.

Sections 4.3.7 and 4.3.8 of the PCIe 3.0 Base Specification develop models and jitter-transfer functions for the three architectures. They also specify maximum jitter values and filters to be applied during measurement.

6. *Common Refclk Rx Architecture Jitter Requirements*

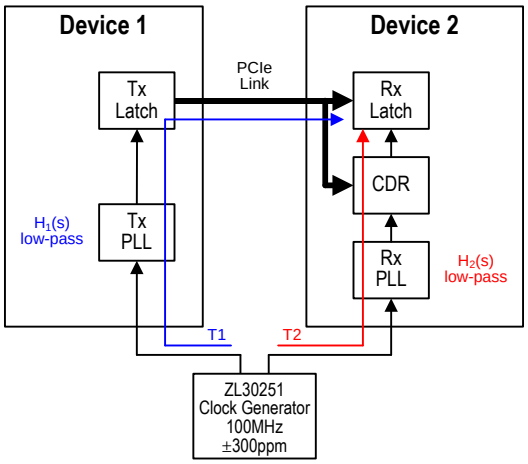


Figure 5 Common Refclk Rx Architecture Model

In the Common Refclk Rx architecture the same reference clock is distributed to both transmit (Tx) and receive (Rx) devices as shown in Figure 5. The jitter of concern at the receiving device is, generally speaking, the difference between the transmit path jitter transfer function and the receive path jitter transfer function, taking into account the delay difference between the transmit path and receive path, T = |T1 – T2|. Each generation of PCIe has a slightly different expression of the overall transfer function, as described in the subsections below, but all generations assume 2nd-order transfer functions for both Tx and Rx PLLs. Therefore:

$$H_1(s) = \frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2} \quad \text{and} \quad H_2(s) = \frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}$$

6.1 *Common Refclk Rx Architecture, PCIe 1.1 (2.5GT/s)*

The following are the Refclk transfer function aspects for PCIe 1.1:

- **Transfer function** $H(s) = [H_1(s) – H_2(s)e^{-sT}]H_3(s)$
- **Delay Delta, T** 10ns max
- **$H_3(s)$** $\frac{s}{s+2\pi*1.5Mrad/s}$
- **Tx PLL Parameters, $H_1(s)$**

-3dB Freq (MHz) f_1	Max Peaking dB	Natural Freq (Mrad/s) ω_1	Damping Factor ζ_1
22	3.0	11.83*2π max	0.54

- **Rx PLL Parameters, $H_2(s)$**

-3dB Freq (MHz) f_2	Max Peaking dB	Natural Freq (Mrad/s) ω_2	Damping Factor ζ_2
1.5	3.0	0.807*2π max	0.54

The jitter requirements, after applying the filtering listed above, are as follows:

Jitter Requirement

Description	Conditions	Min	Max	Units
Total Jitter	10^{12} Samples		108	ps
Total Jitter	10^{6} Samples		86	ps

The 10^{12} Samples requirement is the real goal but scopes do not have enough memory to test that requirement directly. Therefore the 10^{6} Samples requirement is typically tested instead.

6.2 *Common Refclk Rx Architecture, PCIe 2.1 (5GT/s)*

The following are the Refclk transfer function aspects for PCIe 2.1:

- **Transfer function** $H(s) = [H_1(s)e^{-sT} – H_2(s)]H_3(s)$
- **Delay Delta, T** 12ns max
- **$H_3(s)$** HF (>1.5MHz): if($f \geq 1.5MHz$) then 1 else 10^{-3}
  LF (10kHz-1.5MHz): if f<10kHz then 10^{-3} elseif f<1.5MHz then 1.0 else 10^{-3}
- **Tx PLL Parameters, $H_1(s)$**

-3dB Freq (MHz) f_1	Max Peaking dB	Natural Freq (Mrad/s) ω_1	Damping Factor ζ_1
5	1.0	$1.82*2\pi$ max	1.16
8	3.0	$4.31*2\pi$ max	0.54

- **Rx PLL Parameters, $H_2(s)$**

-3dB Freq (MHz) f_2	Max Peaking dB	Natural Freq (Mrad/s) ω_2	Damping Factor ζ_2
16	3.0	$8.61*2\pi$ max	0.54

The two rows in the Tx PLL table represent two separate options specified in the standard. Jitter compliance must be checked for each option in combination with the other aspects listed above.

Note that the $H_3(s)$ function is from PCIe Base Specification Revision 2.1, section 4.3.3.1 where it is denoted as $H_{hi\text{-}5GT/s}$ for the high band and $H_{lo\text{-}5GT/s}$ for the low band. This function is designed to remove spread spectrum clocking and other low-frequency jitter components that are trackable by the Rx CDR from the high-band measurement.

The jitter requirements, after applying each of the filtering options listed above, are as follows:

Jitter Requirements

Symbol	Description	Min	Max	Units
$T_{REFCLK\ HF\text{-}RMS}$	>1.5 MHz to Nyquist jitter		3.1	ps RMS
$T_{REFCLK\ LF\text{-}RMS}$	10kHz to 1.5MHz jitter		3.0	ps RMS

6.3 *Common Refclk Rx Architecture, PCIe 3.0 (8GT/s)*

The following are the Refclk transfer function aspects for PCIe 3.0:

- **Transfer functions** $H(s) = [H_1(s)e^{-sT} – H_2(s)]H_3(s)$

  $H'(s) = [H_2(s)e^{-sT} – H_1(s)]H_3(s)$

- **Delay Delta, T** 12ns max

- **$H_3(s)$ (Rx CDR)** $\frac{s}{s + 2\pi * 10MHz}$

- **Tx PLL Parameters, $H_1(s)$**

-3dB Freq (MHz) f_1	Max Peaking dB	Natural Freq (Mrad/s) ω_1	Damping Factor ζ_1
2.0	0.01	0.448	14
2.0	2.0	6.02	0.73
4.0	0.01	0.896	14
4.0	2.0	12.04	0.73

- **Rx PLL Parameters, $H_2(s)$**

-3dB Freq (MHz) f_2	Max Peaking dB	Natural Freq (Mrad/s) ω_2	Damping Factor ζ_2
2.0	0.01	0.448	14
2.0	1.0	4.62	1.15
5.0	0.01	1.12	14
5.0	1.0	11.53	1.15

The four rows in the Tx PLL table represent four separate options specified in the standard. Similarly, four separate Rx PLL options and two transfer functions are specified in the standard. This means that jitter compliance must be checked for 32 options (4 x 4 x 2).

The jitter requirement, after applying each of the 32 filtering options listed above, is as follows:

Jitter Requirement

Symbol	Description	Min	Max	Units
$T_{REFCLK\_RMS\_CC}$	RMS Refclk jitter for common Refclk Rx architecture		1.0	ps RMS

7. Data Clocked Rx Architecture Jitter Requirements

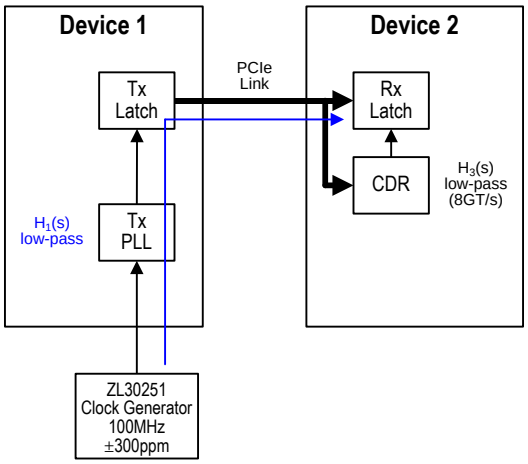


Figure 6 Data Clocked Rx Architecture Model

In the Data Clocked Rx architecture the receiver does not use Refclk directly. Instead it recovers clock from the incoming data, which is 8B/10B or 128B/130B encoded to ensure sufficient ones density for clock recovery. This architecture is not defined for PCIe 1.1.

The Tx PLL transfer function is assumed to be 2nd-order, therefore: $H_1(s) = \frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}$

7.1 Data Clocked Rx Architecture, PCIe 2.1 (5GT/s)

The following are the Refclk transfer function aspects for PCIe 2.1:

- **Transfer function** $H(s) = H_1(s)*H_3(s)$
- **$H_3(s)$** HF (>1.5MHz): if(f ≥ 1.5MHz) then 1 else 10^{-3}
  LF (10kHz-1.5MHz): if f<10kHz then 10^{-3} elseif f<1.5MHz then 1.0 else 10^{-3}
- **Tx PLL Parameters, $H_1(s)$**

-3dB Freq (MHz) f_1	Max Peaking dB	Natural Freq (Mrad/s) ω_1	Damping Factor ζ_1
16	0.5	8.61*2π	1.75
16	3.0	8.61*2π	0.54

The two rows in the Tx PLL table represent the minimum and maximum Tx PLL damping factor specified in the standard. Jitter compliance must be checked for each option in combination with the other aspects listed above.

Note that the $H_3(s)$ function is from PCIe Base Specification Revision 2.1, section 4.3.3.1 where it is denoted as $H_{hi\text{-}5GT/s}$ for the high band and $H_{lo\text{-}5GT/s}$ for the low band. This function is designed to remove low-frequency jitter components that are trackable by the Rx CDR from the high-band measurement.

The jitter requirements, after applying each of the filtering options listed above, are as follows:

Jitter Requirement

Symbol	Description	Min	Max	Units
T_{REFCLK_HF-RMS}	1.5 MHz to Nyquist jitter		4.0	ps RMS
T_{REFCLK_LF-RMS}	10kHz to 1.5MHz jitter		7.5	ps RMS

7.2 *Data Clocked Rx Architecture, PCIe 3.0 (8GT/s)*

The following are the Refclk transfer function aspects for PCIe 3.0:

- **Transfer function** $H(s) = H_1(s)*[1-H_3(s)]$
- **$H_3(s)$ (Rx CDR)** $\frac{2s\zeta_3\omega_{n3}+\omega_{n3}^2}{s^2+2s\zeta_3\omega_{n3}+\omega_{n3}^2}$
- **Tx PLL Parameters, $H_1(s)$**

-3dB Freq (MHz) f_1	Max Peaking dB	Natural Freq (Mrad/s) ω_1	Damping Factor ζ_1
2	0.01	0.448	14
2	1	4.62	1.15
2	2	6.02	0.73
4	0.01	0.896	14
4	2	12.04	0.73
5	0.01	1.12	14
5	1	11.53	1.15

- **CDR PLL Parameters, $H_3(s)$**

-3dB Freq (MHz) f_3	Max Peaking dB	Natural Freq (Mrad/s) ω_3	Damping Factor ζ_3
10	0.5	16.57	1.75
10	2.0	33.8	0.73

The seven rows in the Tx PLL table represent seven separate options specified in the standard. Similarly, two separate CDR PLL options are specified in the standard. This means that jitter compliance must be checked for 14 options (7 x 2). (Note that PCIe appears to have eight Tx PLL cases, but it lists the 2MHz bandwidth, 0.01dB peaking case in two places.)

The jitter requirement, after applying each of the 14 filtering options listed above, is as follows:

Jitter Requirement

Symbol	Description	Min	Max	Units
$T_{REFCLK\_RMS\_CC}$	RMS Refclk jitter for data clocked Rx architecture		1.0	ps RMS

8. *Conclusion*

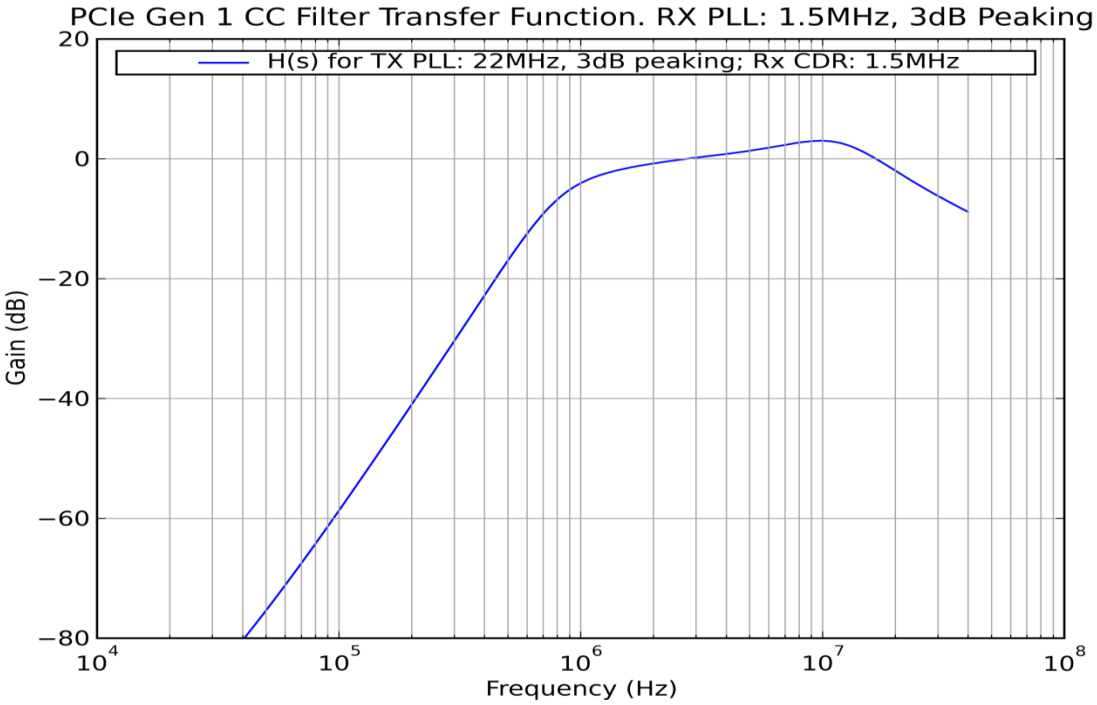
This document shows the complexity of verifying Refclk generator compliance with three generations of PCI Express specifications. Overall, five PCIe clocking design options must be evaluated: Common Refclk Rx architecture at 2.5, 5 and 8GT/s and Data Clocked architecture at 5 and 8GT/s. Each of these options requires the application of up to 32 different filter combinations before determining actual jitter performance. Microsemi evaluates each of its clock synthesis products for all PCIe design options and filters to ensure that devices are fully compliant for use in PCIe clock generation applications.

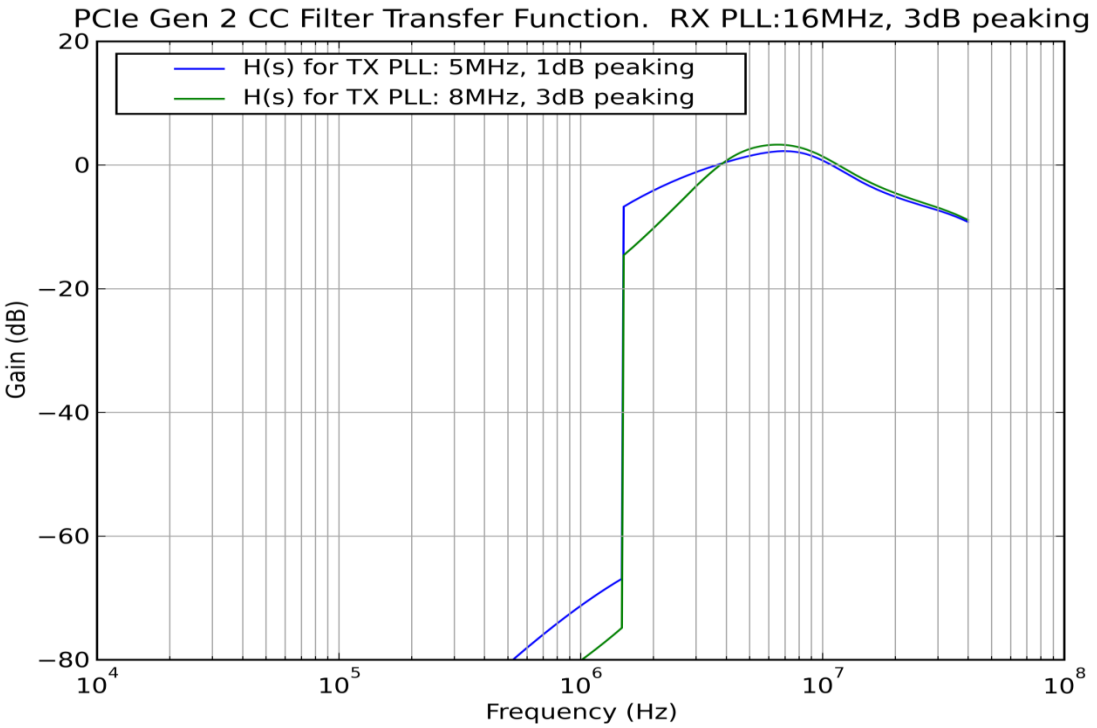
9. *References*

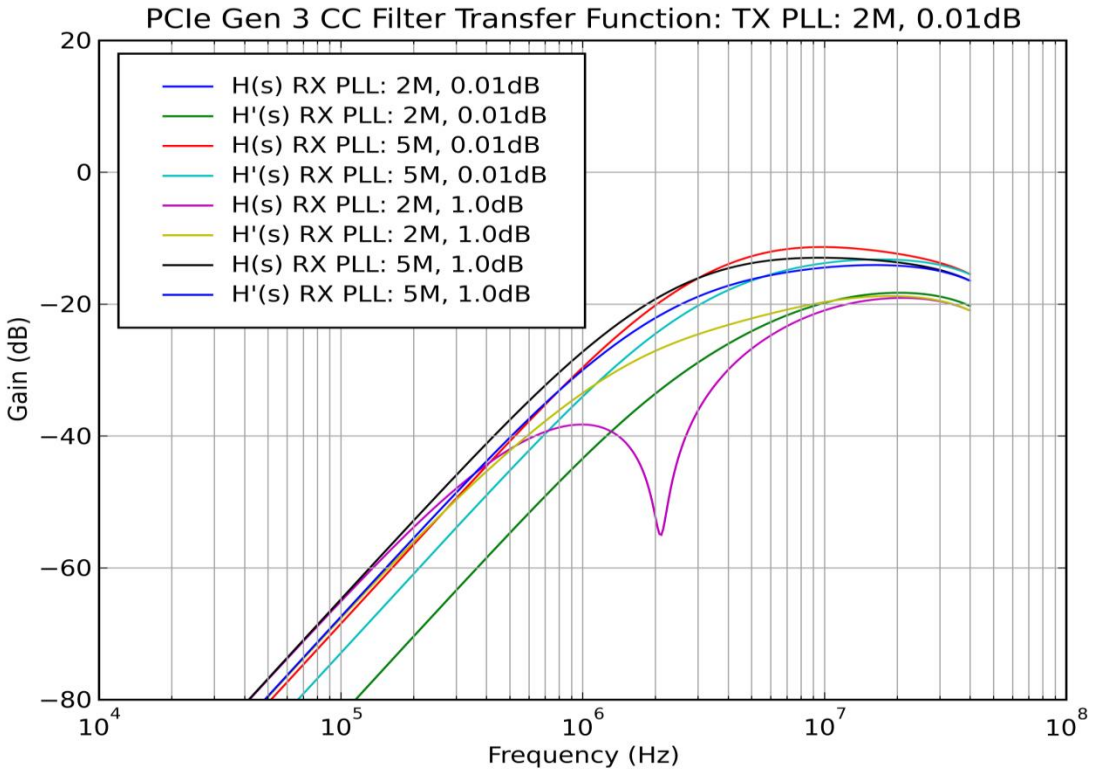
- PCI Express Base Specification Revision 1.1, March 28, 2005.
- PCI Express Base Specification Revision 2.1, March 4, 2009.
- PCI Express Base Specification Revision 3.0, November 10, 2010.
- PCI Express Card Electromechanical Specification Revision 2.0, April 11, 2007.

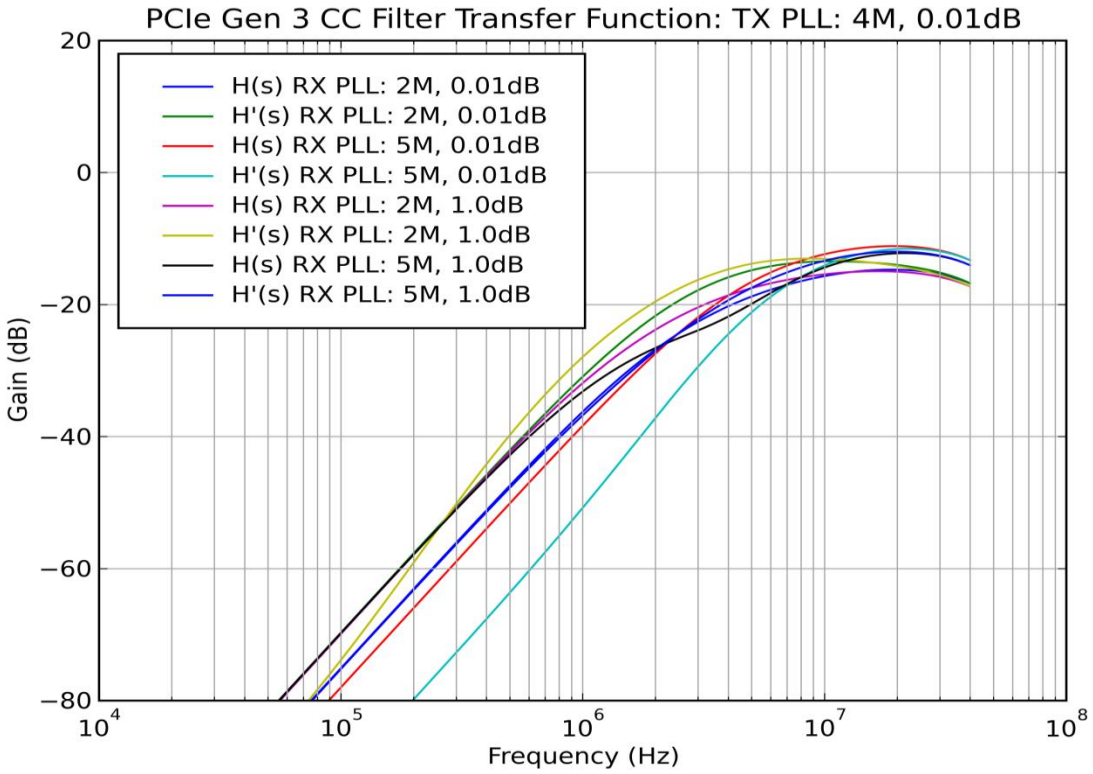
Appendix A. Transfer Function Graphs

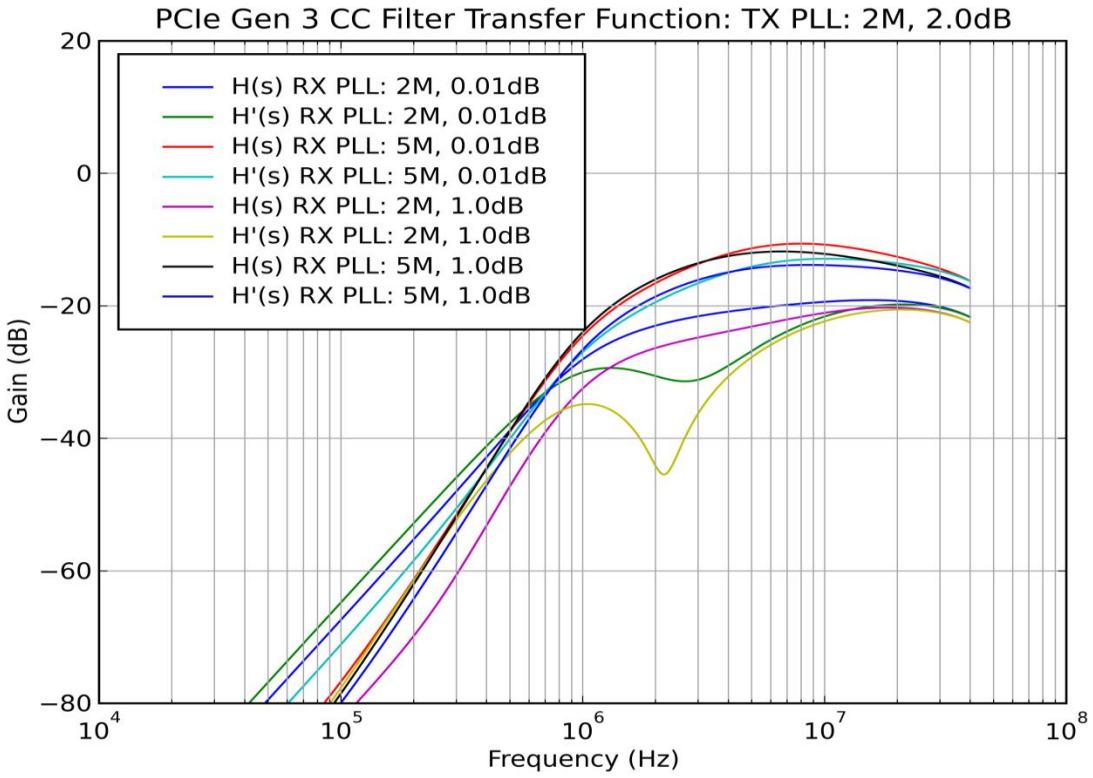
Common Refclk Rx Architecture

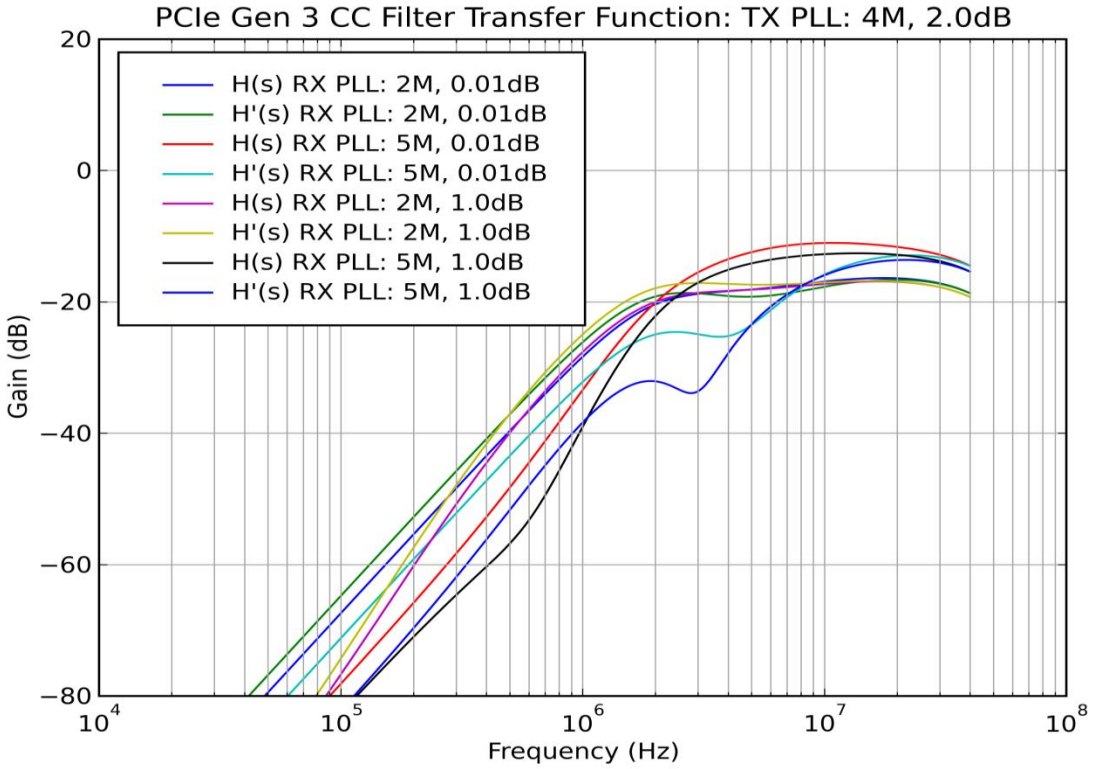




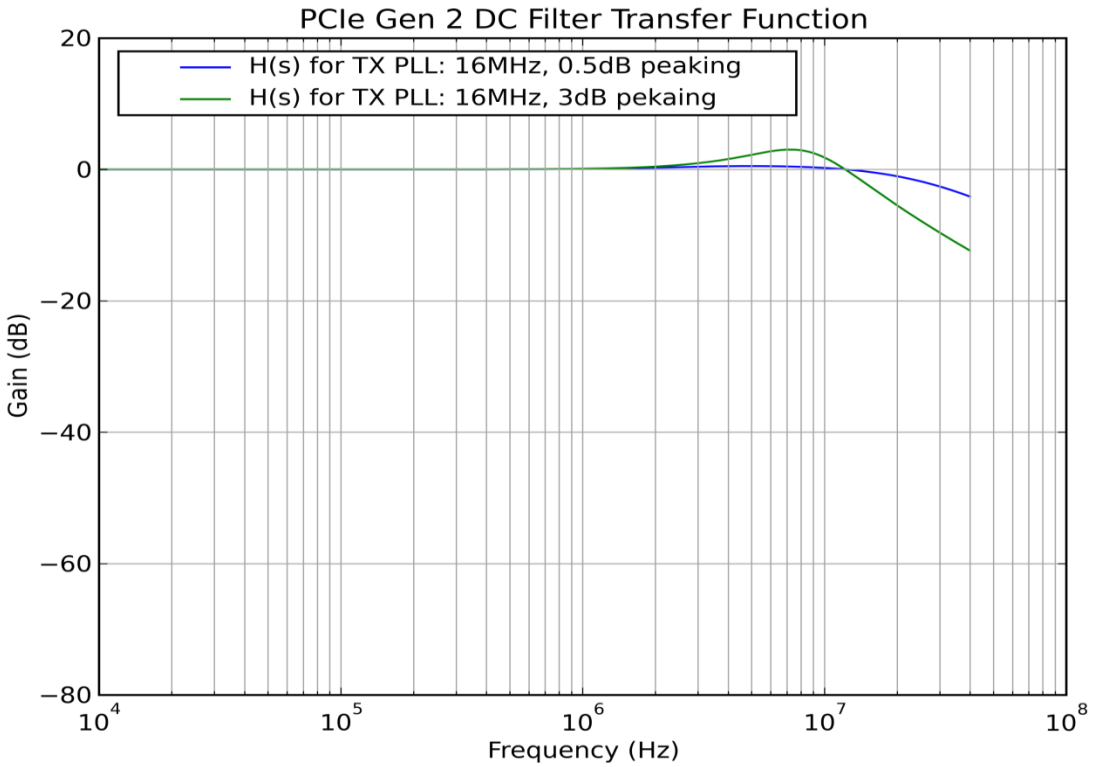

PCIe Gen 3 CC Filter Transfer Function: TX PLL: 2M, 0.01dB
H(s) RX PLL: 2M, 0.01dB
H'(s) RX PLL: 2M, 0.01dB
H(s) RX PLL: 5M, 0.01dB
H'(s) RX PLL: 5M, 0.01dB
H(s) RX PLL: 2M, 1.0dB
H'(s) RX PLL: 2M, 1.0dB
H(s) RX PLL: 5M, 1.0dB
H'(s) RX PLL: 5M, 1.0dB
Gain (dB)
Frequency (Hz)

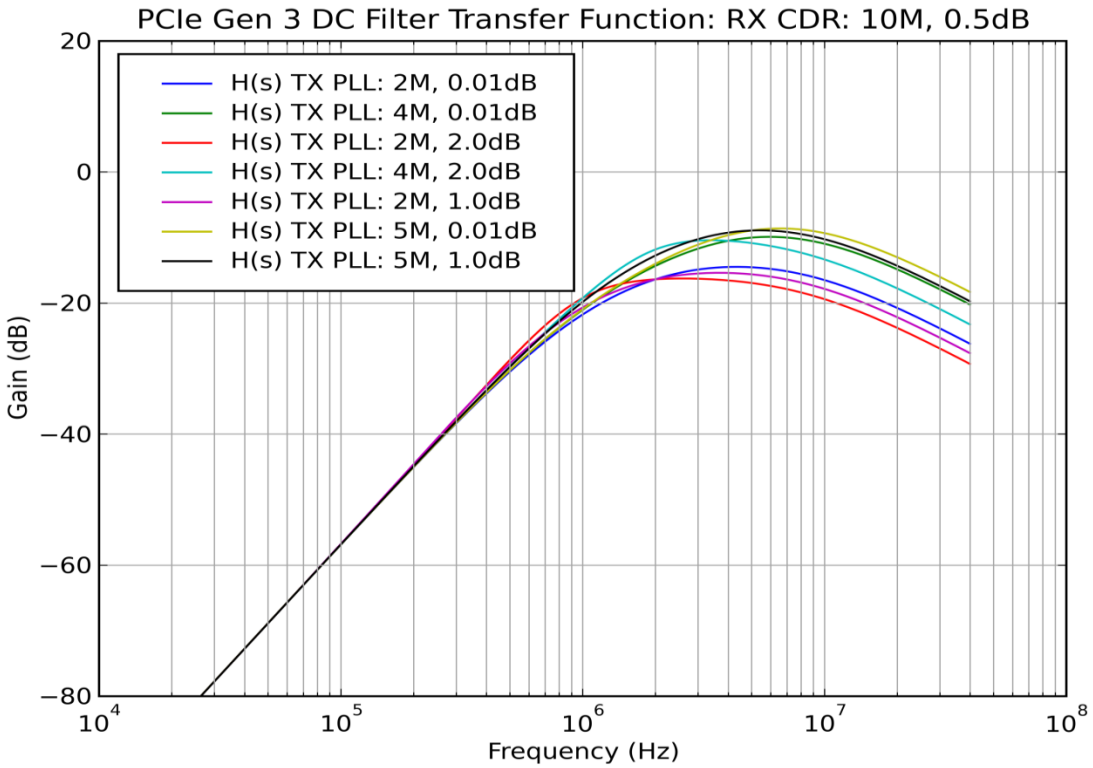

PCIe Gen 3 CC Filter Transfer Function: TX PLL: 4M, 0.01dB
H(s) RX PLL: 2M, 0.01dB
H'(s) RX PLL: 2M, 0.01dB
H(s) RX PLL: 5M, 0.01dB
H'(s) RX PLL: 5M, 0.01dB
H(s) RX PLL: 2M, 1.0dB
H'(s) RX PLL: 2M, 1.0dB
H(s) RX PLL: 5M, 1.0dB
H'(s) RX PLL: 5M, 1.0dB
Gain (dB)
Frequency (Hz)

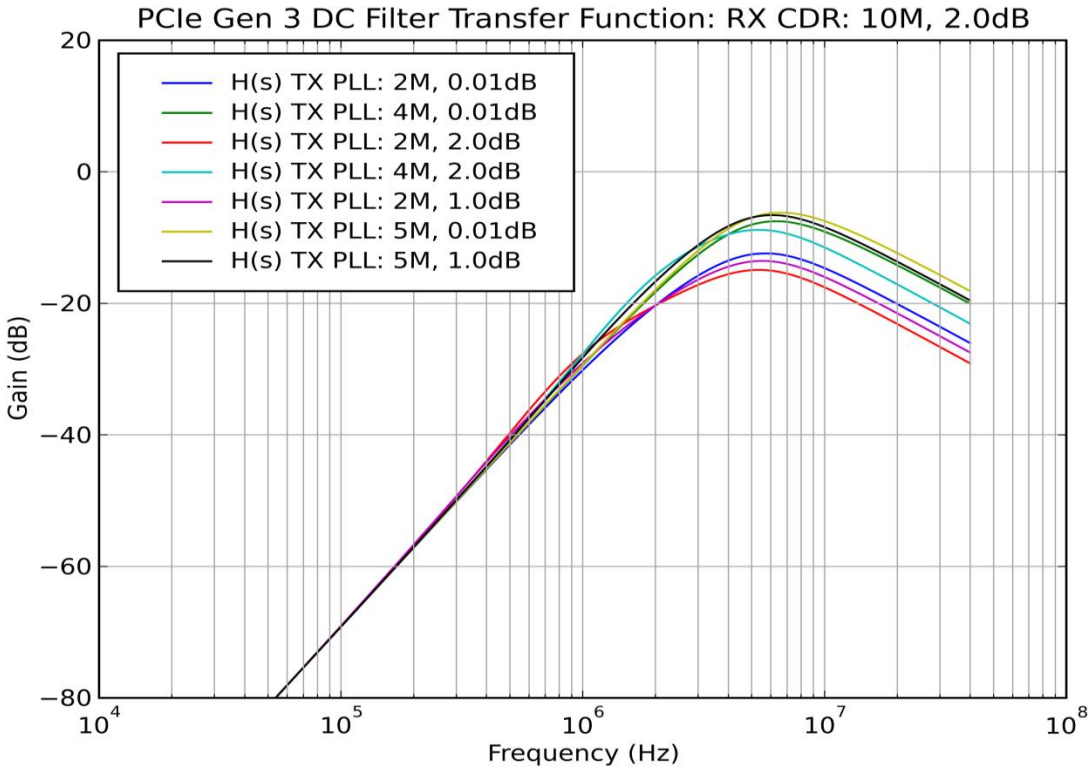

PCIe Gen 3 CC Filter Transfer Function: TX PLL: 2M, 2.0dB
H(s) RX PLL: 2M, 0.01dB
H'(s) RX PLL: 2M, 0.01dB
H(s) RX PLL: 5M, 0.01dB
H'(s) RX PLL: 5M, 0.01dB
H(s) RX PLL: 2M, 1.0dB
H'(s) RX PLL: 2M, 1.0dB
H(s) RX PLL: 5M, 1.0dB
H'(s) RX PLL: 5M, 1.0dB
Gain (dB)
Frequency (Hz)


PCIe Gen 3 CC Filter Transfer Function: TX PLL: 4M, 2.0dB
H(s) RX PLL: 2M, 0.01dB
H'(s) RX PLL: 2M, 0.01dB
H(s) RX PLL: 5M, 0.01dB
H'(s) RX PLL: 5M, 0.01dB
H(s) RX PLL: 2M, 1.0dB
H'(s) RX PLL: 2M, 1.0dB
H(s) RX PLL: 5M, 1.0dB
H'(s) RX PLL: 5M, 1.0dB
Gain (dB)
Frequency (Hz)

Data-Clocked Rx Architecture






PCIe Gen 3 DC Filter Transfer Function: RX CDR: 10M, 2.0dB
H(s) TX PLL: 2M, 0.01dB
H(s) TX PLL: 4M, 0.01dB
H(s) TX PLL: 2M, 2.0dB
H(s) TX PLL: 4M, 2.0dB
H(s) TX PLL: 2M, 1.0dB
H(s) TX PLL: 5M, 0.01dB
H(s) TX PLL: 5M, 1.0dB
Gain (dB)
20
0
−20
−40
−60
−80
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)

Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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