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SmartFusion2 and IGLOO2 CoreJESD204BRX and CoreJESD204BTX Interoperability

TR0022 Test Report

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Table of Contents

SmartFusion2 and IGLOO2 CoreJESD204BRX and CoreJESD204BTX Interoperability

Introduction

Microsemi provides solutions for interfacing to analog-to-digital converter (ADC) and digital -to-analog converter (DAC) devices using the JESD204B JEDEC standard. These solutions are provided as DirectCore IPs - CoreJESD204BRX and CoreJESD204BTX. Both of these are soft IPs interfacing to the high-speed serial interfaces (SERDESIF) of the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA devices.

This interoperability report gives the information that was obtained while working with third party ADC and DAC devices. The interoperability test results describe the JESD204B link parameters, hardware test setup, equipment used, and final test report of Microsemi DirectCores - CoreJESD204BRX and CoreJESD204BTX.

References

- *CoreJESD204BRX v2.5 Handbook*
- *CoreJESD204BTX v2.0 Handbook*
- *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*
- JESD204B - Serial Interface for Data Converters (Revision of JESD204B, July 2011). Date: January 2012 (www.jedec.org)
- AD9250 Datasheet from Analog Devices (www.analog.com)
- ISLA224S Datasheet from Intersil (www.intersil.com)
- DAC1658 Datasheet from IDT (www.idt.com)
- ADC34J44 Datasheet from Texas Instruments (www.ti.com)

Scope

The interoperability test results described in this report are limited to the JESD204B link. To develop a reference platform to work with JESD204B and third party ADC and DAC devices, other IP was used in the SmartFusion2 based design. This report describes the hardware setup used for interoperability testing and reporting the test results of the JESD204B link.

The SmartFusion2 and IGLOO2 JESD204B solution supports link widths of x1, x2, and x4 up to 3.2 Gbps per lane using subclass 0, 1, and 2.

Table 1 shows the configuration for the devices tested.

Table 1 • **Configuration for the Devices Tested**

Device	Link Rate	Link Width	Subclass
Analog Devices - AD9250	2.45 Gbps	x2	0, 1
Intersil - ISLA224S25	2.5 Gbps	x2	0, 2
IDT - DAC1658D1G5NLGA	2.5 Gbps	x2	0, 1
Texas Instruments - ADC34J44	2.5 Gbps	x4	0, 1, 2

Hardware Setup

The interoperability testing is carried out on the SmartFusion2 Advanced Development Kit (MS2150-ADV-KIT) and the FMC cards from the ADC and DAC vendors. The design for interoperability is developed using the Libero® SoC tool by instantiating the CoreJESD204BRX IP and CoreJESD204BTX IP cores in SmartDesign. Identify Debugger, JESD204B Demo GUI and serial terminal programs (for example, RealTerm) are used for the interoperability testing and for the ADC register configuration. CoreJESD204BRX IP is configured in JESD204B Subclass 0, Subclass 1 and Subclass 2 modes. CoreJESD204BTX IP is configured in JESD204B Subclass 0, Subclass 1 modes.

AD9250 Setup

AD9250 ADC is operated in two converters and two-lane mode. Each lane is operated in 2.45 Gbps mode. The fabric logic and SERDES blocks are operated with 122.8 MHz frequency.

Figure 1 shows the hardware setup for the interoperability testing with AD9250

***Figure 1* • Hardware Setup for Interoperability Testing with AD9250**

ISLA224S Setup

ISLA224S ADC is operated in two converters and two-lane mode. Each lane is operated in 2.5 Gbps mode. The fabric logic and SERDES blocks are operated with 125 MHz frequency.

Figure 2 shows the hardware setup for the interoperability testing with ISLA224S.

***Figure 2* • Hardware Setup for Interoperability Testing with ISLA224S**

DAC1658 Setup

DAC1658 DAC is operated in two converters, two-lane mode and the interpolation factor is two. Each lane is operated in 2.5 Gbps mode. The fabric logic and SERDES blocks are operated with 125 MHz frequency.

Figure 3 shows the hardware setup for the interoperability testing with DAC1658.

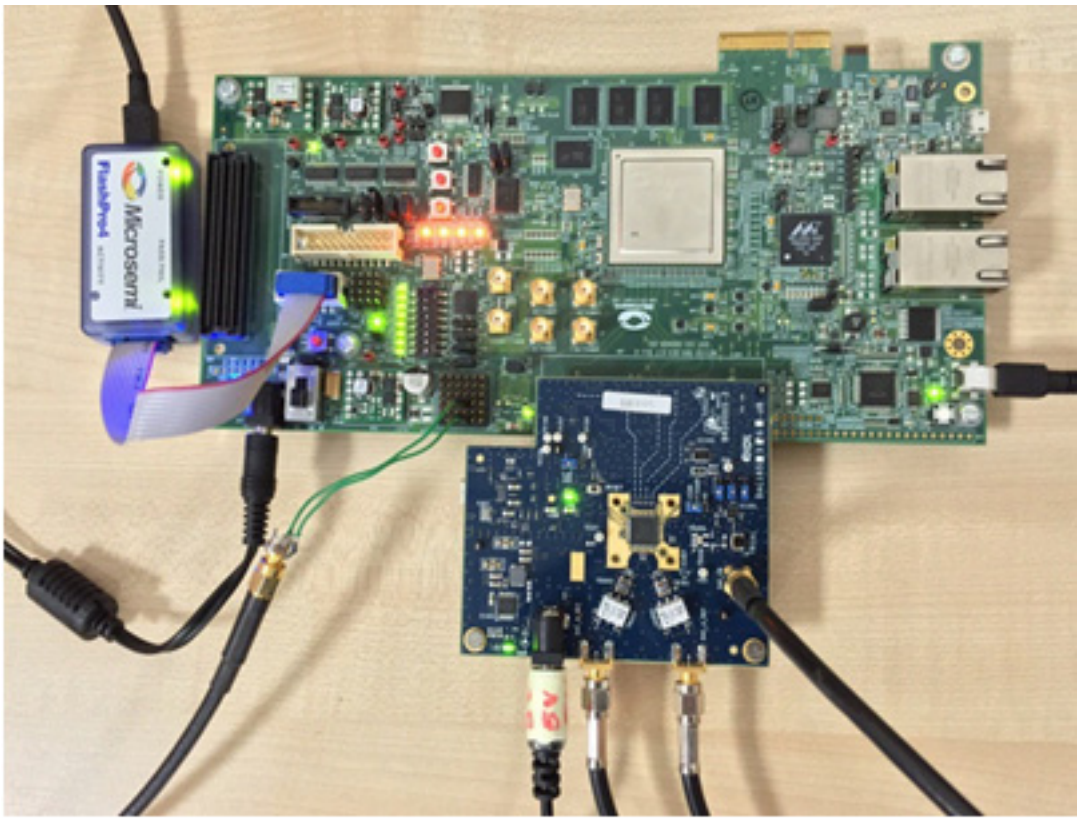

***Figure 3* • Hardware Setup for Interoperability Testing with DAC1658**

ADC34J44 Setup

ADC34J44 ADC is operated in four converters and four-lane mode. Each lane is operated at 2.5 Gbps mode. The fabric logic and SerDes blocks are operated at 125 MHz frequency.

Figure 4 hardware setup for interoperability testing with ADC34J44.

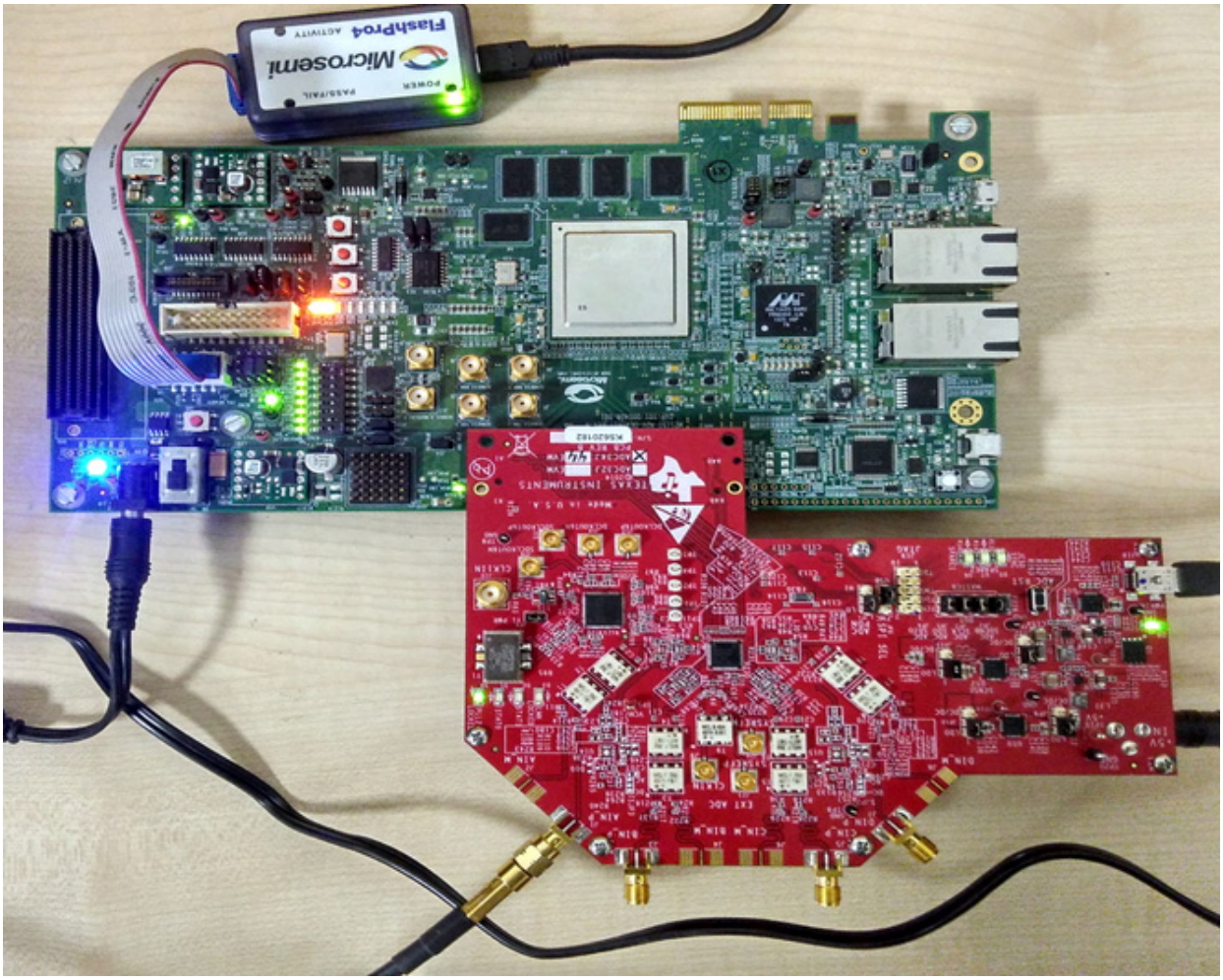

***Figure 4* • Hardware Setup for Interoperability Testing with ADC34J44**

Deterministic Latency Test Setup for ADC

A pulse signal was fed into the analog input of the ADC and channel A of an oscilloscope using a pulse generator. The most significant bit (MSB) of COREJESD204BRX DATA_OUT was routed to the BB_GPIO11 (FPGA pin number: P8) on the SmartFusion2 Advanced Development Kit. This was connected to the channel B on the oscilloscope.

With this setup the latency between the pulse entering the ADC and the MSB toggled at the output of the COREJESD204BRX IP can be measured.

Figure 5 shows the setup used to measure the deterministic latency.

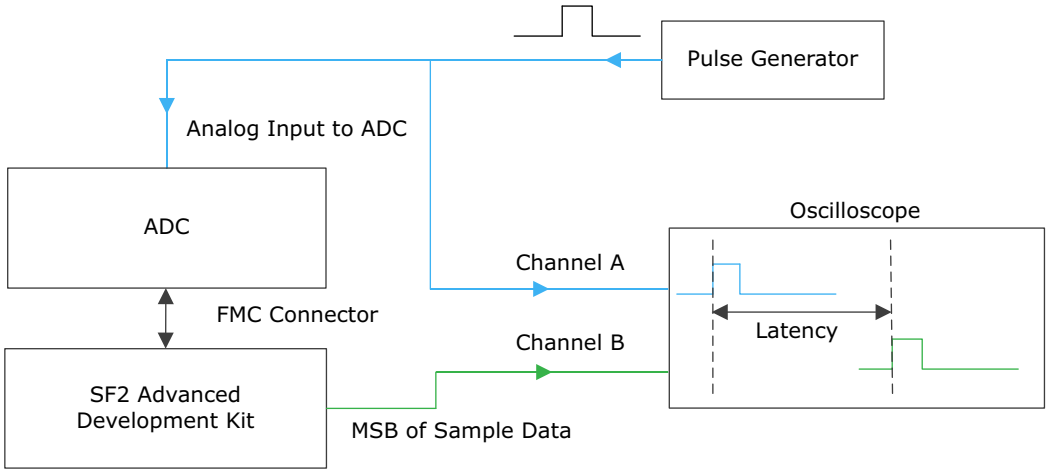

***Figure 5* • Deterministic Latency Setup - ADC**

Deterministic Latency Test Setup for DAC

A pulse signal was generated from the FPGA fabric and was fed to the DAC converter. The MSB of the generated pulse is routed to the BB_GPIO6 (FPGA pin number: P7) on the SmartFusion2 Advanced Development Kit. This was connected to the channel A on the oscilloscope. The analog output from DAC is connected to channel B on the oscilloscope.

With this setup the latency between the pulse sent from CoreJESD204BTX and the pulse observed at the DAC output can be measured.

Figure 6 shows the test setup used to measure the deterministic latency.

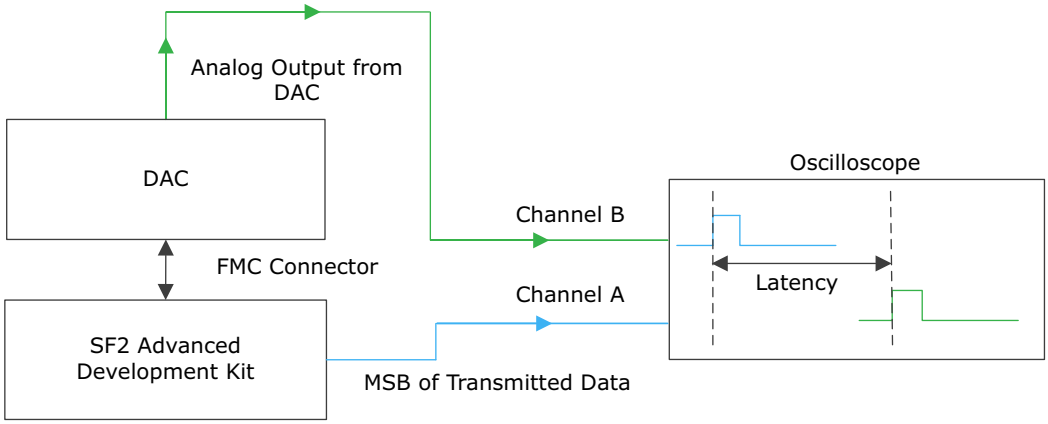

***Figure 6* • Deterministic Latency Setup - DAC**

Interoperability Tests

CoreJESD204BRX, AD9250, ISLA224S, and ADC34J44 are configured for interoperability testing, as shown in Table 2.

Table 2 • **JESD204B Parameter Settings**

Parameter	CoreJESD204 BRX Value	Analog Devices AD9250	Intersil ISLA224S	Texas Instruments ADC34J44	Description
SCR	0/1	0x1/0x0	0x1/0x0	0x1/0x0	Both scramble enable/disable
L	2	0x1	0x1	0x03	Number of lanes
F	2	0x1	0x1	0x1	Number of octets per frame
K	32	0x1F	0x1F	0x08	Number of frames per multi-frame
M	2	0x1	0x1	0x03	Number of converters
CS	0	0x0	0x0	0x0	Control bits per sample
N	14	0xD	0xD	0xD	Sample resolution
N'	16	0xF	0xF	0xF	Sample envelope
S	1	0x0	0x0	0x0	No of samples per converter per frame
HD	0	0x0	0x0	0x0	High density mode
CF	0	0x0	0x0	0x0	Control bits per frame
SUBCLASSV	0/1/2	0x0/0x1	0x0/0x2	0x0/0x1/0x2	Subclass0/Subclass1/Subclass2

CoreJESD204BTX and DAC1658 are configured for interoperability testing, as shown in Table 3.

Table 3 • **JESD204B Parameter Settings**

Parameter	CoreJESD204BTX Value	IDT DAC1658	Description
SCR	0/1	0x1 / 0x0	Scramble enable or disable
L	2	0x1	Number of lanes
F	2	0x1	Number of octets per frame
K	32	0x1F	Number of frames per multi-frame
M	2	0x1	Number of converters
CS	0	0x0	Control bits per sample
N	16	0xF	Sample resolution
N'	16	0xF	Sample envelope
S	1	0x0	No of samples per converter per frame
HD	0	0x0	High density mode
CF	0	0x0	Control bits per frame
SUBCLASSV	0/1	0x0/0x1	Subclass0/Subclass1/Subclass2

The following tests are performed for the interoperability report:

- Test1: Data Link Layer - Code Group Synchronization
- Test2: Data Link Layer - Initial Lane alignment sequence
- Test3: Receiver Transport Layer
- Test4: Descrambling
- Test5: Deterministic latency

AD9250 Interoperability Tests

Test1: Data Link Layer - Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/=/K28.5/. Identify debugger is used to monitor the operation of the receiver data link layer.

Table 4 shows the data link layer - code group synchronization test results.

Table 4 • Data Link Layer - Code Group Synchronization Test Results

Test Case	Objective	Description	Passing Criteria	Result
AD1.1	Check if the receiver asserts SYNC_N signal when the link is down	CoreJESD204BRX _0 → SYNC_N signal is observed in Identify Debugger	SYNC_N goes low	Passed
AD1.2	Check if SYNC_N request is deasserted after the correct reception of at least four successive /K/ characters	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0],SYNC_N signals are observed in Identify Debugger	K28.5 or /K/ character (0xBC) is observed on DATA_OUT and SYNC_N is deasserted after the correct reception of at least four successive /K/ characters.	Passed
AD1.3	Check the full code group synchronization at receiver after the correct reception of another four 8B/10B characters	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0], SYNC_N,CGS_ERR[1:0] signals are observed in Identify Debugger	CGS error not asserted	Passed

Test2: Data Link Layer - Initial Lane Alignment Sequence

Table 5 shows the data link layer - initial lane alignment sequence test results.

Table 5 • Data Link Layer-Initial Lane Alignment Sequence Test Results

Test Case	Objective	Description	Passing Criteria	Result
AD2.1	Check if the ILAS phase starts after the CGS phase	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[1:0],SOMF_L[1:0], SOF_U[1:0],SOF_L[1:0] signals are observed in Identify Debugger	Multi-frame starts with 0x1C and is aligned with SOMF_U[1:0]	Passed
AD2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[1:0],SOMF_L[1:0], SOF_U[1:0],SOF_L[1:0], LINK_CD_ERROR[1:0] signals are observed in Identify Debugger	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data	Passed

Test3: Receiver Transport Layer

Table 6 shows the receiver transport layer test results.

Table 6 • Receiver Transport Layer Test Results

Test Case	Objective	Description	Passing Criteria	Result
AD3.1	Check data integrity in test mode	ADC is configured in PRBS test mode. PRBS checker in the FPGA fabric checks for data reliability. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] RX_PRBS_16 → O_error[3:0],O_bad signals are observed in Identify Debugger	RX_PRBS_16 → O_bad signal not asserted	Passed
AD3.2	Check data integrity in normal mode	ADC is configured in normal mode. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	Received signal correlates with the input signal given for ADC sampling.	Passed

Test4: Descrambling

Scrambler is enabled in ADC and descrambler is enabled in CoreJESD204BRX IP.

Table 7 shows the descrambling test results.

Table 7 • Descrambling Test Results

Test Case	Objective	Description	Passing Criteria	Result
AD4.1	Check descrambler functionality	ADC is configured in PRBS test mode. PRBS checker in the FPGA fabric checks for data reliability. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] RX_PRBS_16 → O_error[3:0], O_bad signals are observed in Identify Debugger	RX_PRBS_16 → O_bad signal should not be asserted	Passed

Test5: Deterministic Latency

CoreJESD204BRX IP is configured in Subclass 1 mode and AD9250 is configured in different LMF modes.

Table 8 shows the CoreJESD204BRX IP parameter settings for different ADC modes.

Table 8 • CoreJESD204BRX IP Parameter Settings for different ADC Modes

ADC Mode	M	L	F	K
11	1	1	2	32
21	2	1	4	32
22	2	2	2	32

Table 9 shows the JESD204B deterministic latency measurement test results.

Table 9 • JESD204B Deterministic Latency Measurement Test Results

Test Case	Objective	Description	Passing Criteria	Result
AD5.1	Check LMFC alignment	CoreJESD204BRX _0 → clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger	SYSREF_IN aligned with clkgen_lmfc	Passed
AD5.2	SYSREF capture	CoreJESD204BRX _0 → c2l_mf_phase and SYSREF_IN signals are observed in Identify Debugger	LMFC counter restarts after the SYSREF_IN capture	Passed
AD5.3	Check the latency	A single pulse input is applied to the ADC and the oscilloscope channel A using 2-port splitter. Core output MSB is connected to the oscilloscope channel B. The delay between captured pulses on channel A and Channel B is measured.	Latency fixed for multiple runs (between the FPGA resets/link resets)	Passed
AD5.4	Check the data latency during user data phase	Check if the data latency is fixed during the user data phase. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	The ramp pattern is seen without distortion	Passed

ISLA224S Interoperability Tests

Test1: Data Link Layer - Code Group Synchronization

When the link starts, the receiver issues a synchronization request and the transmitter emits comma characters /K/=/K28.5/. The receiver data link layer operation is monitored by Identify Debugger.

Table 10 shows the data link layer - code group synchronization test results.

Table 10 • **Data Link Layer - Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Result
ISL1.1	Check if the receiver asserts SYNC_N signal when the link is down	CoreJESD204BRX _0 → SYNC_N signal is observed in Identify Debugger	SYNC_N goes low	Passed
ISL1.2	Check if SYNC_N request is deasserted after the correct reception of at least four successive /K/ characters	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0],SYNC_N signals are observed in Identify Debugger	K28.5 or /K/ character (0xBC) is observed on DATA_OUT and SYNC_N is deasserted after the correct reception of at least four successive /K/ characters.	Passed
ISL1.3	Check full code group synchronization at the receiver after the correct reception of another four 8B/10B characters	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0], SYNC_N,CGS_ERR[1:0] signals are observed in Identify Debugger	CGS error not asserted	Passed

Test2: Data Link Layer -Initial Lane Alignment Sequence

Table 11 shows the data link layer - initial lane alignment sequence test results.

Table 11 • **Data Link Layer - Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Result
ISL2.1	Check if the ILAS phase starts after the CGS phase	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[1:0],SOMF_L[1:0], SOF_U[1:0],SOF_L[1:0] signals are observed in Identify Debugger	Multi-frame starts with 0x1C and is aligned with SOMF_U[1:0]	Passed
ISL2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[1:0],SOMF_L[1:0], SOF_U[1:0],SOF_L[1:0], LINK_CD_ERROR[1:0] signals are observed in Identify Debugger	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data	Passed

Test3: Receiver Transport Layer

Table 12 shows the receiver transport layer test results.

Table 12 • Receiver Transport Layer Test Results

Test Case	Objective	Description	Passing Criteria	Result
ISL3.1	Check data integrity in test mode	ADC is configured in PRBS test mode. PRBS checker in the FPGA fabric checks for data reliability. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] RX_PRBS_16 → O_error[3:0], O_bad signals are observed in Identify Debugger	RX_PRBS_16 → O_bad signal not asserted.	Passed
ISL3.2	Check data integrity in normal mode	ADC is configured in normal mode. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	Received signal correlates with the input signal given for ADC sampling.	Passed

Test4: Descrambling

Scrambler is enabled in ADC and descrambler is enabled in CoreJESD204BRX IP.

Table 13 shows the descrambling test results.

Table 13 • Descrambling Test Results

Test Case	Objective	Description	Passing Criteria	Result
ISL4.1	Check descrambler functionality	ADC is configured in PRBS test mode. PRBS checker in the FPGA fabric checks for data reliability. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] RX_PRBS_16 → O_error[3:0], O_bad signals are observed in Identify Debugger	RX_PRBS_16 → O_bad signal not asserted	Passed

Test5: Deterministic Latency

CoreJESD204BRX IP is configured in Subclass 2 mode and ISLAS224S is configured in L=2 and M=2 modes.

Table 14 shows the deterministic latency test results.

Table 14 • **Deterministic Latency Test Results**

Test Case	Objective	Description	Passing Criteria	Result
ISL5.1	SYNC_N capture	CoreJESD204BRX _0 → c2l_mf_phase and SYNC_N signals are observed in Identify Debugger	LMFC counter restarts after the SYNC_N capture	Passed
ISL5.2	Check the latency	A single pulse input is applied to the ADC and the oscilloscope channel A using 2-port splitter. Core output MSB is connected to the oscilloscope channel B. The delay between captured pulses on channel A and Channel B is measured.	Latency fixed for multiple runs (between the FPGA resets/link resets)	Passed
ISL5.3	Check the data latency during user data phase	Check if the data latency is fixed during the user data phase. CoreJESD204BRX _0 → DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	The ramp pattern is seen without distortion	Passed

DAC1658 Interoperability Tests

Test1: Data Link Layer - Code Group Synchronization

When the link starts, the receiver issues a synchronization request and the transmitter emits comma characters /K/=/K28.5/. The transmitter data link layer operation is monitored by Identify Debugger.

Table 15 shows the data link layer - code group synchronization test results.

Table 15 • **Data Link Layer - Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Result
IDT1.1	Check if SYNC_Request is deasserted on SYNC_N assertion.	CoreJESD204BTX _0 → SYNC_request signal is observed in Identify Debugger	SYNC_request goes low	Passed
IDT1.2	Check if at least four successive /K/ characters are transmitted on SYNC_N assertion	CoreJESD204BTX _0 → EPCS_0_TX_DATA[19:0], EPCS_1_TX_DATA[19:0], SYNC_N signals are observed in Identify Debugger	At least four K28.5 or /K/ characters are observed on EPCS_0_TX_DATA, EPCS_1_TX_DATA, on assertion of SYNC_N	Passed
IDT1.3	Check full code group synchronization at the transmitter after the correct transmission of another four 8B/10B characters	CoreJESD204BTX _0 →TX_STATE[1:0] signal is observed in Identify Debugger Check the DAC register CS_STATE_LNX (address 00EDh).	CoreJESD204BTX TX_STATE changes from SYNC_ST(0x00) to INIT_LANE_ST (0x01). DAC register CS_STATE_LNX is in CS_DATA (0x02) state.	Passed

Test2: Data Link Layer -Initial Lane Alignment Sequence

Table 16 shows the data link layer - initial lane alignment sequence test results.

Table 16 • Data Link Layer - Initial Lane Alignment Sequence Test Results

Test Case	Objective	Description	Passing Criteria	Result
IDT2.1	Check the ILAS phase	1. *CoreJESD204BTX_0 → EPCS_0_TX_DATA[19:0], EPCS_1_TX_DATA[19:0], Signals are observed in Identify Debugger.* 2. *Check DAC K28 registers.*	1. *Observe the /R/, /A/, /Q/ in the correct order as per ILAS.* 2. *The flags /R/, /A/, /Q/ and /K/ set in DAC K28 registers*	Passed
IDT2.2	Check the JESD configuration data	Check if the DAC has received the expected configuration data.	DAC link configuration data matches with CoreJESD204BTX link configuration data	Passed
IDT2.3	Check if ILA phase is completed successfully	1. *CoreJESD204BTX_0 → TX_STATE[1:0] Signal is observed in Identify Debugger.* 2. *Check if the DAC has achieved ILA.*	1. *CoreJESD204BTX TX_STATE changes from INIT_LANE_ST (0x01) to DATA_ENC_ST (0x02).* 2. *In DAC ila_rcv_flag goes high.*	Passed

Test3: Receiver Transport Layer

Table 17 shows the receiver transport layer test results.

Table 17 • Receiver Transport Layer Test Results

Test Case	Objective	Description	Passing Criteria	Result
IDT3.1	Check the data phase	Check if the expected waveform is obtained at the DAC outputs.	Observe the expected waveform on the scope.	Passed
IDT3.2	Check the data rate	CoreJESD204BTX transfer data at 2.5 Gbps per lane for LMF=222.	Observe the expected waveform on the scope.	Passed

Test4: Descrambling

Scrambler is enabled in ADC and descrambler is enabled in CoreJESD204BTX IP.

Table 18 shows the descrambling test results.

Table 18 • Descrambling Test Results

Test Case	Objective	Description	Passing Criteria	Result
IDT4.1	Check the scrambler functionality	Enable scrambler and check data at the output.	Observe the expected waveform on the scope.	Passed

Test5: Deterministic latency

CoreJESD204BTX IP is configured in Subclass 1 mode and DAC1658 is configured in LMF = 222 mode and interpolation factor = 2.

Table 19 shows the deterministic latency test results.

***Table 19* • Deterministic Latency Test Results**

Test Case	Objective	Description	Passing Criteria	Result
IDT5.1	Check the LMFC alignment	CoreJESD204BTX _0 → clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger	SYSREF_IN aligned with clkgen_lmfc	Passed
IDT5.2	SYSREF capture	CoreJESD204BTX _0 → c2l_mf_phase and SYSREF_IN signals are observed in Identify Debugger	LMFC counter restarts after the SYSREF_IN capture	Passed
IDT5.3	Check the latency	A single pulse input generated in FPGA is sent to the DAC and the oscilloscope channel A. The DAC output is connected to oscilloscope channel B. The delay between captured pulses on channel A and Channel B is measured.	Latency fixed for every link reset. (SYNC_N ON/OFF).	Passed

ADC34J44 Interoperability Tests

Test1: Data Link Layer - Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/=/K28.5/. Identify the debugger that is used to monitor the operation of the receiver data link layer.

Table 20 shows the data link layer - code group synchronization test results.

***Table 20* • Data Link Layer - Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC1.1	Check if the receiver asserts SYNC_N signal when the link is down	CoreJESD204BRX _0 → SYNC_N signal is observed in Identify Debugger	SYNC_N goes low	Passed
TI_ADC1.2	Check if SYNC_N request is deasserted after the correct reception of at least four successive /K/ characters	CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0],SYNC_N signals are observed in Identify Debugger	K28.5 or /K/ character (0xBC) is observed on DATA_OUT and SYNC_N is deasserted after the correct reception of at least four successive /K/ characters.	Passed
TI_ADC1.3	Check the full code group synchronization at receiver after the correct reception of another four 8B/10B characters	CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0], SYNC_N,CGS_ERR[1:0] signals are observed in Identify Debugger	CGS error not asserted	Passed

Test2: Data Link Layer - Initial Lane Alignment Sequence

Table 21 shows the data link layer - initial lane alignment sequence test results.

Table 21 • Data Link Layer-Initial Lane Alignment Sequence Test Results

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC2.1	Check if the ILAS phase starts after the CGS phase	CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[3:0],SOMF_L[3:0], SOF_U[1:0],SOF_L[1:0] signals are observed in Identify Debugger	Multi-frame starts with 0x1C and is aligned with SOMF_U[3:0]	Passed
TI_ADC2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] SOMF_U[3:0],SOMF_L[3:0], SOF_U[3:0],SOF_L[3:0], LINK_CD_ERROR[3:0] signals are observed in Identify Debugger	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data	Passed

Test3: Receiver Transport Layer

Table 22 shows the receiver transport layer test results.

Table 22 • Receiver Transport Layer Test Results

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC3.1	Check data integrity in test mode	ADC is configured in PRBS transport layer test mode CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	Observe the DATA_OUT for PRBS pattern	Passed
TI_ADC3.2	Check data integrity in normal mode	ADC is configured in normal mode CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	Received signal correlates with the input signal given for ADC sampling.	Passed

Test4: Descrambling

Scrambler is enabled in ADC and descrambler is enabled in the CoreJESD204BRX IP.

Table 23 shows the descrambling test results.

***Table 23* • Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC4.1	Check descrambler functionality	ADC is configured in PRBS Transport layer test mode CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	Observe the DATA_OUT for PRBS pattern	Passed

Test5.1: Deterministic Latency

The CoreJESD204BRX IP is configured in subclass 1 mode and ADC34J44 is configured in subclass 1 mode with parameters LMFK = 4429.

Table 24 shows the JESD204B deterministic latency measurement test results.

***Table 24* • JESD204B Deterministic Latency Measurement Test Results**

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC5.1.1	Check LMFC alignment	CoreJESD204BRX _0 → clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger	SYSREF_IN is aligned with clkgen_lmfc	Passed
TI_ADC5.1.2	SYSREF capture	CoreJESD204BRX _0 → c2l_mf_phase and SYSREF_IN signals are observed in Identify Debugger	LMFC counter restarts after the SYSREF_IN capture	Passed
TI_ADC5.1.3	Check latency	A single pulse input is applied to ADC and the oscilloscope channel A using 2-port splitter. Core output MSB is connected to the oscilloscope channel B. The delay between captured pulses on channel A and Channel B is measured	Latency is fixed for multiple runs (between the FPGA resets/link resets)	Passed
TI_ADC5.1.4	Check the data latency during user data phase	Check if the data latency is fixed during the user data phase. CoreJESD204BRX _0 CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	The ramp pattern is seen without distortion	Passed

Test5.2: Deterministic Latency

The CoreJESD204BRX IP is configured in subclass 2 mode and ADC34J44 is configured in subclass 2 mode with parameters LMFK = 4429.

Table 25 shows the JESD204B deterministic latency measurement test results.

***Table 25* • JESD204B Deterministic Latency Measurement Test Results**

Test Case	Objective	Description	Passing Criteria	Result
TI_ADC5.2.1	SYNC_N capture	CoreJESD204BRX _0 → c2l_mf_phase and SYNC_N signals are observed in Identify Debugger	LMFC counter and the SYNC_N signals should be aligned	Passed
TI_ADC5.2.2	Check latency	A single pulse input is applied to ADC and the oscilloscope channel A using 2-port splitter. Core output MSB is connected to the oscilloscope channel B The delay between captured pulses on channel A and Channel B is measured	Latency is fixed for multiple runs (between the FPGA resets/core resets)	Passed
TI_ADC5.2.3	Check the data latency during user data phase	Check if the data latency is fixed during the user data phase. CoreJESD204BRX _0 → DATA_OUT[63:48], DATA_OUT[47:32], DATA_OUT[31:16], DATA_OUT[15:0] signals are observed in Identify Debugger	The ramp pattern is seen without distortion	Passed

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 2 (June 2016)	Updated Table 1 for ADC34J44 device entry (SAR 80233).	3
	Added a third-part reference in the "References" section (SAR 80233).	3
	Added the "ADC34J44 Setup" section in this document (SAR 80233).	7
	Added the ADC34J44 entry in the "Interoperability Tests" section and added the ADC34J44 related details in Table 2 (SAR 80233).	9 and 9
	Added "ADC34J44 Interoperability Tests" section in the document (SAR 80233).	17
Revision 1 (August 2015)	Initial release	N/A

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