DG0633
Demo Guide
IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback
Demo - Libero SoC v11.7 SP2
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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Libero SoC and FlashPro design requirements were updated. For more information, see Design Requirements, page 2.
- Throughout the document, all the associated figures were updated.

1.2 Revision 2.0

In revision 2.0 of this document, updated the document for Libero SoC v11.7 software release.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.
2.1 Design Requirements

The following table lists the design requirements for running the demo.

<table>
<thead>
<tr>
<th>Hardware Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGLOO2 Evaluation Kit:</td>
<td>Rev D or later</td>
</tr>
<tr>
<td>• 12 V adapter</td>
<td></td>
</tr>
<tr>
<td>• FlashPro4 programmer</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop (12 GB RAM)</td>
<td>Windows 64-bit Operating System</td>
</tr>
<tr>
<td>Spirent Test Center (Optional)</td>
<td></td>
</tr>
</tbody>
</table>
Table 1 • Design Requirements (continued)

| Software Requirements                      |  
| Libero SoC                                 | v11.7 SP2   |
| FlashPro Programming Software              | v11.7 SP2   |
| Cat Karat Packet Generator Software        | Provided with design files |
| Wireshark Software                         | Provided with design files |

| IP Requirements                             |  
| CoreTSE MAC                                 | License provided on request |

2.2 Demo Design

The demo design files are available for download from the following path:

http://soc.microsemi.com/download/rsc/?f=m2gl_dg0633_liberov11p7sp2_df

The demo design files include:

- Libero project
- Programming files
- Source files
- Readme.txt file

See the Readme.txt file for the complete directory structure.

The following figure shows the top-level structure of the design files.

Figure 1 • Demo Design Files Top-Level Structure

```
 m2gl_dg0633_liberov11p7sp2_df
    |________________________|
    | CoreTSE_1000BaseT_Demo |
    |_______________________|
             |________________________|
             | Libero                 |
             |________________________|
             | ProgrammingFile        |
             |________________________|
             | Source files            |
             |________________________|
             | Readme.txt               |
```
The following figure shows the demo design block diagram.

**Figure 2 • IGLOO2 CoreTSE MAC 1000 Base-T Loopback Demo**

In this demo design CoreTSE MAC is instantiated in the FPGA fabric and connected to the on-board Ethernet PHY using high-speed serial interface (SERDES_IF).

In the previous figure, the dotted arrow in red shows the transfer of Ethernet packet from the host PC to the internal LSRAM and the dotted arrow in blue shows the retransmission of packet from LSRAM to the host.

### 2.2.1 Demo Design Features

The demo design performs Ethernet loopback using CoreTSE MAC in TBI 1000 Base-T on hardware and also in simulation.

Following are the demo design features:

- Simulation model for CoreTSE MAC loopback design.
- CoreTSE MAC loopback design on IGLOO2 Evaluation Kit.

The following section explains the initialization and configuration of CoreTSE MAC, SERDES_IF, and the loopback mechanism.

#### 2.2.1.1 CoreTSE IP MAC Initialization

CoreTSE MAC is configured in TBI mode. The CoreABC soft-core is used to initialize CoreTSE MAC in 1000 Base-T and on-board Ethernet PHY.

*Note:* CoreABC is a Microsemi RISC processor that is implemented in logic gates. The CoreABC IP is available in the Libero SoC software IP tools catalog.

#### 2.2.1.2 High-Speed Serial Interface Configuration

The high-speed SERDES_IF is configured in the external physical coding sub layer (EPCS) mode lane 3 in the Libero GUI and is connected between CoreTSE MAC and on-board Ethernet PHY.

#### 2.2.1.3 Ethernet Packet Loopback

The following Ethernet loopback mechanism is used in this demo:

* **2.2.1.3.1 Ethernet Packet Reception**

  The CoreTSE MAC receives the Ethernet packet from on-board Ethernet PHY through high-speed SERDES_IF.

  The CoreTSE MAC receive (RX) path is connected to LSRAM through the receive interface logic. This interface logic is implemented in Verilog RTL and is used to keep the packet on to LSRAM memory.
2.2.1.3.2 Ethernet Packet Transmission

To loopback the Ethernet packet, the interface logic implemented in Verilog RTL reads the Ethernet packet data from LSRAM memory and keeps it on CoreTSE MAC transmit (TX) path.

CoreTSE MAC transmits the Ethernet packet to on-board Ethernet PHY through high-speed SERDES.

2.2.1.4 Ethernet Test Solution

There are many ways to evaluate the CoreTSE MAC 1000 Base-T loopback demo on the IGLOO2 Evaluation Board.

2.2.1.4.1 Solution 1

- The Cat Karat packet generator software installed on the host PC is used to transmit the Ethernet packet through RJ45 Ethernet copper cable.
- The Wireshark packet receiver software installed on the host PC captures the Ethernet packet (loopback) through RJ45 Ethernet copper cable.

2.2.1.4.2 Solution 2

Spirent test center or an equivalent solution can be used to test the CoreTSE MAC loopback demo. For more information, see Appendix: Running the Demo Design Using Spirent Test Center, page 16.

2.2.2 Demo Design Description

This demo design is implemented by configuring the CoreTSE MAC for the TBI mode. The following figure shows the Libero SoC hardware implementation for this demo design.

Figure 3 • Libero SmartDesign

Libero hardware project uses the following resources:

- CoreTSE MAC
- CoreABC to configure CoreTSE MAC and on-board Ethernet PHY
- LSRAM interface logic uses TPSRAM, receives and transmits logic implemented in Verilog RTL
- High-speed serial interface (SERDES_IF) configured for EPCS lane 3 mode
- Dedicated input pad 0 as the clock source
2.3 Simulating the Design

The testbench design is created for CoreTSE MAC loopback demo. The testbench transmits the Ethernet packet to CoreTSE MAC loopback demo design and receives the loopback Ethernet packet from the CoreTSE MAC loopback demo design.

2.3.1 Simulation

For simulation, the Ethernet packet is defined in a text file:

\(\text{m2gl_dg0633_liberov11p7sp2_df(CoreTSE_1000BaseT_DemoLibero\Simulation\CoreTSE_1000BaseT_Demo\simulation\packetfile.txt)}\).

The Raw Ethernet Packet frame is:

0102030405060708090a0b0c0d0e5555555555555555555555551b1c1d1e1f202122232425262728292a2b2c2d2e2f3031323333435363738393a3b3c3d3e3f40.

Testbench reads the Ethernet packet from the text file and puts the Ethernet packet on to the high-speed SERDES_IF of CoreTSE MAC loopback design.

The loopback packet is received by the testbench and displayed on the ModelSim transcript window.

The following figure and Figure 5, page 7 show the Libero SmartDesign to simulate the CoreTSE MAC loopback demo design. The simulation testbench has the following Libero components:

- CoreTSE MAC
- High-speed SERDES_IF
- Testbench with packet transmit and packet receive logic

The testbench smart design module reads the Ethernet packet from the packetfile.txt file and sends it to the IGLOO2 CoreTSE MAC loopback design through high-speed serial interface. The loopback Ethernet packet is received by the testbench through high-speed serial interface. ModelSim displays the received Ethernet packet on the transcript window. This completes the Ethernet packet loopback simulation.

Figure 4 • SmartDesign for Simulation
The Libero SmartDesign top module contains the CoreTSE MAC loopback design and the testbench module.

Figure 5 • Libero SmartDesign Top Module

The following steps describe how to simulate the demo:

1. Open the Libero project from the following design files:
   \m2gl_dg0633_liberov11p7sp2_df\CoreTSE_1000BaseT_Demo\Libero\Simulation\CoreTSE_1000BaseT_Demo\CoreTSE_1000BaseT_Demo.prjx.

2. In the Design Flow tab, under Verify Pre-Synthesized Design, double-click Simulate. ModelSim runs the design for 180 µs. The following figure shows the received Ethernet packet information displayed on the ModelSim Transcript window.
The following figure and Figure 8, page 9 show the Waveform window. The highlighted portion shows the transmitted and received Ethernet packets.
2.4 Setting Up the Demo Design

The following steps describe how to setup the demo:

1. Connect the jumpers to the IGLOO2 FPGA Evaluation Kit board as shown in the following table.
2. Connect the power supply to the J6 connector and switch ON.
3. Connect the FlashPro4 Programmer to the J5 connector on the IGLOO2 FPGA Evaluation Kit board.

Note: Ensure that the power supply switch SW7 is switched off while connecting the jumpers to the IGLOO2 FPGA Evaluation Kit.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin (From)</th>
<th>Pin (To)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J22</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J23</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>

2.5 Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from the following path: 
   http://soc.microsemi.com/download/rsc/?f=m2gl_dg0633_liberov11p7sp2_df
2. Switch ON the power supply switch, SW7.
3. Launch the FlashPro software.
4. Click New Project.
5. In the New Project window, enter the project name as CoreTSE_Demo.
6. Click Browse and navigate to the location where the project needs to be saved.
7. Select Single device as Programming mode.
8. Click OK to save the project.
Figure 9 • FlashPro New Project

9. Click **Configure Device**.
10. Click **Browse** and navigate to the location where the `Igloo2_1000BaseT_Demo.stp` file is located and select the file. The default location is:
   
   m2gl\dg0633\liberov11p7sp2\df\CoreTSE_1000BaseT_Demo\ProgrammingFile

11. Select **Advanced** as Mode and **PROGRAM** as Action.

12. Click **PROGRAM** to start programming the device. Wait until the programmer status is changed to **RUN PASSED**.
2.5.1 Connecting IGLOO2 Evaluation Kit Board to Host PC

The following steps describe how to connect the IGLOO2 Evaluation Kit Board to the host PC:

1. After successful programming, switch OFF the IGLOO2 Evaluation Kit Board.
2. Connect the host PC to the J13 connector on the IGLOO2 Evaluation Kit using the RJ45 cable.
The following figure shows the IGLOO2 Evaluation Kit board setup.

Figure 12 • IGLOO2 Evaluation Kit Setup

2.5.2 Running the Demo Design with Cat Karat and Wireshark on the Hardware

The following steps describe how to run the demo design:

1. Switch ON the power supply switch, SW7.
2. Install the Cat Karat packet software and Wireshark software on the host PC from the source files. (m2gl_dg0633_liberov11p7sp2_dftCoreTSE_1000BaseT_Demo\Source files)
3. On the host PC, open the Wireshark network analyzer. Select Start as shown in the Figure 13, page 14.
4. On the host PC, open the Cat Karat software as shown in the following figure.

**Figure 14 • Cat Karat Packet Generate Window**

5. Under Protocol View, click the Control tab and enter the value 1 for Packets per Burst as shown in **Figure 15**, page 15.
6. Under **Packet Flow**, click **use RAW** as shown in *Figure 14*, page 14.
7. Under **Protocol View**, select the **RAW** tab and copy and paste the Ethernet net packet from the source files (m2gl_dg0633_liberov11p7sp2_dfCoreTSE_1000BaseT_Demo\Source files\Raw_frame.txt) as shown in *Figure 14*, page 14.
8. Under **Interfaces**, select the Ethernet connection to the IGLOO2 Evaluation Board.
9. Select **Start Transmit** from the menu as shown in *Figure 14*, page 14, to transmit the packet.
10. In the Wireshark software window, double-click Ethernet-II, as shown in the following figure. The transmitted and received Ethernet packets are displayed.

*Figure 16 • Wireshark Software Window*
3 Appendix: Running the Demo Design Using Spirent Test Center

The following steps describe how to run the CoreTSE MAC loopback demo using Spirent test center:

1. Connect the IGLOO2 Evaluation Kit to the slot 1 Ethernet port on the Spirent test equipment using the RJ45 cable.
2. In the host PC, open the Spirent test center configurator.
3. Add port (Ethernet) in Spirent test center, as shown in the following figure.

*Figure 17* • Spirent Test Center Stream Block – General Tab

4. Click Traffic generator under Port, add packet information in stream block editor, and click OK as shown in Figure 19, page 17.
5. Click Start traffic on all ports, as shown in Figure 19, page 17. Ethernet packets are transmitted and received on port1 through the RJ45 cable.

6. Observe the Total TX, RX, RX FCS, and CRC error counts. Figure 19, page 17 shows the total TX, RX, RX FCS, and CRC error count information in Spirent test center. 0 indicates no loss in the packet transmission and reception.