Spread Spectrum Clocking

Introduction

Spread spectrum clocking is a technique used in electronics design to intentionally modulate the ideal position of the clock edge such that the resulting signal's spectrum is "spread", around the ideal frequency of the clock. In timing circuits, this has the advantage of reducing Electromagnetic Interference (EMI) associated with the fundamental frequency of the signal. The amount of EMI a system is allowed to generate is set by various regulatory bodies to ensure systems do not interfere with one another. Spread spectrum clocking is often used to help meet the regulated EMI requirements. A spread spectrum signal has the disadvantage of having much higher jitter than the un-modulated signal.

Spread spectrum clocking is commonly used for microprocessor clocks and USB and PCI-Express reference clocks to reduce EMI.

How Spread Spectrum Works

Figure 1 shows the spectrum of a 100MHz square wave clock signal generated by a Micosemi ZL30251 clock synthesizer. This plot shows a narrow band of the spectrum, 2.5MHz above and below the carrier. The carrier frequency is 100MHz, and power amplitude at that frequency is 0.5dBm. The next highest power peaks are at approximately ±0.75MHz from the carrier, but they are significantly lower power, approximately -55dBm, and can be ignored for the purposes of this discussion.

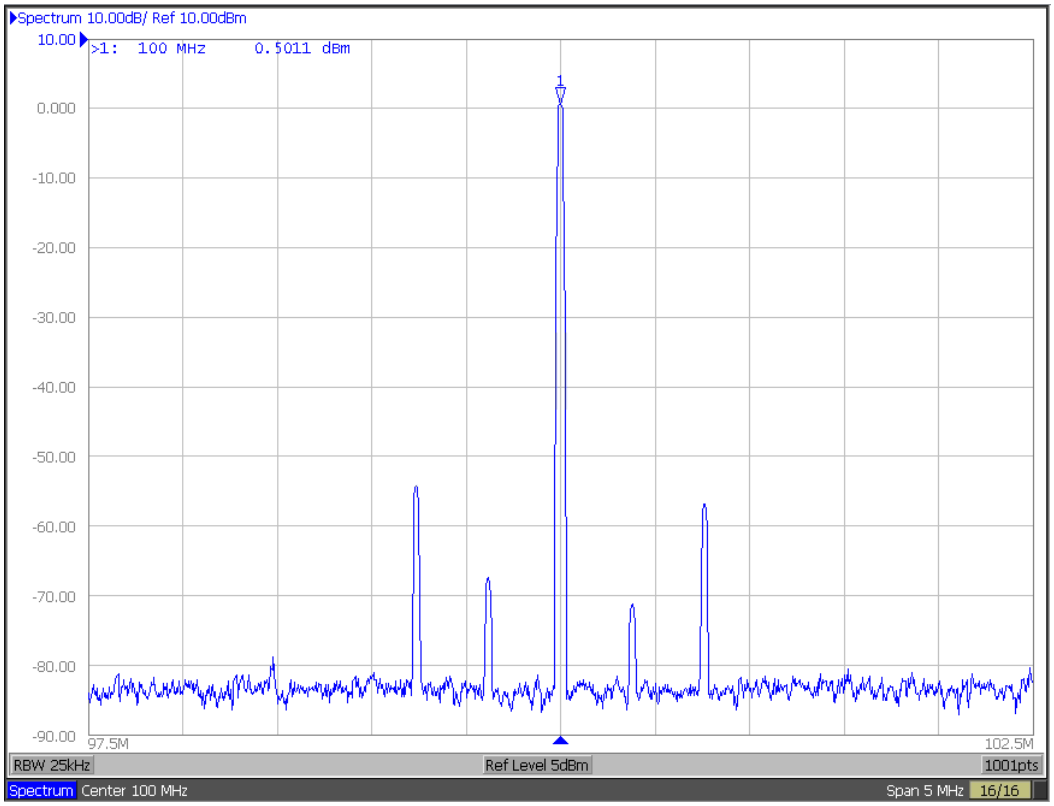

Figure 1 · Typical Spectrum for 100MHz Signal

The high power of the carrier signal can result in radiated emissions and cause EMI if the circuit traces carrying the signals are not perfectly balanced and terminated.

The idea behind spread spectrum is to replace high power in a single narrow frequency band with lower power spread over a wider band. This reduces the EMI associated with the signal, and makes it easier to meet the radiated emissions requirements of organizations like the U.S. Federal Communications Commission (FCC). This is a relatively inexpensive solution compared to alternatives, which include modifications to individual circuits late in the design cycle (for example making use of slew limiting drivers), all the way to making changes to the product chassis (to improve the Faraday cage).

The actual spread-spectrum waveform is created by frequency modulating the carrier wave. For PCIe spread spectrum clocks, a square wave carrier (usually 100MHz) is frequency modulated by a triangle wave with a frequency of 30-33kHz. The amplitude of the triangle-wave modulation is selected to result in a spread amplitude of 0.5% of the nominal carrier frequency.

When the signal shown in Figure 1 is modulated with a 30kHz triangle wave with 0.5% down-spread, the resulting signal spectrum looks like Figure 2.

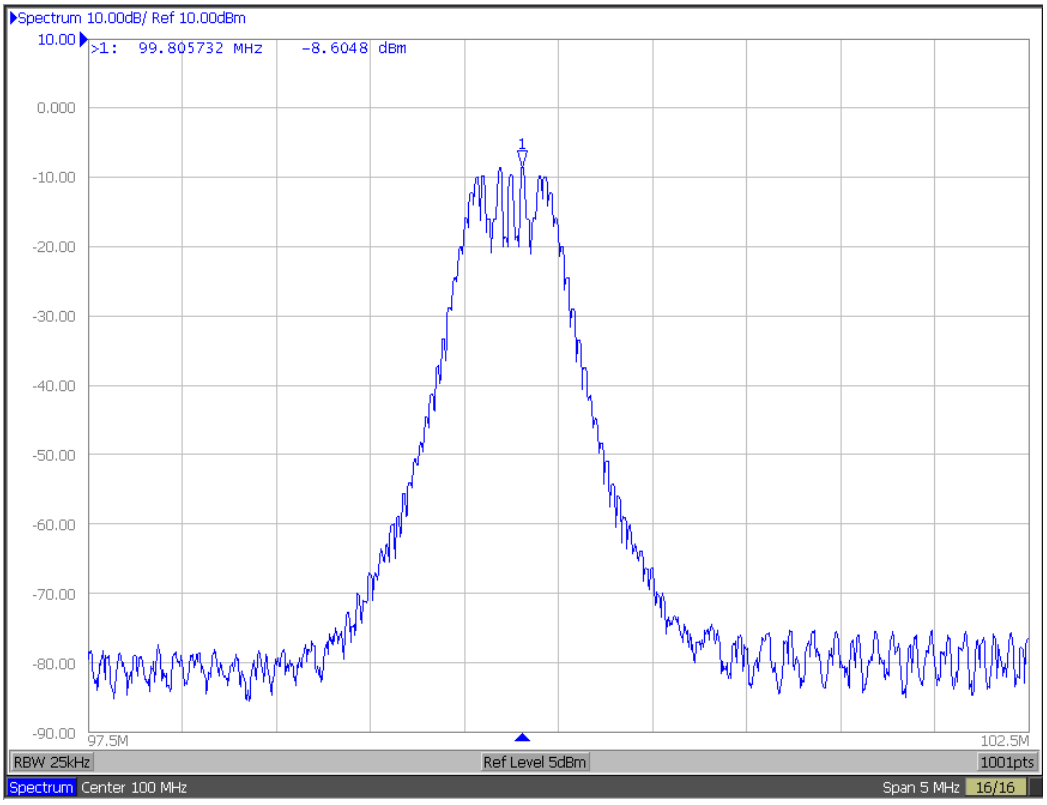

Figure 2 · Spectrum of 100MHz Signal Modulated by 30kHz Triangle Wave with 0.5% Down-spread

The term “down-spread” implies that the carrier is modulated to lower frequencies, not higher, so the maximum frequency of the spread-spectrum signal is the same as the nominal clock frequency without spread, 100MHz in this example. The lowest frequency component is 0.5% below the carrier, at 99.5MHz. An alternative to down-spread is center-spread where the carrier is modulated both lower and higher than the nominal clock frequency by a specified percentage.

Figure 3 shows the two plots from Figure 1 and Figure 2 together, illustrating that the peak power at any frequency for the spread-spectrum signal is reduced by more than 9 dB compared to the unmodulated signal. This translates directly to a decrease in EMI.

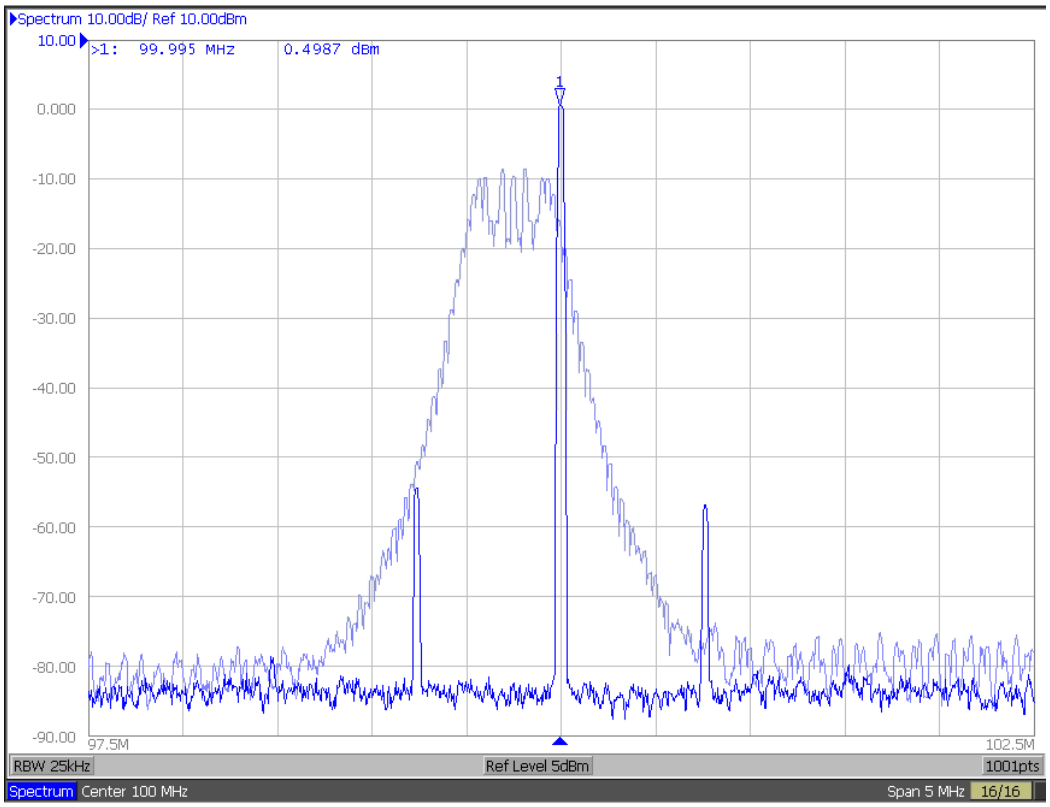

Figure 3 · Unmodulated and Spread Spectrum Signals Superimposed

Jitter of Spread Spectrum Signals

When a clock signal is frequency modulated, the resulting signal is effectively a jittered version of the original. Figure 4 shows the time interval error (TIE) of a 100MHz clock signal modulated with a 30kHz triangle wave with a 0.1% center-spread. TIE is a measure of the difference in edge position of a jittery or wandering clock signal compared to the ideal position. In this case, the unmodulated 100MHz clock signal's edges are at the ideal positions, and the TIE of the modulated signal's edges are measured. The amplitude of TIE is the peak-to-peak jitter introduced by the modulation. In this case, the maximum peak-to-peak jitter due to modulation is a little more than 4ns. With a 0.5% center spread, the jitter would be over 20ns.

This level of jitter is actually quite high compared to most telecom and datacom clock requirements. Many narrowband PLLs would have difficulty tracking and maintaining lock to a signal like this. PCIe and similar protocols support a "Common Refclk Rx Architecture", in which the transmitter and receiver are clocked by the same spread-spectrum reference clock. With this arrangement, the jitter appearing at the CDR is a difference function of the transmit and receive clocks; therefore

the jitter due to the spread spectrum modulation is largely cancelled. PCIe also supports a "Data-clocked Rx Architecture" in which the receiver CDR must tolerate the full 20ns of SSC jitter.[1]

As a side note, though the TIE in Figure 4 appears sinusoidal, it is actually a combination of parabolas corresponding to the integration of the triangle wave modulating the carrier.

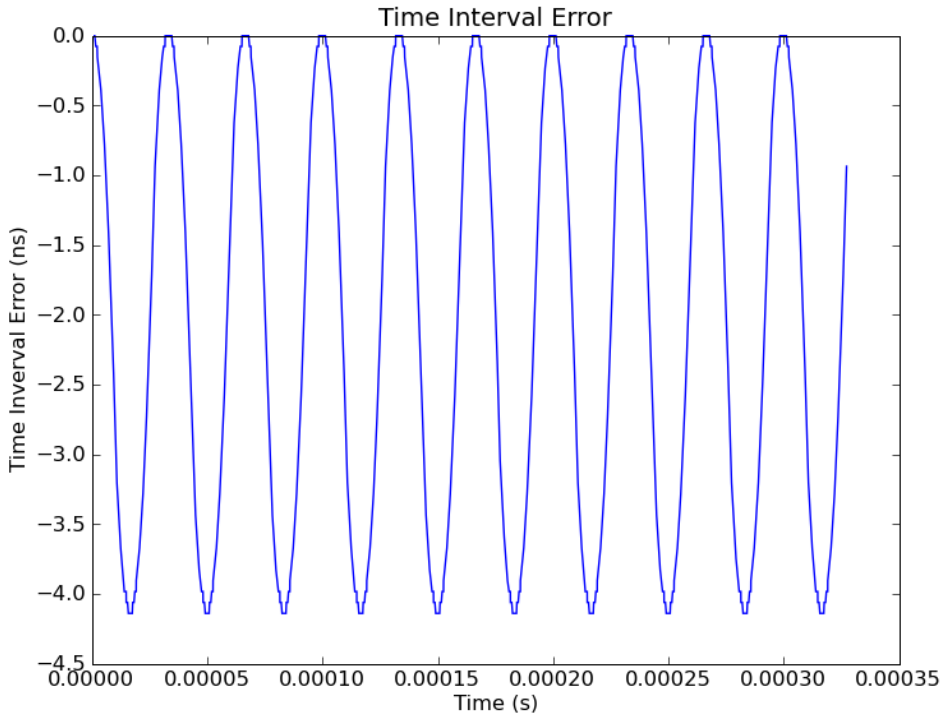

Figure 4 · Time Interval Error of Modulated Signal vs Un-modulated Square Wave

Figure 5 shows a phase noise plot of the same signal. As can be seen, each of the harmonics of the 30kHz triangle wave produces a large spur contributing to the jitter.

[1] *See PCI Express Base Specification Revision 3.0 for more details on the Common Refclk Rx Architecture and Data-clocked Rx Architecture.*

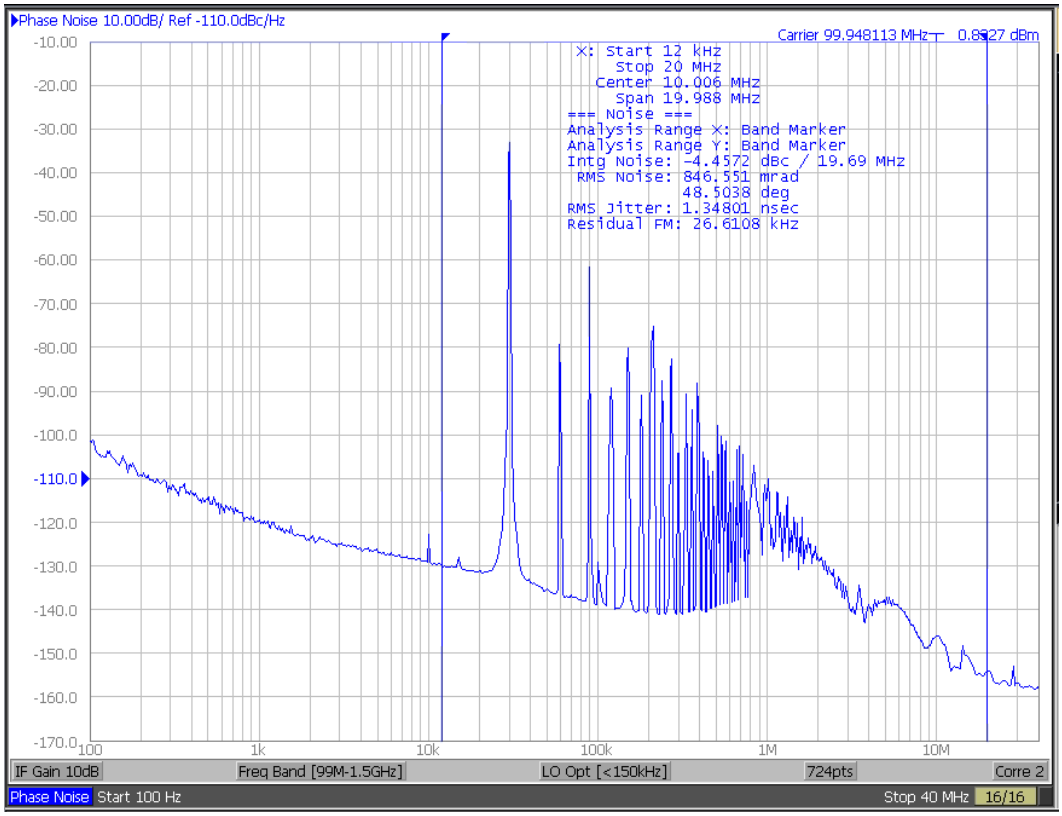

Figure 5 · Phase Noise of 100MHz Signal Modulated with 30kHz Triangle Wave for 0.1% Spread

Even with the large amount of jitter on this signal, especially in the 10kHz to 1.5MHz band, it can still be used effectively for a PCIe reference clock. The PCIe reference clock requirements for data-clocked and common-clocked architectures allow for significant filtering in this band. The filtering can reduce the RMS jitter of the signal in the 10kHz to 50MHz band to achieve PCIe compliance.

Conclusions

Spread spectrum clocking can be used effectively to reduce EMI, principally in PCIe and USB applications. It is often less costly to use spread spectrum clocking than to employ other techniques like careful balancing and termination of signal traces, or improving the Faraday cage of the system. However, spread spectrum clocks have relatively high jitter compared to un-modulated clocks, often at levels that can cause locking and tracking problems for traditional PLLs. Care should be taken to ensure that downstream components can tolerate the jitter added by the spread spectrum modulation.

Microsemi offers several products with spread spectrum modulation capability including frequency synthesis and frequency translation products such as the ZL30250 and ZL30251, and frequency translation and jitter-attenuator products such as the ZL30252 and ZL30253.

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