Improving the Performance of your DC-DC Forward Converter using I²MOS™ MOSFET Technology

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I²MOS advantages

- Highest available SEE performance, 85-90 MeV at full rated BVDss
- Highest Avalanche capability: 5X greater than competition
- TID (Total Ionizing Dose) Rating: 100Krad-500Krad (depending on specific device)
- Commerce Rating: 9A515.e
  - Most Euro countries will not need a license!
- Competitive pricing on new designs
I²MOS FOM versus Competition

![Graph showing I²MOS FOM vs. Voltage (V) compared to competition](image-url)
SEE results - Microsemi vs. Competitor

**SEE Response - R6, 150V, N, MR**
- **Kr Ion;** LET=39±5%; 50±5%µm; 410±5%MeV
- **Xe Ion;** LET=61±5%; 66±7.5%µm; 825±5%MeV
- **Au Ion;** LET=90±5%; 80±5%µm; 1470±5%MeV

**SEE Response - 150V, N**
- **Kr Ion;** LET=35.1; 517MeV; 62.6µm
- **Xe Ion;** LET=56.6; 1023MeV; 80.7µm

**SEE Response - R6, 200V, N, MR**
- **Xe Ion;** LET=42±5%; 205±5%µm; 2450±5%MeV

**SEE Response - 200V, N**
- **Kr Ion;** LET=31.6; 733MeV; 90.6µm
- **Xe Ion;** LET=53.7; 1279MeV; 100.7µm
## I²MOS™ MOS P/N Structure

<table>
<thead>
<tr>
<th>MRH</th>
<th>BVDSS/1</th>
<th>Channel</th>
<th>ID @ 25C</th>
<th>Package</th>
<th>Screening</th>
<th>RAD LEVEL</th>
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<tr>
<td>0</td>
<td>(V)</td>
<td>(A)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>N</td>
<td>22</td>
<td>U3</td>
<td>S</td>
<td>R</td>
<td></td>
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</tbody>
</table>

| Microsemi | 20= 200V | N | U3= SMD0.5 | S= JANS | R= 100K |
| Rad- Hard | 10= 100V | P | T2= TO- 39 | V= JANTXV | G= 500K |
| MOSFET    | 13= 130V |   | T3= TO- 257 | C= EDU |         |
|          | 06= 60V  |   | U5= LCC-18 |         |         |
|          | 03= 30V  |   | C= die     |         |         |
### Phase 1: I²MOS™ portfolio, N- Ch, Sz 3

<table>
<thead>
<tr>
<th>Bvds (V)</th>
<th>Similar JEDEC Number</th>
<th>Industry Equivalent</th>
<th>MSC p/n</th>
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<td>2N7589U3</td>
<td>IRHNJ67134</td>
<td>MRH15N19U3</td>
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<td>IRHNJ67230</td>
<td>MRH20N16U3</td>
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<td>IRHNJ67234</td>
<td>MRH25N15U3</td>
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### Phase 2: I²MOS™ portfolio, N- Ch, Sz 5.5

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<th>Bvds (V)</th>
<th>Similar JEDEC Number</th>
<th>Industry Equivalent</th>
<th>RH2 Base MSC p/n</th>
<th>Package</th>
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<td>IRHNA67264</td>
<td>MRH25N56U1</td>
<td>SMD-2</td>
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</tbody>
</table>
Efficiency Performance of I²MOS

DC-DC Forward Converter (Resonant Reset Topology)
MRH25N15U3 vs. IRHNJ67234
DC-DC Criteria

- Create a Circuit to Reveal Differences in MOSFET Power Losses
- Parallel-Inductor Isolated Forward DC-DC Converter
- Improved Efficiency
  - Resonant Transformer Reset
  - Lower DC Losses in Inductors and Schottky Rectifiers
- Use \( V_{dd} = 50Vdc \)
  - Peak of Resonant Reset Voltage Will Be: \( V_{dd} + (I_d(pk) \times L_m / C_r) \)
    - \( L_m \) is Power Transformer Magnetizing Inductance (~120uH)
    - \( C_r \) is the Resonance Capacitance = \( C_{oss} || C_j (N_s/N_p) \times (~810pF) \)
    - Worst Case Resonance Peak at \( f_{sw} = 350kHz \) and \( V_{out} = 5.0Vdc \) (~120Vpk)
Efficiency Test Criteria

- **Voltage De-Rating = 50%**
  - Use Microsemi MRH25N15U3 and IR IRHNJ67234, 250V devices. (200V Device May Be Used For Higher Efficiency With Lower Voltage Margin.)

- **100W Maximum Output Power**
  - 20A Maximum Output Current
    - 66W For Vout = 3.3Vdc
    - 100W For Vout = 5.0Vdc
Efficiency Test Circuit Schematic
Efficiency Test Circuit Features

- Circuit Used For Power Switch Efficiency Comparison:
  - Circuit Uses U3 Packages For All Power Functions
    - Small Size
    - Ease of Thermal Management
  - Output Uses Paralleled Output Stage For Increased Efficiency
    - Schottkies and Inductors Share Current ~50:50
    - DC Power Losses Reduced by ~1/4 - 1/3!
  - Optimized for 3.3Vdc < V_{out} < 5Vdc
  - Optimized For 1A < I_{out} < 20A
  - Optimized For 350kHz < f_{sw} < 500kHz
  - Uses COTS Micrel MIC4424 Gate Driver IC
    - Rad-Hard Equivalents Available from Intersil
Efficiency Test Parameters

- DC Output \( (V_{\text{out}}) \) Set By Varying Input Duty Cycle
  - Duty Cycle = Desired \( V_{\text{out}} \times \left( \frac{N_s}{N_p} \right) / V_{\text{dd}} \)

- Efficiency:
  \[
  \eta = \frac{P_{\text{out}}}{\left( P_{\text{in}} + P_{\text{bias}} \right)} = \frac{V_{\text{out}} \times I_{\text{out}}}{\left( V_{\text{dd}} \times I_{\text{dd}} \right) + \left( V_{\text{bias}} \times I_{\text{bias}} \right)}
  \]
  - \( I_{\text{out}} \) = Set, Varied from 1A to 20A
  - \( V_{\text{dd}} \) = Set, Constant = 50Vdc
  - \( V_{\text{bias}} \) = Set, Constant = 12Vdc
  - \( V_{\text{out}} \) is Set By Varying the Input Duty Cycle
  - \( I_{\text{dd}} \) and \( I_{\text{bias}} \) Are Measured at Each Operating Point
MOSFET Losses

- Key Contributors to Power MOSFET Switch Losses:
  - DC Losses: $I_d(rms)^2 \times R_{ds(on)} \times D$
  - AC Losses: Gate + Switching
    - Gate Input Losses: $Q_{gt} \times V_{bias} \times f_{sw}$
    - Drain Switching Losses: $\sim V_{dd} \times I_d(rms) \times (t_r + t_f) \times f_{sw} / 2$ + $(C_{oss} \times V_{dd}^2 \times f_{sw})$
Forward Converter Design Parameters

- Duty Cycle = \( D = \left( \frac{V_{out}}{V_{in}} \right) \times \left( \frac{N_s}{N_p} \right) = \frac{t_{on}}{t_{off}} \)
- \( I_d(pk) = \left( \frac{I_d(avg)}{D} \right) + (0.5 \times \left( \frac{V_{dd} \times t_{on}}{L_m} \right)) \)
- \( V_{res(pk)} = V_{dd} + I_d(pk) \times \left( \frac{L_m}{C_r} \right)^{0.5} \)
- \( t_{res} = \pi \times \left( \frac{L_m \times C_r}{0.5} \right) \)
- \( C_r = C_{oss} + \left( \frac{C_j}{(N_p/N_s)} \right) \)
  - \( C_j \) is the Output Schottky Junction Capacitance

![Diagram showing waveforms for Forward Converter Design Parameters](image)
Measured Drain-Source Voltages

\[ V_{out} = 5.0\text{Vdc}, \quad I_{out} = 1\text{Adc}, \quad f_{sw} = 350\text{kHz} \]

\[ V_{DS(pk)} = 122\text{V} \]

\[ V_{out} = 5.0\text{Vdc}, \quad I_{out} = 20\text{Adc}, \quad f_{sw} = 350\text{kHz} \]

\[ V_{DS(pk)} = 148\text{V} \]
Efficiency Parameters

- From Data Sheet Parameters:
  - **$R_{ds(ON)}$**
    - MRH25N15U3 – 175mΩ max.
    - IRHNJ67234 – 210mΩ max.
    - IR Device 20% Higher Than Microsemi
  - **$Q_{gt}$**
    - MRH25N15U3 – 32nC typ. (est. 40nC max.)
    - IRHNJ67234 – 50nC max. (est. 40nC typ.)
  - **$C_{oss}$**
    - IRHNJ67234 – 187pF typ.
Efficiency Data - +3.3Vout, 350 Khz.

At higher currents the improvement in conduction losses provide an advantage.
Efficiency Data, Vout = 5.0V, 350 Khz.

At higher currents the improvement in conduction losses is slightly better at 5.0Vout vs. 3.3Vout.
Efficiency Data, +3.3Vout, 500 Khz.

At 500 Khz. There are more switching losses in both parts but I²MOS part maintains the advantage.
Efficiency Data, 5.0Vout, 500 Khz.

- Efficiency improvements @ higher currents when Vout = 5.0V
Avalanche Energy Performance

MRH25N15U3 vs. IRHNJ67234
Avalanche Basics

- Avalanche Performance Indicates Ruggedness of MOSFET
  - Energy Handling Capability
    - Repetitive
    - Single Pulse
    - Specified in Joules (V * I * t)

- “Unconstrained” Inductors Cause Excursions to $V_{BR}(DSS)$
  - Energy $\sim (L * I_d(pk)^2 / 2) * (1 - (V_{dd} / V_{BR}(DSS)))$
  - Junction Dissipates Enormous Instantaneous Power
    - If $V_{BR}(DSS) = 250V$ and $I_d(pk) = 10A$, $P_{inst} = 2500W!$

- The Greater the Avalanche Energy Rating, The Better
## Data sheet Specs & Avalanche Test Circuit

<table>
<thead>
<tr>
<th>Part #</th>
<th>Eas (mJ)</th>
<th>Ear (mJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRH25N15U3</td>
<td>15</td>
<td>300</td>
</tr>
<tr>
<td>IRHNJ67234</td>
<td>7.5</td>
<td>56</td>
</tr>
</tbody>
</table>
Avalanche Test PCB

Board Size = 5.8 x 4.1 x 0.063”, 4 Layer FR-4, Double Sided
Avalanche Test Procedure

Avalanche Test Has Two Regions:

1. Turn ON Device Under Test (DUT)
   Ramp Inductor Current to Desired $I_d(pk)$ during ON Time ($t_{on}$)
   
   $$I_d(pk) = \frac{V_{dd} \cdot t_{on}}{L}$$

2. Turn OFF DUT
   Drain Voltage “Flys” to VBR(DSS)
   
   Avalanche Time ($t_{av}$) = $L \cdot I_d(pk) / (V_{BR(DSS)} - V_{dd})$
   
   Avalanche Energy ($E_{av}$) = $V_{BR(DSS)} \cdot I_d(pk) \cdot t_{av}$

ON Time Adjusted to Obtain Desired $I_d(pk)$ and Thus $E_{av}$

Vds “Ringout” Due to Residual Energy in L and L-Coss Resonant Circuit

Ideal Waveforms
Measured Avalanche Performance

MRH25N15U3, 7.5mJ

$V_{BR(DSS)} = 283V$, $I_d(pk) = 12A$, $t_{on} = 29.5us$

MRH25N15U3, 15mJ

$V_{BR(DSS)} = 304V$, $I_d(pk) = 11A$, $t_{on} = 71.5us$
Measured Avalanche Performance

MRH25N15U3, 300mJ

\[ V_{BR(DSS)} = 314V, \; I_d(pk) = 15A, \; t_{on} = 750\mu s \]

MRH25N15U3, 300mJ (Expanded)

\[ V_{BR(DSS)} = 314V, \; I_d(pk) = 15A, \; t_{on} = 750\mu s \]
Measured Avalanche Performance

IRHNJ67234, 7.5mJ

$V_{BR(DSS)} = 300V$, $I_d(pk) = 10A$, $t_{on} = 24.5\text{us}$

IRHNJ67234, 56mJ

$V_{BR(DSS)} = 302V$, $I_d(pk) = 16.7A$, $t_{on} = 120\text{us}$
Summary

**Efficiency**
- MRH25N15U3 *Demonstrated More Efficient* Than IR IRHNJ67234
  - By up to 2.75%
- MGN25N15U3 Efficiency holds up over the full current range of 5A – 20A. Especially at higher load currents
- IRHNJ67234 Efficiency decreases due to higher conduction Losses
  - Useful Output Current Range Must Be De-Rated to 18A
- Increased Losses Mean More Aggressive Thermal Management Required (Bigger Heat Sink for Lower $\theta_{JA}$)

**Avalanche Capability**
- Microsemi MRH25N15U3 *Demonstrated 2X Repetitive Avalanche Capability* Over IR IRHNJ67234
- Microsemi MRH25N15U3 *Demonstrated 5.4X Single Event Avalanche Capability* Over IR IRHNJ67234
Thank You

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