Libero SoC v11.6 Release Notes

Libero® System-on-Chip (SoC) is comprehensive and powerful FPGA design and development software available from Microsemi, providing start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such EDA powerhouses as Synplify Pro® and Model*Sim*®.

Libero SoC v11.6 is the premier production release for the new RTG4 Radiation Tolerant 65nm process silicon family.

Libero SoC v11.6 contains critical timing data updates for SmartFusion2 and IGLOO2 families. Microsemi highly recommends that you open your SmartFusion2 and IGLOO2 designs created with Libero SoC v11.5 SP3 or an earlier release, in Libero SoC v11.6, update cores as necessary, and rerun the Verify Timing step.

Use Libero SoC v11.6 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3, and Fusion FPGA families.

To access Datasheets and Silicon User Guides, visit www.microsemi.com, select your Product, then click the Documents tab. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the Design Resources tab.

Refer to the Online Help in Libero SoC for details about new software features and enhancements.

Contents

What's New in Libero SoC v11.6

New Device Support

RTG4

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
RT4G150	1657 CCGA/LGA	STD, -1	MIL	No
RT4G150_ES	1657 CCGA/LGA	STD	MIL	No

There are two RTG4 device options available in Libero SoC v11.6:

- **RT4G150_ES** refers to the Engineering Samples (ES) of the RT4G150 device. RT4G150_ES must be selected when designing with RTG4 ES or Mil-temp ES (MS) devices.
- **RT4G150** (production) should be selected when designing with final silicon, including PROTO and flight units.

Note: There are a number of differences in Libero SoC v11.6 support between the RT4G150_ES device and the RT4G150 device:

Programming Support

In Libero SoC v11.6, programming is enabled for the RT4G150_ES device and not the RT4G150 production device.

PLL TMR Implementation

The PLL mode (Single or TMR) depends on the targeted device and the CCC/PLL Feedback selection, as shown in the following table:

CCC/PLL Feedback Selected Option	***PLL Mode***	
	RT4G150_ES	***RT4G150 (production)***
PLL Internal	Single PLL	Three (3) PLLs (Triple Module Redundancy)
CCC Internal/CCC External	Single PLL	Single PLL

As seen in the table above, for the RT4G150_ES device, PLLs are automatically configured as single PLL instead of Triple Module Redundancy for radiation mitigation, regardless of the selected feedback mode.

Output Resynchronization after Lock Behavior

For the RT4G150_ES device, depending on the feedback option selected (PLL internal, CCC internal, or CCC external), the Output Resynchronization after lock options are as follows:

Output Resynchronization After Lock **Supported option(s)**	PLL Internal		CCC Internal/CCC External	
	RT4G150_ES	***RT4G150 (production)***	***RT4G150_ES***	***RT4G150 (production)***
Held Output in reset (output low) after power up. Released and resynchronized with the PLL Reference clock after the PLL locked.	Available	Available	*Not Available*	Available
Outputs Operate after power up. Resynchronized with the PLL reference clock after the PLL locked.	Available	Available	*Not Available*	Available
Outputs Operate after power up. No automatic resynchronization.	Available	Available	Available	Available

Package Removal

For the Libero SoC v11.6 release, the VQ144 package has been removed for the following devices:

Device	Package Removed
M2S005	VQ144
M2S010	VQ144
M2GL005	VQ144
M2GL010	VQ144
M2S005S	VQ144
M2S010S	VQ144
M2GL005S	VQ144
M2GL010S	VQ144

SmartFusion2 and IGLOO2 – M2S060(T/TS)/M2GL060(T/TS)-FCS(G)325 Internal Package Pin Mapping

If your design targets any of the M2S060(T/TS)/M2GL060(T/TS)-FCS(G)325 devices, the design will be reset to the pre-compile state because of a critical package pin mapping fix for these devices. You will need to recompile, place and route your design and revalidate your timing requirements for this design.

SmartFusion2 and IGLOO2 – Timing Updates

Libero SoC v11.6 contains critical updates to timing modeling for SmartFusion2 and IGLOO2 devices, including:

- DDR-AXI Timing Model Update
- MSS (HPMS) FIC_2 Timing Model Update
- FPGA fabric cells and routing data updates

Microsemi highly recommends that your existing SmartFusion2/IGLOO2 designs are verified for timing using this release. Verifying timing can easily be done without re-running the entire project by simply importing your old Libero SoC project and running "Verify Timing". In most cases the project will keep the post Layout status. For more information, see the Libero SoC v11.6 Timing Validation and Design Migration User's Guide.

SmartFusion2 and IGLOO2 – MSS/HPMS DDR (MDDR) or Fabric DDR (FDDR) with AXI Interface

If your design uses MSS DDR (MDDR) or Fabric DDR (FDDR) with the AXI interface, with a DDR clock to Fabric clock ratio greater than 1, the design will be invalidated because of critical timing changes on the AXI-DDR interface. For more information about how to update your design, refer to the SmartFusion2/IGLOO2 Design Migration User Guide.

SmartFusion2 and IGLOO2 – MSS/HPMS FIC_2 Timing Updates

The MSS (HPMS for IGLOO2) FIC_2 interface is essentially an APB3-like interface which initializes, along with CoreConfigP, the peripherals at Power Up or on a Chip Level reset. In the Libero SoC v11.6 release, the MSS (HPMS) FIC_2 interface timing model has been added. In previous releases, timing analysis for this interface was not available.

If your design uses any of the MSS DDR (MDDR), Fabric DDR (FDDR) or SERDES blocks and you are using the standard Libero SoC solution to create the initialization logic for these peripherals (System Builder), your design uses the MSS (HPMS) FIC_2 interface. The clock of this subsystem is generated

by the MSS (HPMS) FIC_2 block and is defined as ¼ of the MSS (HPMS) frequency clock as per the SmartFusion2 (IGLOO2) MSS (HPMS) clocking architecture.

Refer to the SmartFusion2/IGLOO2 FPGA Timing Constraints User's Guide to:

- Create a clock constraint for the MSS (HPMS) FIC_2 APB clock.
- Create constraints that specify the exact timing requirements for the FIC_2 to CoreConfigP interface.

SmartFusion2 and IGLOO2 – Licensing Changes

With Libero SoC v11.6, the following SmartFusion2 and IGLOO2 devices are now available with the Libero Gold License (they previously required a Platinum License):

Device	Package
M2S005S	All
M2S010S	All
M2S010TS	All
M2GL005S	All
M2GL010S	All
M2GL010TS	All

SmartFusion2 and IGLOO2 – Production Data

Production (post-silicon) Timing and Power analysis is available for M2S090/M2GL090 and M2S150/M2GL150 devices.

SmartFusion2	IGLOO2	Timing	Power
M2S005*	M2GL005*	Production	Production
M2S010*	M2GL010*	Production	Production
M2S025*	M2GL010*	Production	Production
M2S050*	M2GL050*	Production	Production
M2S060*	M2GL060*	*Preliminary*	*Preliminary*
M2S090*	M2GL090*	Production	Production
M2S150*	M2GL150*	Production	Production

Note: M2S060/M2GL060 Timing Data History shows it as "Advanced" in software. That information is incorrect; the information in this table is correct.

*: Includes S/T/TS versions where applicable.

SmartFusion2 and IGLOO2 – Updated Restrictions in SERDES/MSS Feature Availability and Speed

Depending on the selected speed grade and operating range, certain SERDES features may not be available or may be rate-limited. The maximum operating frequency of the Cortex-M3 may also be restricted.

Silicon Feature Support

RT4G150 – I/O Output Drive Strength Changes

Libero SoC v11.6 has the updated I/O Output Drive Strengths for the RT4G150 production device. This addresses Errata #8 in the RTG4 ES FPGA Errata ER0193.

RT4G150 – Memory Support Enhancements

- Unused RAM blocks are now configured in their lowest power consumption state.
- RAMs in the RT4G150_ES devices and RT4G150 devices differ in their response to asynchronous reset.
    - RT4G150_ES:
        - Write operations get blocked on assertion of the asynchronous reset.
        - Read operations get delayed by a clock cycle on de-assertion of asynchronous reset.
    - RT4G150 - the asynchronous reset resets the pipeline register and does not affect the RAM's Write/Read operations (this is expected behavior). In other words, the limitations of the RT4G150_ES above have been removed in the RT4G150 device.

  This distinct behavior difference is accurately modeled in the simulation libraries provided with Libero SoC v11.6. The simulation libraries are sensitive to the device selected, and select the correct RAM behavior model for the active device.

RT4G150-CG1657 – Package Update

The RT4G150 production device with the CG1657 package addresses #3 and #5 issue in the RTG4 ES FPGA Errata. Libero SoC v11.6 contains the updated set of package pins for this device-package combination. All 16 SpaceWire I/O pairs are now available and you can now instantiate up to 16 SpaceWire blocks in your design. RT4G150 production designs created with Libero SoC RTG4 Launch software or prior LCP releases must upgrade to Libero SoC v11.6. Refer to the SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon.

RT4G150 – SYSCTRL_RESET_STATUS

The SYSCTRL_RESET_STATUS macro is now available for RT4G150 production devices. This macro will expose a RESET_STATUS signal that can be used to monitor the status of the System Controller after Power On Reset (PoR) or after Chip reset (DEVRST_N). You can find this macro in the Libero SoC v11.6 Catalog. This macro is not supported for the RT4G150_ES device.

RT4G150 and RT4G150_ES – uPROM Non-volatile Memory Support

Libero SoC v11.6 adds support for the uPROM in RTG4 devices. The uPROM is a 10,400x36 non-volatile memory that can be programmed along with the FPGA fabric. The uPROM cannot be programmed or reprogrammed without programming or reprogramming the fabric as well. At runtime, the FPGA application can access the uPROM in read-only mode. Refer to the RTG4 uPROM Configuration User Guide for details.

All SmartFusion2, IGLOO2, and RTG4 devices – DDR Memory Configurator Enhancements

The following enhancements have been made in Libero SoC v11.6 to better support DDR Memories:

- Memory row/column address mapping: You can now configure the number of rows, columns, and banks in the MDDR/FDDR Configurators.
- You can now enable or disable local ODT or dynamic ODT using the MDDR/FDDR configurators.

Refer to the following user guide for more information:

- SmartFusion2 FPGA Fabric DDR Controller Configuration

All SmartFusion2, IGLOO2, and RTG4 devices – High Speed Serial Interface Configurator Enhancements

The following enhancements have been made in Libero SoC v11.6 High Speed Serial Interface configurators for the SERDES:

- PCIe: Support for Active State Power Management options is now available.
- EPCS: New option to disable receive-idle detect.
- Renamed “L2/P2” to “Expose Wake Signals” for improved clarity.

Refer to the following user guide for more information:

- SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration

Software Enhancements

SmartFusion2 and IGLOO2 – System Builder Enhancements

- **Direct Connection Mode: Libero SoC v11.6** now offers a “Direct Connection” mode in the System Builder Peripherals configuration page. Use the ‘Direct Connection” mode if you want to create your Fabric Interface (FIC) AMBA subsystems outside the System Builder generated component. In this mode, System Builder no longer instantiates bus cores for the MSS/HPMS/FDDR – Fabric interfaces. Instead, System Builder only exposes the AMBA interfaces for these blocks. You can then connect the rest of your design’s AMBA subsystem to these interfaces at the next hierarchical level.
- **CCC Dedicated Input Pads:** System Builder now allows you to use any of the CCC Dedicated Input Pads to drive the CCC used by System Builder (previously you could only use the Dedicated Input Pad 0 via System Builder).

RTG4 – Automatic Peripheral Initialization

Libero SoC v11.6 now supports the automatic peripheral initialization solution for EPCS and XAUI modes. PCIe automatic peripheral initialization is currently not supported and may be added in a future release. When using PCIe with this release, use the initialization method as described in the following Configurator user guide:

RTG4 High Speed Serial Interface (PCIe, EPCS and XAUI)

Refer to the following user guides for more information:

RTG4 High Speed Serial Interface (EPCS and XAUI) – with Initialization

RTG4 High Speed Serial Interface (PCIe, EPCS and XAUI) – with Initialization

SmartFusion2, IGLOO2, and RTG4 – Enhanced Synthesis Options

Libero SoC v11.6 adds a number of options that enable you to fine-tune Synthesis output. To access these options, right click and select “Configure Options” from Synthesis in the Libero SoC v11.6 Design Flow window.

Inferred RAM – Speed vs. Power Options
You can now guide the Synthesis tool to optimize RAM blocks to achieve your design goal; you can choose to optimize inferred RAM for High Speed, or Low Power. These options apply to all inferred RAM modules in your design:

- High Speed – RAM Optimization is geared towards Speed. The resulting synthesized design achieves better performance (higher speed) at the expense of power. This is the default.
- Low Power – RAM Optimization is geared towards Low Power. RAM blocks are inferred and configured to ensure the lowest power consumption.

Retiming during Synthesis
Retiming is the process of automatically moving registers (register balancing) across combinational gates to improve timing, while ensuring identical logic behavior. This option is turned OFF by default.

SmartFusion2, IGLOO2, and RTG4 – Enhanced Globals Management

Libero SoC v11.6 now offers options in Synthesis as well as Compile to manage the number of globals consumed in your design. You can now adjust fanout thresholds for clock pins, asynchronous pins, and data pins for which those respective nets will be promoted to globals. This will enable you to accurately control the number of globals consumed in your design and improve layout performance. Refer to the Online Help for Synthesis Options and Compile Options for usage details.

SmartFusion2, IGLOO2, and RTG4 – CLKINT_PRESERVE macro

To address the use case where you want specific clocks to always be assigned to a global net, Libero SoC v11.6 introduces the CLKINT_PRESERVE macro. This macro is available in the Libero SoC Catalog. Use this macro to drive clock nets that must be distributed on the Global network. Synthesis and Compile will not attempt to demote these nets to local routing resources, regardless of globals management options.

SmartFusion2, IGLOO2, and RTG4 – Repair Minimum Delay Violations

Libero SoC v11.6 introduces Min Delay Repair (MDR) for SmartFusion2, IGLOO2, and RTG4 device families. MDR attempts to automatically repair min delay (hold) violations in your design while ensuring that your design continues to meet max delay constraints (or, if your design does not meet max delay constraints, the worst slack does not worsen). MDR is turned ON by default for new projects created using Libero SoC v11.6, targeting the above device families. You may disable/enable MDR in the Layout Options dialog box (check/uncheck the “Repair Minimum Delay Violations” checkbox). You may notice an increase in the time to complete Layout if MDR is enabled.

SmartFusion2, IGLOO2, and RTG4 – Multiple Pass Layout UI

Place and Route options to run Layout with multiple passes (initial seeds) are now available in the Libero SoC v11.6 User Interface. You can enable Multiple Pass Layout using the Place and Route Options dialog box. As in previous releases, you can also run multiple passes of Place and Route using the batch Tcl script “extended_run_lib.tcl”.

Multiple Pass Layout attempts to improve layout quality, such as Timing performance of the design, by selecting one out of multiple Layout results. This is done by running individual place and route multiple times with varying placement seeds and measuring the best results with the specified criteria. Refer to the ‘*Multiple Pass Layout Configuration (SmartFusion2, IGLOO2 and RTG4)*’ topic in the Libero SoC v11.6 Online Help for more information.

SmartFusion2 and IGLOO2 – Automatic Constraint Generation for CoreResetP

CoreResetP is a core that is used to sequence and manage reset signals in your design. It is an essential component of the Peripheral Initialization solution and is instantiated as part of the System Builder generated component. CoreResetP, by design, has some inter-clock-domain paths, which should be considered false paths for the purpose of timing analysis. In previous releases, violations on these paths may have been reported in timing analysis. In Libero SoC v11.6, if CoreResetP is present in your design, Libero SoC automatically recognizes false paths pertaining to it. You will no longer see extraneous violations on CoreResetP inter-clock-domain paths. You will notice the auto-generated false path constraints in the Constraints Editor. To take advantage of this feature for existing Libero SoC v11.5 projects, you must run Compile again.

RTG4 – Automatic Constraint Generation for CCC and Oscillator

Libero SoC v11.6 now automatically generates clock period constraints for timing analysis for the CCC and Oscillator components. You will notice the auto-generated constraints in the Constraints Editor.

Microsemi recommends that you upgrade all CCC cores to the latest version. This will enable automatic constraint generation for configurations using phase shift.

RTG4 – SmartPower Support

Libero SoC v11.6 now includes SmartPower support for the RTG4 device family. Note: there are some limitations in SmartPower for RTG4 devices in Libero SoC v11.6. Refer to the Known Issues and Limitations section below for details.

RTG4 – I/O Advisor Support and Enhancements

Libero SoC v11.6 now includes I/O Advisor support for the RTG4 device family. For SmartFusion2, IGLOO2, and RTG4, I/O Advisor now supports additional I/O Attributes: Schmitt Trigger, ODT Static, and ODT Impedance.

RTG4 – SmartDebug Support Enhancements

Libero SoC v11.6 now includes SmartDebug support for the RTG4 device family. SERDES configuration read-back support, debug, and SERDES register read/write TCL command support are new enhancements for Libero SoC v11.6.

FlashPro Tcl Support Enhancements

In FlashPro v11.6, you can now export single device chain STAPL files using the Tcl command export_single_stapl with the argument –chain. Refer to the Online Help for more information about usage.

SmartDebug Tcl Support Enhancements

You can now execute SmartDebug TCL scripts from Libero SoC v11.6.

Updating Your Design to Libero SoC v11.6

Refer to the “SmartFusion2 and IGLOO2 Timing Updates” section above for more information. Microsemi recommends that you upgrade any SmartFusion2, IGLOO2, or RTG4 design to Libero SoC v11.6. As part of the upgrade process, depending on the components you use in your design, you may need to upgrade components or rerun some parts of your design flow. The following user guides walk you through the steps to upgrade your designs to Libero SoC v11.6:

SmartFusion2/IGLOO2 Design Migration User Guide

RTG4 Design Migration User Guide

Resolved Issues

Issues Resolved in Libero SoC v11.6

SAR66124: Synplify sometimes produces different EDIF output for the same input RTL

Synplify Pro ME J2015-03M-3 (the version packaged with Libero SoC v11.6) fixes an issue with repeatability of the post-synthesis netlist. In some previous versions of Synplify Pro ME, Synthesis could produce results that were logically and functionally equivalent, but could have different timing performance. This is no longer the case.

SAR60467: LSRAM and uRAM are not released to user design after SmartDebug access

This issue is resolved in Libero SoC v11.6. SmartDebug now releases LSRAM and uRAM control back to the user design after read/write operations.

SAR65145: M2S/M2GL060 live probe issue at the edge of each quadrant

When connected to probe points or flip-flops at the edge of each quadrant, Live Probe may not work correctly. These probe points or flip-flops can be identified in the chip-planner having X-coordinate of 215, 228, 443, 444, 659 and 672.

This issue is resolved in Libero SoC v11.6, and live probe is working for the probe points or flip-flops at all locations.

SAR66209: Incorrect addresses for LSRAM/uSRAM output Probe Points on West Clusters

This issue causes incorrect probe point or flip-flop address to be calculated for A_DOUT[16] and B_DOUT[16] for the LSRAM/uSRAM on the west most side of the device.

This issue is resolved in Libero SoC v11.6, and correct addresses are calculated.

SAR66237 - Remove all custom patterns and PCIe loopbacks from SERDES debug UI

The following SERDES debug features are removed from SmartDebug for SmartFusion2, IGLOO2 and RTG4:

- Rx custom pattern loopback
- All 1's and 0's loopback
- PLESIO loopback for PCIe

Customer Reported SARs Resolved in Libero SoC v11.6

SAR #	Product	Case Number	Summary
64699	CAE	493642-1813055338	In BFM, writemult64 does not look like a burst AXI write.
66192	CAE	493642-1838032095	RTG4 - NC-sim and VCS: APB_S_PSEL is declared twice for CCC; simulation tool flags an error
68745	Designer	493642-1867931754	Maximum input frequency to CCC dividers (GPD, RF, FB) has been updated
61896	Enhancement	493642-1737544555	Libero shows an information dialog box even if the MSS configuration is not changed.
66028	Enhancement	493642-1836406894, 493642-1843736807	SmartTime - Constraints Coverage Report Enhancement
66507	Enhancement	493642-1843284528	Option for "Repair_Minimum_Delay_Violations"
70422	FlashPro	493642-1861903185, 493642-1961681555	Syntax error in STP file
64181	FlashPro	493642-1803924472	Error: programmer '54250' : Line : 2980 Exception : The index is out of range.
67408	FlashPro	493642-1859503365	Error reported on saving PDB in FlashPro (Igloo device)
69619	FlashPro	493642-1916409332	Issues generate a Programming File in FlashPoint
60672	Help	493642-1721446555, 493642-1825092298, 493642-182949396	Update Libero Help Guide - SVF file format not yet supported for M2S/M2GL
62922	Power	493642-1766500065	DDR: ODT Support: SmartPower with ODT using LVCMOS18
60835	Project_Manager	493642-1722569223	Change order for timing constraints does not work in Libero 11.4
62497	Project_Manager	493642-1756620271	Update instance option do not appear for Linked HDL files
64150	Project_Manager	493642-1802214781	"Find and Replace" issues in Libero software
64617	Project_Manager	493642-1809162644	Smart Design components in the design hierarchy cannot be renamed in Libero
66327	Project_Manager	493642-1838059944, 493642-1867314289	VHDL check discrepancy
69055	Project_Manager	493642-1898026386	HDLPLUS: HDL+ definition on Linked RTL file is lost if Libero prj is closed
68929	Project_Manager	493642-1898026386	Libero doesn't pass the required RTL file to Synplify/ModelSim and flow fails

67968	SmartDesign	493642-1868306218	Libero says syntax error but "check HDL" passes for (Linked) HDL edited outside of Libero
62954	SmartGen	493642-1764988552	Pre synthesis simulation of Two Port RAM is not as expected
65059	SmartGen	493642-1813150608	SERDES: PCIe configurator needs to set MSI_OFFSET when enabling > 1 MSI
65317	Synopsys	493642-1566753874, 493642-1822158513	Synthesis failed because of Internal Error in m_proasic.exe (Error Code [proasicbuf.c:1883]).
59595	Synopsys	493642-1684661322, 493642-1810558965, 493642-1832386563	Error in m_generic.exe occurs due to anti-virus issue
60796	Synopsys	493642-1715674901	USRAM inference is incorrect when the write enable has width > 1
62053	Synopsys	493642-1748811030	Crash reported in Synplify (I201309MSP1-1)
62218	Synopsys	493642-1749664537	Synthesis reports internal error in m_proasic.exe
63215	Synopsys	493642-1774400970	Synthesis crashes on test case with VHDL multiplier
64350	Synopsys	493642-1808707374	RTG4 block flow: Internal Error in gdevchip.cxx", line 198 when block flow is enabled
66122	Synopsys	493642-1836815014	Synplify Pro is optimizing the generate statement in Verilog
66660	Synopsys	493642-1846668774	Synplify crash on CoreCordic when Y0 is connected to GND
57437	System Builder	493642-1635115817	System Builder limits user to use only CLK#0 dedicated PAD
63533	System Builder	493642-1779734116	CoreResetP: constraints for false paths should be autogenerated
54350	Timing	493642-1559559606	Cell Delay values :-Customer getting erroneous values for delay calculation
65924	Timing	493642-1811844238	Problem with constraining LVPECL signals
66167	Timing	493642-1818298918	Exported CSV file doesn't include the Failing Paths

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** and the installation will complete successfully.

Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider if you need assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version and security settings all contribute to the end result. Depending on your environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is protected by antivirus tools and other security measures.

RTG4

PCIESS memories error messages during simulation

The PCIESS macro might issue an error message during simulation if configured in the PCIe mode for an abnormal transition on the clock. The error message starts with: "** MEM_Error: Abnormal transition occurred", and can be safely ignored during simulation.

SmartDebug: Some PCIe and XAUI test patterns are not available

PMA built-in PRBS11,23 and 31 test pattern generation are not supported for PCIe and XAUI. These options will be removed in subsequent releases.

Cannot open project created with radiation limit >100 Krad in Libero SoC v11.6

Libero SoC RTG4 Launch users only: The supported maximum value for radiation limit has changed from 300 Krad in Libero SoC RTG4 Launch software to 100 Krad in Libero SoC v11.6. If you have created a project in RTG4 Launch software, you will not be able to open it in Libero SoC v11.6; you will see a dialog stating "The device is not set correctly". You must open your existing project in Libero SoC RTG4 Launch software, set the radiation limit to 100 Krad or less, and save your project. You can then open it in Libero SoC v11.6.

PCIe Signal Integrity Changes

The CTL equalization option has been removed from the Signal Integrity UI.

The following two lane registers were set when a user selected Short/Medium/Long reach, depending on the lane data rate.

- RE_AMP_RATIO
- RE_CUT_RATIO

The above registers are still available in the edit registers view and can be set manually. Refer to the RTG4 FPGA High Speed Serial Interfaces User Guide for details about setting these options manually.

Limited SERDES_REFCLK I/O standards supported

The following I/O standards are supported for the SERDES REFCLK I/O:

Single-ended: LVCMOS25, LVCMOS33, LVTTL

Differential: LVDS25, LVDS33

SpaceWire Clock Recovery Circuits Timing

On the SpaceWire Clock Recovery circuits, SmartTime in Libero SoCv11.6 shows the path from Strobe I/O. However, it does not show the path from the Data I/O. Both paths have the same delay.

Back-annotation is currently not supported for RX Clock/Data Recovery blocks in the CCC.

Power data is unavailable for uPROM and SpaceWire Clock/Data Recovery Circuits

SmartPower for Libero SoC v11.6 does not yet include power data for RTG4's uPROM, or for the clock/data recovery circuits of the RTG4 CCC. This data is expected to be included in a later release.

Upgrade High Speed Serial Interface components

Microsemi recommends that you upgrade any RTG4 High Speed Serial Interface cores to the latest versions. This will enable power estimation for these interfaces.

Upgrade CCC components

Microsemi recommends that you upgrade any RTG4 CCC core to the latest version. This will enable automatic constraint generation for configurations using phase shift.

SmartFusion2 and IGLOO2

M2S150, M2GL150: Must upgrade Fabric DDR Memory Controller component

If you created an M2S150 or M2GL150 design containing a Fabric DDR Memory Controller (FDDR) component with Libero SoC 11.5 SP3 or earlier version, as part of upgrading your project to Libero SoC v11.6, you must upgrade the core to the latest version to enable proper reset behavior.

Firmware Flow

SAR68547: Issue with exporting firmware to locations with spaces in the path

If your Libero SoC project path has spaces in it, and you try to export a firmware project, you may get an error popup with the text "JVM terminated. Exit code= -1", with the export step failing. To avoid this issue, ensure that there are no spaces in the folder hierarchy that the Libero SoC project is created in.

Programming

SAR70489: Cannot program device using FlashPro 3 programmer

With Libero SoC v11.6, you will not be able to program a device using the FlashPro3 programming hardware on Windows 8. There is no workaround.

SAR69162: VERIFY_DIGEST always fails in master file/job when external digest check is restricted

When "Restrict external Fabric/eNVM design digest check..." is set in Debug Policy in the Security Policy Manager, the VERIFY_DIGEST action will always fail for the master STAPL file and the master job (using FlashPro Express). You will see the following error message: "Error: Digest request from SPI/JTAG is protected by user pass key 1." There is no workaround.

SAR67849: Tcl parameter changes for FlashPro

If you are using the Tcl command: “configure_tool -name {PROGRAMMER_INFO}”, its clock mode parameter names have changed from “free_running_clock” and “discrete_clock” to “free_running_clk” and “discrete_clk”, respectively. You must update any Tcl scripts that are using the above parameters to use the changed versions.

SAR66392: Unable to open Programming Connectivity and Interface on RedHat/CentOS 6.4 and higher

On certain RHEL and CentOS 6.4-6.7 machines, when you try to open the Programming Connectivity and Interface dialog, Libero may crash or stop responding. There is no workaround at the moment.

ProASIC3, Fusion, and IGLOO QoR

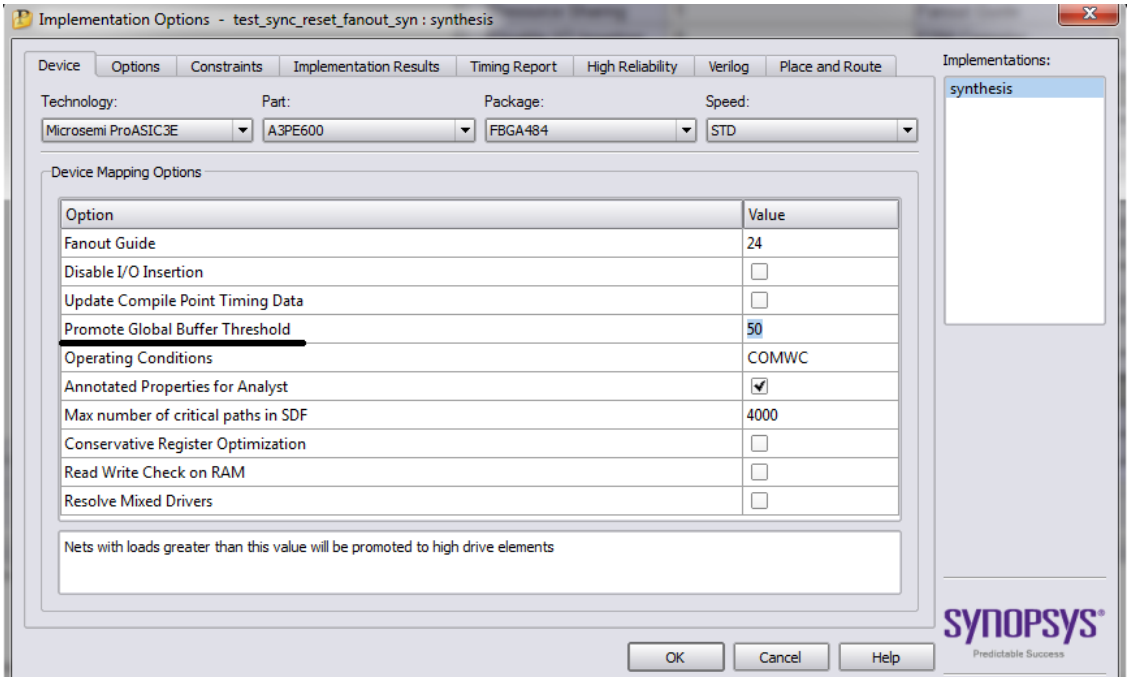
SAR73397 – Some SynplifyPro Configure options should not show for ProASIC3, Fusion, and IGLOO families – it might impact QoR

In the Libero SoC v11.6 release, there is QoR perturbation seen for ProASIC3, Fusion, and IGLOO families. If you are going to run synthesis with this release, use the following workaround to avoid the QoR degradation.

Workaround:

Open SynplifyPro interactively, go to the Implementation Options dialog box, and change the “Promote Global Buffer Threshold” value to **50**. See the figure below.

Click **OK** and run synthesis using this updated value of Gobal buffer threshold.



SmartDebug

SAR68444: Unable to access embedded Flash Memory (eNVM) error due to exclusive access

If you are using SmartDebug to access the eNVM for the M2S/M2GL 060, 090, or 150 devices, you may encounter an error with the message “Error: Unable to access embedded Flash Memory for your selected device: The firmware was unable to obtain exclusive access to the eNVM within the allotted time.”. This happens because there is another master in your design that is locking access to the eNVM to all other masters, including SmartDebug.

Workaround:

Release the lock on the eNVM after your master has completed its access operations. You need to write 0x00 to “REQACCESS” register in eNVM Control Registers (address 0x600801FC) to release the access.

Synopsys Tools

SAR 69615: Clarification on location of new Identify Implementations

When users launch "New Identify Implementation" within SynplifyPro which is invoked interactively through Libero SoC, a folder is created with the Identify implementation name :<Libero project>/synthesis/<impl. name>.

When users invoke "Identify Instrumentor" for this implementation, the implementation results are written to a different folder (<Libero project>/<impl. name>). The folder originally created (<Libero project>/synthesis/<impl. name>) remains empty.

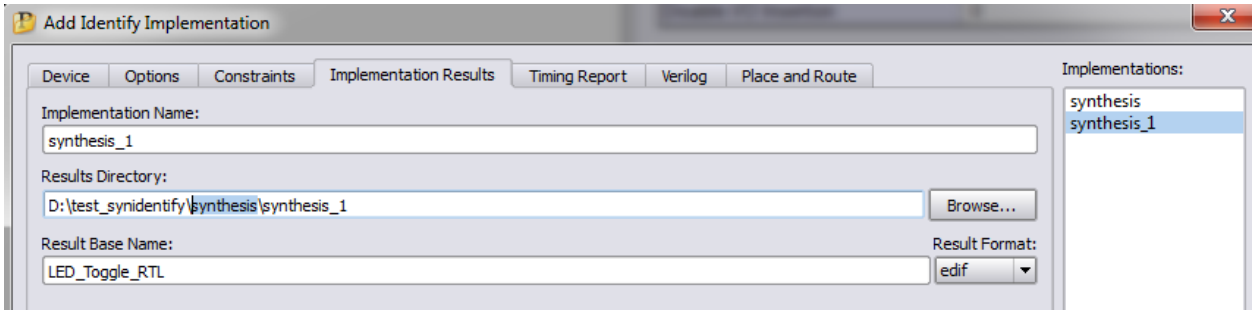
Due to this issue, Libero SoC is unable to find the instrumented .edn file for this Identify implementation, and users may see the error “Unable to find module name in <file path name >.edn”.

Workaround:

Use the “Identify Instrumentor” option to create an Identify Implementation (i.e. do not use the “New Identify Implementation” option)

OR

Manually change the directory path under the “Add Identify Implementation → Implementation Results” tab to <Libero project>/synthesis/<impl. name>.



Also refer to KB: http://soc.microsemi.com/kb/article.aspx?id=KI8980.

SAR67451: GTKWave UI: Unable to store properly the downloaded waveform as .VCD extension

If you are using the GTKWave waveform viewer with Identify, and you try to save the waveform as a .vcd file (using the File -> Export -> Write VCD File as ... option in the GTKWave viewer), the file may not be saved correctly (you may get an empty VCD file). This is due to a bug in the GTKWave viewer.

Workaround:

Type the command “write vcd <vcd file name>” from the Identify Debugger user interface.

SmartFusion2/IGLOO2 and RTG4 DDR_IN and DDR_OUT Static Inputs

The ADn and SDn pins of the DDR_IN and DDR_OUT are static inputs defined at design time. They must be tied to 0 or 1. If not, it may cause a DRC error:

```
Error: CMPG4-129: Pin '<instance_name>:SD' is a static configuration pin and must be
connected to a power net.
```

SmartFusion2, IGLOO2, RTG4 Place-and-Route

SAR 72083: Some High-Utilization Designs no longer complete Place-and-Route

Libero SoC v11.6 includes Quality of Results improvements for SmartFusion2 and IGLOO2 designs. A side effect of these improvements is that certain extremely high utilization designs may no longer be successfully placed. Reducing the size of the design, or relaxing region and floorplanning constraints, may help to improve timing closure and runtime.

SmartFusion2 and IGLOO2 Data Security

SAR 72582: Data Security: Some special sectors on ‘S’ devices are not being programmed

The following device special sectors are not being programmed if the user chooses to disable access:

- M2S060/M2GL060 (TS/S)
  - (0x3d000-0x3dfff)
- M2S060/M2GL060 (TS/S)
  - (eNVM1 (0x3e000-0x3efff, 0x3f000-0x3ffff))
    - These special sectors are invalid for M2S060/M2GL060
- M2S005/M2GL005 (TS/S), M2S010/M2GL010 (TS/S), M2S025/M2GL025 (TS/S)
  - (0x3d000-0x3dfff, 0x3e000-0x3efff)

SmartFusion2 and IGLOO2 Auto Update/Programming Recovery

SAR 73158: Auto Update and Programming Recovery are not supported for M2S050/M2GL050 devices

Auto Update and Programming Recovery are not supported for M2S050 and M2GL050 devices.

System Requirements

Refer to System Requirements on the Microsemi website for more information regarding operating systems support and minimum system requirements. A 64-bit OS is required for designing SmartFusion2, IGLOO2 and RTG4 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents web page.

Changes in OS Support

Supported

Windows 7, Windows 8.1

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6

** RHEL 5 and CentOS 5 do not support programming using FlashPro5.*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.6 installation:

- Synplify Pro ME J2015.03M-3
- ModelSim ME 10.3c
- Identify ME J2015.03M-1
- Synphony Model Compiler 2015.03M

Prerequisite Software: To run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.6

Installation requires Admin privileges.

Windows download

Linux download

SoftConsole v3.4 SP1 should be installed over SoftConsole v3.4 for use with Libero SoC v11.6.

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.6.

Download SoftConsole 3.4 SP1

Installation Note

After installation of Libero on Linux, any attempt to run the udev_install script for FlashPro setup will fail.

When running the script, users will see the following:

```
% ./udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:

The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, as such, is not a valid shell script.

Workaround:

Users must run dos2unix on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
% ./udev_install
```

If dos2unix is not available, users might need to run the following command, and then run dos2unix:

```
% sudo yum install dos2unix
```

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely that your questions have already been answered.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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