SmartTime for Libero SoC v11.6 SmartFusion2, IGLOO2, and RTG4 User's Guide

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Welcome to SmartTime

About SmartTime

SmartTime is a gate-level static timing analysis (STA) tool available for the SmartFusion2, IGLOO2 and RTG4 families. With SmartTime, you can enter Timing Constraints and perform complete timing analysis of your design to ensure that you meet all timing constraints and that your design operates at the desired speed with the right amount of margin across all operating conditions.

Note: See the <u>Timing Constraints</u> and <u>Timing Analysis</u> SmartTime help specifically for SmartFusion2, IGLOO2 and RTG4 if you are using those families.

Static Timing Analysis (STA)

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is well suited for traditional synchronous designs. Unlike dynamic simulation, STA does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements.

STA tools do not automatically detect false paths in their algorithms. STA reports all possible paths, including false paths, in the design. False paths are timing paths in the design that do not propagate a signal. To get a true and useful timing analysis, you need to identify those false paths, if any, as false path constraints to the STA tool and exclude them from timing considerations.

Timing Constraints

SmartTime supports a range of timing constraints to provide useful analysis and efficient timing-driven layout. SmartTime also includes a constraint checker that validates the constraints in the database.

Timing Analysis

SmartTime provides a selection of analysis types that enable you to:

- · Find the minimum cycle time that does not result in a timing violation
- Identify paths with timing violations
- Analyze delays of paths that have no timing constraints
- Perform inter-clock domain timing verification
- · Perform maximum and minimum delay analysis for setup and hold checks

To improve the accuracy of the results, SmartTime evaluates clock skew during timing analysis by individually computing clock insertion delays for each register.

SmartTime checks the timing requirements for violations while evaluating timing exceptions (such as multicycle or false paths).

SmartTime and Place and Route

Timing constraints impact analysis and place and route the same way. As a result, adding and editing your timing constraints in SmartTime is the best way to achieve optimum performance.

See Also

Starting and closing SmartTime SmartTime Components



Components of SmartTime Timing Analyzer Changing SmartTime preferences

Design Flows with SmartTime

You can access SmartTime in Designer either implicitly or explicitly during the following phases of design implementation:

- After <u>Compile</u> Run SmartTime to add or modify timing constraints or to perform pre-layout timing analysis. In the Libero SoC Design Flow window, expand Implement Design > Place and Route> Timing Constraints.
- During <u>Place and Route</u> When you select timing-driven place-and-route, SmartTime runs in the background to provide accurate timing information.
- After <u>Place and Route</u> Run SmartTime to perform post-layout timing analysis and adjust timing constraints. In the Libero SoC Design Flow window, expand **Implement Design > Verify Post-Layout** Implementation, right-click Verify Timing.
- During <u>Back-Annotation</u> SmartTime runs in the background to generate the SDF file for timing simulation.

You can also run SmartTime whenever you need to generate timing reports, regardless of which design implementation phase you are in.

See Also

Compile Layout Back-Annotation

Starting and Closing SmartTime

You must compile your design before using SmartTime. If you have not compiled your design, the software compiles it for you.

To edit timing constraints in SmartTime, in the Design Flow window under **Implement Design > Place and Route**, double-click **Timing Constraints**.

To verify timing, in **Implement Design > Verify Post Layout Implementation** right-click **Verify Timing** and choose **Open Interactively**.

SmartTime reads your design and displays post- or pre-layout

timing information. To close SmartTime, from the **File** menu, choose

Exit.

To save changes to your design, from the File menu, choose Save.

See Also

Importing Files Compiling your design Running Layout

SmartTime Components

SmartTime is composed of two main tools:

- <u>The SmartTime Constraints Editor</u> enables you to view and edit timing constraints in your design. Constraints are sorted by category (requirements and exceptions) and by constraint type.
- The <u>Maximum Delay Analysis View</u> enable you to analyze your design.







With SmartTime, you can:

- Browse through your design's various clock domains to examine the timing paths and identify those that violate your timing requirements
- Add and modify timing requirements and exceptions
- Set constraints on a specific pin or a specific set of paths
- Create customizable timing reports
- Navigate directly to the paths responsible for violating your timing requirements

SmartTime Constraint Scenario

A constraint scenario is an independent set of constraints. By default a scenario is created as *Primary Scenario* to hold all timing constraints defined by the user. This scenario will be used during both analysis and TDPR. Multiple scenarios can be created within SmartTime. Only one scenario can be used for analysis at a time. If multiple scenarios are created they will be displayed in separate Constraint Editor windows.

The scenarios window lists all timing constraints scenarios available for the current design.

To create a new scenario, from the **Constraints Editor choose Tools** > **Scenarios** > **New Scenarios**.

The icons tindicates it is the Primary Scenario. It is the default scenario when the Constraints Editor opens.

The new scenario option is also available from the Tools> Scenario > New Scenario.

You may click the undock is icon at the upper right hand corner to undock a scenario window.

New scenarios are named Scenario_1, Scenario_2 and so on by default when they are first created. From the scenarios window you can select a scenario and from the right-click menu, select:

- Use for Analysis: to use the selected scenario for Timing Analyzer. This command is also available from the <u>Advanced</u> tab in the SmartTime Tools> Options dialog box
- **Use for TDPR**: to use the selected scenario for Timing-driven Layout. This command is also available from the <u>Advanced</u> tab in the SmartTime Options dialog box
- · Clone scenario: to create a new scenario with a set of constraints based on an existing scenario
- Delete scenario: to delete the selected scenario
- · Rename scenario: to rename the selected scenario

New scenario: create a new scenario

Setting SmartTime Options

You can modify SmartTime options for timing analysis by using the <u>SmartTime Options</u> dialog box.

To set SmartTime options:

1. From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools> Options**.

The SmartTime Options dialog box has three categories: General, Analysis and Advanced.

- 2. In the **General** category, select the settings for the operating conditions. SmartTime performs maximum or minimum delay analysis based on the Best, Typical, or Worst case.
- 3. Check or uncheck whether you want SmartTime to use inter-clock domains in calculations for timing analysis.
- 4. Click **Restore Defaults** only if you want the settings in the General pane to revert to their default settings.
- 5. Click Analysis to display the options you can modify in the Analysis view.
- 6. Enter a number greater than 1 to specify the maximum number of paths to include in a path set during timing analysis.
- 7. Check or uncheck whether to filter the paths by slack value. If you check this box, you must then specify the slack range between minimum slack and maximum slack.
- 8. Check or uncheck whether to include clock network details.



- 9. Enter a number greater than 1 to specify the number of parallel paths in the expanded path.
- 10. Click **Restore Defaults** only if you want the settings in the Analysis View pane to revert to their default settings.
- 11. Click Advanced to display advanced options.
- 12. Check or uncheck whether to use loopback in bidirectional buffers (bibufs) and/or break paths at asynchronous pins. Check or uncheck whether to disable non-unate arcs in the clock path. If using **Scenarios**, pick the appropriate scenario for timing analysis and timing driven place-and- route.
- 13. Click **Restore Defaults** only if you want the settings in the Advanced pane to revert to their default settings.
- 14. Click **OK**.

SmartTime Options	? <u>***</u>
Option Categories Select a category: General Analysis Advanced	General Operating Conditions Perform maximum delay analysis based on WORST case Perform minimum delay analysis based on BEST case Clock Domains Include inter-clock domains in calculations for timing analysis. I Include inter-clock domains in calculations for timing analysis. Restore Defaults
Help	OK Cancel

Figure 1 · SmartTime Options Dialog Box – General Options

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Option Categories	Analysis View	
 Select a category: General 	Display of Paths	
Analysis Advanced	Limit the number of paths shown in a path set to: 100	
	 Filter the paths by slack value Slack range from: ns to: ns Show clock network details in expanded path Limit the number of parallel paths in expanded path to: 1 	
Help	Restore Defaults OK Cance	

Figure 2 · SmartTime Options Dialog Box – Analysis Options

Option Categories	Advanced	
 Select a category: General Analysis Advanced 	Special Situtations Use loopback in bi-directional buffers(bibufs) Break paths at asynchronous pins Disable non-unate arcs in clock network Scenarios Use this scenario for timing analysis : Use this scenario for timing-driven place-and-route:	Primary Primary
Help		Cancel

Figure 3 · SmartTime Options Dialog Box – Advanced Options



See Also

SmartTime Options dialog box

SmartTime Toolbar

Table 1 · SmartTime Toolbar

lcon	Description					
	Save the Changes					
<u>រ</u>	Undoes previous changes					
<u>e</u>	Redoes previous changes					
2	Opens the maximum delay analysis view					
×	Opens the minimum delay analysis view					
<u>@</u>	Opens the manage clock domains manager					
×	Opens the path set manager					
8	Recalculates all					
2	Opens the constraints editor					
žn	Opens the create clock constraint dialog box					
Ser.	Opens the create generated clock constraint dialog box					
∞	Opens the set input delay clock constraint dialog box					
¥⊠	Opens the set output delay clock constraint dialog box					
<u>.</u>	Opens the set false path constraint dialog box					
<u>×</u>	Opens the set maximum delay constraint dialog box					
<i>"</i> ∆	Opens the set minimum delay constraint dialog box					



M.	Opens the set multicycle constraint dialog box
C:	Opens the set clock source latency dialog box
<u>1</u>	Opens the set constraint to disable timing arcs dialog box
<u>š</u>	Opens the set clock-to-clock uncertainty constraint dialog box
<u>B.</u>	Opens the constraint wizard

SmartTime Constraints Editor

Components of the SmartTime Constraints Editor

SmartTime Constraints Editor is a tool in the Designer software that enables you to create, view, and edit timing constraints of the selected scenario for use with SmartTime timing analysis and timing-driven optimization tools. This editor includes powerful visual dialogs that guide you toward capturing your timing requirements and timing exceptions quickly and correctly. In addition, it is closely connected to the SmartTime Timing Analysis View, which enables you to analyze the impact of constraint changes.

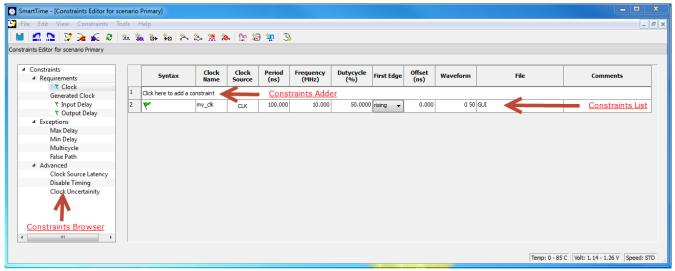


Figure 4 · SmartTime Constraints Editor View

Constraint Hierarchy Browser

The SmartTime Constraints Editor window is divided into a Constraint Browser and a Constraint List. The Constraint Browser categorizes constraints based on requirements, exceptions and Advanced cateogries, while the Constraint List provides details about each constraint and enables the user to add, edit and delete constraints.

You can perform the following tasks in the SmartTime Constraints View:

- Select a constraint type from the Constraint Browser and create or edit the constraint.
- Add a new constraint and check the syntax.
- To add a constraint, double-click on the constraint type; to edit a constraint, select the constraint from the constraint list, right-click and choose Edit Constraint.
- Select a row and right-click to display the shortcut menu, which you can use to edit, delete, or copy the selected constraint to a spreadsheet.
- Select the entire spreadsheet and copy it to another spreadsheet.

See Also

Editable Grid and Quick Adder SmartTime scenarios



Editable Constraints Grid

The Constraints Editor allows you to add, edit and delete constraints directly from the Constraints Editor View.

🗣 Constraints Editor
Constraints Editor Constraints Constraints Clock Name Clock Source Cincs Frequency Dutycycle First Offset Comme Clock Clock Name Clock Source Cincs File Comme Clock Clock Name Clock Source Cincs File Comme Clock Clock Source Clock Clock Source Clock Cloc

Figure 5 · Constraints Editor View

To add a new constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Enter the constraint values in the first row and click OK. Click the Save icon.
- 3. The new constraint is added to the Constraint List. The green syntax flag indicates that the constraint was successfully checked.

To edit a constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Select the constraint, edit the values and click **Save**. The green syntax flag indicates that the syntax check for the constraint was successful.

To delete a constraint:

- 1. Select a constraint type from the constraint browser.
- 2. Select the constraint you want to delete and from the right-click menu, select Delete Constraint.

Constraint Wizard

The SmartTime Constraint Wizard enables you to quickly and easily create clock and timing I/O constraints for your design.

To open the Constraint Wizard (shown below) from the SmartTime Tool menu, click the Constraint

Wizard icon . ____. This window can be resized.



Constraint Wizard

Constraint Wizard	×
Introduction to S	SmartTime Constraint Wizard you in creating constraints for clocks and I/Os in your design. The constraints created by the Wizard can be modified later from the Constraints Editor. You can use the Wizard sequentially by clicking Next at each Alternatively, you can access each individual step in the Wizard by clicking a step in the Constraint Wizard flow, available on the left column of this window. All steps in this Wizard are optional. Click Finish at any time to skip the remaining steps. Don't show this introduction again
Нер	< Back Next > Cancel

Figure 6 · Constraint Wizard

This window provides information about the Constraint Wizard and how to use it. Check the **Don't show this introduction again** box to skip this window next time you use this wizard.

Click Next to continue to the next step in the wizard.

Note: All steps in this Wizard are optional and you can exit the wizard by clicking Finish.



Overall Clock Constraint

Figure 7 · Constraint Wizard – Overall Clock Requirements

In this window you can set a default required period or frequency for all explicit clocks in your design. Clocks that already have a constraint will not be affected.

To set a constraint for all explicit clocks, enter the **Period** or the **Frequency**, and click **Next** to go to the next step or **Finish** to exit the wizard.



Overall I/O Constraint

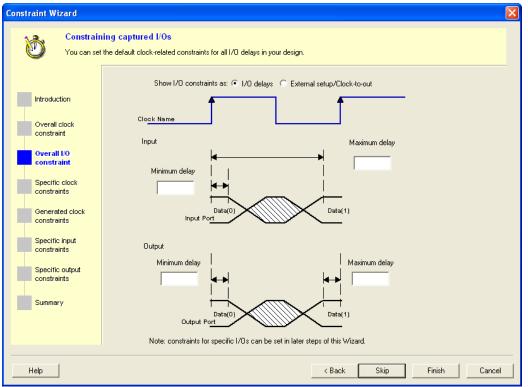


Figure 8 · Constraint Wizard - Overall I/O Constraint

In this window you can set a default constraint for all I/Os in the design. Constraints will be applied with respect to clocks related to the I/Os. This constraint will not override existing I/O constraints.

Show I/O constraints enables you to display I/O constraints as I/O delays (minimum and maximum delays for input and output) or external setup/clock-to-out.

To set a constraint for all I/Os:

- 1. Enter the Maximum and/or Minimum delays for the Input and/or Output.
- 2. Click Next to go to the next step or Finish to exit the wizard.



Specific Clock Constraints

Constraint Wizard									X
Constraining indi You can set constraints									
Introduction	Syntax	Clock Name	Period (ns)		Hold (ns)	Max Input Delay (ns)	Min Input Delay (ns)	Max Clock-to-out (ns)	Min Clock-I (ns)
Overall clock constraint		e to add a cons		potential cloc	k pin				
- Constraint		CLK_IN	4.000						
Overall I/O —		DATA_REG_	2.000						
constraint		SM_RD:Q step[1]:Q	4.000						
Specific clock constraints Generated clock constraints Specific input constraints Specific output constraints Summary									
Va.	ning:Some	potential clock		esign are not o	constrained.				>
Help						< Back	Next >	Finish	Cancel

Figure 9 · Constraint Wizard – Specific Clock Constraints

In this window you can set a period and I/O timing constraints for a specific clock domain. All I/Os within the domain will be affected by the I/O timing constraints. You can modify the constraints from the grid.

To add a constraint for a potential clock:

- 1. Click the first row in the grid, enter the constraint information, and click the green check mark.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is a potential clock in your design.



Generated Clock Constraints

Constraint Wizard	Σ
A TRANS	generated clocks raints for generated clocks.
Introduction	Current Die Defensee Die Melliefer Dieider External External Max Input Min Input Cur
Overall clock constraint	Syntax Clock Pin Reference Pin Multiplier Divider External Setup (ns) External Hold (ns) Max Input Delay (ns) Min Input Delay (ns) Clo Click here to add a constraint on a potential clock pin Click here to add a constraint on a potential clock pin Click here to add a constraint on a potential clock pin Click here to add a constraint on a potential clock pin Click here to add a constraint on a potential clock pin
Overall I/O constraint	
Specific clock constraints	
Generated clock constraints	
Specific input constraints	
Specific output constraints	
Summary	
	Warning: Some potential clocks in your design are not constrained.
Help	< Back Next > Finish Cancel

Figure 10 · Constraint Wizard – Generated Clock Constraints

In this window you can set a period and I/O timing constraints for a specific generated clock domain. You can modify the constraints from the grid.

To add a constraint for a generated clock:

- 1. Click the first row in the grid, enter the constraint information, and click the green check mark.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is a generated clock in your design.



Specific Input Constraints

N TO N	individual in straints for specific						
Introduction	Syntax	Port Name	Clock	External Setup (ns)	Max Input Delay (ns)	Min Input Delay (ns)	
Overall clock	- Y	CPUADD[0]	CLK_IN				
constraint	- Y	CPUADD[1]	CLK_IN				
	- Y	CPUADD[2]	CLK_IN				
Overall I/O	- Y	CPUADD[3]	CLK_IN				
constraint	Y	CPUADD[4]	CLK_IN				
	7	CPUADD[5]	CLK_IN				
Specific clock constraints	- W	CPUADD[6]	CLK_IN				
constraints	- W	CPUDATA[0]	CLK_IN				
Generated clock	- P	CPUDATA[10]	CLK_IN				
constraints	- P	CPUDATA[11]	CLK_IN				
	- P	CPUDATA[12]	CLK_IN				
Specific input	- P	CPUDATA[13]	CLK_IN				
constraints	- P	CPUDATA[14]	CLK_IN				
Specific output	- P	CPUDATA[15]	CLK_IN				
constraints	- P	CPUDATA[1]	CLK_IN				
		CPUDATA[2]	CLK_IN				
Summary	T Y	CPUDATA[3]	CLK_IN				
Summary		CPUDATA[4]	CLK_IN				
	- ·	CPUDATA[5]	CLK_IN				
	- ÷	CPUDATA[6]	CLK_IN				
				-	 		

Figure 11 · Constraint Wizard – Specific Input Constraints

In this window you can set constraints for specific input pins. You can modify the constraints from the grid.

To set a constraint for an input pin:

- 1. Set the maximum and/or minimum input delay for selected pin in the grid.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is an input pin in your design.



Specific Output Constraints

nstraint Wizard								
NTE N	individual ou straints for specific	•						
Introduction				Max				
	Syntax	Port Name	Clock	Clock-to-out (ns)	Min Clock-to-out (ns)	Max Uutput Delay (ns)	Min Output Delay (ns)	
Overall clock	Y	BYPASS	CLK_IN					1
constraint		CPUDATA[0]	CLK_IN					1
Overall I/O	Y	CPUDATA[10]	CLK_IN					1
constraint	Y	CPUDATA[11]	CLK_IN					1
	Y	CPUDATA[12]	CLK_IN					1
Specific clock	- Y	CPUDATA[13]	CLK_IN					
constraints		CPUDATA[14]	CLK_IN					
	Y	CPUDATA[15]	CLK_IN					1
Generated clock constraints	Y	CPUDATA[1]	CLK_IN					1
Constraints	Y	CPUDATA[2]	CLK_IN					1
Specific input		CPUDATA[3]	CLK_IN					
constraints	- Y	CPUDATA[4]	CLK_IN					1
	Ý	CPUDATA[5]	CLK_IN					
Specific output	- Y	CPUDATA[6]	CLK_IN					
constraints	- Y	CPUDATA[7]	CLK_IN					1
	- •	CPUDATA[8]	CLK_IN					1
Summary	- •	CPUDATA[9]	CLK_IN					
	- V	CPU_NREADY	CLK_IN					
	T Y	CRC32_SRAM	_					
		CDC32 CDAM		1	1			
						_	1	
Help				<	Back Next>	Finis	h Car	ncel

Figure 12 · Constraint Wizard – Specific Output Constraints

In this window you can set constraints for specific output pins. You can modify the constraints from the grid.

To set a constraint for an output pin:

- 1. Set the maximum and/or minimum output delay for selected pin in the grid.
- 2. Click **Next** to go to the next step or **Finish** to exit the wizard.

Note: This option is available only when there is an output pin in your design.



Summary

Constraint Wizard	
Summary	stuly completed the Constraint Wizard. te the constraints listed below. Image: Summary Image: All explicit clocks Image: All inputs Maximum input delay: 7 ns Image: All outputs Image: All outputs Image: All outputs Image: All outputs Image: Maximum output delay: 7 ns Image: Maximum output delay: 7 ns Image: Maximum output delay: 3 ns
Summary	
Help	< Back Finish Cancel

Figure 13 · Constraint Wizard – Summary

This window summarizes the requirements specified in the wizard and information about all clock and I/O constraints in the design.

Click Finish to create the constraints.

See Also

Editable Grid and Quick Adder

Using Clock Types

Clock constraints enable you to specify your clock sources and clock requirements, such as the frequency and duty cycle. SmartTime detects possible clocks by tracing back the design from the clock pins of all sequential components until it finds an input port, the output of another sequential element, or the output of a PLL. SmartTime classifies clock sources into three types:

- Explicit clocks
- Potential clocks
- <u>Clock network</u>

Grouping clocks into these three types helps you manage clock domains efficiently when you add a new clock domain for analysis or when you create a new clock constraint using the Select Source Pins for Clock Constraint dialog box (as shown below).



Select Source Pins for Clock Co	nstraint	
Specify pins 💿 by explicit list	C by keyword and wildcard	
Available Pins:	Assigned Pins:	
CPUClk VidRefClk	Add >	
	Add All >	
	< Remove	
	< Remove All	
Filter available objects:		
Pin Type: Explicit clocks	<u> </u>	
*	Filter	
Help	ОК	Cancel

Figure 14 · Select Source Pins for Clock Constraint Dialog Box

See Also

Select Source Pins for Clock Constraint dialog box Understanding explicit clocks Understanding potential clocks Understanding clock networks

Understanding Explicit Clocks

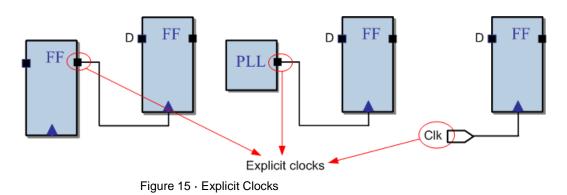
Explicit clocks are pins or ports connected to the clock pin of one or more sequential component, and where each clock is one of the following:

- The output of a PLL
- An input port that does not get gated between the source and the clock pins it drives
- The output pin of a sequential element that does not get gated between the source and the clock pins it drives
- Any pin or port on which a clock constraint was specified

By default, SmartTime displays domains with explicit clocks in the Timing Analysis View. You can browse these domains in the Domain Browser of the Timing Analysis View.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. **View the online help included with software to enable all linked content.**





See Also

Choose the Clock Source dialog box Using clock types Understanding potential clocks Understanding clock networks

Understanding Potential Clocks

Potential clocks are the clock sources that could be either enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks. When associated with gated clocks, SmartTime cannot differentiate between the enabled sources and clock sources. Both sources appear in the potential clocks list and not the explicit clocks list.

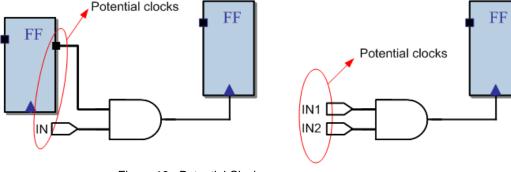


Figure 16 · Potential Clocks

See Also

Choose the Clock Source dialog box Using clock types Understanding explicit clocks Understanding clock networks

Understanding Clock Networks

Clock networks are internal clock network pins used as a clock source. With this network type, you can set the clock constraint on any pin in the clock network. You may want to do this to eliminate clock network pessimism by short-cutting a reconvergent combinational logic on the clock network (as shown below). Clock network pessimism triggers an overestimation of the clock skew, making the timing analysis inaccurate.



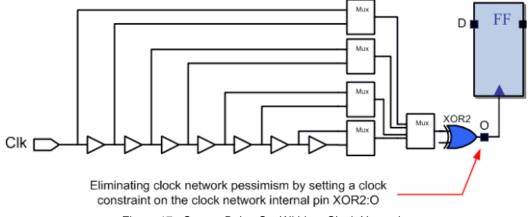


Figure 17 · Source Being Set Within a Clock Network

See Also

Choose the Clock Source dialog box Using clock types Understanding potential clocks Understanding clock networks

Specifying Clock Constraints

Specifying <u>clock</u> constraints is the most effective way to constrain and verify the timing behavior of a sequential design. Use clock constraints to meet your performance goals.

To specify a clock constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Create Clock Constraint</u> dialog box using one of the following methods:
 - Click the icon.
 - Right-click the Clock in the Constraint Browser.
 - Double-click any field in the Generated Clock Constraints grid.

The Create Clock Constraint dialog box appears (as shown below).



Create Clock Constraint			?	x
Clock Name :	Clock Source :		•	
Period :	ns 😽	or Frequency:		Mhz
← Offset : ─ ➡ Duty cycle : ─ ➡ 0.000 ns 50.0000 %				
Comment :				
Help		ОК	Cance	

Figure 18 · Create Clock Constraint Dialog Box

- 2. Select the pin to use as the clock source. You can click the **Browse** button to display the <u>Select</u> <u>Source Pins for Clock Constraint</u> dialog box (as shown below).
 - Note: Do not select a source pin when you specify a virtual clock. Virtual clocks can be used to define a clock outside the FPGA that it is used to synchronize I/Os.

Use the **Choose the Clock Source Pin** dialog box to display a list of source pins from which you can choose. By default, it displays the explicit clock sources of the design. To choose other pins in the design as clock source pins, select **Filter available objects - Pin Type** as **Explicit clocks**, **Potential clocks**, **Input ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. To display a subset of the displayed clock source pins, you can create and apply a filter. Multiple source pins can be specified for the same clock when a single clock is entering the FPGA using multiple inputs with different delays.

Click **OK** to save these dialog box settings.

- 3. Specify the Period in nanoseconds (ns) or Frequency in megahertz (MHz).
- 4. Modify the Clock Name. The name of the first clock source is provided as default.
- 5. Modify the Duty cycle, if needed.
- 6. Modify the **Offset** of the clock, if needed.
- 7. Modify the first edge direction of the clock, if needed.
- 8. Click **OK**. The new constraint appears in the Constraints List.

Note: When you choose File > Save, SmartTime saves the newly created constraint in the database.

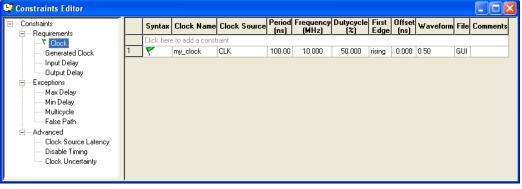


Figure 19 · SmartTime Timing Constraint View



See Also

<u>Clock</u> definition <u>Create a clock</u> <u>Create clock constraint dialog box</u>

Specifying Generated Clock Constraints

Specifying a generated clock constraint enables you to define an internally generated clock for your design and verify its timing behavior. Use generated clock constraints and <u>clock constraints</u> to meet your performance goals.

To specify a generated clock constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Create Generated Clock Constraint</u> dialog box using one of the following methods:
 - From the Actions menu, choose Constraints > Generated Clock.



- Right-click the GeneratedClock in the Constraint Browser.
- Double-click any field in the Generated Clock Constraints grid.

The Create Generated Clock Constraint dialog box appears (as shown below).

Create Generated Clock Constraint	×
Clock Reference:	
Clock Port FPGA	
Generated Clock Name	
The generated frequency is such as	
f(clock) = f(reference) × 1 / 1 Get Pre-Computed Factors	
The generated waveform is the same as 💌 the reference waveform	
Comment:	
	-
Help OK Cancel	

Figure 20 · Create Generated Clock Constraint



Using Automatically Generated Clock Constraints

 Select a Clock Pin to use as the generated clock source. To display a list of available generated clock source pins, click the Browse button. The <u>Select Generated Clock Source</u> dialog box appears (as shown below).

Sele	ect Generated Clock Source	×
5	Select a pin:	
	XCMP33/U0/U2_DDR1:Q XCMP33/U0/U2_DDR2:Q pll1:CLK1 pll1:CLK2	
ſ	Filter available objects:	
	Type: Explicit clocks	
	Filter:	
	* Filter	
	Help OK Cancel	

Figure 21 · Select Generated Clock Source Dialog Box

- 3. Modify the **Clock Name** if necessary.
- 4. Click **OK** to save these dialog box settings.
- 5. Specify a **Clock Reference**. To display a list of available clock reference pins, click the **Browse** button. The <u>Select Generated Clock Reference</u> dialog box appears.
- 5. Click **OK** to save this dialog box settings.
- 6. Specify the values to calculate the generated frequency: a multiplication factor and/or a division factor (both positive integers).
- 7. Specify the first edge of the generated waveform either same as or inverted with respect to the reference waveform.
- 8. Click OK. The new constraint appears in the Constraints List.
- Tip: From the File menu, choose Save to save the newly created constraint in the database.

See Also

Design Constraint Guide: <u>Clock</u> definition Design Constraint Guide: <u>Create a clock</u> <u>Create clock constraint dialog box</u>

Using Automatically Generated Clock Constraints

If your design uses a static PLL, SmartTime automatically generates the required frequency at the output of the PLL, provided you have supplied the input frequency. When you start SmartTime, a generated clock constraint appears in the Constraints List with the multiplication



and division factor extracted from the PLL configuration. The **File** column specifies this constraint as **auto-generated** (as shown below).

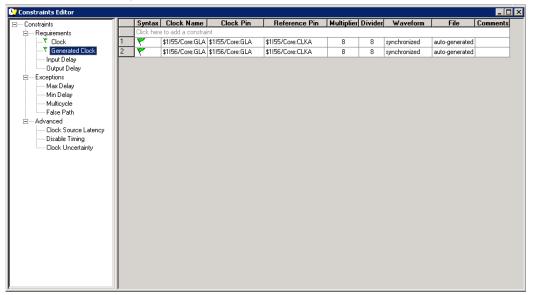


Figure 22 · Constraints Editor

Note: SmartTime does not automatically create a Generated Clock constraint if you have already set a constraint on the PLL output.

If you delete the automatically generated clock constraint, SmartTime does not regenerate it the next time you open the design. However, you can easily create it again by using the following steps:

1. Open the Create Generated Clock Constraint dialog box (as shown below).



Create Generated Clock Constraint	×
Clock Reference:	
Clock Port FPGA	
Generated Clock Name	
The generated frequency is such as	
f(clock) = f(reference) × 1 / 1 Get Pre-Computed Factor	rs
The generated waveform is the same as 💌 the reference waveform	
Comment:	
	-
Help OK Cancel	

Figure 23 · Create Generated Clock Constraint

- 2. Select the PLL output as the Clock Pin source for the generated clock.
- 3. Select the PLL input clock as the **Clock Reference** for the generated clock.

4. Click **Get Pre-Computed Factors**. SmartTime retrieves the factor from the static PLL configuration.

5. Click **OK**.

See Also

Create Generated Clock Constraint (SDC)

Specifying an Input Delay Constraint

Use the input delay constraint to define the arrival time of an input relative to a clock.

To specify an input timing delay constraint:

1. From SmartTime Constraints Editor, Open the Set Input Delay Constraint dialog box using one of the following methods: From the SmartTime **Actions** menu, choose **Constraints > Input Delay**.



- Right-click the Input Delay in the Constraint Browser and choose Add Input Delay Constraint.
- Double-click Input Delay in the Constraints Browser.

The Add Input Delay Constraint dialog box appears (as shown below). The Set Input Delay Constraint dialog box appears (as shown below).



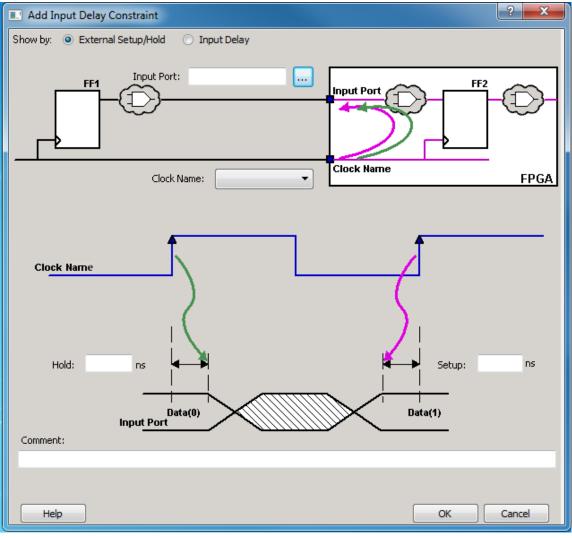


Figure 24 · Add Input Delay Dialog Box

2. Select either External Setup/Hold or Input Delay.

- External Setup/Hold enables you to enter an input delay constraint by
 - specifying the timing budget inside the FPGA using the external setup and hold time. This is the default selection.
- Note: The external hold information is currently used for analysis only and not by the optimization tools. For the basic timing analysis flow of a simple design, select External Setup/Hold.
 - Input Delay enables you to enter an input delay constraint by
 - specifying the timing budget outside the FPGA. You can enter the
 - Maximum Delay, the Minimum Delay, or both.
- Note: The Minimum Delay is currently used for analysis only and not by the optimization tools.

When you change values in one view, SmartTime automatically updates the other view.



2. Specify the **Input Port** or click the **Browse** button to display the **Select Ports for Input Delay** dialog box.

Select Ports for Input Delay		? ×
Specify pins :- () by explicit list () by keyw	vord and wildcard	
Available Pins:	Add Assigned Pins:	
CLK		
EN	Add All	
RST	Remove All	
Filter available pins :		Help
Pin Type : Input Ports	•	ОК
*	Filter	Cancel

Figure 25 · Select Ports for Input Delay Dialog Box

- 1. Select the name of the input pin(s) from the **Available Pins** list. Choose the **Pin Type** from the drop- down list. You can use the filter to narrow the pin list. You can select multiple ports in this window.
- 2. Click Add or Add All to move the input pin(s) from the Available Pins list to the Assigned Pins list.
- 3. Click OK.

The Add Input Delay Constraint dialog box displays the updated Input Port information.



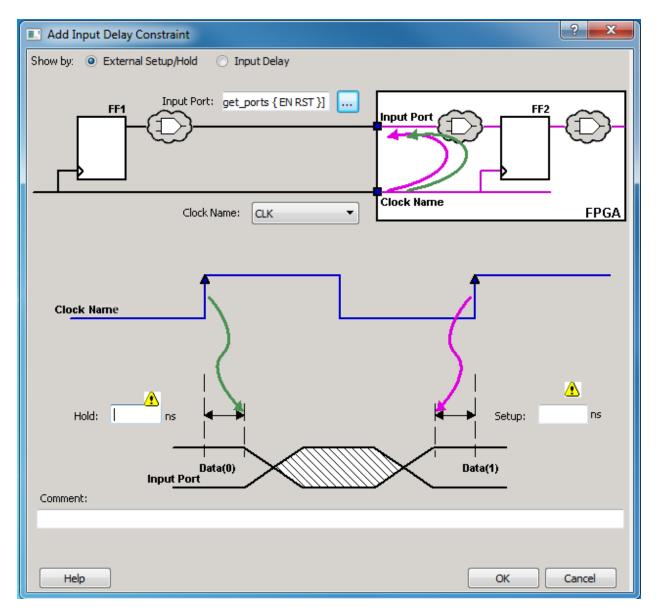


Figure 26 · Updated Add Input Delay Constraint Dialog Box

- 6. Select a clock from the **Clock Port** drop-down list.
- 7. If you selected **Show by: External Setup/Hold**, specifythe External Setup. If you selected **Show by: Input Delay**, specify the Maximum Delay value.
- If you selected Show by External Setup/Hold, specify the External Hold. If you
 - selected Show by: Input Delay, specify the Minimum Delay value.
- 9. Click **OK**.

SmartTime adds this constraint to the Constraints List in the SmartTime Constraints Editor.

See Also

Set Input Delay Constraint dialog box Select Source or Destination Pins for Constraint dialog box



Specifying an Output Delay Constraint

Use the output delay constraints to define the output delay of an output relative to a clock.

To specify an output delay constraint:

- 1. Add Output Delay Constraints using one of the following methods:
- 2. Click the 📩 icon
- Right-click the Output Delay in the Constraint Browser and choose Add Output Delay Constraints.
- Double-click Output Delay in the Constraints Browser.

The Add Output Delay Constraint dialog box appears.

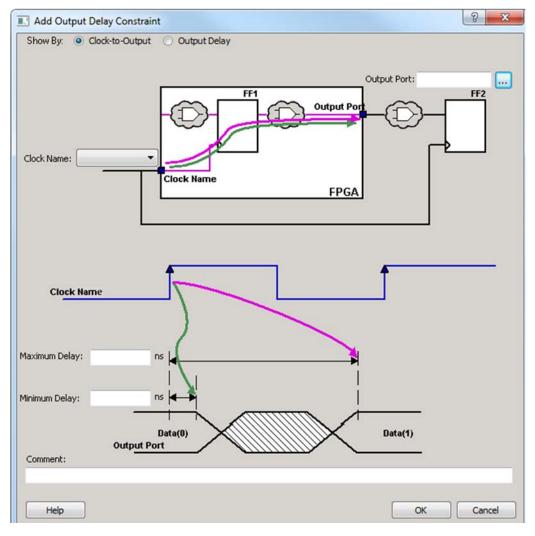


Figure 27 · Add Output Delay Constraint Dialog Box

Specify either Clock-to-Output or Output Delay.

• **Clock-to-Output** enables you to enter an output delay constraint by specifying the timing budget inside the FPGA. This is the default selection.

Note: The Minimum Delay value is currently used for analysis only and not by the optimization tool.



• **Output Delay** enables you to enter an output delay constraint by specifying the timing budget outside the FPGA. You can enter either the Maximum Delay, the Minimum Delay, or both. **Note**: The Minimum Delay is currently used for analysis only and not by the optimization tools.

When you change values in one view, SmartTime automatically updates the values in the other view.

3. Enter the name of the **Output Port** or click the Browse button to display the **Select Ports for Output Delay** dialog box.

Select Ports for Output Delay	? ×
Specify pins :- 💿 by explicit list 🔘 by keyword and wildcard	
Available Pins: Add Add All Q Q[0] Q[1] Q[1] Q[2] Q[3] Remove All	
Filter available pins : Pin Type : Output Ports * Filter	Help OK Cancel

Figure 28 · Select Ports for Output Delay Dialog Box

- 4. Select the output pin(s) from the **Available Pin** list. Choose the **Pin Type** from the dropdown list. You can use the filter to narrow the pin list. You can select multiple ports in this dialog box.
- 5. Click Add or Add All to move the output pin(s) from the Available Pins list to the Assigned Pins list.
- 6. Click **OK**. The **Set Output Delay Constraint** dialog box displays the updated representation of the Output Port graphic.
- 7. Select a clock port from the Clock Port drop-down list.
- 8. Enter the Maximum Delay value.
- 9. Enter the Minimum Delay value.
- 10. Click OK. SmartTime adds this constraint to the Constraints List in the Constraints Editor.

See Also

Set Output Delay Constraint dialog box Select Source or Destination Pins for Constraint dialog box



SmartTime Timing Analyzer

Components of the SmartTime Timing Analyzer

Use the SmartTime Timing Analyzer to visualize and identify timing issues in your design for the selected scenario. In this view, you can evaluate how far you are from meeting your timing requirements, create custom sets to track, set timing exceptions to obtain timing closure, and cross-probe paths with other tools.

The timing analysis view includes:

Demois Desures

- Domain Browser: Enables you to perform your timing analysis on a per domain basis.
- Path List: Displays paths in a specific set in a given domain sorted by slack.
- Path Details: Displays detailed timing analysis of a selected path in the paths list.
- Analysis View Filter: Enables you to filter the content of the paths list.

- ...

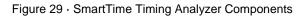
• Path Slack Histogram: When a set is selected in the Domain Browser, the Path Slack Histogram displays a distribution of the path slacks for that set. Selecting one or multiple bars in the Path Slack Histogram filters the paths displayed in the Path List.

```
You can copy, change the resolution and the number of bars of the chart from the right-click menu.
```

	iximum Delay Anal	ysis View	/								E	
C			From	*			То	*				
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- 5	1 Summary	-						Appl	y Filter	Store Filter	Res	et Filter
ļ	St Datashee₩ × @ CLK8M			Source Pin		Sink Pin	Delay (ns)	Slack	Arrival (ns)	Required (ns)	Setup (ns)	Minii Perio
	 Register to R 		U_SBI	/U3/rwra:CLK	U_SE	31/U3/w/R:D	5.658	53.655	7.916	61.571	0.668	1 0110
	External Setup Clock to Output		1 2(2)	PM031/U_CORE/c CLK	P_st	31/U4/bram_a(12):D	48.407	70.731	50.722	121.453	0.867	
	 Register to Asyn External Recover 	iv L	3 U_TOF f_2[2]:	PM031/U_CORE/	^{con} ti_st	BI/U4/bram_a[1]:D	47.470	71.611	49.785	121.396	0.867	
	Asynchronous to		4 U_TOF f_1[3]:	PM031/U_CORE/o	^{con} U_SE	31/U4/bram_a(12):D	47.412	71.726	49.727	121.453	0.867	
Ī	× Register to R		5 U_TOF f_2[2]:	PM031/U_CORE/c CLK	^{con} U_SE	31/U4/bram_a(14):D	47.183	71.910	49.498	121.408	0.867	
1	E litere si s quin		6 U_TOPM031/U_CORE/cor f_0_0[2]:CLK		con U_SE	31/U4/bram_a(12):D	47.269	49.538	121.453	0.867		
	10											>
1	100		From:	s for path U_SBI/U3/rwra SBI/U3/WR:D	:CLK							
	80 -		10.0	Pin Name		Туре	Net I	lame	lay (ns) T	otal (n		
									,			
									-			61.5
	70 -		data re	ouired time								7.9
aths				quired time								
of paths	70 -			quired time rival time	<u> </u>							
# of paths	70 -		data a slack	rival time	ulation							
# of paths	70 - 60 - 50 -		data a slack	rival time arrival time cale	ulation						0.000	
of pa	70 - 60 - 50 - 40 - 30 -		data a slack Data	rival time arrival time cale	ulation	Clock source				•	0.000	53.65
# of paths	70 - 60 - 50 - 40 -		data a slack Data CLK8M CLK8M	rival time arrival time cale	ulation	Clock source	CLK8M					53.65
# of paths	70 - 60 - 50 - 40 - 30 -		data a slack Data CLK8M CLK8M U_10_	rival time arrival time calo			CLK8M U_I0_BUFFE	RS/CLK8M		+	0.000	53.65 0.00
# of paths	70 - 60 - 50 - 40 - 30 - 20 - 10 -		data ar slack Data CLK8M CLK8M U_I0_ U_I0_	rival time arrival time cale BUFFERS:CLK8M	JF:PAD	net		RS/CLK8M	ADLIB:G	+	0.000	53.65 0.00 0.00
# of paths	70 - 60 - 50 - 40 - 30 - 20 -	80	data a slack Data CLK3M CLK3M U_IO_ U_IO_ U_IO_ U_IO_ U_IO_	rival time arrival time cale b BUFFERS:CLK8M BUFFERS/CLK_B	JF:PAD JF:GL	net net cell				+	0.000 0.000 0.000	53.65 0.00 0.00 0.00

Path Slack Histogram

Path Details



See Also

SmartTime scenarios



Analyzing Your Design

The timing engine uses the following priorities when analyzing paths and calculating slack:

- 1. False path
- 2. Max/Min delay
- 3. Multi-cycle path
- 4. Clock

If multiple constraints of the same priority apply to a path, the timing engine uses the tightest constraint. You can perform two types of timing analysis: Maximum Delay Analysis and Minimum Delay Analysis.

To perform the basic timing analysis:

- 1. Open the Timing Analysis View using one of the following methods:
 - In the Design Flow window, click Verify Timing > Open Interactively to display the SmartTime Maximum Delay Analysis View.
 - From the SmartTime Tools menu, choose Max Delay Analysis or Min Delay Analysis
 - Click the icon for Maximum Delay Analysis or the icon for Minimum Delay Analysis from the SmartTime window.

Note: When you open SmartTime from Libero (**Verify Timing > Open Interactively**), the Maximum Delay Analysis window is displayed by default.

1 💁 💁 🍝 🖉 🐵 🛪										-
m Delay Analysis View										
Analysis for scenario										
min Primary	From *					то •				
4 🕅 Summary	Customize table							Apply Filt	er Store Filter Reset	t Filter
▲ X [®] CLK	Contenter toole							- depert - mo		
 Register to Register 				Delay						
× External Hold	Sou	rce Pin	Sink Pin	(ns)	Slack (ns)	Arrival (ns)	Required (ns)	Hold (ns)	Skew (ns)	
Clock to Output	1 Qaux[3]:CL	Oau	(3]:D	0.337	0.304	2.451	2.147	0.000	-0.033	
Register to Asynchronous	r Georgelien								01000	i in
External Removal	2 Qaux[2]:CLK	Qaux	:[2]:D	0.338	0.305	2.453	2.148	0.000	-0.033	
Asynchronous to Register										
Input to Output	3 Qaux[1]:CLk	Qaux	[1]:D	0.393	0.360	2.507	2.147	0.000	-0.033	-
▲ In User Sets		-								
✓ Qaux1_filter	4 Qaux[1]:CLk	Qau	:[2]:D	0.394	0.360	2.508	2.148	0.000	-0.034	
✓ Qaux2_filter	5 Qaux[1]:CLk	Qau	(3):D	0.395	0.362	2.509	2.147	0.000	-0.033	
✓ Qaux3_filter	- George Jean									
	6 Qaux[0]:CLK	Qaux	:[1]:D	0.404	0.365	2.512	2.147	0.000	-0.039	
	7 Qaux[2]:CLk	Qaux	:[3]:D	0.434	0.402	2.549	2.147	0.000	-0.032	
10										•
	Name		Туре	Net		Macro	Op Delay	Total Fanout Edge	2	_
8	✓ Summary									=
6	data arriv							2.451		
		uired time					-	2.147 0.304		
4	slack	_time_calculation						0.304		
2	2 Data_arrival	_ume_calculation					0.000	0.000		
	CLK		Clock source					0.000 r		
0 0.194 0.304 0.414 0.524 0.634	CLK_ibut	/U0/U_IOPAD:PAD	net	CLK				0.000 r		
		/U0/U_IOPAD:Y	cell			ADLIB:IO		1.109 2 r		-
slack distribution(ns)		BLIB (0.0.1.1		AL 14 14			0.100	1.007		

Figure 30 · Maximum Delay Analysis View

- In the Domain Browser, select the clock domain. Clock domains with a green check mark indicate that the timing requirements in these domains were met. Clock domains with a red x indicate that there are violations within these domains. The Paths List displays the timing paths sorted by slack. The path with the lowest slack (biggest violation) is at the top of the list.
- Select the path to view. The Path Details below the Paths List displays detailed information on how the slack was computed by detailing the arrival time and required time calculation. When a path is violated, the slack is negative and is displayed in red color.
- Double-click the path to display a separate view that includes the path details and schematics view.



- Note: In cases where the minimum pulse width of one element on the critical path limits the maximum frequency for the clock, SmartTime displays an icon for the clock name in the Summary List. Click on the icon to display the name of the pin that limits the clock frequency.
- 5. Repeat the above steps as required.

Performing a Bottleneck Analysis

To perform a bottleneck analysis

- 1. From SmartTime's Maximum/Minimum Delay Analysis View select **Tools > Bottleneck Analysis**. The **Timing Bottleneck Analysis Options** <u>dialog box</u> appears.
- 2. Select the options you wish to display for bottleneck information and click OK.

The Bottleneck Analysis View appears in a separate window (see image below).



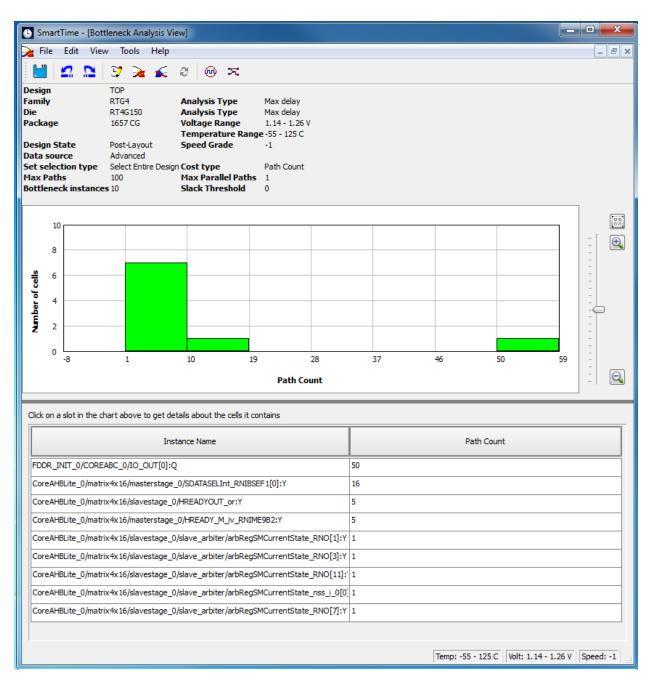


Figure 31 · Bottleneck Analysis View

A bottleneck is a point in the design that contributes to multiple timing violations. The Bottleneck Analysis

View contains two sections

- Device Description
- Bottleneck Description



Device Description

The device section contains general information about the design and the parameters that define the bottleneck computation:

- Design name
- Family
- Die
- Package
- Design state
- Data source
- Set selection type
- Max paths
- Bottleneck instances
- Analysis type
- Analysis max case
- Voltage
- Temperature
- Speed grade
- Cost type
- Max parallel paths
- Slack threshold

Bottleneck Description

This section displays a graphic representation of the bottleneck analysis and lists the core of the bottleneck information for the bar selected in the chart above. If no bar is selected, the grid lists all bottleneck information.

Click the controls on the right to zoom in or out the contents in the chart.

Right-click the chart to export the chart or to copy the chart to the clipboard.

The list is divided into two columns:

- Instance name: refers to the output pin name of the instance. Click the pin name to select the cell and the corresponding instance is selected in MultiView Navigator (MVN).
- Bottleneck cost: displays the pin's cost given the chosen cost type. Pin names are listed in decreasing
 order of their cost type.

See Also

Timing Bottleneck Analysis Options dialog box (SmartTime)

Managing Clock Domains

In SmartTime, timing paths are organized by clock domains. By default, SmartTime displays domains with explicit clocks. Each clock domain includes at least three path sets:

- Register to Register
- External Setup (in the Maximum Analysis View) or External Hold (in the Minimum Analysis View)
- Clock to Out

You must select a path set to display a list of paths in that specific set.



To manage the clock domains:

- 1. Right-click anywhere in the Domain Browser, and choose **Manage Clock Domains**. The <u>Manage</u> <u>Clock Domains</u> dialog box appears (as shown below).
- Tip: You can click the icon in the SmartTime window bar to display the Manage Clock Domains dialog box.

Manage Clock Domains			? <mark>x</mark>
Available clock domains:	Add	Show the clock domains in this ord	er:
	Remove		
	Move Up		
	Move Down		
Help New Clock		ОК	Cancel

Figure 32 · Manage Clock Domains Dialog Box

- 2. To add a new domain, select a clock domain from the **Available clock domains** list, and click either **Add** or **New Clock** to add a non-explicit clock domain.
- 3. To remove a displayed domain, select a clock domain from the **Show the clock domain in this order** list, and click **Remove**.
- To change the display order in the Domain Browser, select a clock domain from the Show the clock domain in this order list, and then use the Move Up or Move Down to change the order in the list.
- 5. Click **OK**. SmartTime updates the Domain Browser based on your specifications. If you have added a new clock domain, then it will include at least the three path sets as mentioned above.

See Also

Manage Clock Domain dialog box

Managing Path Sets

You can create and manage custom path sets for timing analysis and tracking purposes. Path sets are displayed under the **Custom Path Sets** at the bottom of the Domain Browser.

To add a new path set:

- Right-click anywhere in the Domain Browser, and choose Add Set. The <u>Add Path Analysis Set</u> dialog box appears (as shown below).
- Tip: You can click the icon in the SmartTime window bar to display the Add Path Analysis Set dialog box.



Add Path Analysis Set			
Name:	Trace from: 🔍 Sour	ce to sink	C Sink to source
Source Pins: DDR0/U0:CLK DDR1/U0:CLK DDRREG2/INBUF_LVDS_0_inst/U0/U2_DDR1:0 FIFO_inst/FIFO64K36_FULL:RCLK	Sink Pins:		
FIFO_inst/FIFO64K36_FULL:WCLK RAM_inst/RAM64K36_Q_0_inst:RCLK RAM_inst/RAM64K36_Q_0_inst:WCLK RAM_inst/RAM64K36_Q_1_inst:RCLK RAM_inst/RAM64K36_Q_1_inst:WCLK Rdf_pll0/U0:CLK Rdf_pll1/U0:CLK XCMP33/U0/U2_DDR1:CLK XCMP33/U0/U2_DDR2:CLK	 ✓ 		
Select All	Select All		
Filter source pins:	Filter sink pins	:	
Pin Type: Registers by pin names	Pin Type:	Registers	s by pin names 💌
* Filter	*		Filter
Help	ОК]	Cancel

Figure 33 · Add Path Analysis Set Dialog Box

- 2. Enter a name for the path set.
- 3. Select the source and sink pins. You can <u>use the filters</u> to control the type of pins displayed.
- 4. Click **OK**. The new path set appears under **Custom Path Sets** in the Domain Browser (as shown below).



e	SmartTime - [I	Maximum Delay Analysis View]										. 🗆 🗙	
e	File Edit	View Tools Help										- 8	×
	🗎 🙇 🖸	37 🌛 🖌 8 🐵 🕱											
: Ma	ximum Delay Ana												
	Xilliulii Delay Alia												_
	MAX Prim	hary		n * stomize table			TO *	Apply Filter	Store	Filter	Reset	Filter	
	⊿ v @ i												
	Ex	Register to Register ternal Setup		Source Pin			Sink Pin	Dela (ns)	y 51 (1	ack 1s)			
		ock to Output gister to Asynchronous	1	Q_reg:CLK		Q		5.8	00				
	Ext	ternal Recovery											
	As A SE Pi	ynchronous to Register											
		put to Output											
	4 🔀 Us	er Sets											
	m	y_set											
			Nam	ne	Туре	Net	м	acro	Ор	Delay	Total	Fanol 🔨	
				Summary									
				data required time							N/C	E	
				data arrival time					-		9.781		
				slack							N/C		
			4	Data_arrival_time_calculation									
	<u>v</u>	This set has no path.		my_clk							0.000		
	of paths			CLK	Clock source				+		0.000		
	<u></u>			CLK_ibuf/U0/U_IOPAD:PAD	net	CLK			+		0.000		
	*			CLK_ibuf/U0/U_IOPAD:Y	cell		AL	DLIB:IOPAD_IN	+		2.128		
				CLK_ibuf_RNIVQ04:An	net	CLK_ibuf			+		2.480	-	
		slack distribution(ns)	•	, , , , , , , , , , , , , , , , , , , ,								P .	
		suck distribution(its)											
1													- 1
R	eady							Temp: 0 - 85	C Vol	t: 1.14 -	1.26 V	Speed: STD	
_	-												

Figure 34 · Updated Domain Browser with User Sets

To remove an existing path set:

- 1. Select the path set from the User Sets in the Domain Browser.
- 2. Right-click the set to delete, and then choose **Delete Set** from the right-click menu.

To rename an existing path set:

- 1. Select the path set from User Set in the Domain Browser.
- 2. Right-click the set to rename, and then choose Rename Set from the right-click menu.
- 3. Edit the name directly in the Domain Browser.

See Also

Add Path Analysis Set dialog box Using filters Exporting Files

Displaying Path List Timing Information

The Path List in the Timing Analysis View displays the timing information required to verify the timing requirements and identify violating paths. The Path List is organized in a grid where each row represents a timing path with the corresponding timing information displayed in columns. Timing information is customizable; you can add or remove columns for each type of set.

By default, each type of set displays a subset of columns as follows:

- Register to Register: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, Minimum Period, and Skew.
- External Setup: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, and External Setup.
- Clock to Out: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, and Clock to Out.
- Input to Output: Source Pin, Sink Pin, Delay, and Slack.
- Custom Path Sets: Source Pin, Sink Pin, Delay, and Slack.



You can add the following columns for each type of set:

- Register to Register: Clock, Source Clock Edge, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Maximum Delay Constraint, and Multicycle Constraint.
- External Setup: Clock, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Input Delay Constraint, Required External Setup, Maximum Delay Constraint, and Multicycle Constraint.
- Clock to Out: Clock, Source Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Output Delay Constraint, Required Maximum Clock to Out, Maximum Delay Constraint, and Multicycle Constraint.
- Input to Output: Arrival, Required, Setup, Hold, Logic Stage Count, and Max Fanout.
- Custom Path Sets.

To customize the set of timing information in the Path List:

- 1. Select the set to customize.
- 2. Select the whole Paths List by clicking in the upper-left corner.
- 3. Right-click anywhere on the column headings, and then choose **Customize table** from the right-click menu. The <u>Customize Analysis View</u> dialog box appears (as shown below).

Customize Analysis View		
Available fields: Clock Source Clock Edge Destination Clock Edge Clock Constraint (ns) Max Delay Constraint (ns) Multicycle Constraint	Add > < Remove Reset to Default	Show these fields in this order: Source Pin Sink Pin Delay (ns) Slack (ns) Arrival (ns) Required (ns) Setup (ns) Minimum Period (ns) Skew (ns)
Help		Move Up Move Down OK Cancel

Figure 35 · Customize Analysis View Dialog Box

- 4. To add one or more columns, select the fields to add from the Available fields list, and click Add.
- 5. To remove one or more columns, select the fields to remove from the **Show these fields in this order** list, and click **Remove**.
- 6. Click OK to add or remove the selected columns. SmartTime updates the Timing Analysis View.

See Also

Customize Analysis View

Displaying Expanded Path Timing Information

SmartTime displays the list of paths and the path details for all parallel paths.



Maximum Delay Analysis Vie	w											
	From	*				То	*					_
MAX		,					,	Apply	Filter	Store Filter	Reset Fil	ilter
St Datasheet × - CLK8M		Source Pin	1	Sink Pin	Delay (ns)	Slack	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	Γ
Register to Regi	1 1	SBI/U3/rwra:CLK	U SBI/U	3AWR:D	5.658		7,916	61.571	0.668	12.690	0.019	Ĺ
Kernal Setup	2 U	_TOPM031/U_CORE/con 2[2]:CLK	U_SBI/U	4/bram_a[12]:D	48.407	70.731	50.722	121.453	0.867	49.269	-0.005	
Register to Asynchrc External Recovery	3 U, f_	_TOPM031/U_CORE/con 2[2]:CLK	U_SBI/U	4/bram_a[1]:D	47.470	71.611	49.785	121.396	0.867	48.389	0.052	
Asynchronous to Re	4 U.	_TOPM031/U_CORE/con 1[3]:CLK	U_SBI/U	4/bram_a[12]:D	47.412	71.726	49.727	121.453	0.867	48.274	-0.005	
× Register to Regi.	5 U	_TOPM031/U_CORE/con [2[2]:CLK	U_SBI/U	4/bram_a[14]:D	47.183	71.910	49.498	121.408	0.867	48.090	0.040	
		_TOPM031/U_CORE/con 0_0[2]:CLK	U_SBI/U	4/bram_a[12]:D	47.269	71.915	49.538	121.453	0.867	48.085	-0.051	
		Details for parallel pa From: U_SBI/U3/rwra To: U_SBI/U3/WR:D	ths ::CLK									
80-		Pin Name		Туре	N	et Name	Cell	Name Op	Delay (ns) Total (ns) Fa	anout Ed	ge
60	Parallel Path #1											
		data required time								61.571		
40		data arrival time						•		7.916		
		slack								53.655		
20		Data arrival time calc	ulation									
		CLK8M							0.00			
		CLK8M		Clock source				+	0.00		1	
ŭ 60 80		U_IO_BUFFERS:CLK8M		net net	CLK8M	FFERS/CLM		+	0.00		r	

Figure 36 · Expanded Path View

The Path List displays all parallel paths in your design. The Path Details grid displays the path details for all parallel paths.

To display the Expanded Path View:

From the Path List: double-click the path, or right-click a path and select expand selected paths.

		e (ns) Slack (ns) 53.655			Pat Net delay 67.53%	th Profile
Path details Pin Name	Туре	Net Name	Cell Name Op	Dalay (as) T	atal (a a) Eana	ut Edual
Data arrival time calculati CLK8M U_I0_BUFFERS:CLK8M U_I0_BUFFERS:CLK8M U_I0_BUFFERS:CLK_BUF:GL U_I0_BUFFERS:CLK_BUF:GL U_0BUFFERS:cLk8m_in U_SBI/U3:rwra:CLK	Clock source net D net	CLK8M U_IO_BUFFERS/CLK8M U_IO_BUFFERS/Clk8m_in clk8m_in U_SBI/clk8m_in U_SBI/clk8m_in	+ + + ADLIB:GL33 + + + + + +	0.000 0.000 0.000 1.175 0.000 0.000 0.000 1.083	1.175 1.175 1.175 2.258	r r 34 r r r r
III SRI/IIR/nars-O	nal l			0 708	2 966	A .
		U_SBI/U3/wra DQ XCLK DFF	U_SBI A	/U3/rwra_1_i	₽ ¢c⊔	II/U3/WR Q < FFL

Figure 37 · Expanded Path View

The Expanded Path Summary provides a summary of all parallel paths for the selected path. The Path Profile chart displays the percentage of time taken by cells and nets for the selected path. If no parallel path



is selected in this view, the Path Profile shows the percentage for all paths. By default, SmartTime only shows one path for each Expanded Path. You can change this default in the <u>SmartTime Options</u> dialog box.

The Expanded Path View also includes a schematic of the path and a path profile chart for the paths selected in the Expanded Path Summary.

Using Filters

You can use filters in SmartTime to limit the Path List content (that is, create a filtered list on the source and sink pin names). The filtering options appear on the top of the Timing Analysis View. You can save these filters one level below the set under which it has been created.

To use the filter:

- 1. Select a set in the Domain Browser to display a given number of paths, depending on your <u>SmartTime</u> <u>Options</u> settings (100 paths by default).
- 2. Enter the filter criteria in both the **From** and **To** fields and click **Apply Filter**. This limits the display to the paths that match your filter criteria.

From	U_SB*	То	u_TO*		
			Apply Filter	Store Filter	Reset Filter

Figure 38 · Maximum Delay Analysis View

3. Click **Store Filter** to save your filter criteria with a special name. The Create Filter Set dialog box appears (as shown below).

Create Filter Set		? ×
Name : my_filter01		
	OK	Cancel
Help	OK	Cancei

Figure 39 · Create Filter Set Dialog Box

4. Enter a name for the filter such as my_filter01, and click **OK**. Your new filter name appears below the set under which it was created.



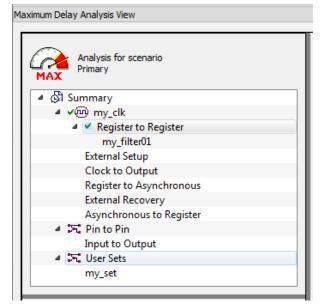


Figure 40 · My_filter01

~	~	_	U_SB*			u_TO*					_
6	*	From	0_30.		То	[u_10.					
MA E- @	AX 3 Summary					Appl	y Filter	Store Filter	Rese	t Filter	r
Ĩ.,	- 🔄 Datasheet 👘	H	6 D'	0:1.0:	Delav	Slack.	Arrival	Required	Setup	Mir	n /
P	CLK8M		Source Pin	Sink Pin	(กร)้	(ns)	(ns)	(ns)	(ns)	Peri	i
	External Setup		U_SBI/U1/A[15]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	43.496	75.612	45.790	121.402	0.867		
	Clock to Output Register to Asynchrc		U_SBI/U1/A_0(2):CLK	U_TOPM031/U_CORE/eve nts[15]:D	43.178	75.937	45.465	121.402	0.867		
	External Recovery		U_SBI/U1/WRITE:CLK	U_TOPM031/U_CORE/eve nts[15]:D	42.393	76.728	44.674	121.402	0.867		
-	PLL_CLK_IN Register to Regi.		U_SBI/U1/A_0[8]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	42.387	76.746	44.656	121.402	0.867		
	External Setup		U_SBI/U1/A[15]:CLK	U_TOPM031/U_CORE/eve nts[14]:D	42.227	76.898	44.521	121.419	0.867		
•	Clock to Output		U_SBI/U1/A[15]:CLK	U_TOPM031/U_CORE/eve nts[13]:D	42.030	77.078	44.324	121.402	0.867		
100.			U_SBI/U1/A[4]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	42.028	77.101	44.301	121.402	0.867		
90-		8	U_SBI/U1/A[13]:CLK	U_TOPM031/U_CORE/eve nts[15]:D	41.987	77.142	44.260	121.402	0.867		•
		<								>	J
80 · 70 ·			Details for parallel p From: U_SBI/U1/A[To: U_TOPM031/U	aths 15]:CLK _CORE/events[15]:D							
				Pin Name		T	уре	Net Name	Cell Na	Op	
60 ·		Parall Path 1									
50			data required time								ſ.
50 ·			data arrival time							•	Ē
			slack								Ē
30 -			Data arrival time ca	culation							
20 -	+ _		CLK8M								ſ.
			CLK8M			Clock s	ource			+	Ē.
10-			U_IO_BUFFERS:CLK8	4		net		CLK8M		+	Ē
			U_IO_BUFFERS/CLK_	BUF:PAD		net		U_IO_BUFFER		+	Ē
			U IO BUFFERS/CLK	PLIE:GI		cell			ADLIB:G	4	E.
0.	10 60 80			DOLUE		000			ADLID.U	1 -	
	40 60 80 slack distribution (ns)		U_IO_BUFFERS:clk8m			net		U_IO_BUFFER		+	F,

Figure 41 · Updated Maximum Delay Analysis View

Repeat the above steps and cascade as many sets as you need using the filtering mechanism.

To remove a set created with filters:

1. Select the set that uses filters.



2. Right-click the set, and choose **Delete Set** from the shortcut menu.

To rename a set created with filters:

- 1. Select the set that uses filters.
- 2. Right-click the set, and choose Rename Set from the shortcut menu.
- 3. Edit the name directly in the Domain Browser.

To edit a specific filter in the set:

- 1. Select the filter to edit.
- 2. Right-click the filter, and choose Edit Set from the shortcut menu.

See Also

SmartTime Options Store Filter as Analysis Set Edit Set dialog box Exporting Files

Advanced Timing Analysis

Understanding Inter-Clock Domain Analysis

When functional paths exist across two clock domains (the register launching the data and the one capturing it are clocked by two different clock sources), you must provide accurate specification of both clocks to allow a valid inter-clock domain timing check. This is important especially when the clocks are specified with different waveforms and frequencies.

When you specify multiple clocks in your design, the first step is to consider whether the inter-clock domain paths are false or functional. If these paths are functional, then you must perform setup and hold checks between the clock domains in SmartTime. Unless specified otherwise, SmartTime considers the inter-clock domain as false, and therefore does not perform setup or hold checks between the clock domains.

If you have several clock domains that are subset of a single clock (such as if you want to measure clock tree delay from an input clock to a generated clock), you must configure Generated Clock Constraints for each of the clock domains in order for SmartTime to do execute the calculation and show timing for each of the inter-clock-domain paths.

Once you include the inter-clock domains for timing analysis, SmartTime analyzes for each inter-clock domain the relationship between all the active clock edges over a common period equal to the least common multiple of the two clock periods. The new common period represents a full repeating cycle (or pattern) of the two clock waveforms (as shown below).

For setup check, SmartTime considers the tightest relation launch-capture to ensure that the data arrives before the capture edge. The hold check verifies that a setup relationship is not overwritten by a following data launch.

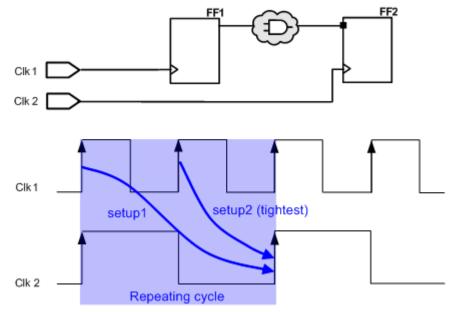


Figure 42 · Example Showing Inter-Clock Domains

See Also

Activating inter-clock domain analysis Deactivating a specific inter-clock domain Displaying inter-clock domain paths



Activating Inter-Clock Domain Analysis

To activate the inter-clock domain checking:

- 1. In SmartTime, from the **Tools** menu choose **Options**. The <u>SmartTime Options</u> dialog box appears (as shown below).
- 2. In the general category, check the Include inter-clock domains in calculations for timing analysis.

SmartTime Options		×
Option Categories - Select a category: - General - Analysis View - Advanced	General Operating Conditions Perform maximum delay analysis based on WORST < case Perform minimum delay analysis based on BEST < case Clock Domains Clock Domains Include inter-clock domains in calculations for timing analysis. Enable recovery and removal checks. Restore Defaults	
Help	OK Cancel	

Figure 43 · SmartTime Options Dialog Box

3. Click **OK** to save the dialog box settings.

See Also

Understanding inter-clock domain analysis Deactivating a specific inter-clock domain Displaying inter-clock domain paths SmartTime Options dialog box

Displaying Inter-Clock Domain Paths

Once you <u>activate the inter-clock domain checking</u> for a given clock domain CK1, SmartTime automatically detects all other domains CKn with paths ending at CK1. SmartTime creates inter-clock domain sets CKn to CK1 under the domain CK1. Each of these sets enables you to display the inter-clock domain paths between a given clock domain and CK1.

To display an inter-clock domain set:

- 1. Expand the receiving clock domain of the inter-clock domain in the Domain Browser to display its related sets. For the inter-clock domain CK1 to CK2, expand clock domain CK2.
- Select the inter-clock domain that you want to see expanded from these sets. Once selected, all paths between the related two domains are displayed in Paths List in the same way as any register to register set.



Maximum Delay Analysis Vi	ew								
Analysis for scenario	From *			то	*				
Primary Scenario				,					
FINA						Apply Filter	Store	Filter	Reset Filte
୍ କ୍ଷି Summary 🔺						1.4221			
🔄 🔄 Datasheet 👘							-		
🖃 🗡 🕡 av1 clk	Source Pin	Sink Pin		Slack	Arrival	Required	Setup		
× Register to Regi.	1 Control word 0f01:CLK	ufp/fp_entr[13]:D	(ns) 7,793	(ns) -1.510	(ns) 9.131	(ns) 7.621	(ns) 0.381		
× External Setup	2 control word 0[0]:CLK	ufp/fp_cntr[6]:D	7.575	-1.282	8.913		0.381		
Clock to Output	3 control word 0[0]:CLK	ufp/fp_cntr[3]:D	7.431	-1.121	8,765		0.381		
	4 control word 0/01:CLK	ufp/fp_cntr[12]:D	7.220	-0.913	8,558		0.357		
External Recov	5 control word 0101:CLK	ufp/fp_ontr[2];D	7.194	-0.909	8,532		0.381		
Asynchronous to Re	6 control word 0101:CLK	ufp/fp_cntr[14]:D	7,192	-0.909	8,530		0.381		
× cpu clk to av1	7 control word 0[0]:CLK	ufp/fp_cntr[9]:D	7.100	-0.821	8.438		0.381		
E × @ cpu_clk	8 control_word_0[0]:CLK	ufp/fp_cntr[10]:D	7.085	-0.792	8.423		0.381		
× Register to Regi.	9 control_word_0[0]:CLK	ufp/stretch_fp[3]:D	7.082	-0.773	8.420	7.647	0.381		
× External Setup	10 Control word 0001/CLK	ufn/fn_entr[15]:D	6 942	-0.659	8 280	7 621	0 381		
Clock to Output	Details for parallel paths	3							
Register to Asynchrc	From: control_word_0[0]]:CLK							
 External Recov 	To: ufp/fp_cntr[13]:D								
Asynchronous to Re	Pin Name	Туре	<u> No</u>	et Name		Cell Name	Op [)elay (ns) 1	
av1 clk to cpu	slack								-1.510
F The Pin to Pin									
Input to Output	Data arrival time calcula	ation	·					0.000	0.000
The Set	cpu_clk	Clock source					+	0.000	0.000
•	cpu_cik cpu_cik_pad/U0/U0:PAD	net	cpu_clk				+	0.000	0.000
	cpu_cik_pad/00/00.PAD	cell	сра_ск			ADLIB:IOPAD II		0.632	0.632
24	cpu_clk_pad/U0/U1:A	net	cpu clk pad	/U0/NET1			+	0.000	0.632
	cpu clk_pad/U0/U1:Y	cell	opa_on(_pdd	roomen.		ADLIB:CLKIO	+	0.231	0.863
22-	control word 0[0]:CLK	net	cpu clk c		ĺ	DED.OEMO	+	0.475	1.338
20	control word 0/01:0	cell				ADLIB:DFN1E10	20 +	0.489	1.827
20-	ufp/un1 fp cntr 2 i0 a3 (0 0 0:A net	control word	0[0]			+	1.259	3.086
18-	ufp/un1 fp cntr 2 i 0 a3 (1-7		ADLIB:NOR2	+	0.337	3.423
	ufp/un1 fp cntr 2 i 0 a3 (D 7:A net	ufp/un1 fp o	on tr 2 i 0	a3 0 0		+	0.237	3.660
16	ufp/un1_fp_cntr_2_i_0_a3_0	D_7:Y cell			/	ADLIB:NOR3A	+	0.441	4.101
	ufp/un1_fp_cntr_2_i_0_a3_0	D_8:C net	ufp/un1_fp_c	ontr_2_i_0_	_a3_0_7		+	0.729	4.830
14-	ufp/un1_fp_cntr_2_i_0_a3_0	D_8:Y cell				ADLIB:NOR3C	+	0.442	5.272
12-	ufp/un1_fp_cntr_2_i_0_a3_0		ufp/un1_fp_c	ontr_2_i_0_			+	0.237	5,509
12	ufp/un1_fp_cntr_2_i_0_a3_0					ADLIB:NOR3C	+	0.442	5.951
	ufp/un1_fp_cntr_2_i_0_o2:A		_ufp/un1_fp_c	ontr_2_i_0_			+	0.288	6.239
10-	ufp/un1_fp_cntr_2_i_0_o2:Y					ADLIB:OA1	+	0.653	6.892
	ufp/fp_cntr_6_0_a2[13]:C	net	ufp/un1_fp_c	ontr_2_i_0_			+	1.784	8.676
8-	ufp/fp_cntr_6_0_a2[13]:Y	cell	L		/	ADLIB:XA1B	+	0.228	8.904
6-	ufp/fp_cntr[13]:D	net	ufp/fp_cntr_6	5[13]			+	0.227	9.131
	data arrival time								9.131
4-		4-6							
	Data required time calcu							0.007	0.007
2	av1_clk	Clock Constraint						6.667	6.667
	av1_clk av1_clk_pad/U0/U0;PAD	Clock source					+	0.000	6.667
	av1_ck_pad/UU/UU:PAD av1_ck_pad/U0/U0:Y	cell	av1_clk			ADLIB:IOPAD II	+	0.000	7.299
-5 0 5 10	av1_cik_pad/00/00:1	Cell	aut alk nad	410 MIET 1		ADDIB:IOFAD_II	4 +	0.632	7.299
slack distribution (ns)	A STATE OF CONTRACT OF CONTRACT								7 /44

Figure 44 · Maximum Delay Analysis View

See Also

Understanding inter-clock domain analysis Activating inter-clock domain analysis Deactivating a specific inter-clock domain

Deactivating a Specific Inter-Clock Domain

To deactivate the inter-clock domain checking for the specific clock domains clk2->clk1, without disabling this option for the other clock domains:

- 1. From the **Tools** menu, choose **Constraints Editor > Primary Scenario** to open the Constraints Editor View.
- 2. In the Constraints Browser, double-click **False Path** under **Exceptions**. The "<u>Set False Path</u> <u>Constraint</u> dialog box appears.
- 3. Click the **Browse** button to the right of the **From** text box. The **Select Source Pins for False Path Constraint** dialog box appears.
- 4. For Specify pins, select by keyword and wildcard.
- 5. For Pin Type, select Registers by clock names from the Pin Type drop-down list.
- 6. Type the inter-clock domain name, for example Clk2 in the filter box and click Filter.
- 7. Click **OK** to begin filtering the pins by your criteria. In this example, [get_clocks {Clk2}] appears in the **From** text box in the **Set False Path Constraint** dialog box.



- 8. Repeat steps 3 to 7 for the **To** option in the <u>Set False Path Constraint</u> dialog box, and type Clk2 in the filter box.
- 9. Click OK to validate the new false path and display it in the Paths List of the Constraints Editor.
- 10. Click the Recalculate All icon 2 in the toolbar.
- 11. Select the inter-clock domain set clk2 -> clk1 in the Domain Browser (as shown below).
- 12. Verify that the set does not contain any paths.

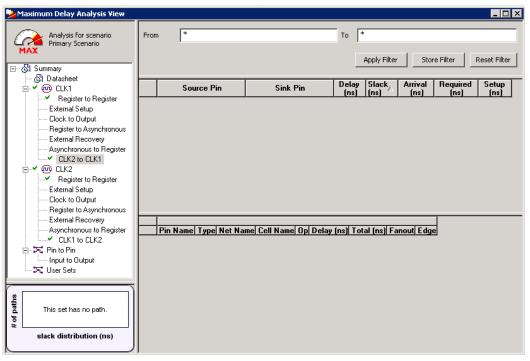


Figure 45 · Maximum Delay Analysis View

See Also

<u>Understanding inter-clock domain analysis</u> <u>Activating inter-clock domain analysis</u> <u>Displaying inter-clock domain paths</u> <u>Select Source or Destination Pins for Constraint dialog box</u> Set False Path Constraint dialog box

Timing Exceptions Overview

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the
 optimization flow.
- Setting a maximum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

See Also

Specifying maximum delay constraint Specifying multiple path constraint Specifying false path constraint Changing output port capacitance



Specifying a Maximum Delay Constraint

You set options in the <u>Maximum Delay Constraint dialog</u> box to relax or to tighten the original clock constraint requirement on specific paths.

To specify Max delay constraints:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Set Maximum Delay Constraint</u> dialog box using one of the following methods:
 - Click the Konstraints Editor.
 - From the Constraint Editor, right-click the Constraints menu and choose Max Delay.

The Set Maximum Delay Constraint dialog box appears (as shown below).

Set Maximum Delay Constraint	×
Maximum delay: ns	
From:	
· · · · · · · · · · · · · · · · · · ·	
Through:	
То:	
Connecto	
Comment:	
Help OK Cancel	

Figure 46 · Set Maximum Delay Constraint Dialog Box

- 2. Specify the delay in the Maximum delay field.
- 3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the **Select Source Pins for Max Delay Constraint** dialog box (as shown below).



lect Source Pi	ins for Max Delay	y Constraint		×
Specify pins	\odot by explicit list	C by keyword and wild	dcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK qaux[12]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
gaux[4]:CLK	e objects:		1	
Pin Type:	All pins	•		
*		Filter		
Help			ОК	Cancel

Figure 47 · Select Source Pins for Max Delay Constraint

- 4. Select by explicit list. (Alternatively, you can select by keyword and wildcard.)
- 5. Select the input pin(s) from the **Available Pins** list. You can also use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- 7. Click OK. The Set Maximum Delay Constraint dialog box displays the updated From pin(s) list.
- 8. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click OK.

SmartTime adds the maximum delay constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Timing exceptions overview Set Maximum Delay Constraint dialog box Specifying maximum delay constraint Specifying multicycle constraint Specifying false path constraint Changing output port capacitance



Specifying a Minimum Delay Constraint

You set options in the Minimum Delay Constraint dialog box to relax or to tighten the original clock constraint requirement on specific paths.

To specify Min delay constraints:

- 1. Open the Set Minimum Delay Constraint dialog box using one of the following methods:
 - Click the ² icon in the Constraints Editor.
 - From the Constraints Editor, right-click Constraints Menu and choose Min delay.

The Set Minimum Delay Constraint dialog box appears (as shown below).

Set Minimum Delay Constraint	×
Minimum delay: ns	
From:	
Through:	
To:	
Comment:	
Help OK Cancel	

Figure 48 · Set Minimum Delay Constraint Dialog Box

- 2. Specify the delay in the Minimum delay field.
- 3. Specify the From pin(s). Click the Browse button next to From to open the Select Source Pins for Min Delay Constraint dialog box (as shown below).



Select Source Pi	ins for Min Delay	r Constraint		
Specify pins	• by explicit list	C by keyword and wild	lcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable		Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK qaux[12]:CLK		Add All >		
qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK qaux[4]:CLK		< Remove All		
Filter available	e objects:			
Pin Type:	All pins	•		
*		Filter		
Help			ОК	Cancel

Figure 49 · Select Source Pins for Max Delay Constraint

- 4. Select by explicit list. (Alternatively, you can select by keyword and wildcard.)
- 5. Select the input pin(s) from the **Available Pins** list. You can also use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- 7. Click OK. The Set Minimum Delay Constraint dialog box displays the updated From pin(s) list.
- 8. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click **OK**.

SmartTime adds the minimum delay constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Timing exceptions overview Set Minimum Delay Constraint dialog box Specifying multicycle constraint Specifying false path constraint Changing output port capacitance

Specifying a Multicycle Constraint

You set options in the <u>Set Multicycle Constraint</u> dialog box to specify paths that take multiple clock cycles in the current design.

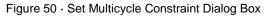


To specify multicycle constraints:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Set Multicycle Constraint</u> dialog box using one of the following methods:
 - From the SmartTime Actions menu, choose Constraint > MultiCycle.
 - Click the 🕅 icon.
 - Right-click the **Multicycle** option in the Constraint Browser.

The Set Multicycle Constraint dialog appears (as shown below).

iet Multicycle Constraint	
Specify multiplier(s) for: Setup Check only Setup Path Multiplier:	
Default setup edge Hold edge	New setup edge
From:	····
	····
To:	
Help	Cancel





- 2. Specify the number of cycles in the Setup Path Multiplier.
- Specify the From pin(s). Click the browse button (...) next to From to open the <u>Select Source Pins for</u> <u>Multicycle Constraint</u> dialog box (as shown below).

Select Source Pi	ins for Multicycle C	onstraint		
Specify pins	• by explicit list	🔿 by keyword and wild	lcard	
Available Pins:			Assigned Pins:	
Aclr Clock Enable	2	Add >		
qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK		Add All >		
qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[15]:CLK		< Remove		
qaux[1]:CLK qaux[2]:CLK qaux[3]:CLK		< Remove All		
aaux[4]:CLK		9	I	
Filter available				
Pin Type:	All pins	_		
*		Filter		
Help			ОК	Cancel

Figure 51 · Select Source Pins for Multicycle Constraint

- 4. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to <u>Select Source or Destination Pins for Constraint</u>.)
- 5. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 6. Click Add or Add All to move theinput pin(s) move from the Available pins list to the Assigned Pins list.
- 7. Click **OK**.

The **Set Multicycle Constraint** dialog box displays the updated representation of the From pin(s) (as shown below).



Set Multicycle Constraint	×
Specify multiplier(s) for: Setup Check only Setup Path Multiplier:	
Pefault setup edge Hold edge	
Adr Clock Enable qaux[0]:CLK]
To:	
····	
Comment: Help OK Cancel	

Figure 52 · Set Multicycle Constraint Dialog Box

- 8. Click the browse button for **Through** and **To** and add the appropriate pins. The displayed list shows the pins reachable from the previously selected pin(s) list.
- 9. Enter comments in the **Comment** section.
- 10. Click **OK**. SmartTime adds the multicycle constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Set Multicycle Constraint dialog box



Select Source Pins for Multicycle Constraint dialog box

Specifying a False Path Constraint

You set options in the Set False Path Constraint dialog box to define specific timing paths as false.

To specify False Path constraints:

- 1. Add the constraint in the <u>Editable Constraints Grid</u> or open the <u>Set False Path Constraint</u> dialog box. You can do this by using one of the following methods:
 - From the SmartTime Constraints menu, choose False Path.
 - Click the 🔊 icon.
 - Right-click False Path in the Constraint Browser and choose Add False Path Constraint.

The Set False Path Constraint dialog box appears (as shown below).

et False Path Constraint	
From:	
1	
₹	
Through:	
<	>
To:	
	· · · · · · · · · · · · · · · · · · ·
<u><</u>	>
Comment:	
Help	OK Cancel

Figure 53 · Set False Path Constraint Dialog Box

2. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the **Select Source Pins for False Path Constraint** dialog box (as shown below).



Select Source Pi	ins for False Path	i Constraint		
Specify pins Available Pins:	• by explicit list	C by keyword and wild	lcard Assigned Pins:	
Aclr Clock Enable qaux[0]:CLK qaux[10]:CLK qaux[11]:CLK qaux[12]:CLK qaux[13]:CLK qaux[14]:CLK qaux[2]:CLK qaux[2]:CLK qaux[3]:CLK qaux[4]:CLK		Add > Add All > Add All > < Remove		
Filter available Pin Type:	e objects:	Filter		
Help			ОК	Cancel

Figure 54 · Select Source Pins for False Path Constraint Dialog Box

- 3. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to <u>Select Source or Destination Pins for Constraint</u>.)
- 4. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
- 5. Click Add or Add All. The input pin(s) move from the Available Pins list to the Assigned Pins list.
- 6. Click OK.

The Set False Constraint dialog box displays the updated representation of the From pin(s).

- 7. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
- 8. Enter comments in the Comment section.
- 9. Click OK.

SmartTime adds the False Path constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Set False Constraint dialog box Select Source Pins for False Path Constraint dialog box.

Changing Output Port Capacitance

Output propagation delay is affected by both the capacitive loading on the board and the I/O standard. The I/O Attribute Editor in ChipPlanner provides a mechanism for setting the expected capacitance to improve the propagation delay model. SmartTime automatically uses the modified delay model for delay calculations.



To change the output port capacitance and view the effect of this change in SmartTime Timing Analyzer, refer to the following example. The figure below shows the delay from FF3 to output port OUT2. It shows a delay of 6.603 ns based on the default loading of 35 pF.

<u>></u>	1aximum Delay Analysis View								
	Analysis for scenario Primary Scenario	Fro	m /*		To *				
	1AX හි Summary				, A	pply Filter	Stor	e Filter F	Reset Filter
	୍ରତ୍ତି Datasheet ⊡ ✓ ๗୦ CLK2		Source Pin	Sink Pin	(ns)	Slack (ns)	Arrival (ns)	Required (ns)	Clock to Out (ns)
	Register to Register External Setup Clock to Output	1 2 3	FF3:CLK \$1139/RAMBLOCK0:CLKA \$1139/RAMBLOCK0:CLKA	OUT2 DATAOUTRAM(3) DATAOUTRAM(1)	4.995 6.300 6.234		6.603 8.121 8.055		6.603 8.121 8.055
	Register to Asynchronous External Recovery Asynchronous to Register	4	\$1139/RAMBLOCK0:CLKA \$1139/RAMBLOCK0:CLKA	DATAOUTRAM(0) DATAOUTRAM(2)	5.801 5.658		7.622 7.479		7.622 7.479
	Set Sets		Details for path From: FF3:CLK To: OUT2						<u> </u>
L			Pin Name	Туре	Ne	t Name		ll Name	Op [
		-	FF3:QN	cell	A1100		ADLIB	DFIO	+
		-	AND_2:A AND_2:Y	net cell	\$1N26		ADUR	AND2	+
		-	OUT2 pad/U0/U1:D	net	OUT2_c		ADLIB	ANDZ	+
0			OUT2_pad/U0/U1:DOUT	cell			ADLIB	IOTRI_OB_E	
f	This set has no slack		OUT2_pad/U0/U0:D	net	OUT2_pac	1/U0/NET1			+
of paths	for any of its paths.		OUT2_pad/U0/U0:PAD	cell			ADLIB	IOPAD_TRI	+
ů.			OUT2	net	OUT2				+
	slack distribution (ns)		data arrival time						_ _
		1		1					

Figure 55 · Maximum Delay Analysis View

If your board has output capacitance of 75pf on OUT2, you must perform the following steps to update the timing number:

1. Open the I/O Attribute Editor and change the output load to 75pf.

	Port Name	Macro Cell	Pin #	Locked	Bank Name	1/0 Standard	Output Drive (mA)	Slew	Resistor Pull	Skew	Output Load	Use I/O Reg
1	CLK2	ADLIB:CLKBUF	13		Bank1	LVTTL			None			Г
2	CLK4	ADLIB:INBUF	15		Bank1	LVTTL			None	-		Г
3	WADDR(3)	ADLIB:INBUF	85		Bank0	LVTTL			None			Г
4	DATAOUTRAM(2)	ADLIB:OUTBUF	86		Bank0	LVTTL	12	High	None	Г	35	Г
5	OUT2	ADUB.OUTBUF	16		Bank1	LVITL	12	High	None		75	

Figure 56 · I/O Attribute Editor View

- 2. Select **File > Save**.
- 3. Select **File > Close**.
- 4. Open the SmartTime Timing Analyzer.

You can see that the Clock to Output delay changed to 7.723 ns.

Specifying Clock Source Latency

Use clock source latency to specify the delay from the clock generation point to the clock definition point in the design.

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint.

You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

To specify the clock source latency:

1. Add the constraint in the <u>editable constraints grid</u> or open the Set Clock Source Latency dialog box using one of the following methods:



 From the SmartTime Constraints Editor window, choose Constraints > Clock Source Latency.



- Click the icon in the Constraints Editor.
- Click **Clock Source Latency** in the Constraint Browser.
- 2. Select a clock pin on which to set the source latency. You can only specify a clock source latency on a clock pin that has a clock constraint. Additionally, you may apply only one clock source latency constraint to each constrained clock pin.
- 3. Enter the Late Rise, Early Rise, Late Fall, and Early Fall values as required for your design.

Note: An 'early' value larger than a 'late' value can result in optimistic timing analysis.

- 4. Select the **Falling Same As Rising** check box to indicate that falling clock edges have the same latency as rising clock edges.
- 5. Select the **Early Same As Late** check box to use a single value for the clock latency, rather than a range, by clicking the checkbox.
- 6. Enter any comments to be attached to the constraint.
- 7. Click OK. The new constraint appears in the constraints list.
 - Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

See Also

Set Clock Source Latency dialog box

Specifying Disable Timing Constraint

Use disable timing constraint to specify the timing arcs being disabled.

To specify the disable timing constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Set Constraint to Disable Timing Arcs</u> <u>dialog box</u> using one of the following methods:
 - From the SmartTime Constraints Editor, choose Constraints > Disable Timing.
 - Click the
 icon in the Constraints Editor.
 - In the Constraints Editor, right-click **Disable Timing** and choose **Add Constraints** to disable timing.
- 2. Select an instance from your design.
- 3. Select whether you want to exclude all timing arcs in the instance or if you want to specify the timing arc to exclude. If you selected specify timing arc to exclude, select a from and to port for the timing arc.
- 4. Enter any comments to be attached to the constraint.
- 5. Click OK. The new constraint appears in the constraints list.
 - Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

See Also

Set Constraint to Disable Timing Arcs Dialog Box

Specifying Clock-to-Clock Uncertainty Constraint

Use the clock-to-clock uncertainty constraint to model tracking jitter between two clocks in your design.



To specify the clock-to-clock uncertainty constraint:

- 1. Add the constraint in the <u>editable constraints grid</u> or open the <u>Set Clock-to-Clock Uncertainty</u> <u>Constraint dialog box</u> using one of the following methods:
 - From the Constraints Editor, choose Constraints > Clock-to-Clock Uncertainty Constraint.
 - Click the icon.
 - Right-click Clock-to-Clock Uncertainty Constraint in the Constraint Browser.
- 2. Specify the from and to clocks and specify the uncertainty in ns.
- 4. Enter any comments to be attached to the constraint.
- 5. Click **OK**. The new constraint appears in the constraints list.
 - Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

See Also

Set Clock-to-Clock Uncertainty Constraint Dialog Box

Generating Timing Reports

Types of Reports

Using SmartTime you can generate the following types of reports:

- Timing report This report displays the timing information organized by clock domain.
- **Timing violations report** This flat slack report provides information about constraint violations.
- Datasheet report This report describes the characteristics of the pins, I/O technologies, and timing
 properties in the design.
- Bottleneck report This report displays the points in the design that contribute to the most timing violations.
- Constraints coverage report This report displays the overall coverage of the timing constraints set on the current design.
- Combinational loop report This report displays loops found during initialization.

See Also

Generating timing report Generating timing violation report Generating a datasheet report Generating a bottleneck report Generating a constraints coverage report Generating a Combinational Loop Report

Generating a Timing Report

The timing report enables you to quickly determine if any timing problems exist in your design. The Maximum Delay Analysis timing report lists the following information about your design:

- Maximum delay from input I/O to output I/O
- · Maximum delay from input I/O to internal registers
- · Maximum delay from internal registers to output I/O
- · Maximum delays for each clock network
- Maximum delays for interactions between clock networks

To generate a timing report:

- From the SmartTime Max/Min Delay Analysis View, choose Reports > Timer. The <u>Timing Report Options dialog box</u> appears.
- 2. Select the options you want to include in the report, and then click **OK**.

You can double-click **Verify Timing** in Libero's Design Flow Window to generate a Max Delay Analysis Timer Report.

The timing report appears in a separate window.

See Also

<u>Understanding timing report</u> <u>Timing Report Options dialog box</u>



Understanding Timing Reports

The timing report contains the following sections:

Header

The header lists:

- The report type
- The version of SmartTime used to generate the report
- The date and time the report was generated
- General design information (name, family, die, package, etc.)

Summary

The summary section reports the timing information for each clock domain.

By default, the clock domains reported are the explicit clock domains that are shown in SmartTime. You can filter the domains and get only specific sections in the report (see <u>Timing Report Options</u>).

Path Sections

The paths section lists the timing information for different types of paths in the design. This section is reported by default. You can deselect this option in the <u>Timing Report Options</u> dialog box.

By default, the number of paths displayed per set is 5.

You can filter the domains using the <u>Timing Report Options</u> dialog box.

You can also view the stored filter sets in the generated report using the timing report options (see <u>Timing</u> <u>Report Options</u>). The filter sets are listed by name in their appropriate section, and the number of paths reported for the filter set is the same as for the main sets.

By default, the filter sets are not reported.

Clock domains

The paths are organized by clock domain.

Register to Register set

This set reports the paths from the registers clock pins to the registers data pins in the current clock domain.

External Setup set

This set reports the paths from the top level design input ports to the registers in the current clock domain.

Clock to output set

This set reports the paths from the registers clock pins to the top level design output ports in the current clock domain.

Register to Asynchronous set

This set reports the paths from registers to asynchronous control signals (like asynchronous set/reset).

External Recovery set

This set reports the external recovery check timing for asynchronous control signals (like asynchronous set/reset).

Asynchronous to Register set

This set reports the paths from asynchronous control signals (like asynchronous set/reset) to registers.



Inter-clock domain

This set reports the paths from the registers clock pins of the specified clock domain to the registers data pins in the current clock domain. Inter-domain paths are not reported by default.

Pin to pin

This set lists input to output paths and user sets. Input to output paths are reported by default. To see the user-defined sets, use the <u>Timing Report Options</u> dialog box.

Input to output set

This set reports the paths from the top level design input ports to top level design output ports.

Expanded Paths

Expanded paths can be reported for each set. By default, the number of expanded paths to report is set to 1. You can select and change the number when you specify <u>Timing Report Options</u>.



File Actions Help Timing Report Max Delay Ana SmartTime Version v11.6 Microsemi Corporation - Mic Date: Thu Apr 30 15:53:18 2	lysis rosemi Libero Software Release v11.6 (Version 11.6.0.16)	
SmartTime Version v11.6 Microsemi Corporation - Mic		
Microsemi Corporation - Mic	rogemi libero Software Deleage w11 6 (Vergion 11 6 0 16)	
Microsemi Corporation - Mic	rogemi Tibero Software Delease w11 6 (Version 11 6 0 16)	
Design: false_path		l
Family: SmartFusion2 Die: M2S050		
Package: 484 FBGA		
Temperature Range: 0 - 85 C		
Voltage Range: 1.14 - 1.26		
Speed Grade: STD		
Design State: Post-Layout		
Data source: Production		
Min Operating Conditions: B		
Max Operating Conditions: W Scenario for Timing Analysi		
Scenario for liming Analysi	S: Frimary	
SUMMARY		
	my_clk	
	1.706	
Frequency (MHz): Required Period (ns):	586.166	
Required Frequency (MHz):		
External Setup (ns):	-0.025	
	0.753	
Min Clock-To-Out (ns):	5.117	
Max Clock-To-Out (ns):	9.781	
	Input to Output	
Min Delay (ns):	N/A	
Max Delay (ns):	N/A	
END SUMMARY		
Clock Domain my clk		
SET Register to Register		
Megiobel bo Megiobel		
Path 1		
From:	D2_reg:CLK	
To:	Q_reg:D	
Delay (ns): Slack (ns):	1.341 8.294	
Arrival (ns):	5.333	
Required (ns):	13.627	
Setup (ns):	0.298	
Minimum Period (ns):	1.706	

Figure 57 · Timer Report

See Also

<u>Generating timing report</u> <u>Timing Report Options dialog box</u>



Generating a Timing Violation Report

The timing violations report provides a flat slack report centered around constraint violations.

To generate a timing violation report

- 1. From the SmartTime Max/Min Delay Analysis View Window, choose **Tools > Reports > Timing > Timing Violations**. The <u>Timing Violation Report Options dialog box</u> appears.
- 2. Select the options you want to include in the report, and then click **OK**. The timing violations report appears in a separate window.

You can also generate the timing violations report from within SmartTime. From the the Maximum/Minium Delay Analysis View's **Tools** menu, choose **Reports** > **Timing Violations**.

See Also

<u>Understanding timing violation report</u> <u>Timing Violations Report Options dialog box</u>

Understanding Timing Violation Reports

The timing violation report contains the following sections:

Header

The header lists:

- The report type
- The version of SmartTime used to generate the report
- The date and time the report was generated
- General design information (name, family, die, package, etc.)

Paths

The paths section lists the timing information for the violated paths in the design.

The number of paths displayed is controlled by two parameters:

- A maximum slack threshold to report
- A maximum number or path to report

By default, the slack threshold is 0 and the number of paths is limited. The default maximum number of paths reported is 100.

All clock domains are mixed in this report. The paths are listed by decreasing slack.

You can also choose to expand one or more paths. By default, no paths are expanded. For details, see the timing violation report options.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



Generating a Constraints Coverage Report

Timing_violations Report		_ _ ×
File Actions Help		
Timing Violation Report Max De	alay Analysis	
SmartTime Version v11.6 Microsemi Corporation - Micros 11.6.0.16) Date: Thu Apr 30 16:18:45 2015	semi Libero Software Release v11.6	(Version
Design: false_path Family: SmartFusion2 Die: M2S050 Package: 484 FBGA Temperature Range: 0 - 85 C Voltage Range: 1.14 - 1.26 V Speed Grade: STD Design State: Post-Layout Data source: Production Min Operating Conditions: BEST Max Operating Conditions: WORS Scenario for Timing Analysis:	ST - 1.14 V - 85 C	
<pre>Path 1 From: To: Delay (ns): Slack (ns): Arrival (ns): Required (ns):</pre>	D2_reg:CLK Q_reg:D 1.341 -0.373 5.333 4.960	

Figure 58 · Timing Violations Report

See Also

Generating a timing violation report (SmartTime) Timing Violations Report Options dialog box (SmartTime)

Generating a Constraints Coverage Report

The constraints coverage report contains information about the constraints in the design.

To generate a constraints coverage report, from the SmartTime Max/Min Delay Analaysis View, select Tools > Reports > Constraints Coverage. The report appears in a separate window.

See Also

Understanding constraints coverage reports



Understanding Constraints Coverage Reports

The constraint coverage displays the overall coverage of the timing constraints set on the current design. You can generate this report either from within Designer or within SmartTime Analyzer. The report contains three sections:

- Coverage Summary
- Results by Clock Domain
- Enhancement Suggestions

File Actions Help Design Family Die								
Design Family								
Family		folgo poth						-
-		false_path SmartFusior	- 2					
Die			12					1
		M2S050						
Package		484 FBGA						
Temperature Rang	je	0 - 85 C						
Voltage Range		1.14 - 1.20	6 V					
Speed Grade		STD						
Design State		Post-Layout	t.					
Analysis Min Cas	зе	BEST						
Analysis Max Cas	se	WORST						
Scenario for Tim	ming Analysis	Primary						
Coverage Summary								
+ Type of check +								
		10	40		50			
Recovery			20		20			
Output Setup	0	0	10	1	0			
Total Setup					20			
Total Setup +	++	++	+	+	20			
Total Setup +	+ 10	++	+	+	20 + 50			
Total Setup + Hold Removal	+ 10 0	0 0	+ 40 20	5 2	20 + 50 20			
Total Setup + Hold Removal Output Hold Total Hold	10 0 0 15	0 0 0	40 20 10 10 105	5 2 12	20 + 20 20 20 20			
Total Setup Hold Removal Output Hold Total Hold		0 0 0	40 20 10 10 105	5 2 12	20 + 20 20 20 20			
Total Setup +	10 0 0 15 -clk	0 0 0 0 Violated	+ 40 20 10 105 +	5 2 1 12 12	20 + 50 20 20 20 +			
Total Setup + Hold Removal Output Hold Total Hold +	10 0 0 15 	0 0 0 0 Violated	40 20 10 105	5 2 1 12 12	20 + 50 20 20 20 + +			
Total Setup + Hold Removal Output Hold Total Hold +	10 0 0 15 -clk Met	0 0 0 0 Violated	40 20 10 105 Untested 12 6	5 2 1 12 12 7 7 7 7 7 7 1	20 + 50 20 20 20 + +			
Total Setup Hold Removal Output Hold Total Hold +	10 0 15 15 	0 0 0 Violated 3 0	40 20 10 105 05	5 2 1 12 12 7 7 7 7 7 7 1	20 + 50 10 20 20 + 1 55 6			
Total Setup Hold Removal Output Hold Total Hold Clock domain: my Type of check Setup Recovery Output Setup Total Setup	10 0 15 15 15 15 15 15 15 15	0 0 0 0 0 0 0 0 0 0 0 0 0	40 20 10 105 Untested 12 6 3 42	5 2 1 12 12 12 12 1 1 1 1 1	20 + 50 20 20 + 1 + 55 66 3 28			
Total Setup Hold Removal Output Hold Total Hold Clock domain: my Type of check Setup Recovery Output Setup Total Setup Total Setup	10 0 15 16 15 16 16 15 16 15 16 15 16 1	0 0 0 0 0 0 Violated 3 0 0 6	40 20 10 105 Untested 12 6 3 42	5 2 1 12 12 70tal	20 + 50 20 20 20 + 1 5 6 3 88 + 55			
Total Setup Hold Removal Output Hold Total Hold Clock domain: my Type of check Setup Recovery Output Setup Total Setup Total Setup	10 0 15 15 15 15 15 15 15 15	0 0 0 0 0 0 0 0 0 0 0 0 0	40 20 10 105 Untested 12 6 3 42	5 2 1 12 12 70tal	20 + 50 20 20 20 + 1 5 6 3 88 + 55			
Total Setup Hold Removal Output Hold Total Hold 	10 0 0 15 	0 0 0 0 0 0 0 0 0 0 0 0 0	40 20 10 105 Untested 12 6 3 42 12 6	5 2 1 12 12 70tal	20 50 50 50 50 50 51 55 6 53 18 +			

Figure 59 · Constraints Coverage Report



Coverage Summary

The coverage summary gives statistical information on the timing constraint in the design. For each type of timing checks (Setup, Recovery, Output, Hold and Removal), it specifies how many are Met (there is a constraint and it is satisfied), Violated (there is a constraint and it is not satisfied), or Untested (no constraint was found).

Clock Domain

This section provides a coverage summary for each clock domain.

Enhancement Suggestions

The enhancement suggestion reports, per clock domain, a list of constraints that can be added to the design to improve the coverage. It also reports if some options impacting the coverage can be changed.

Detailed Stats

This section provides detailed suggestions regarding specific clocks or I/O ports that may require to be constrained for every pin/port that requires checks.

See Also

<u>Clock</u> <u>Input delay</u> <u>Output delay</u> Setting SmartTime Options

Generating a Bottleneck Report

The bottleneck report provides a list of the bottlenecks in the design. To generate a bottleneck report, from the,SmartTime Max/Min Delay Analaysis View select **Tools > Reports > Bottleneck**. The report appears in a separate window.

See Also

Understanding the bottleneck report Timing Bottleneck Report Options dialog box

Understanding Bottleneck Reports

A bottleneck is a point in the design that contributes to multiple timing violations. The purpose of the bottleneck report is to provide a list of the bottlenecks in the design. You can generate this report either from within Designer or within SmartTime Analyzer. It contains two sections

- Device Description
- Bottleneck Analysis



BottleNeck Report							
File Actions Help							
Bottleneck Report Max Delay Analysis							
SmartTime Version 11.6.0.15							
Smartlime Version 11.6.0.15 Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.15)							
Date: Fri May 01 15:35:29 2015	x r						
Design	TOP						
Family	RTG4						
Die	RT4G150						
Package	1657 CG						
Radiation Exposure	0						
Temperature Range	-55 - 125 C						
Voltage Range	1.14 - 1.26 V						
Speed Grade	-1						
Design State	Post-Layout						
Data source	Advanced						
Analysis Max Case	WORST - 1.14 V - 125 C						
Set selection type	Select Entire Design						
Cost type	Path Count						
Max Paths	100	=					
Max Parallel Paths	1						
Bottleneck instances	10						
Slack Threshold	0						
Scenario for Timing Analysis	Primary						
Bottleneck Analysis							
Instance Name		Path Count					
FDDR_INIT_0/COREABC_0/I0_OUT[50						
CoreAHBLite_0/matrix4x16/mast	16						
CoreAHBLite_0/matrix4x16/slav	15 1						
CoreAHBLite_0/matrix4x16/mast	15 1						
CoreAHBLite_0/matrix4x16/slav	1						
CoreAHBLite_0/matrix4x16/slav	1						
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_RNO[11]:Y 1							
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_nss_i_0[0]:Y 1							
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_RN0[7]:Y 1							
++							
		-					
		.ii.					

Figure 60 · Bottleneck Report

The bottleneck can only be computed if a cost type is defined. There are two options available:

- **Path count:** This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Device Description

The device section contains general information about the design, including:

- Design name
- Family
- Die

.

- Package
- Software version

Bottleneck Analysis

This section lists the core of the bottleneck information. It is divided into two columns:

• Instance name: refers to the output pin name of the instance.



• Path Count: Displays the number of violating paths which include the instance pin..

See Also

<u>Generating a bottleneck report</u> <u>Timing Bottleneck Report Options dialog box</u>

Generating a Datasheet Report

The datasheet reports information about the external characteristics of the design. To generate a datasheet report, from the SmartTime Max/Min Delay Analaysis View, select **Tools > Reports > Datasheet**. The report appears in a separate window.

See Also

<u>Understanding the datasheet report</u> <u>Timing Datasheet Report Options dialog box</u>

Understanding Datasheet Reports

The datasheet report displays the external characteristics of the design. You can generate this report from SmartTime Max/Min Delay Analysis view. It contains three tables:

- Pin Description
- DC Electrical Characteristics
- AC Electrical Characteristics



	77 74 55 57 77 79 79 139 39 39										
AU7 AW4 AV5 BA5 AY5 BA7 BA7 BA6 AY3 AG6 AG6 AG6 AG6	77 74 55 57 77 79 79 139 39 39	Input Input Input Input Input Input Input Input Input Output									
AW4 AV4 BA5 AY5 BA7 AY5 AY5 AY5 AN3 AL5 AG5 AG6 AM5	74 75 75 77 79 79 739 739 739	Input Input Input Input Input Input Input Input Output									
AV4 BA5 AY5 BA7 AY7 BA6 AY9 AN3 AG3 AG4 AM3	74 15 75 17 19 79 139 139 139	Input Input Input Input Input Input Input Output									
BAS AYS BAY BAY AY7 BAS AY9 AN3 AL3 AG4 AM3	45 75 47 49 79 73 9 39 39	Input Input Input Input Input Input Output									
AYS BA7 AY7 BA9 AY7 BA9 AY3 AY5 BA7 AY7 BA7 BA7	75 47 49 79 139 439	Input Input Input Input Input Output									
BA7 AY7 BA9 AY9 AN3 AL3 AG4 AG4 AM3	47 (7 (9 (39 (39 (39)	Input Input Input Input Output									
AY7 BA9 AY9 AN3 AL3 AG3 AG4 AM3	77 19 139 139 139	Input Input Input Output	i I	1							
BAS AYS ANS ALS AGS AGS AGS	19 (9 139 139 539	Input Input Output	1								
AY9 AN3 AL3 AG3 AG4 AM3	(9 (39 ,39 ;39	Input Output									
AN3 AL3 AG3 AG4 AM3	139 .39 339	Output									
AL3 AG3 AG4 AM3	.39 39			1							
AG3 AG4 AM3	39	Output	t SSTL	18I (1)							
AG4 AM3		Output	t SSTL	18I (1)							
AM3	:40	Output	t SSTL	18I (1)							
AM3		Output	t SSTL	18I (1)							
0 OUT 1 ACS		Output	t SSTL	18I (1)							
			t SSTL								
AE4	40	Output	t SSTL	18I (1)							
AH3											
ANS											
AJ3	139	Output	t SSTL	18I (1)							
F5	i	Output	t LVCM	OS18 (2)							
AJ3	738	Output	t LVCM	OS18 (2)							
L33	3	Output	t LVCM	OS18 (2)							
AT3	13	Output	t	1							
AU3	13	Output	t	1							
AT5	15	Output	t	1							
		Output	t	1							
AV6	76	Output	t								
AW6	16	Output	t								
AV8	78	Output									
AW8	10										
+		Output									ſ
cci Vccr	:s -+	Output	t + Output	 + Odt_Static	Odt	Input	Resistor	Schmitt	Slew	Output	1
+ cci Vccr V) (V)	:5 -+ Direc 	Output ++ ction 	t + Output Load (pF)	Odt_Static 	Odt Imp (Ohm)	Input Delay 	Resistor Pull 	Schmitt Trigger 	Slew	Output	1
Cci Vccr V) (V) 	23 -+ 	Output ++- ction 	Uutput Load (pF)	Odt_Static +	Odt Imp (Ohm) +	Input Delay +	Resistor Pull 	Schmitt Trigger +	Slew	Output Drive (mA) +	1
Cci Vccr V) (V) .8	:3 	Output ++- ction t	Output Load (pF)	Odt_Static +	Odt Imp (Ohm) +	Input Delay +	Resistor Pull None	Schmitt Trigger +	Slew 	Output Drive (mA) +	1
Ccci Vccr V) (V) 	:s Direc Input Outpu Outpu	Output ++- ction t ut ut	Uutput Load (pF) 5 5	Odt_Static 	Odt Imp (Ohm) + 	Input Delay + Off 	Resistor Pull 	Schmitt Trigger + Off 	Slew	Output Drive (mA) +	1
Ccci Vccr V) (V) 	:s Direc Input Outpu Outpu	Output ++- ction t ut ut	Uutput Load (pF) 5 5	Odt_Static 	Odt Imp (Ohm) + 	Input Delay + Off 	Resistor Pull 	Schmitt Trigger + Off 	Slew SLOW	Output Drive (mA) + 4	1
	AN AC FS AC LC AT AT AT AC AV AV AV	AN38 AJ39 F5 AJ38 L33 AT3 AU3 AU3 AT5 AU5 AV6 AW6	AN38 Outpu AJ39 Outpu F5 Outpu AJ38 Outpu L33 Outpu AT3 Outpu AT3 Outpu AT5 Outpu AU5 Outpu AV6 Outpu AW6 Outpu	AN38 Output SSTL: AJ39 Output SSTL: F5 Output SSTL: F5 Output LVCM AJ38 Output LVCM AT3 Output AU3 Output AU5 Output AV6 Output	AJ39 Output SSTL18I (1) F5 Output LVCMOS18 (2) AJ38 Output LVCMOS18 (2) L33 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output AU3 Output AU3 Output AT5 Output AU5 Output AV6 Output	AN38 Output SSTL181 (1) AJ39 Output SSTL181 (1) F5 Output LVCMOS18 (2) AJ38 Output LVCMOS18 (2) L33 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output AU3 Output AU3 Output AU5 Output	AN38 Output SSTL181 (1) AJ39 Output SSTL181 (1) F5 Output UVCMOS18 (2) AJ38 Output LVCMOS18 (2) L33 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output AU3 Output AU5 Output	AN38 Output SSTL181 (1) AJ39 Output SSTL181 (1) F5 Output UVCMOS18 (2) AJ38 Output LVCMOS18 (2) L33 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output AU3 Output AU3 Output AU5 Output	AN38 Output SSTL18I 1 AJ39 Output SSTL18I 1 F5 Output IVCMOS18 2 AJ38 Output LVCMOS18 2 L33 Output LVCMOS18 2 AT3 Output LVCMOS18 2 AT3 Output LVCMOS18 2 AT3 Output I I AT3 Output I I AT3 Output I I AU3 Output I I AT5 Output I I AU5 Output I I	AN38 Output SSTL18I (1) AJ39 Output SSTL18I (1) F5 Output SSTL18I (1) F5 Output IVCMOS18 (2) AJ38 Output IVCMOS18 (2) L33 Output IVCMOS18 (2) AT3 Output I I AU3 Output I I AU3 Output I I AU5 Output I I	AN38 Output SSTL18I (1) AJ39 Output SSTL18I (1) F5 Output LVCMOS18 (2) AJ38 Output LVCMOS18 (2) L33 Output LVCMOS18 (2) AT3 Output LVCMOS18 (2) AT3 Output AT3 Output AU3 Output AU3 Output AU5 Output

Figure 61 · Datasheet Report

Pin Description

Provides the port name in the netlist, location on the package, type of port, and I/O technology assigned to it. Types can be input, output, inout, or clock. Clock ports are ports shown as "clock" in the Clock domain browser.

DC Electrical Characteristics

Provides the parameters of the different I/O technologies used in the design. The number of parameters displayed depends on the family for which you have created the design.

AC Electrical Characteristics

Provides the timing properties of the ports of the design. For each clock, this section includes the maximum frequency. For each input, it includes the external setup, external hold, external recovery, and external



removal for every clock where it applies. For each output, it includes the clock-to-out propagation time. This section also displays the input-to-output propagation time for combinational paths.

See Also

<u>Generating a datasheet report</u> <u>Timing Datasheet Report Options dialog box</u>

Generating a Combinational Loop Report

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

To generate a combinational loop report, from the Designer **Tools** menu, select **Reports > Timing > Combinational Loops**. The report appears in a separate window.

You can also generate the combinational loop report from within SmartTime. From the **Tools** menu, choose **Reports > Combinational Loops**.

See Also

Understanding Combinational Loop Reports

Understanding Combinational Loop Reports

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.



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Combinational_loops Report

File Actions Help				
Combinational Loop Report SmartTime Version 11.6.0.15 Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version 11.6.0.15)				
Date: Fri May 01 15:50:15 2015				
Radiation Exposure Temperature Range Voltage Range Speed Grade Design State Analysis Min Case	TOP RTG4 RT4G150 1657 CG 0 -55 - 125 C 1.14 - 1.26 V -1 Post-Layout BEST - 1.26 V55 C WORST - 1.14 V - 125 C Primary			
No combinational loops were det	ected in the design.			

Figure 62 · Combinational Loop Report

To view a graphical representation of the broken loop, open MultiView Navigator, find each pin and add them as a logical cone. For more information on how to find each pin and how to set up the logical cones, refer to <u>What is a LogicalCone</u>.

See Also

Generating a Combinational Loop Report



Timing Concepts

Static Timing Analysis Versus Dynamic Simulation

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements. The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms.

Delay Models

The first step in timing analysis is the computation of single component delays. These components could be either a combinational gate or block or a single interconnect connecting two components.

Gates that are part of the library are pre-characterized with delays under different parameters, such as inputslew rates or capacitive loads. Traditional models provide delays between each pair of I/Os of the gate and between rising and falling edges.

The accuracy with which interconnect delays are computed depends on the design phase. These can be estimated using a simple Wire Load Model (WLM) at the pre-layout phase, or a more complex Resistor and Capacitor (RC) tree solver at the post-layout phase.

Timing Path Types

Path delays are computed by adding delay values across a chain of gates and interconnects. SmartTime uses this information to check for timing violations. Traditionally, timing paths are presented by static timing analysis tools in four categories or "sets":

- Paths between sequential components internal to the design. SmartTime displays this category under the Register to Register set of each displayed clock domain.
- Paths that start at input ports and end at sequential components internal to the design. SmartTime
 displays this category under the External Setup and External Hold sets of each displayed clock
 domain.
- Paths that start at sequential components internal to the design and end at output ports. SmartTime
 displays this category under the Clock to Out set of each displayed clock domain.
- Paths that start at input ports and end at output ports. SmartTime displays this category under the Input to Output set.

Maximum Clock Frequency

Generally, you set clock constraints on clocks for which you have a specified requirement. The absence of violations indicates that this clock will be able to run at least at the specified frequency. However, in the absence of such requirements, you may still be interested in computing the maximum frequency of a specific clock domain.

To obtain the maximum clock frequency, a static timing analysis tool computes the minimum period for each path between two sequential elements. To compute the maximum period, the tool evaluates the maximum data path delay and the minimum skew between the two elements, as well as the setup on the receiving sequential element. It also considers the polarity of each sequential element. The maximum frequency is the



inverse of the largest value among the maximum period of all the paths in the clock domain. The path responsible for limiting the frequency of a given clock is called the critical path.

Setup Check

The setup and hold check ensures that the design functions as specified at the required clock frequency.

Setup check specifies when data is required to be present at the input of a sequential component in order for the clock to capture this data effectively into the component. Timing analyzers evaluate the setup check as a maximum timing budget allowed between adjacent sequential elements. For more details on how setup check is processed, refer to <u>Arrival time, required time, and slack</u>.

See Also

Static timing analysis Arrival time, required time, and slack

Arrival Time, Required Time, and Slack

You can use arrival time and required time to verify timing requirements in the presence of constraints. Below is a simple example applied to verifying the clock requirement for setup between sequential elements in the design.

The arrival time represents the time at which the data arrives at the input of the receiving sequential element. In this example, the arrival time is considered from the setup launch edge at CK, taken as a time reference (instant zero). It follows the clock network along the blue line until the clock pin on FF1 (delay d1). Then it continues along the data path always following the blue line until the data pin D on FF2. Therefore,

Arrival_Time_{FF2:D} = d1 + d2

The required time represents when the data is required to be present at the same pin FF2:D. Assume in this example that in the presence of an FF with the same polarity, the capturing edge is simply one cycle following the launch edge. Using the period T provided to the tool through the clock constraint, the event gets propagated through the clock network along the red line until the clock pin of FF2 (delay d3). Taking into account FF2 setup (delay d4), this means that the clock constraint requires the data to be present d4 time before the capturing clock edge on FF2. Therefore, the required time is:

Required_Time_{FP2:D} = T + d3 - d4

The slack is simply the difference between the required time and arrival time:

Slack_{FF2:D} = Required_Time_{FF2:D} - Arrival_TimeFF2:D

If the slack is negative, the path is violating the setup relationship between the two sequential elements.

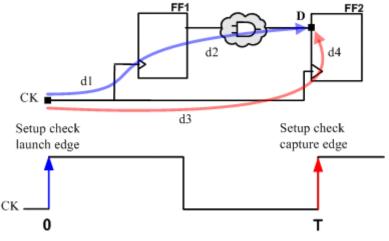


Figure 63 · Arrival Time and Required Time for Setup Check



Timing Exceptions

Design requirements are often imported using clock, input delay, and output delay constraints. By default, most static timing analyzers assume that all paths are sensitizable. They also assume that the design is operating in a single-cycle mode (that is, only one clock cycle is allowed for the data to transfer from one sequential stage to another).

If any paths in your design exhibit a different behavior, you must use timing exceptions to overwrite the default behavior. Timing exceptions include:

- Setting a false path constraint to identify non sensitizable paths that should not be included in the analysis or the optimization flow.
- Setting a maximum delay constraint on specific paths to relax or tighten the original clock constraint requirement on them.
- Setting a multicycle constraint to specify paths that by design will take more than one cycle to exchange data between sequential components.

SmartTime supports all these exceptions.

See Also

set_false_path (SDC) Set False Path Constraint dialog box set_max_delay (SDC) Set Maximum Delay Constraint dialog box set_multicycle_path (SDC) Set Multicycle Constraint dialog box

Clock Skew

The clock skew between two different sequential components is the difference between the insertion delays from the clock source to the clock pins of these components. SmartTime calculates the arrival time at the clock pin of each sequential component. Then it subtracts the arrival time at the receiving component from the arrival time at the launching component to obtain an accurate clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.



Dialog Boxes

Add Path Analysis Set Dialog Box

Use this dialog box to specify a custom path analysis set.

. .

Note: The Analysis menu is available only in Maximum or Minimum Delay Analysis view.

To open the **Add Path Analysis Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, right-click a path group in the Domain Browser and select **Add Set**.

You may also click the 🌇 icon to	open the Add P	ath Analysis Set Dia	alog box.
Add Path Analysis Set			X
Name:	Trace from:	Source to sink	C Sink to source
Source Pins:	Sink	Pins:	
DDR0/U0:CLK DDR1/U0:CLK DDRREG2/INBUF_LVDS_0_inst/U0/U2_DDR1:C FIFO_inst/FIFO64K36_FULL:RCLK FIFO_inst/FIFO64K36_Q_0_inst:RCLK RAM_inst/RAM64K36_Q_0_inst:WCLK RAM_inst/RAM64K36_Q_1_inst:RCLK RAM_inst/RAM64K36_Q_1_inst:WCLK Rdf_pll0/U0:CLK Rdf_pll1/U0:CLK XCMP33/U0/U2_DDR1:CLK XCMP33/U0/U2_DDR2:CLK			
Select All		Select All	
Filter source pins:	Filt	er sink pins:	
Pin Type: Registers by pin names		Pin Type: Regist	ers by pin names 💌
Filter		*	Filter
Help		ОК	Cancel

Figure 64 · Add Path Analysis Set Dialog Box

Name

Enter the name of your path set.



Trace from

Select whether you want to trace connected pins from **Source to sink** or from **Sink to source**. By default, the pins are traced Source to sink.

Source Pins

Displays a list of available and valid source pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the Source Pins list.

Select All

Selects all the pins in the Source Pins list to include in the path analysis set.

Filter Source Pins

Enables you to specify thesource **Pin Type** and the **Filter**. The default pin type is Registers by pin name. You can specify any string value for the **Filter**. If you change the pin type, the **Source Pins** shows the updated list of available source pins.

Sink Pins

Displays list of available and valid pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the **Sink Pins list.**

Select All

Selects all the pins in the Sink Pins list to include in the path analysis set.

Filter Sink Pins

Enables you to specify thesink **Pin Type** and the **Filter**. The default pin type is Registers (by pin). You can specify any string value for the **Filter**. If you change the pin type, the **Sink Pins** shows the updated list of available sink pins.

Analysis Set Properties Dialog Box

Use this dialog box to view information about the user created set.

To open the **Analysis Set Properties** dialog box (shown below) from the Timing Analysis View, right-click any user-created set in the Domain Browser, and choose **Properties** from the shortcut menu.

Analysis Set Pro	operties 2
Name :	my_set
Parent set :	
From :	CoreAHBLite_0/matrix4x16/masterstage_0/SDATASELInt[0]:CLK
To :	SERDES_IF_0/SERDESIF_INST/INST_PCIE_IP:AXI_M_WREADY_HREADY
Help	OK Cancel

Figure 65 · Analysis Set Properties Dialog Box

Name

Specifies the name of the user-created path set.



Parent Set

Specifies the name of the parent path set to which the user-created path set belongs.

Creation filter

From

Specifies a list of source pins in the user-created path set.

То

Specifies a list of sink pins in the user-created path set.

See Also

Using filters

Edit Filter Set Dialog Box

Use this dialog box to specify a filter.

To open the **Edit Filter Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, right-click an existing user set in the clock domain browser, and then choose **Edit Set** from the shortcut menu.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



Select Source Pins for Clock Constraint Dialog Box

Edit Path Analysis Set	? <mark>×</mark>
Name :- my set1	Trace from :- 💿 Source to sink 💿 Sink to source
Source pins:	Sink Pins:
CFG0 GND INST:Y	SerDes AHBBUS 0/PCIE SERDES IF 0/SERDESIF INST RNO
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IP_0/SERDESIF_INST_RNO
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite 0/matrix4x16/masterstage 0/DEFSLAVEDATAS	SerDes AHBBUS 0/PCIE SERDES IF 0/SERDESIF INST RNO
CoreAHBLite 0/matrix4x16/masterstage 0/DEFSLAVEDATAS	SerDes AHBBUS 0/PCIE SERDES IF 0/SERDESIF INST RNO
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO
CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS	SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_
Select All	Select All
Filter source pins:	Filter sink pins:
Pin Type: All pins	Pin Type: All pins
* Filter	* Filter
Help	OK Cancel

Figure 66 · Edit Filter Set Dialog Box

Name

Specifies the name of the filtered set you want to edit.

Creation filter

From - Specifies a list of source pins in the user-created path set.To - Specifies a list of sink pins in the user-created path set.

See Also

Using filters

Select Source Pins for Clock Constraint Dialog Box

Use this dialog box to find and choose the clock source from the list of available pins.

To open the **Select Source Pins for the Clock Constraint** dialog box (shown below) from the SmartTime Constraints Editor, click the **Browse** button to the right of the Clock source field in the <u>Create Clock</u> <u>Constraint</u> dialog box.



Select Source Pins for Clock Constraint	? ×
Specify pins :- () by explicit list () by keyword and wildcard	
Available Pins: Add Add All Remove Remove All	
Filter available pins : Pin Type : Explicit clocks * Filter	Help OK Cancel

Figure 67 · Choose the Clock Source Pin Dialog Box

Available Pins

Displays all available pins.

Filter Available Pins

Explicit clock pins for the design is the default value. To identify any other pins in the design as clock pins, right-click the Pin Type pull-down menu and select one of the following:

- Explicit clocks,
- Potential clocks,
- Input ports,
- All Pins,
- All Nets,
- Pins on clock network, or
- Nets in clock network.

You can also use the Filter to filter the clock source pin name in the displayed list

See Also

Specifying clock constraints

Create Clock Constraint Dialog Box

Use this dialog box to enter a clock constraint setting.

It displays a typical clock waveform with its associated clock information. You can enter or modify this information, and save the final settings as long as the constraint information is consistent and defines the clock waveform completely. The tool displays errors and warnings if information is missing or incorrect.

To open the **Create Clock Constraint** dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Clock**.



Create Clock Constraint		8 22
Clock Name :	Clock Source :	•
Heriod :	ns 🗕 or Frequency:	Mhz
← Offset : ▶ ← Duty cycle : ● 0.000 ns 50,0000 %	•	
Comment :		
Help	ОК	Cancel

Figure 68 · Create Clock Constraint Dialog Box

Clock Source

Enables you to choose a pin from your design to use as the clock source.

The drop-down list is populated with all explicit clocks. You can also select the Browse button to access all potential clocks. The **Browse** button displays the <u>Select Source Pins for Clock Constraint</u> dialog box.

Clock Name

Specifies the name of the clock constraint. This field is required for virtual clocks when no clock source is provided.

T(zero) Label

Instant zero used as a common starting time to all clock constraints.

Period

When you edit the period, the tool automatically updates the frequency value. The period must be a positive real number. Accuracy is up to 3 decimal places.

Frequency

When you edit the frequency, the tool automatically updates the period value. The frequency must be a positive real number. Accuracy is up to 3 decimal places.

Offset (Starting Edge Selector)

Enables you to switch between rising and falling edges and updates the clock waveform. If the current setting of starting edge is rising, you can change the starting edge from rising to falling. If the current setting of starting edge is falling, you can change the starting edge from falling to rising.

Duty Cycle

This number specifies the percentage of the overall period that the clock pulse is high. The duty cycle must be a positive real number. Accuracy is up to 4 decimal places. Default value is 50%.

Offset

The offset must be a positive real number. Accuracy is up to 2 decimal places. Default value is 0.



Comment

Enables you to save a single line of text that describes the clock constraints purpose.

See Also

<u>create_clock (SDC)</u> <u>Clock definition</u> Specifying clock constraint

Create Generated Clock Constraint Dialog Box

Use this dialog box to specify generated clock constraint settings.

It displays a relationship between the clock source and its reference clock. You can enter or modify this information, and save the final settings as long as the constraint information is consistent. The tool displays errors and warnings if the information is missing or incorrect.

To open the **Create Generated Clock Constraint** dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Generated Clock**.

Create Generated Clock Constraint
Reference Pin:
Clock Port FPGA
Generated Clock Name
The generated frequency is such as
f(clock) = f(reference) × 1 / 1 Get Pre-Computed Factor
The generated waveform is the same as 🔹 the reference waveform
Comment:
Help OK Cancel

Figure 69 · Create Generated Clock Constraint

Clock Pin

Enables you to choose a pin from your design to use as a generated clock source.

The drop-down list is populated with all unconstrained explicit clocks. You can also select the Browse button to access all potential clocks and pins from the clock network. The Browse button displays the <u>Select</u> <u>Generated Clock Source</u> dialog box.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. **View the online help included with software to enable all linked content.**



Reference Pin

Enables you to choose a pin from your design to use as a generated reference pin.

Generated Clock Name

Specifies the name of the clock constraint. This field is required for virtual clocks when no clock source is provided.

Generated Frequency

The generated frequency is a factor of reference frequency defined with a multiplication element and/or a division element.

Generated Waveform

The generated waveform could be either the same as or inverted w.r.t. the reference waveform.

Comment

Enables you to save a single line of text that describes the generated clock constraints purpose.

See Also

create_generated_clock (SDC) Specifying generated clock constraint Select Generated Clock Source

Customize Analysis View Dialog Box

Use this dialog box to customize the timing analysis grid.

To open the **Customize Analysis View** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, click the Customize table button (circled in red in the Figure below) in the Max/Min Delay Analysis View.

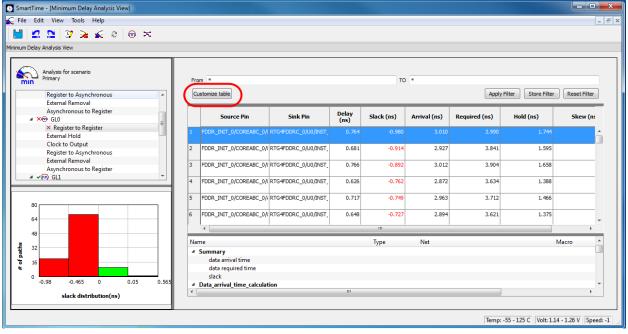


Figure 70 · Customize Table Button

The Customize Paths List Table Dialog Box appears.



Customize Paths List Table	5 ×
Available fields: Clock Source Clock Edge Destination Clock Edge Logic Stage Count Clock Constraint (ns) Multicycle Constraint	Add Source Pin Sink Pin Delay (ns) Slack (ns) Arrival (ns) Required (ns) Hold (ns) Skew (ns)
Help Restore Default	OK Cancel

Figure 71 · Customize Paths List Dialog Box

Available Fields

Displays a list of all the available fields in the timing analysis grid.

Show These Fields in This Order

Shows the list of fields you want to see in the timing analysis grid. Use **Add** or **Remove** to move selected items from **Available fields** to **Show these fields in this order** or vice versa. You can change the order in which these fields are displayed by using **Move Up** or **Move Down**.

Restore Defaults

Resets all the options in the General panel to their default values.

Manage Clock Domain Dialog Box

Use this dialog box to specify the clock pins you want to see in the Expanded Path view. To open the **Manage Clock Domain** dialog box (shown below) from the SmartTime Max/Min Delay Analysis

View, click the icon.



Manage Clock Domains	S ×
Available clock domains:	Show the clock domains in this order: My_clk1 my_clk2
	Remove
	Move Up
	Move Down
Help New Clock	OK Cancel

Figure 72 · Manage Clock Domains Dialog Box

Available Clock Domains

Displays alphanumerically sorted list of available clock pins. The first clock pin is selected by default.

Show the Clock Domains in this Order

Shows the clock pins you want to see in the Expanded Path view. Use **Add** or **Remove** to move selected items from **Available clock domains** to **Show the clock domains in this order** or vice versa. You can change the order in which these clock pins are displayed by using **Move Up** or **Move Down**.

New Clock

Invokes the <u>Choose the Clock Source Pin</u> dialog box. The new clock gets added at the end of the **Show the** clock domains in this order list box.

See Also

Managing clock domains

Select Generated Clock Source Dialog Box

Use this dialog box to find and choose the generated clock source from the list of available pins. To open the **Select Generated Clock Source** dialog box (shown below) from the SmartTime Constraints Editor, open <u>Create Generated Clock Constraint</u> dialog box and click the **Browse** button for the **Clock Pin**.



Select Generation	ted Clock Source
Filter available p	pins :
Pin Type :	Explicit docks
*	Filter
Help	OK Cancel

Figure 73 · Select Generated Clock Source Dialog Box

Filter Available Pins

Explicit clock pins for the design is the default value. To identify any other pins in the design as the generated clock source pins, from the **Pin Type** pull-down list, select **Explicit clocks**, **Potential clocks**, **All ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. You can also use the **Filter** to filter the generated clock source pin name in the displayed list.

See Also

Specifying generated clock constraint (SDC)

Select Generated Clock Reference Dialog Box

Use this dialog box to find and choose the generated clock reference pin from the list of available pins. To open the **Select Generated Clock Reference** dialog box (shown below) from the SmartTime Constraints Editor, open <u>Create Generated Clock Constraint</u> dialog box and click the **Browse** button for the **Clock Reference**.



Select Source or Destination Pins for Constraint Dialog Box

Select Generate	d Clock Source		? X
FDDR_ADDR FDDR_ADDR[0] FDDR_ADDR[10] FDDR_ADDR[11] FDDR_ADDR[12] FDDR_ADDR[13] FDDR_ADDR[14] FDDR_ADDR[15] FDDR_ADDR[1]			•
Filter available pir	IS :		
Pin Type :	All Ports		•
*			Filter
Help		ОК	Cancel

Figure 74 · Select Generated Clock Reference Dialog Box

Filter Available Pins

To identify any other pins in the design as the generated master pin, select **Filter available objects - Type** as **Clock Network**. You can also use the **Filter** to filter the generated reference clock pin name in the displayed list.

See Also

Specifying generated clock constraint (SDC)

Select Source or Destination Pins for Constraint Dialog Box

Use this dialog box to select pins or ports:

- By explicit list
- By keyword and wildcard

To open the **Select Source or Destination Pins for Constraint** dialog box from the SmartTime Constraints Editor, right-click the Constraint Type in the Contraint Browser to open the Add Constriant dialog box. From this dialog box, click the Browse button to open the Select Source or Destination Pins for Constraint dialog box.

By Explicit List

This is the default. This mode stores the actual pin names. The following figure shows an example dialog box for **Select Source Pins for Multicycle Constraint > by explicit list**.



Select Source Pins for Multicy Specify pins :-	
Available Pins: FDDR_DM_RDQS FDDR_DM_RDQS[0] FDDR_DM_RDQS[1]	Assigned Pins:
FDDR_DQ FDDR_DQS FDDR_DQS[0] FDDR_DQS[1] FDDR_DQS_N FDDR_DQS_N[0] FDDR_DQS_N[1]	Add All Remove Remove All
FDDR_DQS_TMATCH_0_IN Filter available pins : Pin Type : Input Ports *	▼ Help OK Filter Cancel

Figure 75 · Select Source Pins for Multicycle (Specify pins by explicit list) Dialog Box

Available Pins

The list box displays the available valid objects. If you change the filter value, the list box shows the available objects based on the filter.

Use Add, Add All, Remove, Remove All to add or delete pins from the Assigned Pins list.

Filter Available Pins

Pin type – Specifies the filter on the available object. This can be by **Explicit clocks**, **Potential clocks**, **Input ports**, **All Pins**, **All Nets**, **Pins on clock network**,or **Nets in clock network**

Filter

Specifies the filter based on which the **Available Pins** list shows the pin names. The default is *. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_ports, get_pins, etc.). The following figure shows an example dialog box for **Select Source Pins for Multicycle Constraint > by keyword and wildcard**.



Select Source Pins for Multicycle Constraint	8 23
Specify pins :- 🔘 by explicit list 🔘 by keyword and wildcard	
Resulting Pins :	
FDDR_DM_RDQS	*
FDDR_DM_RDQS[0]	
FDDR_DM_RDQS[1]	=
FDDR_DQ	
FDDR_DQS	
FDDR_DQS[0]	
FDDR_DQS[1]	
FDDR_DQS_N	
FDDR_DQS_N[0]	
FDDR_DQS_N[1] FDDR_DQS_TMATCH_0_IN	
	T
Filter available pins :	Help
Pin Type : Input Ports	
* Eiter	ОК
* Filter	Cancel

Figure 76 · Select Source Pins for Multicycle (Specify pins by keyword and wildcard) Dialog Box

Pin Type

Specifies the filter on the available pins. This can be Registers by pin names, Registers by clock names, Input Ports, or Output Ports. The default pin type is Registers by pin names.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *. You can specify any string value.

Resulting Pins

Displays pins from the available pins based on the filter.

Set False Path Constraint Dialog Box

Use this dialog box to define specific timing paths as being false.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints.

To open the **Set False Path Constraint** dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > False Path**.



t False Path Constraint	
From:	
1	<u>^</u>
<	>
Through:	
	~
To:	
<	
C	
Comment:	
1	
Help	OK Cancel

Figure 77 · Set False Path Constraint Dialog Box

From

Specifies the starting points for false path. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

Through

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

То

Specifies the ending points for false path. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Comment

Enables you to provide comments for this constraint.

See Also

Specifying false path constraint

Set Clock Source Latency Dialog Box

Use this dialog box to define the delay between an external clock source and the definition pin of a clock within SmartTime.



To open the **Set Clock Source Latency** dialog box (shown below) from the Timing Analysis View, you must first <u>create a clock constraint</u>. From the **Constraints** menu, choose Clock Source **Latency**.

Set Clock Source Latency Constraint	? ×
Clock Name or Source:	•
Clock Source	
Late Rise ns 🔶 Late Fall	ns
Early Rise ns 🔶 Early Fall	ns
Clock Name or Source	
Clock Edges: 🔲 Falling same as rising 📄 Early same as late	
Comment:	
Help	Cancel

Figure 78 · Set Clock Source Latency Dialog Box

Clock Name or Source

Displays a list of clock ports or pins that do not already have a clock source latency specified. Select the clock name or source for which you are specifying the clock source latency.

Late Rise

Specifies the largest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Early Rise

Specifies the smallest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Late Fall

Specifies the largest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.



Early Fall

Specifies the smallest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Clock Edges

Select the latency for the rising and falling edges:

Falling same as rising: Specifies that Rising and Falling clock edges have the same latency.

Early same as late: Specifies that the clock source latency should be considered as a single value, not a range from "early" to '"late".

Comment

Enables you to save a single line of text that describes the clock source latency.

See Also

Specifying clock constraints

Set Constraint to Disable Timing Arcs Dialog Box

Use this dialog box to specify the timing arcs being disabled to fix the combinational loops in the design. To open the **Set Constraint to Disable Timing Arcs** dialog box (shown below) from the Timing Analysis View, from the **Constraints** menu, choose **Disable Timing**.

Set constraint to disable timing arcs	x
Instance Name:)
 Exclude all timing arcs in the instance 	
 Specify timing arc to exclude: From Port To Port: 	•
Comment: Help OK Cancel	

Figure 79 · Set Constraint to Disable Timing Arcs Dialog Box

Instance Name

Specifies the instance name for which the disable timing arc constraint will be created.



Exclude All Timing Arcs in the Instance

This option enables you to exclude all timing arcs in the specified instance.

Specify Timing Arc to Exclude

This option enables you to specify the timing arc to exclude. In this case, you need to specify the from and to ports:

From Port

Specifies the starting point for the timing arc.

To Port

Specifies the ending point for the timing arc.

Comment

Enables you to save a single line of text that describes the disable timing arc.

See Also

Specifying Disable Timing Constraint

Set Clock-to-Clock Uncertainty Constraint Dialog Box

Use this dialog box to model tracking jitter between two clocks in your design.

To open the **Set Clock-to-Clock Uncertainty Constraint** dialog box (shown below), from the **Constraint** menu, choose **Clock-to-Clock Uncertainty Constraint**.



Set Clock-to-	clock Uncertainty Con	straint	
From Clock:			
Edge	C rising	C falling	⊙ both
	Ī		Ī
To Clock:			▼
Edge	C rising	C falling	⊙ both
Uncertainty:	ns		
Use uncertain	nty for: 🔘 setup checks	O hold checks	 all checks
Comment:			
Help]	[OK Cancel

Figure 80 · Clock-to-Clock Uncertainty Constraint Dialog Box

From Clock

Specifies clock name as the uncertainty source.

Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

To Clock

Specifies clock name as the uncertainty destination.

Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

Uncertainty

Enter the time in ns that represents the amount of variation between two clock edges.

Use Uncertainty For

This option enables you select whether the uncertainty constraint applies to setup, hold, or all checks.

Comment

Enables you to save a single line of text that describes this constraint.



See Also

Specifying Disable Timing Constraint

Add Input Delay Constraint Dialog Box

Use this dialog box to apply input delay constraints or external setup/hold constraints. This constraint defines the arrival time of an input relative to a clock.

To open the **Set Input Delay Constraint** dialog box (shown below) from the SmartTime Constraints Editor Constraints menu, choose **Input Delay** (**Constraints > Input Delay**).

External Setup/hold

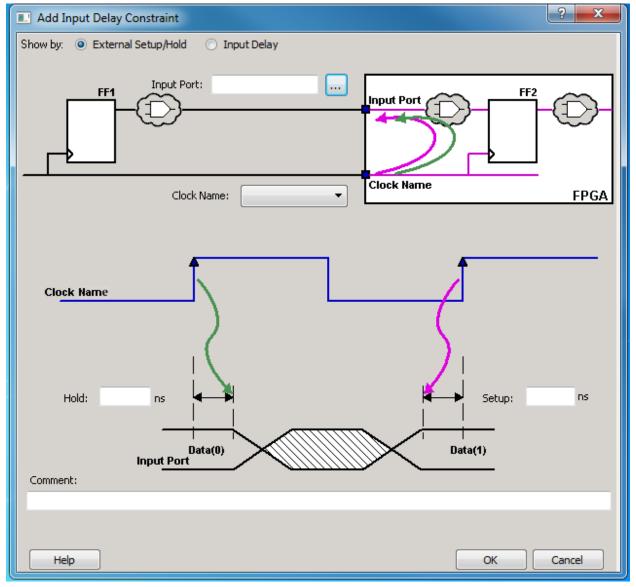


Figure 81 · Set Input Delay Constraint (Show by: External Setup/Hold) Dialog Box

Input Port

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.



Clock Name

Specifies the clock reference to which the specified External Setup/Hold is related.

External Hold

Specifies the external hold time requirement for the specified input ports.

External Setup

Specifies the external setup time requirement for the specified input ports.

Comment

Enables you to provide comments for this constraint.

Input Delay

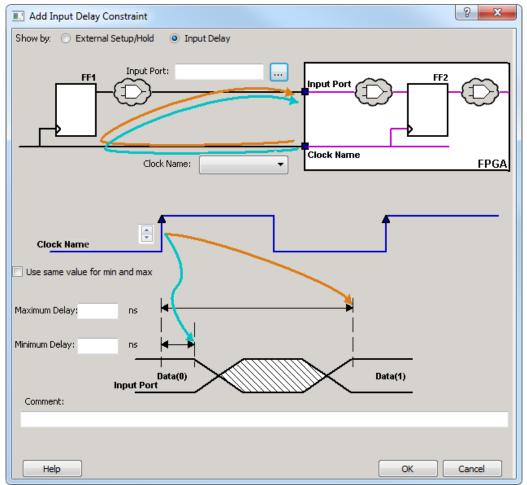


Figure 82 · Set Input Delay Constraint (Show by: Input Delay) Dialog Box

Input Port

Specifies a list of input ports in the current design to which the constraint is assigned. You can apply more than one port.

Clock Name

Specifies the clock reference to which the specified input delay is related.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



Clock edge

Indicates the launching edge of the clock.

Use max delay for both min and max

Specifies that the minimum input delay uses the same value as the maximum input delay.

Maximum Delay

Specifies that the delay refers to the longest path arriving at the specified input.

Minimum Delay

Specifies that the delay refers to the shortest path arriving at the specified input.

Comment

Enables you to provide comments for this constraint.

See Also

Specifying input timing delay constraint

Set Maximum Delay Constraint Dialog Box

Use this dialog box to specify the required maximum delay for timing paths in the current design.

SmartTime automatically derives the individual maximum delay targets from clock waveforms and port input or output delays. So the maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

To open the **Set Maximum Delay Constraint** dialog box (shown below) from the SmartTime Constraints Editor, click the **Constraints** menu and choose **Max Delay** (**Constraints > Max Delay**).



et Maximum Delay Constraint	×
Maximum delay: ns	
From:	
Through:	
То:	
Comment:	
Help OK Cancel	

Figure 83 · Set Maximum Delay Constraint Dialog Box

Maximum Delay

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

From

Specifies the starting points for max delay constraint. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

Through

Specifies the through points for the multiple cycle constraint.



То

Specifies the ending points for maximum delay constraint. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Comment

Enables you to provide comments for this constraint.

See Also

Specifying maximum delay constraint

Set Minimum Delay Constraint Dialog Box

Use this dialog box to specify the required minimum delay for timing paths in the current design.

SmartTime automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. So the minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

To open the **Set Minimum Delay Constraint** dialog box (shown below) from the SmartTime Constraints Editor, click the **Constraints menu** and choose **Min Delay** (**Constraints > Min Delay**).

Set Minimum Delay Constraint				×
Minimum delay:	ns			
From:				
Through:			>	
			~	
To:				
3				
Comment:				
Help		ОК	Can	cel

Figure 84 · Set Minimum Delay Constraint Dialog Box



Minimum Delay

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

From

Specifies the starting points for minimum delay constraint. A valid timing starting point is a clock, a primary input, an input port, or a clock pin of a sequential cell.

Through

Specifies the through points for the multiple cycle constraint.

То

Specifies the ending points for minimum delay constraint. A valid timing ending point is a clock, a primary output, an input port, or a data pin of a sequential cell.

Comment

Enables you to provide comments for this constraint.

See Also

Specifying minimum delay constraint

Set Multicycle Constraint Dialog Box

Use this dialog box to specify the paths that take multiple clock cycles in the current design.

Setting the multiple-cycle paths constraint overrides the single-cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks.

Note: When multiple timing constraints are set on the same timing path, the false path constraint has the highest priority and always takes precedence over multiple cycle path constraint. A specific maximum delay constraint overrides a general multicycle path constraint.

To open the **Set Multicycle Constraint** dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraint> Multicycle**.



Set Multicycle Constraint	
Specify multiplier(s) for: Setup Check only Setup Path Multiplier:	New setup edge
From:	···
د To:	▲
	····
Comment:	
Help OK	Cancel

Figure 85 · Set Multicycle Constraint Dialog Box

Setup Path Multiplier

Specifies an integer value that represents a number of cycles the data path must have for a setup check. No hold check will be performed.

From

Specifies the starting points for the multiple cycle constraint. A valid timing starting point is a clock, a primary input, an inout port, or the clock pin of a sequential cell.



Through

Specifies the through points for the multiple cycle constraint.

То

Specifies the ending points for the multiple cycle constraint. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Comment

Enables you to provide comments for this constraint.

When you select the Setup and Hold Checks option, an additional field appears in this dialog box: **Hold Path Multiplier**.



et Multicycle Constraint	×
Specify multiplier(s) for: © Setup Check only © Setup and Hold Checks Setup Path Multiplier: Default setup edge Hold edge Hold Path Multiplier: 0	New setup edge
From:	
Through:	
Comment: Help OK (Cancel

Figure 86 · Set Multicycle Constraint Dialog Box with Setup and Hold Checks Selected

Hold Path Multiplier

Specifies an integer value that represents a number of cycles the data path must have for a hold check, starting from one cycle before the setup check edge.

See Also

Specifying multicycle constraint



Add Output Delay Constraint Dialog Box

Use this dialog box to apply output delay constraints. This constraint defines the output delay of an output relative to a clock.

To open the **Set Output Delay Constraint** dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Output Delay**.

Clock-to-Output

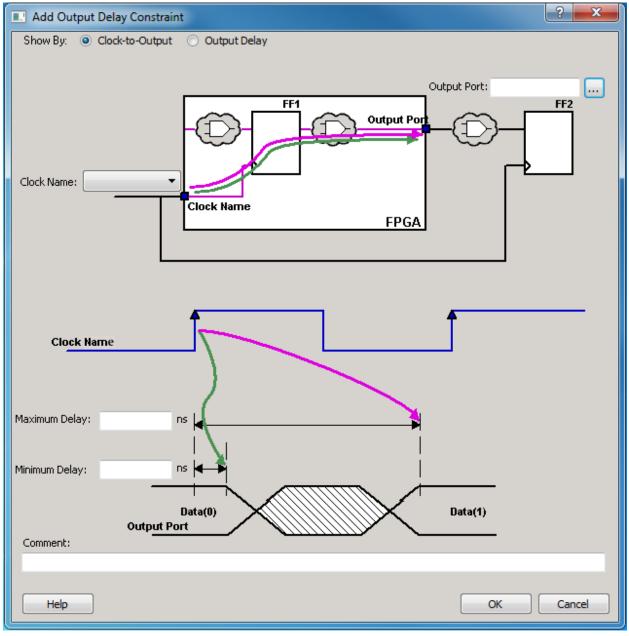


Figure 87 · Add Output Delay (Show By: Clock-to-Output) Dialog Box

Output Port

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.



Clock Name

Specifies the clock reference to which the specified **Clock-to-Output** is related.

Maximum Delay

Specifies the delay for the longest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

Minimum Delay

Specifies the delay for the shortest path from the clock port to the output port. This constraint includes the combinational path delay from output of the launched edge to the output port.

Comment

Enables you to provide comments for this constraint.



Output Delay

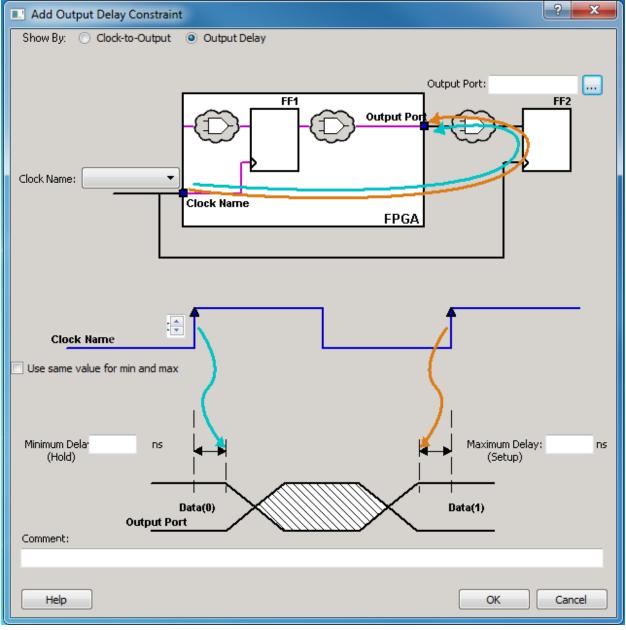


Figure 88 · Add Output Delay (Show By: Output Delay) Dialog Box

Output Port

Specifies a list of output ports in the current design to which the constraint is assigned. You can apply more than one port.

Clock Name

Specifies the clock reference to which the specified output delay is related.

Maximum Delay

Specifies the delay for the longest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library setup time.



Minimum Delay

Specifies the delay for the shortest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library hold time.

Comment

Enables you to provide comments for this constraint.

See Also

Specifying output timing delay constraint

SmartTime Options Dialog Box

Use this dialog box to specify the SmartTime options to perform timing analysis.

This interface includes the following categories:

- General
- Analysis View
- Advanced

To open the **SmartTime Options** dialog box (shown below) from the SmartTime tool, choose **Tools > Options**.

General

SmartTime Options	? <u>* × * * * * * * * * * * * * * * * * * </u>
Option Categories Select a category: General Analysis Advanced	General Operating Conditions Perform maximum delay analysis based on WORST • case Perform minimum delay analysis based on BEST • case Clock Domains Include inter-clock domains in calculations for timing analysis. Include inter-clock domains in calculations for timing analysis. Enable recovery and removal checks.
Help	OK Cancel

Figure 89 · SmartTime Options - General Dialog Box

Operating Conditions

Allows you to perform maximum or minimum delay analysis based on the Best, Typical, or Worst case. By default, maximum delay analysis is based on WORST case and minimum delay analysis is based on BEST case.



Clock Domains

- Include inter-clock domains in calculations for timing analysis: Enables you to specify if SmartTime must use inter-clock domains in calculations for timing analysis. By default, this option is unchecked.
- Enable recovery and removal checks: Enables SmartTime to check removal and recovery time on asynchronous signals. Additional sets are created in each clock domain in Analysis View to report the corresponding paths.

Restore Defaults

Resets all the options in the General panel to their default values.

Analysis

SmartTime Options		? ×
Option Categories Select a category: General Analysis Advanced	Analysis View Display of Paths Limit the number of paths shown in a path set to: Filter the paths by slack value Slack range from: Ns to: Show dock network details in expanded path Limit the number of parallel paths in expanded path to:	100 ns
Help		Restore Defaults OK Cancel

Figure 90 · SmartTime Options - Analysis View Dialog Box

Display of Paths

Limits the number of paths shown in a path set for timing analysis. The default value is 100. You must specify a number greater than 1.

Filter the paths by slack value

Specifies the slack range between minimum slack and maximum slack. This option is unchecked by default.

Show clock network details in expanded path

Displays the clock network details as well as the data path details in the Expanded Path views.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime displays. The default number of parallel paths is 1.

Restore Defaults

Resets all the options in the Analysis View panel to their default values.



Advanced

SmartTime Options		? <mark>×</mark>
Option Categories Select a category: General Analysis Advanced	Advanced Special Situtations Use loopback in bi-directional buffers(bibufs) Break paths at asynchronous pins Disable non-unate arcs in clock network Scenarios Use this scenario for timing analysis : Use this scenario for timing-driven place-and-route:	Primary Primary
Help		Restore Defaults OK Cancel

Figure 91 · SmartTime Options - Advanced Dialog Box

Special Situations

Enables you to specify if you need to use loopback in bi-directional buffers (bibufs) and/or break paths at asynchronous pins.

Scenarios

Enables you to select the scenario to use for timing analysis and for timing-driven place-and-route.

Restore Defaults

Resets all the options in the Analysis View panel to their default values.

Create Filter Set Dialog Box

Use this dialog box to specify a filter.

To open the **Create Filter Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, select a path and click the **Store Filter** button in the Analysis View Filter.



Create Filter Set		? <mark>×</mark>
Name i nu filiant		
Name : my_filter01		
Help	ОК	Cancel

Figure 92 · Create Filter Set Dialog Box

Name

Specifies the name of the filtered set.

See Also

Using filters



Timing Bottleneck Analysis Options Dialog Box

Use this dialog box to customize the timing bottleneck report.

You can set report bottleneck options for the following categories:

- General pane
- Bottleneck pane
- Sets pane

To open the **Timing Bottleneck Analysis Options** dialog box (shown below) from the SmartTime tool, choose **Tools > Bottleneck Analysis**.

General Pane

Timing Bottleneck Analysis Option	IS ?	x
Option Categories Select a category: General Bottleneck Sets	General Slack Maximum slack to include 0 ns	
Help	Restore Defaults OK Cancel]

Figure 93 · Timing Bottleneck Report - General Pane Dialog Box

Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

Restore Defaults

Resets all the options in the General pane to their default values.



Timing Bottleneck Analysis Options		? ×
Option Categories Select a category:	Bottleneck options	
General Bottleneck	Cost Type:	Path Count 👻
Sets	Limit the number of paths per section to:	100
	Limit the number of parallel paths per section to:	1
	Limit the number of reported instances to:	10
		Restore Defaults
Help		OK Cancel

Bottleneck Pane

Figure 94 · Timing Bottleneck Report - Bottleneck Pane Dialog Box

Bottleneck Options

Cost Type: Select the cost type that SmartTime will include in the bottleneck report.

You may select one of the following two items from the drop-down list:

- **Path count:** This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance. This is the default.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Limit the number of reported paths per section to: Specify the maximum number of paths per set type that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of parallel paths per section to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. Only cells that lie on these violating paths are reported. The default number of parallel paths is 1.

Limit the number of reported instances to: Specify the maximum number of cells that SmartTime will include per section in the report. The default number of cells is 10.

Restore Defaults

Resets all the options in the Bottleneck panel to their default values.



Sets Pane

Option Categories Select a category: General Bottleneck Sets	Bottleneck options Set Selection Entire design Clock Domain Clock: Type: Type: Use existing user set Name: my_set Use Input to Output Set Filter From: To:
Help	Restore Defaults OK Cancel

Figure 95 \cdot Timing Bottleneck Report - Sets Pane Dialog Box

This pane has four mutually exclusive options:

- Entire Design
- Clock Domain
- Use existing user set
- Use Input to Output Set

Entire Design: Select this option to display the bottleneck information for the entire design.

Clock Domain: Select this option to display the bottleneck information for the selected clock domain. You can specify the following options:

- Clock: Allows pruning based on a given clock domains. Only cells that lie on these violating paths are reported.
- Type: This option can only be used in conjunction with -clock. The acceptable values are:

Value	Description
Register to Register	Paths between registers in the design
Asynchronous to Register	Paths from asynchronous pins to registers
Register to Asynchronous	Paths from registers to asynchronous pins
External Recovery	The set of paths from inputs to asynchronous pins
External Setup	Paths from input ports to register
Clock to Output	Paths from registers to output ports



Use existing user set: Displays the bottleneck information for the existing user set selected. Only paths that lie within the name set are will be considered towards the bottleneck report.

Filter: Allows you to filter the bottleneck report by the following options:

- From: Reports only cells that lie on violating paths that start at locations specified by this option.
- To: Reports only cells that lie on violating paths that end at locations specified by this option.

Filter defaults to all outputs.

Restore Defaults

Resets all the options in the Paths panel to their default values.

See Also

Performing a bottleneck analysis

Timing Datasheet Report Options Dialog Box

Use this dialog box to select the output format for your timing datasheet report.

To open the **Timing Datasheet Report Options** dialog box (shown below) from the SmartTime Max/Min Delay Analaysis View, choose **Tools > Report S > Report Datasheet**.

DataSheet Report Options	? * *
Option Categories Select a category: General	General Format Plain Text Comma Separated Values Edit generated XML file name Edit generated XML file name
Help	OK Cancel

Figure 96 · DataSheet Report Options Dialog Box

You can generate your report in one of two formats:

Plain Text

Select this option to save your report to disk in plain ASCII text format.

Comma Separated Values

Select this option to save your report to disk in comma-separated value format (.CSV) format, which you can import into a spreadsheet

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Restore Defaults

Resets the option to its default value, which is Plain Text.

See Also

Generating a datasheet report Understanding datasheet reports report (Datasheet) using SmartTime

Timing Report Options Dialog Box

Use this dialog box to customize the timing report.

You can set report options for the following categories:

- General
- Paths
- <u>Sets</u>
- Clock Domains

To open the **Timing Report Options** dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Timer**.

General

Timing Report Options	? <mark>×</mark>
Option Categories Select a category: General Paths Sets Clock Domains	General Format Plain Text Edit generated XML file name Summary Include a summary of timing results in this report Slack Filter paths by slack threshold Maximum slack to include 0
Help	Restore Defaults OK Cancel

Figure 97 · Timing Report Options - General Dialog Box

Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

Summary

Specifies whether or not the summary section will be included in the report. By default, this option is selected.



Analysis

Specifies the type of analysis to be included in the timing report. It can be either a Maximum Delay Analysis report or Minimum Delay Analysis report. By default, the Maximum Delay Analysis report is included in the timing report.

Slack

Specifies whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default, the paths are not filtered by slack.

Restore Defaults

Resets all the options in the General panel to their default values.

Paths

Timing Report Options	
Option Categories Select a category: General Paths Sets Clock Domains	Paths Display of paths Include detailed path information in this report Limit the number of reported paths per section to: 1 Limit the number of expanded paths per section to: 1 Limit the number of parallel paths in expanded path to: 1 Restore Defaults
Help	OK Cancel

Figure 98 · Timing Report Options - Paths Dialog Box

Display of Paths

Include detailed path information in this report: Check this box to include the detailed path information in the timing report.

Limit the number of reported paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

Restore Defaults

Resets all the options in the Paths panel to their default values.



Sets

Timing Report Options		X
Option Categories - Select a category: - General - Paths - Sets - Clock Domains	Display of Sets Include user sets in this report Include Input to Output sets in this report	ults
Help	OK Cancel	

Figure 99 · Timing Report Options - Sets Dialog Box

Display of Sets

Specifies whether or not the user sets will be included in the timing report.

User sets are either filters that you have created and stored on the default paths sets (Register to Register, Inputs to Register, etc.) or Pin to Pin user sets. By default, the paths for these sets are not reported. In addition, specify whether the Inputs to Output sets will be included in the report. By default, the Input to Output sets are reported.

Restore Defaults

Resets both options in the Sets panel to their default values.



Clock Domains

Timing Report Options	×
Option Categories	Clock Domains
⊡ Select a category: —General —Paths —Sets —Glock Domains	Display of Clock Domains Include clock domains Limit reporting on clock domains to specified domains CLK PLL_CLK ULEDLS_BLOCK/U[1]_count[1]:C ULEDLS_BLOCK/U[2]_count[2]:C ULEDLS_BLOCK/U[2]_count[2]:C ULEDLS_BLOCK/U[3]_count[3]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6]:Count[6]:C ULEDLS_BLOCK/U[6]_count[6]:C ULEDLS_BLOCK/U[6
	Restore Defaults
Help	OK Cancel

Figure 100 · Timing Report Options - Clock Domains Dialog Box

Display of Clock Domains

Lets you specify what clock domains will be included in the report. By default, the current clock domains used by the timing engine will be reported.

Include Clock Domains

Enables you to include or exclude clock domains in the report. Click the checkbox to include clock domains.

Limit reporting on clock domains to specified domains

Lets you include one or more of the clock domain names in the box, or include additional clock domain names using **Select Domains**.

Restore Defaults

Resets all options in the Clock Domains panel to their default values.

See Also

Generating timing report Understanding timing report report (Timing) using SmartTime

Timing Violations Report Options Dialog Box

Use this dialog box to customize the timing violation report.

You can set report violation options for the following categories:

- General
- Paths



To open the **Timing Report Options** dialog box (shown below) from the SmartTime tool, choose **Tools > Report > Report Violations**.

General

Timing Violations Report Options	-? <mark>-</mark> *	
Option Categories Select a category: General Paths	General Format Plain Text Edit generated XML file name Slack Filter paths by slack threshold Maximum slack to include 0 ns Restore Defaults	
Help	OK Cancel	

Figure 101 · Timing Violations Report - General Dialog Box

Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

Restore Defaults

Resets all the options in the General panel to their default values.



Paths

II Timing Violations Report Options		? ×
Option Categories Select a category:	Display of paths	
General Paths	$\boxed{\ensuremath{\mathcal{V}}}$ Limit the number of reported paths	
	Limit the number of paths per section to:	100
	Limit the number of expanded paths per section to:	0
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults
Help		OK Cancel

Figure 102 · Timing Violations Report - Paths Dialog Box

Display of paths

Limit the number of reported paths: Check this box to limit the number of paths in the report. By default, the number of paths is limited.

Limit the number of reported paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report. The default number of expanded paths is 0.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

Restore Defaults

Resets all the options in the Paths panel to their default values.

See Also

Generating timing violation report Understanding timing violation report report (Timing violations) using SmartTime



Menus, Tools, and Shortcut Keys

File Menu

This menu is available in both Timing Constraint Editor View and Timing Min/Max Delay Analysis View.

Command	lcon	Shortcut	Function		
Save	1	CTRL + S	Save your changes.		
Print Preview			Displays the active design in a Preview window		
Print		CTRL + P	Displays the Print dialog box from which you can print your active design		
Close			Close the Constraint Editor or the Max/Min Delay Analaysis View Window		
Exit			Closes SmartTime		

Edit Menu

This menu is available in both Timing Constraint Editor View and Max/Min Delay Analysis View.

Command	lcon	Shortcut	Function
Undo	ŝ	CTRL + Z	Reverses your last action
Redo	٦ <u>ا</u>	CTRL + Y	Reverses the action of your last Undo command
Сору		CTRL + C	Copies the selection to the Clipboard

View Menu

This menu is available in the Timing Constraint Editor View and Max/Min Delay Analysis View.

Command	lcon	Shortcut	Function
Recalculate All	Q	F9	Recalculates all the generated values
Status Bar			Shows or hides the status bar at the bottom of the window
Scenarios			Shows or hides the scenarios panel



Available in the Max/Min Delay Analysis View

Command	lcon	Shortcut	Function
Customize Table			Enables you to select columns and the order of the columns for the Paths List in the Timing Analysis View

Constraints Menu

This menu is available from the Constraints Editor.

Command	lcon	Shortcut	Function
Clock	m		Displays the Create Clock Constraint dialog box
Generated Clock	MA		Displays the Create Generated Clock Constraint dialog box
Input Delay	% ⊠ ≯		Displays the Set Input Delay Constraint dialog box
Output Delay	₩2		Displays the Set Output Delay Constraint dialog box
Max Delay	×		Displays the Set Maximum Delay Constraint dialog box
Min Delay	\gtrsim		Displays the Set Minimum Delay Constraint dialog box
False Path	0		Displays the Set False Path Constraint dialog box
Multicycle	% N 		Displays the Set Mulitcycle Constraint dialog box
Clock Source Latency	fs.		Displays the Set Clock Source Latency dialog box
Disable Timing	5		Displays the Set Constraint to Disable Timing Arcs dialog box
Clock to Clock Uncertainty	11		Displays the Set Clock-to-Clock Uncertainty dialog box

Available in the Max/Min Delay Analysis View

Command	lcon	Shortcut	Function
Clock Domain	٩		Displays Manage Clock Domain dialog box



Command	lcon	Shortcut	Function
Path Set	К		Displays Add Path Analysis Set dialog box

Constraints Editor Tools Menu Items

This menu is available in the Timing Constraint Editor View and Max/Min Delay Analysis View.

Command	lcon	Shortcut	Function
Constraints Editor >	3		Displays the Constraints Editor
Maximum Delay Analysis	1		Displays the Maximum Delay Analysis View
Minimum Delay Analysis	\checkmark		Displays the Minimum Delay Analysis View
Constraint Wizard	3		Opens the Constraint Wizard for creating clock and I/O constraints
Scenario			To create new scenario and switch between scenarios

Constraints Editor > Tools > Scenario

Command	lcon	Shortcut	Function
Primary Scenario (and all other available scenarios)			Displays the primary set of timing constraints for the selected scenario
Scenarios			Opens the scenario panel, which lists all available scenarios
New scenarios			Creates a new scenario

Max/Min Delay Analysis View Tools Menu Items

Command	lcon	Shortcut	Function
Constraints Editor	3		Displays the Constraints Editor
Maximum Delay Analysis	M		Displays the Maximum Delay Analysis View
Minimum Delay Analysis	\leq		Displays the Minimum Delay Analysis View
Bottleneck Analysis			Displays the Bottleneck Analysis View



Command	lcon	Shortcut	Function
Options			Displays the SmartTime Options
Reports			Displays various reports: • Timer • Timer Violation • Bottleneck • Datasheet • Constraints Coverage • Combinational Loops

Max/Min Delay Analysis View Tools > Reports Menu Items

Command	lcon	Shortcut	Function	
Timer			Displays the Timing Report Options dialog box	
Timing Violations			Displays the Timing Violations Report Options dialog box	
Datasheet			Displays the Datasheet Report Options dialog box	
Constraints Coverage			Displays the Constraints Coverage Report Options dialog box	
Combinational Loops			Displays the Combinational Loops Report Options dialog box	

Help Menu

This menu is available in both Timing Constraint Editor View and Timing Analysis View.

Command	Function
Help Topics	Displays the first Help topic for the SmartTime tool
SmartTime User's Guide	Displays the SmartTime User's Guide
About SmartTime	Displays the current version number and copyright information for the SmartTime tool
Data Change History	Displays features and enhancements, bug fixes and known issues for the current software release that may impact timing data of the current design

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



SmartTime Toolbar

The SmartTime toolbar contains commands for constraining or analyzing designs. Tool tips are available for each button.

lcon	Description
2	Undoes previous changes
<u>C</u>	Redoes previous changes
\geq	Opens the maximum delay analysis view
	Opens the minimum delay analysis view
<u>@</u>	Opens the manage clock domains manager
X	Opens the path set manager
8	Recalculates all
27	Opens the constraints editor
ň	Opens the create clock constraint dialog box
to.	Opens the created 1generated clock constraint dialog box
*** **	Opens the Add input delay clock constraint dialog box
₩2	Opens the Add output delay clock constraint dialog box
	Opens the set false path constraint dialog box
*	Opens the set maximum delay constraint dialog box
2	Opens the set minimum delay constraint dialog box
<u>M</u>	Opens the set multicycle constraint dialog box
<u>F</u>	Opens the set clock source latency dialog box
1	Opens the set constraint to disable timing arcs dialog box



NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.

lcon	Description		
<u>š</u>	Opens the set clock-to-clock uncertainty constraint dialog box		
<u>B</u>	Opens the constraint wizard		



Data Change History - SmartTime

The data change history lists features, enhancements and bug fixes for the current software release that may impact timing data of the current design.

To generate a data change history, from the **Help** menu, choose **Data Change History**. This opens a data change history in text format.

Data Change History Report	- 0 - X
File Actions Help	
SmartTime Data Change History	
Family: SmartFusion2/IGL002	
Die: M2S050T/M2S050/M2GL050T/M2GL050	
Data source: Production	
Libero 11.5	
59832 - Add new I/O standard sub-LVDS	
59410 - Update values of input programming delays	
59143 - Timing data (MIL) updated from advanced to production	
62008 - Update shadowseq timing delays	
Libero 11.4 SP1	
60089 - Update MSS temperature/voltage derating factors	
58112 - Update Mini-LVDS outdrive strength	
58113 - Update M/B-LVDS outdrive strength	
59410 - Update values of input programming delays	
Libero 11.4	
58678 - Add MPW timing arcs in IOPAD timing model	
58677 - Update Serdes block timing model	
58675 - Update MSS block timing model	
58676 - Update FDDE block timing model	
Libero 11.3	
51895 - Change data state to "production" to align with datasheet	
55478 - Change URAM FMAX to 250MHz	
54138 - Change URAM timing model with new data	
Libero 11.2	
50923 - Timing data (IND/COM) updated from advanced to production	

Figure 103 · SmartTime Data Change History Report

SmartTime Tutorial - Libero SoC for SmartFusion2/IGLOO2/RTG4

The following tutorials explore common SmartTime features with example designs:

Tutorial 1 - 32-Bit Shift Register with Clock Enable

Goal: Learn how to apply a clock constraint, perform maximum delay analysis and minimum delay analysis. Also, use the feature to dynamically update timing analysis by changing constraints in the constraints editor.

Tutorial 2 - Count16 Counter

Goal: Import timing constraints file (SDC)/Add Clock Constraint, add input delay and output delay constraints. Create filters and user sets to isolate design paths for analysis in SmartTime.

Tutorial 3 - Design Using Both Clock Edges

Goal: Learn how to apply a clock constraint, perform maximum delay analysis for a design using both edges of the clock (rising & falling). Generate a custom timing report using SmartTime.

Tutorial 4 - False Path Constraints

Goal: Add false path constraints to identify non-timing critical design paths.

Tutorial 5 - Cross Clock Domain Analysis

Goal: Analyze the timing results for a design with cross clock domain paths.

Many actions described in the tutorials can be performed from the menus or in the SmartTime Toolbar. The table below lists all the SmartTime Toolbar actions.

SmartTime Toolbar

lcon	Description		
	Save the Changes		
<u>1</u>	Undoes previous changes		
CI	Redoes previous changes		
>	Opens the maximum delay analysis view		
×	Opens the minimum delay analysis view		



<u>@</u>	Opens the manage clock domains manager
X	Opens the path set manager
2	Recalculates all
37	Opens the constraints editor
m	Opens the create clock constraint dialog box
-	Opens the create generated clock constraint dialog box
	Opens the set input delay clock constraint dialog box
× ₩Ø	Opens the set output delay clock constraint dialog box
	Opens the set false path constraint dialog box
<u>×</u>	Opens the set maximum delay constraint dialog box
2	Opens the set minimum delay constraint dialog box
<u>M</u>	Opens the set multicycle constraint dialog box
(fr	Opens the set clock source latency dialog box
<u>a</u>	Opens the set constraint to disable timing arcs dialog box
<u></u>	Opens the set clock-to-clock uncertainty constraint dialog box
3	Opens the constraint wizard



Tutorial 1 - 32-Bit Shift Register with Clock Enable

This tutorial describes how to enter a clock constraint for the 32-bit shift register shown. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

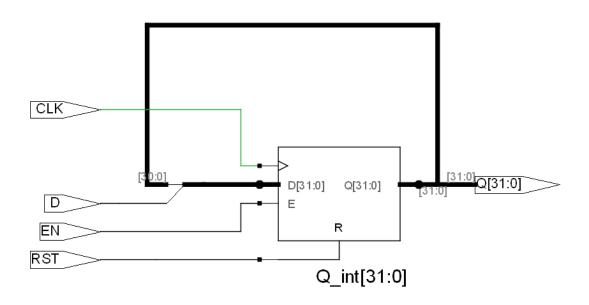


Figure 104 · 32-bit Shift Register

Set up your project

- 1. Invoke Libero SoC. From the Project menu choose New Project.
- 2. Enter shift32 for your new project name and browse to a folder for your project location.
- 3. Select Verilog as the Preferred HDL Type.
- 4. Leave all other settings at their default values.



New project			
Project details Specify project details			
Project Details	Project name:	sf2_shfit32	
Device Selection	Project location: Description:	d. \actelprj	Browse
Device Settings			
Design Template	Preferred HDL type		
Add HDL Sources			
Add Constraints			
Liberoor Chip			
Help		< Back Next > Finis	Cancel

Figure 105 · New Project Creation - 32 Bit Shift Register

- 5. Click Next to go to Device Selection page. Make the following selection from the pull-down menu:
 - Family: SmartFusion2
 - Die: M2S090TS
 - Package: 484FBGA
 - Speed:STD
 - Core Voltage: 1.2 V
 - Range: COM
- 6. Click the M2S090TS-1FG484 part number and click Next.

New project Device selection Select a part for your project	t from the part number list		illine (illi		and heads		Selected part: M2	5090TS-1FG48
Project Details	Part filter Family: SmartFusi Speed: -1	on2	Die: Core voltage:	M2S090TS	▼ Packa	age: 484 FBGA	T	
Device Settings	Search part:	4LUT	DFF	User I/Os	uSRAM 1K	Res LSRAM 18K	et filters Math (18x18)	PLLs and
Design Template	M2S090TS-1FG484	86184	86184	267	112	109	84	6
Add HDL Sources								
	٠							4
Help						Back Next	> Finish	Cancel



- 7. Accept the default settings in the Device Settings page and click Next.
- 8. Accept the default settings in the Design Template page and click Next.
- 9. In the Add HDL sources page, click Import file to import the source file, Navigate to the location of the source Verilog file for the 32-bit shift register you have downloaded from the Microsemi website. Click to select the source file and click Open. After project creation, the source Verilog file you import will appear in the project's hdl folder under the File tab.

📀 New project			
Add HDL source files Specify HDL files to import/link	s to your project.		Selected part: M2S090TS-1FG484
Project Details	Import file Link file		Delete
	File type	File name	File location
Device Selection	Imported	shift_reg32.v	D:/shift_reg32/hdl
Device Settings			
Design Template			
Add HDL Sources			
Add Constraints			
Libero			
Help		<	Back Next > Finish Cancel

- 10. Click Next to go to the Add Constraints Page.
- 11. We are not adding any constraints. Click **Finish** to exit the New Project Creation wizard.
- 12. After you have created the project, confirm that the imported Verilog source file appears in the Files window (as shown in the figure below).



Files	
component	
▷ 🗀 constraint	
🖻 🗀 designer	
🔺 🗀 hdl	
B shift_reg32.v	
imulation	
🗀 smartgen	
🗀 stimulus	
Synthesis	
🖻 🗀 tooldata	
-	

- Figure 106 · HDL File shift_reg32.v in the Libero SoC File Window
- 13. Confirm that the shift_reg32 design appears in the Design Hierarchy window (as shown in the figure below).



	Hierarchy				
Show:	Components 🔻				
4	🖉 work				
	🗎 shift_reg	32 (shift_reg3	32.v)		
		III		1	•

Figure 107 · shift_reg32 in the Design Hierarchy Window

- In the Design Flow window, double-click Synthesize to run Synplify Pro with default settings.
 A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
- Double-click **Compile** in the Design Flow window to run Compile with default settings.
 A green check mark appears next to Compile when it completes successfully (as shown in the figure below).



Project File Edit View Design Tools Help					
🗋 🚰 🖳 😂 🧇 🖸 🗿 📿					
esign Flow 🗗 🗙	StartPage 🗗 🗙	Reports 🗗 ×			
shift_reg32 Tool Tool Yerify Pre-Synthesized Design Simulate You Constraints Timing Constraints Timing Constraints Timing Constraints Timing Constraints You Constraints You Configure Flash*Freeze Design Hie Desig Stimulus Hie Catalog g Messages From Marines Stimulus Hie Catalog g Messages From Marines The 'set_compile_info' command succeeded The 'set_compile_info' command su	shift_re Synthesize Synthesize Synthesize Synthesize Synthesize Synthesize Synthesize Synthesize Shift_re	2 332_pinrpt 332_pinrpt the 332_pinrpt the the 332_pinrpt the the the 332_pinrpt the the the the the the the the	All 0 trons 0 warnin 'set_compile_info'	command succeeded command succeeded.	1. 1. 1. 1. 1. 1. 1. 1. 1. 1.
The 'set_compile_info' command succeede The 'set_compile_info' command succeede The 'set_compile_info' command succeede The 'set_compile_info' command succeede OINFO: No User PDC file(s) was specifi	ed. ed.				
The 'compile' command succeeded. The Execute Script command succeeded.					-

Figure 108 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

Add a Clock Constraint - 32 Bit Shift Register Example

To add a clock constraint to your design:

1. In the **Design Flow** window, expand **Edit Constraints** and double-click **Timing Constraints** to open the Constraints Editor (as shown in the figure below).



SmartTime - [Constraints Editor for scen	nario P	rimary]											x
File Edit View Constraints Too	ls H	elp										-	. 8 ×
🔚 🖉 💊 📦 🛶 🖉 🗠 🖉	e Ne	<u>*.</u> *_	4 <u>4</u> 4 <u>4</u>	4N 5A	(h. 19. 1								
🖸 Constraints Editor for scenario Primary 📃 🖂													
Constraints Editor for scenario Primary													
,													
✓ Constraints			Clock	Clock	Period	F	D. L		Offset				-
A Requirements		Syntax	Name	Source	(ns)	Frequency (MHz)	Dutycycle (%)	First Edge	(ns)	Waveform	File	Comment	5
Clock	-						() · · · /						-
Generated Clock	1	Click here to	add a constr	raint									
Input Delay													
Output Delay													
 Exceptions 													
Max Delay													
Min Delay													
Multicycle													
False Path													
 Advanced Clock Source Latency 													
Disable Timing													
Clock Uncertainity													
Clock Uncertainity													
<		1											•
		•											
	_												
										Temp: 0	- 85 C Vol	:: 1.14 - 1.26 V Speed	: -1

Figure 109 · SmartTime Constraints Editor

2. In the left pane, under Constraints > Requirements, right-click Clock and choose **Add Clock Constraint** to open the Create Clock Constraint dialog box (as shown in the figure below).

Create Clock Constraint		? X
Clock Name : my_clk	Clock Source : CLK	▼ …
Period	ns — or Frequenc	C Mhz
← Offset : → ← Duty cycle → 0.000 ns 50.0000 %		
Comment : Help	ОК	Cancel

Figure 110 · Create Clock Constraint Dialog Box

- 3. From the Clock Source dropdown menu choose the CLK pin.
- 4. Enter my_clk in the Clock Name field.
- 5. Set the **Frequency** to 800 **MHz** (as shown in the figure below) and leave all other values at the default setting. Click **OK** to continue.



Create Clock Constraint		? ×
Clock Name : my_clk	Clock Source :	•
Period : 1.25	ns	00 Mhz
← Offset : → ► Duty cycle : →		
0.000 ns 50.0000 %		
Comment :		
Help	ОК	Cancel

Figure 111 · Add a 800 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).

Constraints 🔺			Clock	Clock	Period	Frequency	Dutycycle	First Edge	Offset		File	<i>c</i>
A Requirements		Syntax	Name	Source	(ns)	(MHz)	(%)	First Edge	(ns)	Waveform	File	Comments
Clock												
Generated Clock	1	Click here to add a	a constraint									
Input Delay	2	1	my_clk	CLK	1.250	800.000	50.0000	rising 🚽	0.000	0 0.625	GUI	
Output Delay =												
A Exceptions												
Max Delay												
Min Delay												
Multicycle												
False Path												
Advanced												
Clock Source Latency +												
4 III	1											

Figure 112 · 800 MHz Clock Constraint in the Constraint Editor

- 6. From the **File** menu choose **Save** to save the constraints.
- 7. From the SmartTime File menu choose Exit to exit SmartTime.

Run Place and Route

Constraints Editor for scenario Primary

- 1. Right-click Place and Route and choose Configure Options.
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.



Layout Options	? ×
Timing-driven	
Power-driven	
High Effort Layout	
📝 Repair Minimum Delay Violations	
Incremental Layout	
Use Multiple Passes	
Configure	
Неlp ОК	Cancel

Figure 113 · Layout Options

Double-click Place and Route inside the Design Flow window to start the Place and Route.
 A green check mark appears next to Place and Route after successful completion of Place and Route.

Maximum Delay Analysis with Timing Analyzer- 32-Bit Shift Register Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Right-click Verify Timing inside the Design Flow window and choose **Open Interactively** to open SmartTime. The Maximum Delay Analysis View window appears.

A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays:

- Maximum operating frequency for the design
- External setup and hold requirements
- Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 609.75 MHz.



e Ed	lit View Tools Help									-
2	🞦 😳 🏂 🍝 😢 🐵 🛪									
im Dela	y Analysis View									
2	Analysis for scenario Primary	Design		shift r	eq32					
AX		Family			Fusion2					
Summary ✓m my_clk		Die		M2S0						
	 Register to Register 	Package			BGA					
	External Setup			0 - 85						
	Clock to Output Register to Asynchronous	-			-					
Keguster to Asynchronous External Recovery Asynchronous to Register 4 次 Pin to Pin Input to Output ▼			5 5		1.26 V					
		Speed Grad		STD						
		Design Stat	е	Post-l	*					
		Data source		Produ	ction					
		Min Operati	Min Operating Conditions		- 1.26 V - 0 C					
1		Max Operat	Max Operating Conditions		ST - 1.14 V - 85 C					
		Scenario for	Scenario for Timing Analysis		ry					
of paths	Select a set of paths to see its slack distribution.	Summa	r y Period	Frequency	Required Perior	Required Frequency	External Setup	External Hold	Min Clock-To-Out	Max Clock Te Out
		Domain		(MHz)	(ns)	(MHz)	(ns)	(ns)	(ns)	(ns)
		my_clk	1.640	609.756	1.250	800.000	1.258	0.429	3.823	9.486
					ax Delay (ns)					
	slack distribution(ns)	Input to Out	put IN/A	N//	٩					

Figure 114 · Maximum Delay Analysis - Summary

- 2. Expand my_clk to display the Register to Register, External Setup and Clock to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.

Analysis for scenario Primary												
X '	Fro	m *					TO *					
୍ଡିଗ Summary	16	istomize table								Apply	Filter Store Filter	Reset Filter
⊿ v@ my_clk												
 Register to Register 								_		_		
External Setup		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required	Setup (ns)	Minimum Per	od o	ikew (ns)	
Clock to Output		Source I in	2008100	Delay (IIS)	Shick (iis)	,	(ns)	Secup (iis)	(ns)	-		
Register to Asynchronous	1	Q int[18]:CLK	Q int[19]:D	0.716	0.159	4.810	4.969	0.298	1.	091	0.077	
External Recovery												
Asynchronous to Register	2	Q_int[25]:CLK	Q_int[26]:D	0.704	0.164	4.809	4.973	0.298	1.	086	0.084	
4 🚟 Pin to Pin												
Input to Output	3	Q_int[11]:CLK	Q_int[12]:D	0.688	0.174	4.823	4.997	0.298	1.	076	0.090	
🔀 User Sets		1										
	4	Q_int[5]:CLK	Q_int[6]:D	0.712	0.177	4.832	5.009	0.298	1.	073	0.063	
		1							-			
	5	Q_int[7]:CLK	Q_int[8]:D	0,706	0,182	4.827	5.009	0.298	1/	068	0.064	
	l ľ	Condylacat	d Turdolin		0.102		0.000	0.200			0.001	
	6	Q_int[19]:CLK	Q_int[20]:D	0.701	0.219	4.777	4,996	0.298	1	031	0.032	
		Contrainers	6Tudfrolip	0.701	0.215			0.200			0.002	
	7	Q_int[26]:CLK	Q_int[27]:D	0.673	0.245	4.753	4,998	0.299	1	005	0.033	
30		Conception.	d index in	0.075	01210			0.200			0.000	-
				-				Mad		D.1 T.	1.0.1.01	
	Nar			Туре	Net			IVIac	cro U	p Delay lot	al Fanout Edge	
24	4	Summary								4.9		
		data required tim	e							4.9		
		data arrival time								4.8		
		slack								0.1	04	
18	4	Data_arrival_time_c	alculation							0.000 0.0	20	
		my_clk								0.000 0.0		=
		CLK		Clock source					+	0.000 0.0		
		CLK_ibuf/U0/U_I		net	CLK				+	0.000 0.0		
12		CLK_ibuf/U0/U_I		cell				ADL	.IB:IOPAD_IN +	2.128 2.1		
		CLK_ibuf_RNIVQ		net	CLK_ibut	f			+	0.197 2.3		
		CLK_ibuf_RNIVQ		cell				ADL	.IB:GBM +	0.105 2.4		
			4/U0_RGB1_RGB1:An		CLK_ibut	f_RNIVQ04/U0_\	YWn		+	0.691 3.1		_
6			4/U0_RGB1_RGB1:YL						.IB:RGB +	0.372 3.4		
ř i i i i i i i i i i i i i i i i i i i		Q_int[25]:CLK		net	CLK_ibut	f_RNIVQ04/U0_F	RGB1_RGB1_rgb		+	0.612 4.1		
		Q_int[25]:Q		cell				ADL	IB:SLE +			
		Q_int[26]:D		net	Q_c[25]				+	0.602 4.8		
		data arrival time								4.8	09	
	45 4	Data_required_time	_calculation									
0.0635 0.159 0.2545 0.35 0.4					int					1.250 1.2		

Figure 115 · SmartTime Register to Register Delay

4. Double-click a path row to open the **Expanded Path Window**. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).



Note: The Timing Numbers in these reports may vary slightly with different versions of the Libero Software and may not be exactly the same as what you will see when you run the tutorial.

🕒 Sma	rtTime - [Maximum Delay - Exp	oanded Path view :From: Q	_int[25]:CLK -> To: Q_int[26]:D]							- • ×
🍃 File	Edit View Tools Help									_ 8 ×
- u										
	🔄 📴 💱 🏂 🗲	8 🐵 🗵								
From: To: Q_	ary for path Q_int[25]:CLK int[26]:D Required Time (ns) Data Arri	val Time (ns) Slack (ns)							Path Profile Cel Delay 0.00%	
4.973		0.164								
	1		J							
l —										
Name		Туре	Net	Macro	Op	Delay Tot	al Fanout Edge	e		~
⊿ D	ata_arrival_time_calculation									
	my_clk					0.000 0.00	00			
	CLK	Clock source			+	0.000 0.0				E
	CLK_ibuf/U0/U_IOPAD:PAD	net	CLK		+	0.000 0.0				-
	CLK_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	2.128 2.1				
	CLK_ibuf_RNIVQ04:An	net	CLK_ibuf		+	0.197 2.3				
	CLK_ibuf_RNIVQ04:YWn	cell		ADLIB:GBM		0.105 2.4				
	CLK_ibuf_RNIVQ04/U0_RGB1		CLK_ibuf_RNIVQ04/U0_YWn			0.691 3.1				
	CLK_ibuf_RNIVQ04/U0_RGB1			ADLIB:RGB		0.372 3.4				
	Q_int[25]:CLK	net	CLK_ibuf_RNIVQ04/U0_RGB1_RGB1_rgbl_net_1			0.612 4.1				
	Q_int[25]:Q Q_int[26]:D	cell net	Q_c[25]	ADLIB:SLE		0.602 4.8				
	data arrival time	net	Q_c(25)		+	4.8				
	data anivai time					4.0	,9			*
	ακ[CLK buffU0 PAD IOPAU	Y An YEn	CLK_buf_RI	An ENn	04/U0_R YL YR		f_RNIVQ04/U0_RGB1_RGB2 An YL ENN YR RGB Q_int[25] ADn ALN CLK D Q EN LAT SD SLE	Q_int[26] - ADn - ALn - CLK - CLK - CLK - CLK - CL - EN - LAT - SD - SLE - SLE	*
•									Temp: 0 - 85 C Volt: 1.14 - 1.	.26 V Speed: STD

Figure 116 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 3**. The Input Arrival time from the EN pin to Q_int[27]:EN is 4.547ns (as shown in the figure below).



File E	dit View Tools Help													-
	: 🎦 📴 🏂 🖌 🖉 🐵 ≍ .													
num Dela	y Analysis View													
\frown	Analysis for scenario													
~	Primary	From *					то *							
MAX							10							
	ummary	Customize table								Apply I	Filter	Store Filt	er Reset	Filter
⊿ v	'@ my_clk				_	_		_						
	 Register to Register 		Sink F	. Delav	Slack	Arrival	Required	Setup	External					
	External Setup	Source Pin	Sink F	n (ns)	(ns)	(ns)	(ns)	(ns)	Setup (ns)					
	Clock to Output	1 EN	Q_int[31]:EN	4.54	17	4.547		0.399	1.258					
	Register to Asynchronous External Recovery													E
	Asynchronous to Register	2 EN	Q_int[30]:EN	4.54	17	4.547		0.399	1.248					1
4.3	T Pin to Pin													
	Input to Output	3 EN							1.248					
2	User Sets				-									
		4 EN	Q_int[29]:EN	4.54	17	4.547		0.399	1.248					
		5 EN	O int[28]:EN	4.54		4.547		0.399	1.248					-
			IO Intizolitin			4.547		0.399				_	_	
		Name		Туре	Net				Macro	Ор	Delay	Total Fa	nout Edge	
		✓ Summary												
		data required time										N/C		
1		data arrival time										4.547 N/C		
		slack Data_arrival_time_calcula	e									N/C		
		EN	uon								0.000	0.000	f	
		EN_ibuf/U0/U_IOPAD:F	AD	net	EN						0.000		÷.	
		EN_ibuf/U0/U_IOPAD:		cell					ADLIB:IOPAD IN	+	2.720		1 f	
		EN_ibuf/U0/U_IOINFF:		net	EN_ibuf/U)/YIN1				+	0.000		f	
		EN_ibuf/U0/U_IOINFF:		cell					ADLIB:IOINFF_BYP	ASS +	0.106	2.826	32 f	
		Q_int[27]:EN		net	EN_c					+	1.721	4.547	f	
	This set has no path.	data arrival time										4.547		
	ma accrua no puen.	4 Data_required_time_calculation	lation											
		my_clk									N/C			
		CLK		Clock source						+	0.000		r	
		CLK_ibuf/U0/U_IOPAD		net cell	CLK					+	0.000	N/C	r 2 r	
		CLK_ibuf/U0/U_IOPAD CLK ibuf RNIVQ04:An		net	CLK ibuf				ADLIB:IOPAD_IN	+	0.177		2 r f	
		CLK_ibuf_RNIVQ04;XII		cell	CEK_IDUI				ADLIB:GBM			N/C	5 f	
		CLK_ibuf_RNIVQ04/U0			CLK ibuf I	RNIVQ04/U0	YWn		Abtibiobili	+	0.623		f	
		CLK_ibuf_RNIVQ04/U0							ADLIB:RGB	+		N/C	5 r	
		Q_int[27]:CLK		net	CLK_ibuf_I	RNIVQ04/U0	_RGB1_RGB3_	rgbl_net_1		+	0.553	N/C	. r	
		Q_int[27]:EN		Library setup time					ADLIB:SLE		0.399	N/C		
	slack distribution(ns)													

Figure 117 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 1. The maximum clock to output time from Q_int[16]:CLK to Q[16] is 9.486ns.



	idit View Tools Help													-
um Dela	ay Analysis View													
2	Analysis for scenario													
AX	Primary	From	n *					то •	•					
8	Summary		stomize table								Apply Fil	ter S	tore Filter	leset Filter
4	∕™ my clk										1400111			
	✓ Register to Register													
	External Setup		Source Pin		ink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Clock to C	Out (ns)			
	Clock to Output						(113)		(113)					
	Register to Asynchronous	1											6	^
	External Recovery	2	o talinitari	ofurl		5.054		0.454				0.40		=
	Asynchronous to Register	2	Q_int[15]:CLK	Q[15]		5.354		9.461				9.46	1	
Din to Pin Input to Output			Q_int[28]:CLK	Q[28]		3.946		8.054				8.05		
			Q_Int[20]:CLK	Q[20]		3.940		0.054				0.03	1	
- 1	🔭 User Sets	4	Q_int[4]:CLK	Q[4]		3.817		7.937				7.93	17	
			Q_int[i].con	41.0		3.01/		1.557				7.55	"	-
		Nam			Type	Net				Macro	0.0		I Fanout Edg	
					туре	ivet				viacro	Up De	ay lota	Fanout Edg	e
		- 4 2	Summary									N/9	~	
			data required time data arrival time									9.48		
			slack									9.40 N/0		
			SIACK Data_arrival_time_calcul	Intion								14/4	-	
			my_clk	ation							0	00.0 000	0	
			CLK		Clock sour	rce						00.0 000		
			CLK_ibuf/U0/U_IOPA	Π-ΡΔΠ	net	CLK						00.0 000		
			CLK_ibuf/U0/U_IOPA		cell	CLIN			4	ADLIB:IOPAD_IN		128 2.12		
			CLK_ibuf_RNIVQ04:A		net	CLK ibuf					+ 0.	197 2.32	5 f	
			CLK_ibuf_RNIVQ04:Y		cell				4	ADLIB:GBM	+ 0.	105 2.43	0 5 f	
			CLK_ibuf_RNIVQ04/U			CLK ibuf	RNIVQ04	/U0 YWn			+ 0,	587 3.11	7 f	
			CLK_ibuf_RNIVQ04/U			-			4	ADLIB:RGB	+ 0.	372 3.48	9 8 r	
	This set has no path.		Q_int[16]:CLK	-	net	CLK_ibuf	RNIVQ04	U0_RGB1_RGB0	_rgbl_net_1		+ 0,	518 4.10	7 r	
			Q_int[16]:Q		cell					ADLIB:SLE		127 4.23		
			Q_obuf[16]/U0/U_I00	DUTFF:A	net	Q_c[16]					+ 1/	571 5.90	5 f	
			Q_obuf[16]/U0/U_IO0	OUTFF:Y	cell				A	ADLIB:IOOUTFF_BYPASS		403 6.30		
			Q_obuf[16]/U0/U_IOF		net	Q_obuf[1	6]/U0/DO	UT				000 6.30		
			Q_obuf[16]/U0/U_IOF	PAD:PAD	cell				A	ADLIB:IOPAD_TRI		178 9.48		
			Q[16]		net	Q[16]					+ 0.	000 9.48		
			data arrival time									9.48	6	
		4 [Data_required_time_cal	culation										
	L		my_clk									I/C N/0		
			CLK		Clock sour	rce					+ 0.	000 N/0		
	slack distribution(ns)		Q[16]									N/0	C f	

Figure 118 · SmartTime Clock to Output Path Analysis

Minimum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

1. From the SmartTime Constraints Editor **Tools** menu, choose **Minimum Delay Analysis**. The Minimum Delay Analysis View appears (as shown in the figure below).



🕒 SmartTin	ne - [Minimum Delay Analysis View]										- C - X		
🧲 File 🛛 Ec	lit View Tools Help										- 5		
i 📔 🔄	N 🖸 🖓 ≽ 🍝 🕫 🐵 🛪												
	y Analysis View												
	,,												
	Analysis for scenario												
min	Primary		Design			shift_reg32							
	Summary					SmartFusion2							
	/ my_clk					M2S090TS							
	✓ Register to Register External Hold Clock to Output =					484 FBGA							
				ure Range	e	0 - 85 C							
	Register to Asynchronous	-	Voltage R	ange		1.14 - 1.26 V		-					
	External Removal Asynchronous to Register			ade		STD							
4 :	Asynchronous to Register		Design St			Post-Layout							
	Input to Output		Data sour			Production							
•	••• u . c .				ditions	BEST - 1.26 V - 0	0						
			Min Opera	-									
			Max Operating Conditions			WORST - 1.14 V	- 85 C						
			Scenario for Timing Analysis		g Analysis	Primary							
	Select a set of paths to see		Summa										
# of paths			Clock Domain	Period (ns)	Frequent (MHz)	cy Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock- To-Out (ns)		
*			my_clk	1.640	609.756	1.250	800.000	1.258	0.429	3.823	9.486		
						ns) Max Delay (n	s)						
			Input to O	utput N/	A	N/A							
	slack distribution(ns)												
Ready									Temp:	0 - 85 C Volt: 1.14	- 1.26 V Speed: STD		

Figure 119 · SmartTime Minimum Delay Analysis View- Summary

- 2. Expand my_clk to display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Register path sets.
- 3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
- 4. Click to select the first path and observe the hold analysis calculation details (as shown in the figure below).



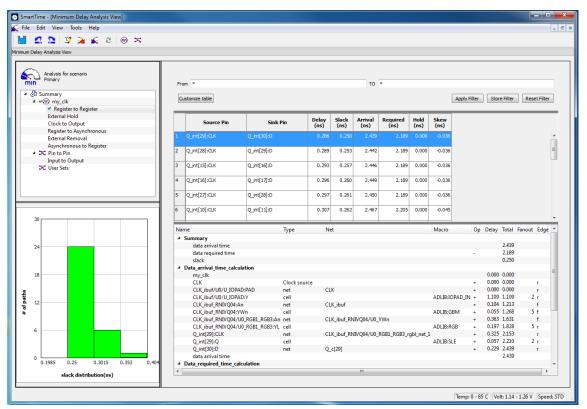


Figure 120 · SmartTime Minimum Delay Analysis

Changing Constraints and Observing Results - 32-Bit Shift Register Example

You can use SmartTime to adjust constraints and view the results in your design. To do so:

1. Open the SmartTime Constraints Editor (Tools > Constraints Editor).

The Constraints Editor displays the clock constraint at 800 MHz that you entered earlier (as shown in the figure below).

File Edit View Constrai				<u>%</u> % %	%	9 <u>%</u> 19						_
straints Editor for scenario Prima					- 141 44							
Constraints Requirements	^		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File
₹ Clock Generated Clock		1	Click here to add a	constraint								
Input Delay	-	2	٣	my_clk	CLK	1.250	800.000	50.0000	rising 👻	0.000	0 0.625	GUI
Output Delay	=								·			
4 Exceptions												
Max Delay Min Delay												
Multicycle												
False Path												
▲ Advanced												
Clock Source Late	nc) =											
٠ III	•		•									

Figure 121 · Clock Constraint Set to 800 MHz



- Select the second row. Right-click and select Edit Clock Constraint. This will open the Edit Clock Constraint dialog box. Change the clock constraint from 800 MHz to 1000 MHz and click the green check mark to continue.
- 3. From the **View** menu, choose **Recalculate All** to recalculate the delays using your new clock constraint.
- 4. From the Tools menu, choose Maximum Delay Analysis View to view the max delay analysis.
- 5. Expand my_clk in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the slacks decrease after you increase the frequency and recalculate. You may see the slacks go negative indicating Timing Violations. Negative slacks are shown in red.

Note: The actual timing numbers	s you see may be slightly different.
---------------------------------	--------------------------------------

m Delay Analysis View													
Analysis for scenario Primary	Fr						TO *						
🗟 Summary		ustomize table								G	looly Filter	Store Filter	Reset Filter
Kegister to Register	_										0.00		
External Setup							Required		finimum Perio	d			
Clock to Output		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	(ns)	Setup (ns)	(ns)		Skew (ns)		
Register to Asynchronous	1	Q_HI[18]:CLK	Q_int[19]:0	0.716	-0.091	4.810	4.719	0.298	1.0	91		0.077	
External Recovery Asynchronous to Register		and the second second	and the second					a de la composición d	199			- and the	
A Synchronous to Register	2	Q_ht[25]:C.K	Q_int[26]:D	0.704	-0.085	4.809	4.723	0.298	1.0	86		0.084	
Input to Output	3	Q_mt[11]:CLK	Q_mt[12]:D	0.688	-0.076	4.823	4.747	0.298	1.0	76		0.090	
PC ON SIL	4	Q_int[5]:CLK	Q_int[6]:D	0.712	-0.073	4.832	4.759	0.298	1.0	73		0.063	
	5	Q_M[7]:CLK	Q_int[8]:D	0.706	-0.068	4.927	4.759	0.298	1.0	68		0.064	
	6	Q_H4[19]:CLK	Q_;rt[20]:D	0.701	-0.031	4.777	4.746	0.298	1.0	31		0.032	
	7	Q_H4[26]:CLK	Q_int[27]:D	0.673	-0.005	4.753	4.748	0.299	1.0	05		0.033	
30	a	Q_int[30]:CLK	Q_int(31):D	0.587	0.043	4.695	4.738	0.299	0.9	57		0.071	
	9	Q_ht[9]:CLK	Q_int[10]:D	0.576	0.048	4.711	4,759	0.298	0.9	52		0.075	
	10	Q_H4[17]:CLK	Q_mt[18]:D	0.577	0.052	4.684	4.735	0.298	0.9	48		0.073	
24	11	Q_int[12]:CLK	Q_int[13]:D	0.571	0.058	4.678	4.736	0.298	0.9	42		0.073	
	12	Q_int(2):CLK	Q_int[3]:D	0.577	0.061	4.712	4,773	0.298	0.9	39		0.064	
18	13	Q_int[3]:CLK	Q_int(4):D	0.563	0.061	4.698	4,759	0,298	0.9	39		0.078	
	Na			Туре	Net			Macr	o Op	Delay	Total Fanout	Edge	
12		Summary data required tin data arrival time slack									4.719 4.810 -0.091		
6		Data_arrival_time_c my_clk	alculation							0.000	0.000		
		CLK		Clock source							0.000	1	
		CLK_ibuf/U0/U_J		net	CLK				*		0.000	r 1	
		CLK_ibuf/U0/U_ CLK_ibuf_RNIVQ		cell	CLK_ibu			ADUE	NIOPAD_IN -		2.325		
0 -0.091 0 0.0045 0.1	0,195	CLK_ibuf_RNEVQ		cell	CLA,000			ADU	RGBM +				
slack distribution(ns)			04/UD RGE1 RGE0:An		CLK ibu	RNIV004/UD	YWn	Hous	+		3.117	1	

Figure 122 · Maximum Delay Analysis After Setting Clock Constraint to 1000 MHz

6. Close SmartTime. Click **No** when prompted to save changes.



Tutorial 2 - Adding an *.sdc File to Constrain Clock

This tutorial uses the 4-bit count16 example to step you through the process of entering constraints and analyzing the timing performance of the design. Two options for entering clock constraints are covered: using SmartTime's Constraint Editor or importing an *.sdc file into Libero SoC.

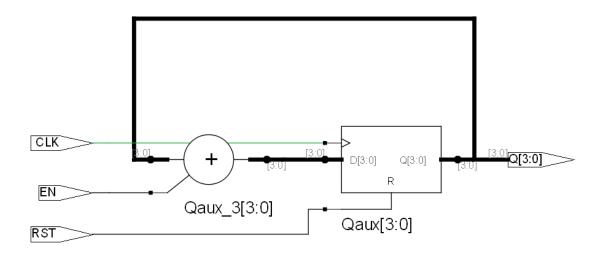


Figure 123 · Tutorial 2 – 4-bit counter

- 1. From the Project menu, choose New Project to create a new Libero project.
- 2. Name the project **smarttime_tutorial** and set the project location according to your preferences. Enter the following values for **the new project**:
 - Family: SmartFusion2
 - Die: M2S050
 - Speed: STD
 - Die Voltage: 1.2 V
 - Package: 484 FBGA
 - Range: COM
- 3. Click Finish to create the new project.
- 4. Import the count16_behave.v into your project (File > Import > HDL Source Files) from the folder where you have downloaded the tutorial files.
- 5. Double-click **Compile** in the Design Flow window to run both Synthesis and Compile with default settings.

Refer to <u>Compile</u> and <u>Layout</u> for more information.

You are ready to create your clock constraints.

Creating a Clock Constraint

You may create a Clock Constraint in one of two ways:

- Option 1 Add Clock Constraint in the Constraint Editor
- Option 2 Import an *.sdc file that contains the Clock Constraint



Option 1 - To create a clock constraint in the Constraint Editor:

 In the Design Flow window, expand Edit Constraints, right-click Timing Constraints, and choose Open Interactively to start SmartTime and open the SmartTime Constraints Editor (as shown in the figure below).

SmartTime - [Constraints Editor for scenar File Edit View Constraints Tools	• ·										X
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Constraints Editor for scenario Primary											
Constraints		Clock	Clock	Period	Frequency	Dutycycle		Offset			
A Requirements	Syntax	Name	Source	(ns)	(MHz)	(%)	First Edge	(ns)	Waveform		File
Clock	Click here to add a co										
Generated Clock	Click here to add a co	nstraint									
Input Delay											
Output Delay											
4 Exceptions											
Max Delay											
Min Delay Multisure											
Multicycle False Path											
4 Advanced											
Clock Source Latency											
Disable Timing											
Clock Uncertainity											
4	•				m						F.
									Ter	mp: 0 - 85 C Volt: 1.14 - 1.2	6 V Speed: STD

Figure 124 · SmartTime Constraints Editor

- 2. Add a clock constraint in one of the followng three ways:
 - Click the New Clock Constraint icon
 in the SmartTime toolbar.
 - Double-click **Clock** under Requirements in the Constraints Pane.

Right-click Clock and choose Add Clock Constraint.

The Create Clock Constraint dialog box appears (as shown below).

Create Clock Constraint		8 23
Clock Name :	Clock Source :	•
Period :	ns or Frequency:	Mhz
5 <u>.</u>		
Image: Offset : Image: Display the second seco		
Comment :		
Help	ОК	Cancel

Figure 125 · Create Clock Constraint Dialog Box

3. Select the **CLK** pin from the pull-down menu in the **Clock source** field, or click the **Browse** button to open the **Select Source Pins for Clock Constraint** dialog box, select the **CLK** pin and click **OK**.



- 4. Enter my_clk under Clock Name. The name of the first clock source is provided as default.
- 5. Type **100** in the **Period** field of the **Create Clock Constraint** box and accept all other default values.
- 6. Click **OK** to close the dialog box.

Create Clock Constraint	8 2
Clock Name : my_clk	Clock Source : CLK 🔹 🛄
Period : 100	ns 时 or Frequency: 10 Mhz
● Offset : ● Duty cycle : ● 0.000 ns 50.0000 %	
Comment :	
Help	OK Cancel

Figure 126 · Create Clock Constraint Dialog Box With Values

	for scen	nario I	Primary]										
File Edit View Constrain	s Tool	s F	lelp										- é
l 🗠 🎦 💱 🏂 🍝	e *	n 🐕	n 🖏 🌠 🎽	< 🏂 🐘	🔈 (fr	场 🧐	3						
traints Editor for scenario Primary													
,													
 Constraints] [Clock	Clock	Period	Frequency	Dutycycle		Offset	-		
A Requirements			Syntax	Name	Source	(ns)	(MHz)	(%)	First Edge	(ns)	Waveform		File
Clock	1	CI.	k here to add a c					50.0000	rising 🖵	0.000	0.0	GUI	
Generated Clock	<u> </u>	Clic	ix nere to add a co										
Input Delay	2	17	•	my_clk	CLK	100.000	10.000	50.0000	rising 🚽	0.000	0 50	GUI	
Output Delay				1						I			
Æ Exceptions													
Max Delay													
Min Delay													
Multicycle													
False Path													
 Advanced 													
Clock Source Latence													
Disable Timing													
Clock Uncertainity													
clock officertainity													
clock oncertainity													

Figure 127 · SmartTime Constraints Editor with Clock Constraint

Option 2 - Import a Timing Constraint *.sdc File

The SDC file contains a Clock Constraint of 10.0 ns for the CLK.

- 1. From the File menu choose Import > Timing Constraint (SDC) Files.
- 2. Navigate to the folder that contains the file count16.sdc that you have downloaded. Click to select it and click **Open**.



- 3. A pop-up dialog asks if you want to organize the constraint files for your current root (count16) for (Compile). Click **Yes** to continue.
- 4. In the Libero SoC Files window, check that the count16.sdc file appears in the constraint directory.

Contemporary Conte		×
Project File Edit View Design Tools Help		
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Files & X	Reports A X StartPage X count16_behave.v* A X count16.sdc A X	Ŧ
component constraint constraint constlo.sdc fp jo designer hdl count16_behave.v simulation smartgen simulus synthesis fo tooldata	<pre> Preate_clock -name (my_clk) -period 10 -waveform {0 5} [get_ports {CLK}] </pre>	
Desi Desig Stimulu Catalog Files HDL	(<u> </u>	F.
Log		8×
🔳 Messages) 😵 Errors 🗼 Warnings info		
The count16 project was created.		
Log Message Cores		
× A Find: Clock Next Replace with: CLK Replace		
	Fam: SmartFusion2 Part: M2S050-FG484	Verilog

Figure 128 · count16.sdc under the Constraints folder in Files tab

Adding an Input Delay Constraint

To add an input delay constraint for Inputs EN and RST in one of the following three ways:

- Click the Add Input Delay Constraint icon
- Double-click Input Delay under Requirement in the Constraint Pane.
- In the Constraint pane, right-click Input Delay and choose Add Input Delay Constraint.

The <u>Set Input Delay Constraint</u> dialog box appears.



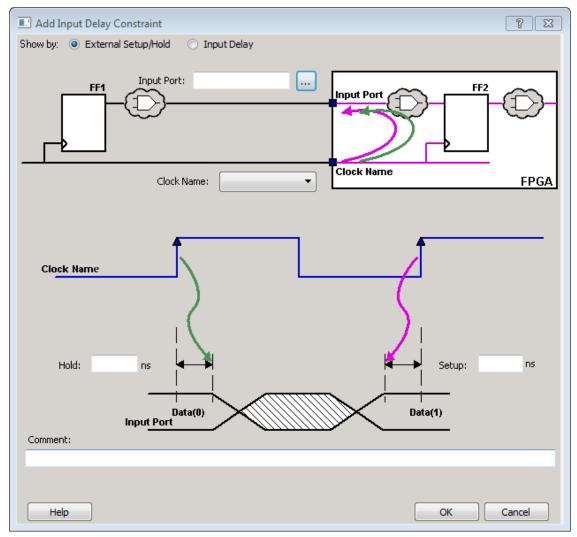


Figure 129 · Set Input Delay Dialog Box

- 1. In the Show by field, select External Setup/Hold.
- Click the Browse button in the Input Port field to select the ports for the external setup constraints. The Select Ports for Input Ports dialog box appears and displays the input ports in the design (see the figure below).



Select Ports for Input Delay Specify pins :- by explicit list by ke	eyword and wildcard	8 2
Available Pins: CLK EN RST	Add All Remove All	
Filter available pins : Pin Type : Input Ports *	Filter	Help OK Cancel

Figure 130 · Select Ports for Input Delay Dialog Box

- 3. Select the ports EN and RST, and then click Add to move the pins from the Available Pins list to the Assigned Pins list. Click OK to close the Select Ports for Input Delay dialog box.
- 4. Enter the following values in the Set Input Delay Constraint dialog box:
 - Clock Name: Select my_clk from the Clock Name drop-down list.
 - Hold Delay: 1 ns
 - Setup Delay: 8 ns
- 5. Add text in comment field if required for better readability
- 6. Click **OK** to close the <u>Set Input Delay Constraint</u> dialog box.

The Input Delay constraints appear in the SmartTime Constraint Editor. Note that the Timing Constraints Editor View displays the external setup/hold requirement.

ile Edit View Constraints T		Primary] Help								
	ĩn 1	n 🗛 🏍 🏷 🏷 🐘 🔌	15 12 <u>1</u> 1 13							
raints Editor for scenario Primary										
Constraints										
A Requirements		Input Ports	Clock	Setup (ns)	Hold (ns)	Max Delay (ns)	Min Delay (ns)	Clock Edge	File	Comments
* Clock	1	1						rising 👻	GUI	
Generated Clock			_							
📑 🕅 Input Delay	2	[get_ports { EN RST }]	my_clk →	8.000	1.000			rising 👻	GUI	
Output Delay		1		· · · · ·						
Exceptions										
Max Delay										
Min Delay										
Multicycle										
Multicycle False Path										
Multicycle False Path 4 Advanced										
Multicycle False Path Advanced Clock Source Latency										
Multicycle False Path Advanced Clock Source Latency Disable Timing										
Multicycle False Path Advanced Clock Source Latency										
Multicycle False Path Advanced Clock Source Latency Disable Timing										
Multicycle False Path Advanced Clock Source Latency Disable Timing Clock Uncertainity		4				""				
Multicycle False Path Advanced Clock Source Latency Disable Timing		4								

Figure 131 · SmartTime Constraints Editor with Input Delay Constraint

Continue to add an output delay constraint.



Adding an Output Delay Constraint

To add an output delay constraint in one of three ways:

- Click the Add Output Delay Constraint icon in the SmartTime toolbar.
- Double-click Output Delay in the Requirement pane.
- Right-click Output Delay and choose Add Output Delay Constraint.

The <u>Set Output Delay Constraint</u> dialog box appears.

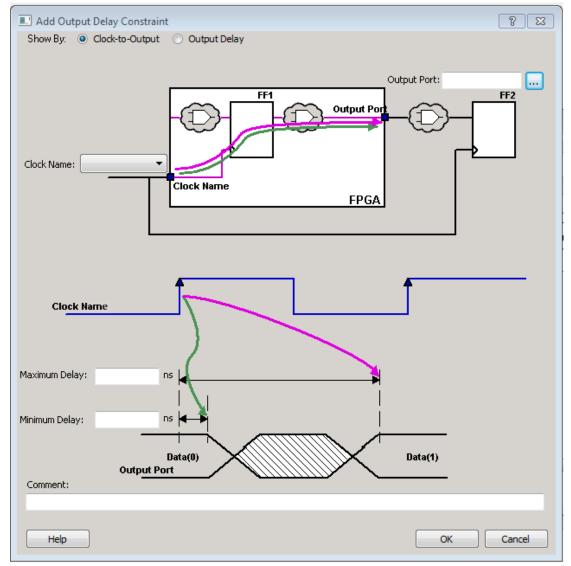


Figure 132 · Set Output Delay Constraint Dialog Box

- 1. In the **Show by** field, select **Clock-to-Output**.
- 2. Click the **Browse** button in the **Output Port** field to select the ports for the output delay constraint. The **Select Ports for Output Delay** dialog box appears and displays the output ports in the design.



Select Ports for	Output Delay				? ×
Specify pins :- 🔘	by explicit list 🔘 by keyword and wildcard				
Available Pins:		Ass	signed Pins:		
Q Q[0] Q[1] Q[2]		Add			
Q[3]		Add All			
		Remove			
		Remove All			
Filter available pin	15 :				Help
Pin Type :	Output Ports			•	ОК
*				Filter	Cancel

Figure 133 · Select Ports for Output Delay

- 3. Click Add All to select all the output ports. SmartTime moves the output pins from the Available Pins list to the Assigned Pins list.
- 4. Click OK to close the Select Ports for Output Delay dialog box.
- 5. Select my_clk from the Clock Name drop-down list in the Add Output Delay Constraint dialog
- 6. Enter 10 in the Maximum Delay field and 8 in the Minimum Delay field.
- 7. Add comments if required (Optional)
- 8. Click **OK** to close the <u>Set Output Delay Constraint</u> dialog box. After the dialog box closes, the clk-toout delay constraints appear in the SmartTime Constraint Editor.



ile Edit View Constraints	Tool	s Help								_
l 🛃 🗅 😏 🏂 🍝 🤅) – <u>*</u>	. <u>‱</u> ‰∍	🍇 📉 🌭 🐘 🔈 😭 🗐	🏪 🕒						
raints Editor for scenario Primary										
Constraints					Clk To Out	Cik To Out	Max Delay	Min Delay	Clock	
 Requirements 		Syntax	Output Ports	Clock	Max(ns)	Min(ns)	(ns)	(ns)	Edge	File
Clock Generated Clock	1	Click here to		-					rising 👻	GUI
Tinput Delay	2		[get_ports { Q Q[0] Q[1] Q[2] Q[3] }]		10.000	8.000				GUI
C Input Delay	2	٣		my_clk 👻	10.000	8.000			rising 🚽	GOI
Exceptions										
Max Delay										
Min Delay Multicycle										
Multicycle										
Multicycle False Path										
Multicycle										
Multicycle False Path Advanced Clock Source Latenc										
Multicycle False Path Advanced Clock Source Laten Disable Timing										
Multicycle False Path Advanced Clock Source Latenc										
Multicycle False Path Advanced Clock Source Laten Disable Timing										
Multicycle False Path Advanced Clock Source Latend Disable Timing Clock Uncertainity										
Multicycle False Path Advanced Clock Source Laten Disable Timing		۲			ı.					

Figure 134 · SmartTime Constraints Editor with Output Delay Constraint

- 9. Click the Save icon in the SmartTime toolbar to save your constraints.
- 10. Exit (**File** \rightarrow **Exit**) the SmartTime tool.

Place and Route Your Design

To run Place and Route:

- 1. Right-click Place and Route in the Design Flow window.and choose Configure Options.
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to close the Layout Options dialog box.
- Right-click Place and Route and choose Run.
 A green check mark appears next to Place and route when it completes successfully.

You are now ready to analyze your design.

Analyzing the Maximum Operating Frequency

The Maximum Delay Analysis View indicates the maximum operating frequency for a design and displays any setup violations.

To perform Maximum Delay Analysis:

Right click Verify Timing and choose Open Interactively to open the Maximum Delay Analysis

View. Alternatively, you may click the Max Delay Analysis icon *Maximum Delay Analysis* View

A green flag next to the name of the clock indicates there are no timing violations for that clock domain (as shown below).

The **SmartTime Maximum Delay Analysis** View displays the maximum operating frequency for a design and any setup violations.



	me - [Maximum Delay Analysis View] dit View Tools Help									_
2	1 🗅 😏 🎽 🖌 🕲 📼									
m Dela	ay Analysis View									
_										
*	Analysis for scenario Primary	Design		count16						
AX		Family		SmartFus	sion2					
	Summary	Die		M2S050						
	∕ጬ my_clk ▲ ✔ Register to Register				-					
	Qaux0 filter	Package		484 FBG	A					
	✓ External Setup	Temperature	Range	0 - 85 C						
	✓ Clock to Output	Voltage Rang	le	1.14 - 1.2	6 V					
	Register to Asynchronous ✓ External Recovery	Speed Grade	, ,	STD						
	Asynchronous to Register	Design State		Post-Lay	out					
4	Fin to Pin	Data source		Productio						
	Input to Output									
4	✓ Oaux1 filter	Min Operatin	•		.26 V - 0 C					
	✓ Qaux2_filter	Max Operati	ng Conditio	ns WORST	- 1.14 V - 85 C					
	✓ Qaux3_filter	Scenario for	Timing Ana	lysis Primary						
		Summar	у							
	Select a set of paths to see its slack distribution,	Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Out (ns)
	its slack distribution.	my_clk	1.983	504.286	100.000	10.000	1.384	0.253	3.788	7.517
			Min De	elay (ns) Max I)elay (ns)					
		Input to Outp		N/A	Soluj (iloj					
	slack distribution(ns)	input to Out	Nu DUA	n/A						
_	Image: State Sta									1.14 - 1.26 V Speed: S

Figure 135 · SmartTime Maximum Delay Analysis View Summary

The **Summary** in the **Maximum Delay Analysis** View displays the maximum operating frequency for the design, the required frequency if any, the external setup and hold requirements, and the maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 504 MHz.

You can now View Register-to-Register paths as part of the Maximum Delay Analysis.

See Also

Analyzing the design (SmartTime)

Viewing Register-to-Register Paths

To view register to register paths:

- 1. Expand my_clk domain in the Domain Browser and display the Register to Register, External Setup, and Clock to output path sets.
- Click Register to Register to display the register to register paths in the Paths List. It displays a list of register-to-register paths at the top of the Path List and detailed timing analysis for the selected path in the Path Details.

Note: All slack values are positive, indicating that no setup time violations exist (see the figure below).



imary for path n: Qaux[0]:CLK Qaux[3]:D a Required Time (ns) Data Arrival	Time (ns) Slack (ns)							Path Profile Cel Delay 18.05%
8.646 5.629	98.017							[Net Delay]
ne	Туре	Net	Macro	Ор	Delay	Total	Fanout Edge	
Data_arrival_time_calculation								
my_clk					0.000	0.000		
CLK	Clock source			+	0.000	0.000	r	
CLK_ibuf/U0/U_IOPAD:PAD	net	CLK		+	0.000	0.000	r	
CLK_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	2.128	2.128	2 r	
CLK_ibuf_RNIVQ04:An	net	CLK_ibuf	_	+	0.352	2.480	f	
CLK_ibuf_RNIVQ04:YWn	cell		ADLIB:GBM	+	0.105	2.585	2 f	
CLK_ibuf_RNIVQ04/U0_RGB1_RG	6B0:An net	CLK_ibuf_RNIVQ04/U0_YWn		+	0.507	3.092	f	
CLK_ibuf_RNIVQ04/U0_RGB1_RG	BO:YL cell		ADLIB:RGB	+	0.372	3.464	1 r	
Qaux[0]:CLK	net	CLK_ibuf_RNIVQ04/U0_RGB1_RGB0_rgbl_net_1	L	+	0.546	4.010	r	
Qaux[0]:Q	cell		ADLIB:SLE	+	0.102	4.112	5 r	
Qaux_3_1.CO0:A	net	Q_c[0]		+	0.659	4.771	r	
Qaux_3_1.CO0:Y	cell		ADLIB:CFG2	+	0.088	4.859	1 r	
Qaux_3_1.SUM[3]:B	net	Qaux_3_1_CO0		+	0.496	5.355	r	
Qaux_3_1.SUM[3]:Y	cell		ADLIB:CFG4	+	0.186	5.541	1 r	
Qaux[3]:D	net	Qaux_3[3]		+	0.088	5.629	r	
		6C-(-)				5.629		
data arrival time CLK_ibuf/L CLK		CLK_ibuf_RNIVQ04	f_RNIVQ04/U0_YW	Qa	aux[0]			CLK_buf_RNIVQ04/U0_RGB1 Qaux[3]
		CLK_ibuf_RNIVQ04/	U0_RGB1_RGB0	ALn				Qaux_3_1.SUM[3]
			iix.	-CLK -D -EN	Q	ç	aux_3_1.CO0	
				LAT SD			CFG2	-p -sun CFG4 SLE
				SLn				

Figure 136 · SmartTime Register to Register Paths List

3. Double-click a path row to open the **Expanded Path View** (see figure below). The top of the view shows a calculation of the required and arrival times. A schematic of the path is shown at the bottom of the view.



File Edit View Tools Help Image: Summary for path from: Quay(3)5CLK Image: Solution of the soluti	
ummary for path ron: Qaux (G) CLK o: Qaux(3):D Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) Data Required Time (ns) Data Arrival Time (ns) Slack (ns) CLK, ibuf (NU/0U) (DADA: PAD net CLK + 0.000 0.000 r CLK, ibuf (NU/0U) (DADA: PAD net CLK, ibuf (ns) PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD net CLK, ibuf (ns) PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD net CLK, ibuf (ns) PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK, ibuf (NU/0U) DADA: PAD Net AllB: RGBM + 0.015 2.585 2 f CLK (NU	
ummary for path more: Qaudy Qick so: Qaudy 3J:0 Nata Required Time (ns) Data Arrival Time (ns) Slack (ns) So:Ga66 5.629 98.017 Name * Data_arrival_time_calculation my_clk * Data_arrival_time_calculation my_clk CLK, ibuf/V0/UJ OPAD:PAD net CLK, ibuf/N0/UJ OPAD:PAD net CLK ibuf/N0/UJ OPAD net CLK ibuf/N0/UJ OPAD:PAD net CLK ibuf/N0/ND net CLK i	
Image: Section Control Contro Control Conte Control Control Control Control Control Control Con	I NET DPAY I
A Data_arrival_time_calculation my_clk 000 000 CLK Clock source 000 000 CLK, ibut/10/U_JOPAD:PAD net CLK 0000 r CLK, ibut/10/U_JOPAD:PAD net CLK 0000 r CLK, ibut/10/U_JOPAD:PAD net CLK 2000 r CLK, ibut/10/U_JOPAD:PAD net CLK, ibut/10/U_JOPAD:PAD r CLK, ibut/10/U_JOPAD:PAD net CLK, ibut/10/U_JOPAD:PAD r CLK, ibut/RNIVQ04/U_N cell ADLIB:R6B + 0.000 r CLK, ibut/RNIVQ04/UD_R6B1_R6B0:An net CLK, ibut/RNIVQ04/UD_R6B1_R6B0:An net CLK, ibut/RNIVQ04/UD_R6B1_R6B0:An net CLK ibut/RNIVQ04/UD_R6B1_R6B0:An net ADLIB:R6B + 0.372 3464 1 r	
my_clk 0.000 CLK CLK_ibuf/U0/U_JOPAD:PAD net CLK_ibuf/U0/U_JOPAD:PAD net CLK_ibuf/U0/U_JOPAD:PAD r CLK_ibuf/U0/U_JOPAD:PAD net CLK_ibuf/U0/U_JOPAD:PAD r r CLK_ibuf/NU/U_JOPAD:PAD:PAD net CLK_ibuf/NU/DAD_IN 2.128 2 r CLK_ibuf/NU/OU-MAD:PAD:PAD net CLK_ibuf/NU/DAD_IN 4.0152 2.480 f CLK_ibuf/NU/Q04/U0_R681_R680:An net CLK_ibuf_NU/Q04/U0_SG81_R680:An net CLK_ibuf_RNIVQ04/U0_SG81_R680:An 6 7 CLK_ibuf_RNIVQ04/U0_R681_R680:An CLK_ibuf_RNIVQ04/U0_SG81_R680:An ADULB:R68 + 0.372 3.464 1 r	
CLK Clock source + 0.000 r CLK,ibu/U/U/U_JOPAD.PAD net CLK + 0.000 r CLK,ibu/U/U/U_JOPAD.Y cell ADLIB:OPAD_IN + 2.128 2 r CLK,ibu/RNIVQ04/An net CLK,ibu/RNIVQ04/Wn + 0.352 2.480 f CLK,ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK,ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK,ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK_ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK_ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK_ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK_ibu/RNIVQ04/U0_RGBL_RGB0:An net CLK_ibu/RNIVQ04/U0_RGBL_RGB0:An net ADLIB:RGB + 0.372 3.464 1 r	
CLK_ibuf/U0/U_IOPAD-PAD net CLK + 0.000 r CLK_ibuf/U0/U_IOPAD-PAD cell ADLB:OPAD_IN + 2.128 2 r CLK_ibuf/U0/U_IOPAD-PAD net CLK_ibuf_RNIVQ04:An + 0.325 2.480 f CLK_ibuf_RNIVQ04:VWn cell ADLB:GBM + 0.352 2.585 2 f CLK_ibuf_RNIVQ04/U0_RGB1_RGB0:An net CLK_ibuf_RNIVQ04/U0_YWn + 0.507 3.092 f CLK_ibuf_RNIVQ04/U0_RGB1_RGB0:An net CLK_ibuf_RNIVQ04/U_RGB1_RGB0:An 1 ADLIB:RGB + 0.372 3.464 1 r	
CLK_jbuf/U0/U_JOPAD:Y cell ADLIB:OPAD_IN + 2.128 2.128 2 r CLK_jbuf_RNIVQ04/an net CLK_jbuf + 0.352 2.480 f CLK_jbuf_RNIVQ04/VNn cell ADLIB:GBM + 0.105 2.585 2 f CLK_jbuf_RNIVQ04/U0_RGB1_RGB0:An net CLK_jbuf_RNIVQ04/U0_YWn + 0.507 3.992 f CLK_jbuf_RNIVQ04/U0_RGB1_RGB0:YL cell ADLIB:RGB + 0.372 3.464 1 r	
CLK_ibuf_RNIVQ04/us n net CLK_ibuf + 0.352 2.480 f CLK_ibuf_RNIVQ04/VWn cell ADLB-R6B + 0.105 2.385 2 f CLK_ibuf_RNIVQ04/U0_R6BL_R6B0.An net CLK_ibuf_RNIVQ04/U0_YWn + 0.507 3.092 f CLK_ibuf_RNIVQ04/U0_R6BL_R6B0.YL Cell ADLIB-R6B + 0.372 3.464 1 r	
CLK_ibuf_RNIVQ04/U0_RGBL_RGB0:An net CLK_ibuf_RNIVQ04/U0_rVWn 0.105 2.58 2 f CLK_ibuf_RNIVQ04/U0_RGBL_RGB0:An net CLK_ibuf_RNIVQ04/U0_rVWn + 0.507 3.092 f CLK_ibuf_RNIVQ04/U0_rGBL_RGB0:VL cell ADLIBR:GB + 0.372 3.464 1 r	
CLK_ibuf_RNIVQ04/U0_RGB1_RGB0:An net CLK_ibuf_RNIVQ04/U0_YWn + 0.507 3.092 f CLK_ibuf_RNIVQ04/U0_RGB1_RGB0:YL cell ADLIB:RGB + 0.372 3.464 1 r	
CLK_ibuf_RNIVQ04/U0_RGB1_RGB0:YL cell ADLIB:RGB + 0.372 3.464 1 r	
Qaux[0]:CLK net CLK_ibuf_RNIVQ04/U0_RGB1_RGB0_rgbl_net_1 + 0.546 4.010 r	
Qaux(0):Q cell ADLIB:SLE + 0.102 4.112 5 r	
Qaux,3,1.C00:A net Q_c[0] + 0.659 4.771 r	
Qaux_3_1.CO0:Y cell ADLIB:CFG2 + 0.088 4.859 1 r	
Qaux_3_1.SUM[3]:B net Qaux_3_1_CO0 + 0.496 5.355 r	
Qaux_3_1.SUM[3];Y cell ADLIB:CFG4 + 0.186 5.541 1 r	
Qaux[3]:D net Qaux_3[3] + 0.088 5.629 r	
data arrival time 5.629	

Figure 137 · SmartTime Expanded Paths View

Tip: Left-click and drag the mouse to zoom in or out in the schematic window.

4. Close the Expanded Paths View.

Viewing External Setup Paths

To view External Setup paths, click **External Setup** in the Domain Browser to display the external setup timing (as shown below).

Note: Slack is positive in the tutorial example, indicating there are no timing violations.



2 🎦 🎦 😏 🖌 🖉	⊚ ≍													
ım Delay Analysis View														
_														
Analysis for scenario														
AX Primary		From	*				TO *							
ගි Summary		Custo	mize table							Applu	y Filter	Store	ilter Dese	et Filter
4 √@ my_clk		Custo	inize table							Apply	yritter	Store	Rese	etriter
 Register to Register 														
 External Setup 			Source Pin	Sink Pin	Delay	Slack	Arrival	Required	Setup	Extern				
 Clock to Output 	8				(ns)	(ns)	(ns)	(ns)	(ns)	Setup (ns)			
Register to Asynchronous		1 EN									1.384			
 External Recovery 														
Asynchronous to Register		2 EN	N	Qaux[0]:D	4.219	7.092	4.219	11.311	0.298	0	0.908			
Pin to Pin		3 EN		Qaux[2]:D	4.151	7.151	4.151	11.302	0.298		0.849			
User Sets			•	Qaux[2].D	4.151	7.151	4.151	11.302	0.250		0.045			
		4 EN	4	Qaux[1]:D	4.052	7.260	4.052	11.312	0.298		0.740			
			•	doov[1]to					0.250					
		Name		Type		Net		Macro		On	o Delav	Total	Fanout Edge	e
		Name 4 Sur	mmary	Туре	1	Net		Macro)	Ор	Delay	Total	Fanout Edge	e
		⊿ Sur		Туре	1	Net		Macro	5	Ор		11.302	Fanout Edge	e
		⊿ Sur	mmary	Туре	1	Net		Macro		Op		11.302 4.686	Fanout Edge	e
		⊿ Sur	mmary data required time data arrival time slack			Net		Macro		, i		11.302	Fanout Edge	e
		4 Sur	mmary data required time data arrival time slack ta_arrival_time_calculat			Net		Macro		, i		11.302 4.686 6.616	Fanout Edge	e
4		4 Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk	ion		Net		Macro			0.000	11.302 4.686 6.616 0.000		e :
4		⊿ Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk EN	ion Input Delay Co	nstraint			Macro		, i	0.000	11.302 4.686 6.616 0.000 0.000	f	e
		⊿ Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk EN EN_ibuf/U0/U_IOPAD:P/	ion Input Delay Cor AD net	nstraint	Net					0.000 0.000 0.000	11.302 4.686 6.616 0.000 0.000 0.000	f	e
4 3		⊿ Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk EN EN_ibuf/U0/U_IOPAD:P EN_ibuf/U0/U_IOPAD:Y	ion Input Delay Cor AD net cell	nstraint E	EN)/YIN1		o :IOPAD_IN	-	0.000	11.302 4.686 6.616 0.000 0.000 0.000 2.720	f	e i
		⊿ Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk EN EN_ibuf/U0/U_IOPAD:P/	ion Input Delay Cor AD net cell net	nstraint E)/YIN1	ADLIB		- + + +	0.000 0.000 0.000 2.720	11.302 4.686 6.616 0.000 0.000 0.000 2.720 2.720	f f 1 f	e i
		4 Sur	mmary data required time data arrival time slack ta_arrival_time_calculat my_clk EN_ibuf/U0/U_IOPAD:P/ EN_ibuf/U0/U_IOPAD:P/ EN_ibuf/U0/U_IOPAD:P/ EN_ibuf/U0/U_IOPAD:P/	ion Input Delay Cor AD net cell net	nstraint E	EN)/YIN1	ADLIB	:IOPAD_IN	- + + +	0.000 0.000 0.000 2.720 0.000	11.302 4.686 6.616 0.000 0.000 0.000 2.720 2.720 2.826	f f 1 f f	e
3		4 Sur	mmary data required time data arrival time slack EN EN EN_bit/100/U_IOPAD:PP EN_ibut/100/U_IOPAD:P EN_ibut/100/U_IOINFF:A EN_ibut/100/U_IOINFF:Y Qaux_3_1.CO0:Y	ion Input Delay Cor AD net cell net cell net cell	nstraint E E	N N_ibuf/UC N_c		ADLIB	:IOPAD_IN :IOINFF_BYF	- + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944	f f f f f f f f f	e
3		4 Sur	mary data required time data arrival time slack ta_arrival_time_calculat my_clk EN_ibut/100/U_IOPAD:P EN_ibut/100/U_IOPAD:P EN_ibut/100/U_IOPAD:P EN_ibut/100/U_IOINFF:Y Qaux_3_1_CO0B Qaux_3_1_CO0F Qaux_3_1_CO0F	ion Input Delay Cor AD net cell net cell net	nstraint E E	EN EN_ibuf/UC		ADLIB ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	- + + + + + + + + 2ASS + + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425	f f 1 f f 4 f f 1 f f	e i
3		4 Sur	mary data required time data arrival time slack ta, arrival time_calculat my_clk EN_ibuf/00/U_IOPAD:P EN_ibuf/00/U_IOPAD:P EN_ibuf/00/U_IOINFF:Y Gaux 3_1.CO0:B Gaux 3_1.CO0:B Gaux 3_1.CO0:B Gaux 3_1.CO0:B	ion Input Delay Cor AD net cell net cell net cell net cell	nstraint E E (EN EN_ibuf/UC EN_c Qaux_3_1_C		ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	+ + + + ASS + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481 0.173	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425 4.598	f f f f f f f f f	e
3		4 Sur	mary data required time data arrival time slack EN EN EN, biot/100/U_IOPAD:PP EN_ibut/100/U_IONPAD:PP EN_ibut/100/U_IONFF:Y Qaux 3_1.CO0:P Qaux 3_1.CO0:P Qaux 3_1.SUM[3]:P Qaux 3_1.SUM[3]:P	ion Input Delay Cor AD net cell net cell net	nstraint E E (N N_ibuf/UC N_c		ADLIB ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	- + + + + + + + + 2ASS + + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425 4.598 4.686	f f 1 f f 4 f f 1 f f	e
3 2 1		4 Sur	mary data required time data arrival time slack ta,arrival_time_calculat my_clk EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi Qaux_3_1_C00:Pi Qaux_3_1_C00:Pi Qaux_3_1_SUM[3]:Pi Qaux_3_1_SUM[3]:Pi Qaux_31_	ion Input Delay Cor AD net cell net cell net cell net cell net	nstraint E E (EN EN_ibuf/UC EN_c Qaux_3_1_C		ADLIB ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	- + + + + + + + + 2ASS + + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481 0.173	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425 4.598	f f 1 f f 4 f f 1 f f	e
2	7.26 7.582	Sur Dat	mary data required time data arrival time slack En, <u>ibuf/00/UJOPAD:P</u> EN, <u>ibuf/00/UJOPAD:P</u> EN, <u>ibuf/00/UJONFFA</u> EN, <u>ibuf/00/UJONFFA</u> EN, <u>ibuf/00/UJONFFA</u> Qaux; 3,1.C00;8 Qaux; 3,1.C00;8 Qaux; 3,1.SUM[3]:P Qaux;3].SUM[3]:P Qaux;3].SUM[3]:P Qaux;3].SUM[3]:P	ion Input Delay Cor AD net cell net cell net cell net cell net cell net	nstraint E E C C	EN EN_ibuf/UC EN_c Qaux_3_1_C		ADLIB ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	- + + + + + + + + 2ASS + + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481 0.173 0.088	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425 4.598 4.686 4.686	f f 1 f f 4 f f 1 f f	e
	7.26 7.582	 Sur Dat Dat 	mary data required time data arrival time slack ta,arrival_time_calculat my_clk EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi EN_ibuf/U0/U_IOPAD:Pi Qaux_3_1_C00:Pi Qaux_3_1_C00:Pi Qaux_3_1_SUM[3]:Pi Qaux_3_1_SUM[3]:Pi Qaux_31_	ion Input Delay Cor AD net cell net cell net cell net cell net	nstraint E E C C	EN EN_ibuf/UC EN_c Qaux_3_1_C		ADLIB ADLIB	:IOPAD_IN :IOINFF_BYF :CFG2	- + + + + + + + + 2ASS + + + +	0.000 0.000 2.720 0.000 0.106 0.925 0.193 0.481 0.173 0.088 8.000	11.302 4.686 6.616 0.000 0.000 2.720 2.720 2.826 3.751 3.944 4.425 4.598 4.686	f f 1 f f 4 f f 1 f f	e i

Figure 138 · SmartTime External Setup Path List

Viewing Clock-to-Output Paths

To view Clock-to-output paths, click **Clock to Output** in the Domain Browser to display the register to output timing. Again, the slack is positive in the tutorial example, indicating there are no timing violations.



n Delay Analysis View										
Primary	From *			то	•					
ଭି Summary	Customize table						Apply Filter	Store Fi	Iter Dece	et Filter
Summary	Customize table						Apply Filter	Store FI	Rese	et Filter
 Register to Register 										
 ✓ External Setup 	Source Pin	Sin	k Pin Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	C	lock to Ou	ıt (ns)	
 Clock to Output 										
Register to Asynchronous	1 Qaux[2]:CLK									7.517
✓ External Recovery		0[2]			2 0 50	10,000				2.050
Asynchronous to Register	2 Qaux[3]:CLK	Q[3]	3.3	50 2.65	0 7.350	10.000				7.350
Pin to Pin	3 Qaux[1]:CLK	Q[1]	3.0	39 2.65	0 7.350	10.000				7.350
Iser Sets	5 Qaux[1]:CLK	914	5	2.03	7.350	10.000				7.550
	4 Qaux[0]:CLK									7.341
		0001	31	31 2.65		10 000				
	4 Qaux[0]:CLK	Q[0]	3.3	31 2.65	9 7.341	10.000				7.341
	4 Qaux[0]:CLK	Q[0]	3.3	2.65	9 7.341	10.000				7.341
	4 Qaux[0]:CLK	Q[0]	3.:	2.65	9 7.341	10.000				7.341
							0.01	7.1		
	Name	Q[0]		Net	9 7.341 Macro		Op Dela	ıy T otal	Fanout Edg	
	Name						Op Dela			
	Name A Summary data required time							10.000		
	Name Summary data pequired time data drival time						Op Dela	10.000 7.517		
	Name A Summary data required time data arrival time slack	Тур						10.000		
4	Name Summary data yequired time data afrival time slack Data arrival time_calcl	Тур					-	10.000 7.517 2.483		
4	Name Summary data required time data drival time slack Data arrival time calcu my.clk	Tyr	pe				-	10.000 7.517 2.483 00 0.000	Fanout Edg	
	Name Summary data required time data invial time slack Data arrival_time_calcumy_clk CLK	Tyr ulation Clo	pe bck source	Net			- 0.00 + 0.00	10.000 7.517 2.483 00 0.000 00 0.000		
4 3	Name Summary datarequired time data arrival time slack Data_arrival time_calcu my_clk CLK CLK,ibuf/U0/U_IOPA	Ulation Clo AD:PAD net	pe bock source		Macro	<u> </u>	- - + 0.00 + 0.00	10.000 7.517 2.483 00 0.000	Fanout Edg	
	Name Summary data required time data arrival time slack Data_arrival time_calcu my_clk CLK ids/1/00/U_JOPA CLK,ids/1/00/U_JOPA	Ulation Clo AD:PAD net AD:Y cell	pe bock source t	Net	Macro		- - 0.00 + 0.00 + 0.00 + 2.12	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000	Fanout Edg	
3	Name Summary data required time data service time slack Data arrival time_calct my_clk CLK CLK, ibuf, NUVQ04J CLK, ibuf, NUVQ04J	ulation Clo AD:PAD net AD:Y cell An net	pe bok source t	Net	Macro	; iopad_in	- + 0.00 + 0.00 + 2.11 + 0.32	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 28 2.128	Fanout Edg r r 2 r	
	Name Summary data required time data arrival time slack Data_arrival_time_calcu my_clk CLK_ibdr/U0/U_JOPA CLK_ibdr/U0/U_JOPA	ulation Clo AD:PAD net AD:Y cell An net Wvn cell	pe bock source t	Net	ADLIB	; iopad_in	- + 0.00 + 0.00 + 2.11 + 0.31 + 0.10	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 00 0.000 28 2.128 52 2.480	Fanout Edg r r f	
2	Name Summary data required time data arrival time slack Data arrival time, calcu my_clk CLK CLK, ibuf, Y00/U J09V CLK, ibuf, RNIVQ04// CLK, ibuf, RNIVQ04//	Ulation Clo AD:PAD net AD:Y cell An net YWn cell QD_RGB1:An net	pe bok source t t	Net CLK CLK_ibuf	ADLIB	:IOPAD_IN :GBM	- - 0.00 + 0.00 + 0.00 + 2.11 + 0.33 + 0.10 + 0.48	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 028 2.128 52 2.480 05 2.585	Fanout Edg r r 2 r f 2 f	
3	Name * Summary data required time data afrival time slack * Data_arrival_time_calcu my_clk CLK, ibur/100/U_IOP/ CLK, ibur/100/U_IOP/ CLK, ibur/100/U_IOP/ CLK, ibur/100/U_IOP/ CLK, ibur/100/U_IOP/ CLK, ibur/100/U_IOP/	Ulation Clo AD:PAD net AD:Y cell An net YWn cell QD_RGB1:An net	pe bock source t t t	Net CLK CLK_ibuf	ADLIB /U0_YWn	:IOPAD_IN :GBM	- + 0.00 + 0.00 + 2.11 + 0.33 + 0.10 + 0.44 + 0.33	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 028 2.128 52 2.480 05 2.585 87 3.072	Fanout Edg r r 2 r f 2 f f	
2	Name Summary data required time data afrival time slack Data_arrival time_calct my_clk CLK_ibuf_RNIVQ04/ CLK_ibuf_RNIVQ	Ulation Clo AD:PAD net AD:Y cell An net WVn cell U0_RGB1:An net U0_RGB1:AL cell	pe bock source t t t	Net CLK CLK_ibuf CLK_ibuf_RNIVQ04	ADLIB /U0_YWn	:IOPAD_IN :GBM :RGB	- + 0.00 + 0.00 + 2.11 + 0.33 + 0.10 + 0.44 + 0.33 + 0.55	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 00 0.000 028 2.128 52 2.480 05 2.585 87 3.072 72 3.444	Fanout Edg r r 2 r f 2 f f 3 r	
	Name Summary data required time data afrival time slack Data_arrival_time_calcum my_clk CLK CLK_ibuf/V0/V_JOP/ CLK_ibuf/V0/V_JOP/ CLK_ibuf_RNIVQ04/ CLK_ibuf_NV04/	Ulation Clo AD:PAD net AD:Y cell An net YWn cell U0_RGB1:YL cell net U0_RGB1:YL cell	pe bok source t t t t t	Net CLK CLK_ibuf CLK_ibuf_RNIVQ04	ADLIB 4DLIB 4DLIB ADLIB	:IOPAD_IN :GBM :RGB	- - 0.00 + 0.00 + 2.11 + 0.33 + 0.10 + 0.48 + 0.35 + 0.55 + 0.11	10.000 7.517 2.483 00 0.000 00 0.000 00 0.000 028 2.128 52 2.480 52 2.585 37 3.072 72 3.444 56 4.000	Fanout Edg r r 2 r f 2 f f 3 r r	
2	Name Summary data required time data Brival time slack Bata_arrival time_calcu my_clk CLK, ibuf, 7U0/U_JOP/ CLK, ibuf, RNIVQ04/ CLK, ibuf, SNIVQ04/ CLK, ibuf, SNIVCNA/ CLK, ibuf, SNIVCNA/ CLK, ibuf, SNIVCNA/ CLK, ibuf, SNIVCNA/	Ulation Clo AD.PAD net AD.Y cell AAn net UU, RGB1:AL net uU, RGB1:AL net cell DUTFF-A net	pe bock source t t t t t t	Net CLK CLK,ibuf CLK,ibuf,RNIVQ04 CLK_c	ADLIB ADLIB ADLIB UUQ_YWN ADLIB ADLIB	:IOPAD_IN :GBM :RGB	- 0.00 + 0.00 + 2.11 + 0.33 + 0.10 + 0.44 + 0.33 + 0.59 + 0.11 + 0.78	10.000 7.517 2.483 00 0.000 00 0.000 028 2.128 52 2.480 055 2.585 7 3.072 2 3.444 56 4.000 27 4.127	Fanout Edg r r 2 r f 2 f f 3 r r 3 r	

Figure 139 · SmartTime Clock to Output Paths List

Using Filters and Creating Analysis Sets

Filters can be used and saved to display analysis sets in the Maximum Delay Analysis window and the Minimum Delay Analysis window.

To create a filter:

- 1. When the Place and Route step is complete, click Verify Timing > Open Interactively.
- 2. In the Maximum Delay Analysis View, select the **Register to Register path**. Enter the following in the Filter fields (as shown in the figure below) then click **Apply Filter**:

From: Qaux[0]:CLK To: *:D



📗 💁 🎦 🏂 🍝 🖉 🐵 ≍ um Delay Analysis View													
Analysis for scenario													
Primary	Fro	m Qaux[0]:CLK				то	*:D						
ା ଭି Summary	Q	stomize table							Apply	Filter	Store Fi	Iter Reset f	-ilter
4 √(0) my clk													
✓ Register to Register									Minimum P				
✓ External Setup		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	(ns)	eriod	S	kew (ns)	
✓ Clock to Output		0	Qaux[3]:D	1.619	8.017	5.629	13.646	0.298		1.983			.066
Register to Asynchronous	× .	Qaux[0]:CLK					13.040						.000
✓ External Recovery	2	Qaux[0]:CLK	Qaux[2]:D	1,145	8,491	5.155	13.646	0.298		1.509		Ö	.066
Asynchronous to Register	1											-	
The Pin to Pin Input to Output	3	Qaux[0]:CLK	Qaux[1]:D	1.059	8.587	5.069	13.656	0.298		1.413		0	.056
T User Sets													
and oser bets	4	Qaux[0]:CLK	Qaux[0]:D	0.743	8.904	4.753	13.657	0.298		1.096		0	.055
	Nar	ne		Туре	Net			Ма	cro	Op D	elay Tota	al Fanout Ed	lge
		ne Summary		Туре	Net			Ma	cro	Op D	elay Tota	al Fanout Ed	lge
10		Summary data required tim	ie .	Туре	Net			Ma	cro	Op D	13.6	46	dge
10		Summary data required tim data arrival time	ie	Туре	Net			Ma	cro	Op D	13.6	46 i29	lge
10	4	Summary data required tim data arrival time slack		Туре	Net			Ma	cro	Op D	13.6	46 i29	dge
	4	Summary data required tim data arrival time slack Data_arrival_time_ca		Туре	Net			Ma	cro	-	13.6 5.6 8.0	46 29 117	lge
	4	Summary data required tim data arrival time slack Data_arrival_time_ca my_clk			Net			Ма	cro	-	13.6 5.6 8.0	46 29 117	dge
8	4	Summary data required tim data arrival time slack Data_arrival_time_ca my_clk CLK	alculation	Clock source			_	Ма	cro	- (13.6 5.6 8.0	i46 i29 i17 i00 i00 r	dge
	4	Summary data required tim data arrival time slack Data_arrival_time_ca my_clk	alculation OPAD:PAD		Net				cro LIB:IOPAD_IN	- (13.6 5.6 8.0 0.000 0.0	i46 i29 i17 i00 i00 r i00 r	dge
8	4	Summary data required time data arrival time slack Data_arrival_time_ca my_clk CLK CLK_ibuf/U0/U0_IG	alculation OPAD:PAD OPAD:Y	Clock source net		f				- ((+ () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4	446 229 117 000 r 000 r 28 2 r 80 f	dge
8	4	Summary data required time slack Data_arrival_time_ca my_clk CLK CLK_ibuf/U0/U_IC CLK_ibuf/U0/U_IC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC	alculation OPAD:PAD OPAD:Y 04:An 04:YWn	Clock source net cell net cell	CLK CLK_ibut			ADI		- + ((+ (+ 2 + (+ (13.6 5.6 8.0 0.000 0.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5	i46 i29 i17 i00 r i00 r i28 2 r i80 f i85 2 f	lge
8	4	Summary data required tim data arrival time slack Data_arrival_time_ca my_clk CLK CLK_ibuf/U0/U_IC CLK_ibuf/U0/U_IC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC	alculation DPAD:PAD DPAD:Y M:An M:YWn M(JU0_RGB1_RGB0:An	Clock source net cell net cell net	CLK CLK_ibut	f f_RNIVQ04/U0.		ADI	LIB:IOPAD_IN LIB:GBM	- + ((+ (+ (+ (+ (+ ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.507 3.0	46 229 117 000 r 28 2 r 80 f 885 2 f 992 f	dge
8	4	Summary data required tim slack Data_arrival_time_cd my_clk CLK CLK_ibuf/U0/UJK CLK_ibuf/U0/UJK CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC	alculation OPAD:PAD OPAD:Y 04:An 04:YWn	Clock source net cell net cell net cell	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0	-	ADI ADI ADI	LIB:IOPAD_IN	- + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.507 3.0 0.372 3.4	46 29 100 000 r 28 2 r 80 f 185 2 f 192 f 164 1 r	dge
8	4	Summary data required tim data arrival time slack Data_arrival_time_cc my_clk CLK ibuf/U0/U_IX CLK_ibuf/U0/U_IX CLK_ibuf/NIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC CLK_ibuf_RNIVQC	alculation DPAD:PAD DPAD:Y M:An M:YWn M(JU0_RGB1_RGB0:An	Clock source net cell net cell net cell net	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0	_YWn _RGB1_RGB0_rg	ADI ADI aDI aDI_net_1	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + () + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.507 3.0 0.372 3.4 0.546 4.0	446 529 117 000 r 000 r 000 r 28 2 r 80 f 185 2 f 192 f 164 1 r 10 r	dge
8	4	Summary data required tim data arrival time slack Data_arrival_time_ct my_clk CLK_ibuf/NU/UJ CLK_ibuf/NU/UJ CLK_ibuf/RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ Qaux(0):CLK Qaux(0):Q	alculation DPAD:PAD DPAD:Y M:An M:YWn M(JU0_RGB1_RGB0:An	Clock source net cell net cell net cell net cell	CLK CLK_ibu CLK_ibu CLK_ibu	f_RNIVQ04/U0	-	ADI ADI aDI aDI_net_1	LIB:IOPAD_IN LIB:GBM	- + () + () + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.105 3.4 0.105 3.4 0.105 3.4 0.507 3.0 0.372 3.4	446 529 117 100 100 100 100 100 100 100	dge
8 6 4	4	Summary data required tim data arrival time_cci my_clk CLK ibut/10/U_JR CLK.ibut/10/U_JR CLK.ibut/RNIVQ CLK.ibut/RNIVQ CLK.ibut/RNIVQ QLK_ibut/RNIVQ Qaux[0]:CLK Qaux[0]:Q Qaux[0]:CLK	alculation DPAD:PAD DPAD:Y M:An M:YWn M/U0_RGB1_RGB0:An	Clock source net cell net cell net cell net cell net	CLK CLK_ibut CLK_ibut	f_RNIVQ04/U0	-	ADI ADI abl_net_1 ADI	LIB:IOPAD_IN LIB:GBM LIB:RGB LIB:SLE	- + ((+ (+ (+ (+ (+ (+ () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.507 3.0 0.372 3.4 0.372 3.4 0.546 4.0 0.546 4.1 0.659 4.7	446 229 117 000 r 28 2 r 80 f 85 2 f 64 1 r 10 r 11 5 r 71 r	dge
8	4	Summary data required tim data arrival time slack Data, arrival, time, ci data, arrival, time, ci data, dime, ci clK, ibuf/U0/UJ ClK, ibuf/RNIVQ CLK, ibuf, RNIVQ CLK, ibuf, RNIVQ Qau(0):CLK Qau(0):CLK Qau(3):CO:A Qau(3):CO:A Qau(3):CO:A	alculation DPAD:PAD DPAD:Y 4:An W:YWn M:YUN M:YUU RGB1_RGB0:An M:/U0_RGB1_RGB0:YL	Clock source net cell net cell net cell net cell net cell et cell	CLK CLK_ibut CLK_ibut CLK_ibut Q_c[0]	f_RNIVQ04/U0_ f_RNIVQ04/U0_	-	ADI ADI abl_net_1 ADI	LIB:IOPAD_IN LIB:GBM LIB:RGB	- + () + () + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.105 3.4 0.105 3.4 0.105 3.4 0.507 3.0 0.372 3.4	446 229 117 1000 r 28 2 r 80 f 85 2 f 92 f 64 1 r 10 r 12 5 r 71 r 71 r 759 1 r	dge
	4	Summary data required tim data arrival time_cci my_clk CLK ibut/10/U_JR CLK.ibut/10/U_JR CLK.ibut/RNIVQ CLK.ibut/RNIVQ CLK.ibut/RNIVQ QLK_ibut/RNIVQ Qaux[0]:CLK Qaux[0]:Q Qaux[0]:CLK	alculation DPAD:PAD DPAD:Y M:An M:YWM M:U0L RGBL_RGB0:An M:U0L RGBL_RGB0:YL	Clock source net cell net cell net cell net cell net	CLK CLK_ibu CLK_ibu CLK_ibu	f_RNIVQ04/U0_ f_RNIVQ04/U0_	-	ADI ADI abl_net_1 ADI ADI	LIB:IOPAD_IN LIB:GBM LIB:RGB LIB:SLE	- + () + () + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 0.000 0.0 2.128 2.1 0.352 2.4 0.105 2.5 0.507 3.0 0.577 3.0 0.577 3.4 0.546 4.0 0.546 4.0 0.546 4.0 0.546 4.0	446 229 177 000 r 28 2 r 885 2 f 685 2 f 64 1 r 11 r 71 r 71 r 755 r r	dge .
	4	Summary data required tim data arrival time slack Data_arrival_time_cci my_clk CLK_ibuf/U0/U_JC CLK_ibuf/U0/U_JC CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ CLK_ibuf_RNIVQ Qaux(0):CLK Qaux(0):CQ Qaux(3).COON Qaux(3).LOON	alculation DPAD:PAD DPAD:Y M:An M:YWM M:U0L RGBL_RGB0:An M:U0L RGBL_RGB0:YL	Clock source net cell net cell net cell net cell net cell net	CLK CLK_ibut CLK_ibut CLK_ibut Q_c[0]	f_RNIVQ04/U0_ f_RNIVQ04/U0_ 1_CO0	-	ADI ADI abl_net_1 ADI ADI	lib:iopad_in Lib:gbm Lib:rgb Lib:sle Lib:cfg2	- + () + () + () + () + () + () + () + ()	13.6 5.6 8.0 0.000 0.0 0.000 0.0 0.128 2.1 0.352 2.4 0.507 3.0 0.105 2.5 0.507 3.0 0.372 3.4 0.546 4.0 0.102 4.1 0.659 4.7 0.658 4.5 0.088 4.8 0.496 5.3	A46 29 117 000 r 28 2 r 80 f 85 2 f 902 f 64 1 r 10 r 11 5 r 71 r 59 1 r 55 r 55 r	dge

Figure 140 · Applying a Filter in the Maximum Delay Analysis View

 Click Store Filter to save the filter. Enter Qaux0_filter in the Name field of the Create Filter Set dialog box. The set will be visible in the Maximum Delay Analysis View under Register to Register (as shown in the figure below).

Image: Second of the scenario o
Analysis for scenario From * TO *
Primary TO * Openanty To *
Primary TO * Openanty To *
Primary TO * Openanty To *
Summary Apply Filter Store Filter R
Image: Source Pin Sink Pin Delay (ns) Slack (ns) Arrival (ns) Required (ns) Setup (ns) Himmum Period (ns) V Clock to Output Register to Register I Qaux(0):CLK Qaux(2):D 1.619 8.017 5.629 13.646 0.798 1.983 0.066 Register to Register to Asynchronous V External Recovery 1 Qaux(2):CLK Qaux(2):D 1.145 8.491 5.155 13.646 0.298 1.509 0.066 3 Qaux(0):CLK Qaux(2):D 1.145 8.491 5.155 13.646 0.298 1.413 0.056 4 Qaux(0):CLK Qaux(0):CL
Image: Source Pine Source Pine Sink Pin Delay (ns) Slack (ns) Arrival (ns) Required (ns) Setup (ns) Minimum Period (ns) Skew (ns) * Clock to Output Clock to Output Register to Asynchronous * Delay (ns) Slack (ns) Arrival (ns) Required (ns) Setup (ns) Minimum Period (ns) Skew (ns) * Clock to Output Register to Asynchronous * Delay (ns) 1.619 8.017 5.629 10.64 0.029 1.983 0.066 * Delay (ns) Aux (0):CLK Qaux (1):D 1.145 8.491 5.155 13.646 0.298 1.143 0.056 4 Qaux (0):CLK Qaux (0):D 1.059 8.897 5.069 13.657 0.298 1.098 0.055 3 Qaux (0):CLK Qaux (0):D 0.0743 8.904 4.753 13.657 0.298 1.096 0.055 4 Qaux (0):CLK Qaux (0):D 0.0743 8.904 4.753 13.657 0.298 1.096 0.055 5 Name Type Net Macro Op Delay Total Fanout Edge

Caternal Recovery
4 a
A A A A A A A A A A A A A A A A A A A
Name Type Net Macro Op Delay Total Fanout Edge
Name Type Net Macro Op Delay Total Fanout Edge
2
^a Summary
data required time 13.646 data arrival time - 5.629
1
4 Data arrival time calculation
0 my dk 0,000 0,000
7.5735 8.017 8.4605 8.904 9.347 CLK Clock source + 0.000 0.000 r

Figure 141 · Qaux0_filter Path Set

- 4. Click the Reset Filter button.
- 5. Right-click Register to Register and choose Add Set to open the Add Path Analysis Dialog box.



Add Path Analysis Set	? ***
Name :- Source pins:	Trace from :- Source to sink Sink to source Sink Pins:
Qaux[0]:CLK Qaux[1]:CLK Qaux[2]:CLK Qaux[3]:CLK	
Select All	Select All
Filter source pins: Pin Type: Registers by pin names * Filter	Filter sink pins: Pin Type: Registers by pin names * Filter
Help	OK Cancel

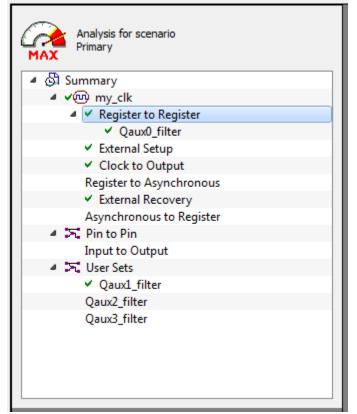
Figure 142 · Add Path Analysis Set

6. Use the values in the Table below to add timing path sets.

From	То	Name
Qaux[1]:CLK	*:D	Qaux1_filter
Qaux[2]:CLK	*:D	Qaux2_filter
Qaux[3]:CLK	*:D	Qaux3_filter

The path sets appear under User Sets in the Maximum Delay Analysis View (as shown in the figure above).





7. Close SmartTime and Libero SoC.



Tutorial 3 - Design Using Both Clock Edges

This tutorial analyzes SmartTime reports that include both rising and falling edges of a clock in the same design. The design (Figure 24) consists of a 16-bit serial-in parallel-out (SIPO) shift register. The shift register tmp1 is clocked on the rising edge of the clock. The output register tmp2 is clocked on the falling edge of the clock.

You will import the RTL verilog file shiftreg16.v and enter a clock constraint of 100 MHz. After routing the design you will analyze the timing to determine the maximum operating frequency and export a timing report.

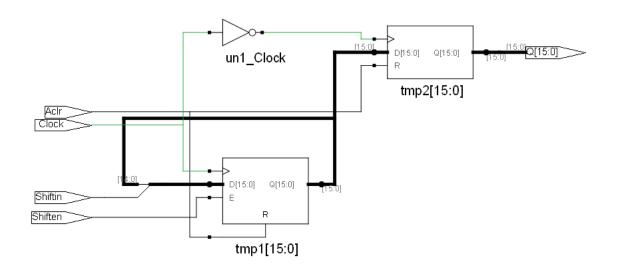


Figure 143 · Example Design that Uses Both Clock Edges

Set Up Your Example Design Project

- 1. Open Libero and create a new project (from the Project menu choose New Project).
- 2. Name the project **shiftreg16** and set the project location according to your preferences. Enter the following values for your new project:
 - Family: SmartFusion2
 - Die: M2S090TS
 - Package: FG 484
 - Speed: STD
 - Die Voltage: 1.2 V
 - Range: COM
- 3. Click Finish to create the project.

Import the Verilog Source File - Design Uses Both Clock Edges

You must import the shiftreg16.v Verilog file into your design for this tutorial. Download the design files from the Microsemi website.



To import the Verilog soure file:

- 1. From the File menu choose **Import > HDL Source Files**.
- 2. Browse to the location of the shiftreg16.v file you have downloaded and select it. Click **Open** to import the file.
- 3. Verify that the file appears in your project (as shown in the figure below).

Libero - D:\2Work\G4_SmartTime_UG\shiftreg16\shiftreg16.prjx*		
Project File Edit View Design Tools Help		
🗅 🚰 🔛 🔼 🖸 🗿 🔛		
Design Hierarchy 🗗 🗙	K Reports ♂ × StartPage ♂ × shiftreg16.v ♂ ×	=
Show: Components	$\mathbf{e} \equiv \mathbf{e}$	
🔺 🇰 work	<pre>49 _module shifttreg_16(Shiften, Shiftin, Aclr, Clock, Q); 50input Shiften;</pre>	^
shifttreg_16 (shiftreg16.v)	51 input Shiftin;	
(HDL	52 input Aclr;	
	53 input Clock;	
	54 output [15:0] Q;	
	55 56 reg [15:0] Oaux:	
	56 reg [15:0] Qaux; 57 reg [15:0] tmp1;	
	58 reg [15:0] tmp2;	
	59 59	
	always @ (posedge Aclr or posedge Clock)	
	61 begin	
	62	
	63 if (Aclr)	
	$64 \qquad Qaux = 0;$	=
	65 else if (Shiften) 66 Oaux = {Oaux[14:0], Shiftin};	
	66 Qaux = {Qaux[14:0], Shiftin}; 67 tmp1 = Qaux;	
	68	
	69 end	
	70 -	
	71 always @(negedge Clock)	-
Desi Design Stimulus Catalog Files HDL		
Log		₽×

Figure 144 · shifter.edn in the Design Hierarchy

Add a Clock Constraint - Design Uses Both Clock Edges

To add a clock constraint to your example design:

- 1. In the Design Flow window expand **Edit Constraint** and choose **Timing Constraints** (right-click) > **Open Interactively**.
- 2. This will trigger both synthesis and compile steps to run.
- 3. The SmartTime Constraints Editor GUI will open once compile step is completed.
- 4. Right-click in the Constraints pane on Requirements > Clock and choose Add clock constraint.
- 5. Enter a constraint with Clock Source (Clock), Clock Name (my_clk) of 100 MHz at a 50% duty cycle.



Create Clock Constraint					9	23
Clock Name : my_clk		Clock Source :	Clock		•	
	Period : 10	ns —	►	or Frequency:	100	Mhz
×						
	Duty cycle :					
Comment :						
Help				ОК	Can	cel

Figure 145 · Add 100 MHz Clock Constraint

The new constraint appears in the Constraints Editor (as shown in the figure below).

File Edit View Constra													
The Edit View Constra	ints l	ools F	Help										- 1
🎒 🙋 🎦 😏 🏂 🖌	2	m 🐮	n 🖏 🌠 🎠	🖄 🐄 🐒	🔉 📴 🌾) 💯 🗍 🖸							
straints Editor for scenario Prima													
su airts Euror for scenario Frina	y												
 Constraints 							-						Т
A Requirements			Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File	
Clock													
Generated Clock		1	Click here to add a c	onstraint									
Input Delay		2	*	my_clk	Clock	10.000	100.000	50.0000	rising 🚽	0.000	0 5	GUI	
Output Delay			· ·										-
 Exceptions 	=												
Max Delay													
Max Delay Min Delay													
Min Delay													
Min Delay Multicycle False Path Advanced													
Min Delay Multicycle False Path Advanced Clock Source Late	nc)												
Min Delay Multicycle False Path Advanced	nc)												
Min Delay Multicycle False Path Advanced Clock Source Late	-		٩										

Figure 146 · 100 MHz Clock Constraint in the Constraint Editor

- 6. Save the constraints (File > Save).
- 7. Exit SmartTime Constraints Editor (File > Exit).

Run Place and Route for a Design that Uses Both Clock Edges

To run Place and Route on the design 'shiftreg_16':

- 1. In the Design Flow window, right-click Place and Route and choose Configure Options.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at



the default settings. Click **OK** to exit the Layout Options Dialog box. Right-click Place and Route and choose **Run**.

A green check mark appears next to Place and Route to indicate successful completion of Place and Route.

Maximum Delay Analysis - Design Using Both Clock Edges

The SmartTime Maximum Delay Analysis window displays the design's maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. In the Design Flow window, right-click Verify Timing and choose **Open Interactively** to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below).

A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

e	SmartTir	ne - [Maximum Delay Analysis View]									- x
	File E	dit View Tools Help									_ 8 ×
	兰 🖌	l 🗅 🕑 🏂 🖌 Ə 🐵 🌫 👘									
Ma	iximum Dela	ay Analysis View									
	4	Analysis for scenario Primary Commy_clk V Register to Register External Setup Clock to Output Register to Asynchronous External Recovery Asynchronous to Register X Pin to Pin Input to Output X User Sets	Design Family Die Package Temperatu Voltage Ra Speed Gra Design Sta Data sourc Min Opera Max Opera Scenario fr	inge de itte e ting Condi ting Cond or Timing J	S N 44 0 1 S P P tions B	hiftreg_16 martFusion2 125090TS 84 FBGA - 85 C 14 - 1.26 V TD ost-Layout ost-Layout roduction EST - 1.26 V - 0 C /ORST - 1.14 V - 8 rimary					
			Clock	·	F	Description d	Described.	Enternal	E.t	Min Clock-To-	Max Clock-To-
			Domain	Period (ns)	Frequenc (MHz)	y Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)
		Select a set of paths to see its slack distribution.	my_clk	1.980	505.051	10.000	100.000	5.457	0.955	4.311	9.127
	# of paths			Min	Delay (ns)	Max Delay (ns)					
	4		Input to Ou	tput N/A		N/A					
		slack distribution(ns)									_
R	eady								Tem	p: 0 - 85 C Volt: 1.1	14 - 1.26 V Speed: STD

Figure 147 · Maximum Delay Analysis for Design shifter

The Summary in the Maximum Delay Analysis window indicates the maximum operating frequency for this design is 505.05 MHz.

- 2. Expand my_clk to display the Register to Register, External Setup and Clock to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.
- 4. Click to select row 1 and study the timing analysis (resize the Maximum Delay Analysis window as required). The path is from register tmp1 to register tmp2. Note that SmartTime uses 5 ns in the data required calculation (circled in red in the figure below). This is because the source flip-flop uses the rising edge of the clock and the destination flip-flop uses the falling edge of the clock.



Edit View Tools Help												
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Delay Analysis View												
	_											
Analysis for scenario Primary	Fre	om *				то	*					
🖓 Summary	- 6	ustomize table							Apply Filter	Store F	ilter	Reset Filte
⊿ v@ my_clk		astomic table							hppil i i i i i			COCCT NC
 Register to Register 							Required		Minimum Period			
External Setup		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	(ns)	Setup (ns)	(ns)	5	kew (ns)	
Clock to Output	1	tmp1[8]:CLK	tmp2[8]:D	0.574	4,159	5,554	9.713	0.298	1.68			-0.031
Register to Asynchronous												
External Recovery Asynchronous to Register	2	tmp1[0]:CLK	tmp2[0]:D	0.574	4.160	5.553	9.713	0.298	1.680	1		-0.032
4 🔀 Pin to Pin												
Input to Output	3	tmp1[10]:CLK	tmp2[10]:D	0.562	4.170	5.543	9.713	0.298	1.660			-0.030
T User Sets	4	1 1707 0011										
	4	tmp1[2]:CLK	tmp2[2]:D	0.573	4.172	5.552	9.724	0.298	1.656			-0.043
	5	tmp1[9]:CLK	tmp2[9]:D	0.571	4,172	5.552	9,724	0.298	1.656			-0.041
	-											
				1	1					1		
	Na	me		Туре	Net			N				nout Edg
			ID/U0_RGB1_RGB0:		Clock_i	ibuf_RNIHSID/I	J0_YWn		+	0.714		f
		tmp1[8]:CLK	SID/U0_RGB1_RGB0:	YL cell net	Charles	ibuf RNIHSID/I			DLIB:RGB +	0.372		12 r
		tmp1[8]:Q		cell	Clock_	IDUT_KINIHSID/I	JO_KOB1_KOB(DLIB:SLE +	0.024		2 r
		tmp2[8]:D		net	tmp1(8	31			+	0.472		- r
20		data arrival time									5.554	
16	4	Data_required_time	calculation							-		
8		my_clk		Clock Const						5.000		
4		Clock		Clock sourc					+	0.000		f
0 1.696 4.159 6.622 9.085 13	1.54	Clock_ibuf/U0/U_		net	Clock				+	0.000		f
1.696 4.159 6.622 9.065 1.		Clock_ibuf/U0/U_	IOPAD:Y	cell				A	DLIB:IOPAD_IN +	2.993	7.993	2 f
slack distribution(ns)	•											
	_											

Figure 148 · Slack Calculation in Maximum Delay Analysis View

Generate a Timing Report - Design Uses Both Clock Edges

Timing reports can be generated from SmartTime. Timing reports enable you to quickly determine if there are any timing problems. The timing report lists the following information:

- Design information including device, speed grade and operating conditions.
- Design performance summary (maximum frequency, external setup and hold, minimum and maximum clock-to-out)
- Clock domain details.
- Inter clock domain details.
- Pin to pin timing

The timing report can be printed and saved.

To generate a Timing Report:

1. From the **Maximum Delay Analysis View** menu, choose **Tools > Reports > Timer** to open the Timing Report Options Dialog box (as shown in the figure below).



I Timing Report Options		? ×
Option Categories Select a category: General Paths Sets Clock Domains	Display of paths Include detailed path information in this report Limit the number of paths per section to:	5
	Limit the number of expanded paths per section to:	-
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults
Help	(OK Cancel

Figure 149 · Timing Report Options Dialog Box

2. Click the **Paths** category. Limit the number of reported paths to **5 (default)**, and click **OK**. The timing report opens in a new window (as shown in the figure below).



File Actions Help		
Timing Report Max Delay An	alysis	
SmartTime Version v11.6		
	crosemi Libero Software Release v11.6 (Version 11.6.0.15)	
Date: Mon Apr 27 09:10:59	2015	
Design: shifttreg 16		
Family: SmartFusion2		
Die: M2S090TS		
Package: 484 FBGA		
Temperature Range: 0 - 85		
Voltage Range: 1.14 - 1.26	· •	
Speed Grade: STD		
Design State: Post-Layout Data source: Production		
Min Operating Conditions:	BEST - 1.26 V - 0 C	
Max Operating Conditions:		
Scenario for Timing Analys		
SUMMARY		
Clock Domain:	my_clk	
Period (ns):	1.980	
Frequency (MHz):	505.051	
Required Period (ns): Required Frequency (MHz):		
	5.457	
	0.955	
	4.311	
	9.127	
	Input to Output	
Min Delay (ns):	N/A	
Min Delay (ns):		
Min Delay (ns): Max Delay (ns): END SUMMARY	N/A	
Min Delay (ns): Max Delay (ns): END SUMMARY	N/A	
Min Delay (ns): Max Delay (ns): END SUMMARY Clock Domain my_clk	N/A N/A	
Min Delay (ns): Max Delay (ns): END SUMMARY Clock Domain my_clk Info: The maximum frequenc	N/A	
Min Delay (ns): Max Delay (ns): END SUMMARY Clock Domain my_clk Info: The maximum frequenc	N/A N/A	
Min Delay (ns): Max Delay (ns): END SUMMARY 	N/A N/A	

Figure 150 · Timing Report for shifter

The timing report contains the following sections:

- Header
- Summary
- Clock domain details for my_clk and expanded path information
- External setup information
- Clock to output delay information
- 3. Save the timing report (File > Save As...) as shifter_timing.rpt and close the report window.
- 4. Close SmartTime and Libero.



Tutorial 4 - False Path Constraints

This tutorial describes how to enter false path constraints in SmartTime. You will import an RTL source file from the design shown below. After routing the design, you will analyze the timing and set false path constraints and observe the maximum operating frequency in the SmartTime Timing Analysis window.

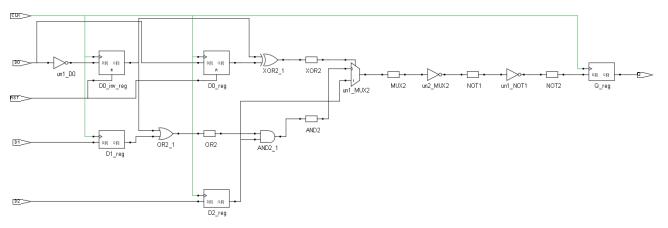


Figure 151 · Example Design with False Paths

Set Up Your False Path Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **false_path** and set the project location according to your preferences. Click **Next**. Enter the following values for your Device Selection settings:
 - Family: SmartFusion2
 - Die: M2S050
 - Package: 484 FBGA
 - Speed: STD
 - Die Voltage: 1.2 V
 - Range: COM
- 3. Click **Finish** to create the new project.

Import the false_path Verilog File and Add Constraints

You must import the false_path.v Verilog source file into your design for this tutorial. Download the design files from the Microsemi website.

To import the Verilog source file:

- 1. From the File menu, choose Import > HDL Source Files.
- 2. Browse to the location of the false_path.v file you have downloaded from the Microsemi website and select it. Click **Open** to import the file.
- 3. Verify that the file appears in your project (as shown in the figure below).

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



C Libero - D:\2Work\G4_SmartTime_UG\false_path\false_path.prjx*				
Project File Edit View Design Tools Help				
Design Hierarchy 8	× Re	ports 🗗 🗙	StartPage & × false_path.v & ×	Ŧ
Show: Components	-	<u> </u>		
✓ ₩ work		21 input 22 input 23 output 24	851; CLR; ; Q;	^
		25 reg 26 reg 27 reg 28 reg 29	D0_reg; D1_reg; D1_reg; D2_reg;	
		30 reg 31 32 wire	Q_reg; XOR2 /*synthesis syn_keep=1*/;	
		33 wire 34 wire 35 wire 36 wire 37 wire 38	AND2 /*synthesis syn_keep=1*/; ND2 /*synthesis syn_keep=1*/; ND32 /*synthesis syn_keep=1*/; ND32 /*synthesis syn_keep=1*/;	
		40 41 always 42 pbegin	<pre>1 Q = Q_reg /*synthesis syn_keep=1*/; 0 (posedge CLK or posedge RST) </pre>	E
			<pre>(RST) gin D0_reg <= 1'b0; D0_inv_reg <= 1'b0; dd </pre>	
		49 el 50 el be 51 52 53 er	.se igin DD_reg <= D0; DD_rteg <= -D0; d	
(57 assign	x X0R2 = D0_reg ^ D0_inv_reg; 0R2 = D0_inv_reg D1_reg;	-

Figure 152 · false_path Design in Design Hierarchy

- In the Design Flow window, double-click Synthesize to run synthesis.
 A green check mark appears when the Synthesis step completes successfully.
- In the Design Flow window double-click **Compile** to Compile with default settings.
 A green check mark appears next to Compile to indicate that it has completed successfully.
- 6. Expand Edit Constraints. Right-click Timing Constraints and choose Open Interactively.
- 7. In the SmartTime Constraints Editor, right-click Requirements > Clock and choose Add clock constraint under the Constraints pane on the left.
- 8. Enter a constraint for the clock source (**CLK**) with clock name (my_clk) of **100 MHz** (50% duty cycle), as shown in the figure below.

SmartTime - [Constraints Edito	or for s	cenario Primary]									
File Edit View Constrain	nts 1	Tools Help									- 5
🖬 💁 🎦 😏 🍝	α	* * * *	W. W.	30N 365	5 (G)	n D.					
		JUL AND EN PE	a (r •	nn 🥐	(+) -820	₩ . .					
straints Editor for scenario Primary	y										
Constraints								1			
A Requirements		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	
Clock			Name	Source	(IIS)	(PIEZ)	(%)		(IIS)		
Generated Clock	1	Click here to add a c	constraint								
Input Delay	2	٣	my_clk	CLK	10.000	100.000	50.0000	risina 👻	0.000	0 5	GUI
Output Delay		P		CER							
▲ Exceptions											
Max Delay											
Min Delay											
Multicycle											
🕈 False Path											
Advanced											
Clock Source La											
Disable Timing											
Clock Uncertain											
4 III +		•									•
								Temp: () - 85 C Vol	t: 1.14 - 1.26 V	Speed: STD
								Trempt of			1-2-0-010

Figure 153 · Clock Constraint of 100 MHz in false_path design



9. Save your changes (File > Save) and close SmartTime (File > Close).

Place and Route Your FALSE_PATH Design

1. In Libero SoC, right-click Place and Route and choose Configure Options.

Layout Options
☑ Timing-driven
Power-driven
High Effort Layout
Repair Minimum Delay Violations
Incremental Layout
Use Multiple Passes
Configure
Help OK Cancel

Figure 154 · Layout Options

2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to close the Layout Options dialog box.

- 3. Right-click Place and Route and choose Run.
 - A green check mark appears next to Place and Route in the Design Flow Window when Place and Route completes successfully.



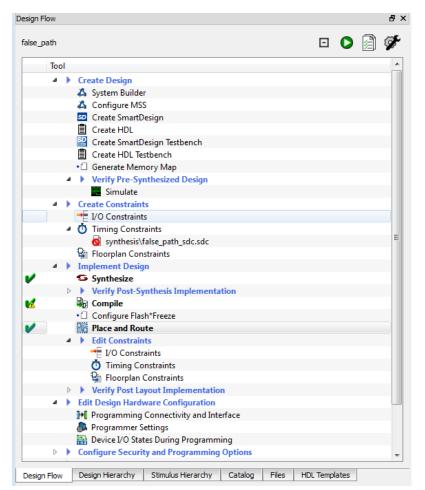


Figure 155 · Synthesize, Compile and Place and Route Successful Completion

Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Expand Verify Post Layout Implementation. Right-click Verify Timing and choose **Open Interactively** to open SmartTime. The Maximum Delay Analysis View appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at a maximum frequency of 442.48 MHz.

Note: You may see a slightly different maximum frequency with a different Libero software version.



	ime - [Minimum Delay Analysis View] Edit View Tools Help									- 8 ×
i 🖬 🖆	2 🞦 🕑 🏂 🖌 🖉 😁 🤜									
Minimum Dela	ay Analysis View									
	Analysis for scenario Primary	Design		false_path						
		Family		SmartFusion	2					
	Summary √ໜ my_clk	Die		M2S050						
	✓ Register to Register	Package		484 FBGA						
	External Hold Clock to Output	Temperature	Range	0 - 85 C						
	Register to Asynchronous	Voltage Ran		1.14 - 1.26 V						
	External Removal Asynchronous to Register	Speed Grad	~	STD						
1 4	P. Pin to Pin	Design Stat	e	Post-Layout						
	Input to Output St User Sets	Data source		Production						
	PL USE JES	Min Operation	ng Conditions	BEST - 1.26	V - 0 C					
		Max Operat	ing Conditions	WORST - 1.1	4 V - 85 C					
		Scenario for	Timing Analys	sis Primary						
		Summai	rv.							
		Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Out (ns)
I	Select a set of paths to see its slack distribution.	my_clk	2.260	442.478	10.000	100.000	-0.025	0.753	5.117	9.781
# of paths			1							·
jo a				y (ns) Max Dela	iy (ns)					
		Input to Out	put N/A	N/A						
	slack distribution(ns)									
		_							Temp: 0 - 85 C	olt: 1.14 - 1.26 V Speed: STD
_									Trendrie and It	The second

Figure 156 · Maximum Delay Analysis Summary

- 2. Expand my_clk to expand the display and show the Register to Register path sets.
- 3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
- 4. Click to select the row in the path list with the path is from the CLK pin of flip-flop D0_inv_reg to the D input of flip-flop Q_reg. Note that the path goes through the S input of multiplexer un1_MUX2.

Figure 48 shows that the S input of un1_MUX2 will always be logic 1; consequently, all the paths through the 0 input of un1_MUX2 and the S input of un1_MUX2 are false paths. You must set a false path on these paths in order to determine the true maximum operating frequency.

5. To set the path from D0_inv_reg:CLK to Q_reg :D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint** (as shown in the figure below). The Set False Path Constraint dialog box appears.

martTime - [Maximum Delay Analysis View]											
File Edit View Tools Help											+
imum Delay Analysis View											
Analysis for scenario Primary		om * Listomize table]					TC	o *		Apply Fitter] [Store Filter] [Reset Filter]
External Setup Clock to Output Register to Asynchronous External Recovery		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
Asynchronous to Register	1	D0_mv_reg:CLK	Q_ingiD	1.906	2.740					0.056	
Pin to Pin Input to Output	2	D0_reg:CLK	Copy Print		7.882	5.745	13.627	0.298	2.118	0.066	
Cliser Sets	3	D1_reg:CLK	Add False Path Co	and sound	7.896	5.731	13.627	0.298	2,104	0.067	
	4	02_reg:CLK	Add Max Delay Co	onstraint <table-cell></table-cell>	8.294	5.333	13.627	0.298	1.706	0.067	
	-	1	Add Min Delay Co Add Multicycle Pi		-						
			Expand selected p	aths							

Figure 157 · Right-Click > Add False Path Constraint



Set False Path Constraint		? x
From :		
þ0_inv_reg:CLK	*	
4	Ψ •	
Through :		
	*	
4	•	
То :		
Q_reg:D	*	
4	Ψ.	
Comment :		
Help	C	ancel

Figure 158 · Set False Path Constraint Dialog Box

- 6. Click **OK** to close the Set False Path Constraint dialog box.
- 7. From the View menu choose Recalculate All to recalculate the delays.
- 8. There are a total of three register-to-register false paths in this design (see Table x below). Repeat steps 5 through 8 to set the false path constraint on the other two false paths (#2 and #3) using the values as shown in the table below.

False Path	From	То
False Path #1	D0_inv_reg:CLK	Q_reg:D
False Path #2	D0_reg:CLK	Q_reg:D
False Path #3	D1_reg:CLK	Q_reg:D

9. Open the Constraint Editor (**Tools > Constraints Editor**) and click **Exceptions > False** Path (in the left pane under Constraints). The three False Path constraints are listed (as shown in the figure below).



🕰 🎦 😏 🏂 🍝 🖉	m	🀜 🐎 🏍 🔭 🎘	👷 🔈 😭 🗐 🔅	3			
ints Editor for scenario Primary							
Constraints							
A Requirements		Syntax	From	Through	То	File	Commen
Clock	1	Click here to add a constrair				GUI	
Generated Clock							
Input Delay	2	Y	D0_inv_reg:CLK		Q_reg:D	GUI	
Output Delay	3	*	D0_reg:CLK		Q_reg:D	GUI	
 Exceptions Max Delay 	4	· ·	D1_reg:CLK		Q_reg:D	GUI	
Min Delay	-	7	DI_legicik		Q_regio	901	
Multicycle							
Multicycle False Path Advanced							
Multicycle False Path Advanced	nstraints	of this kind are correct and	l valid.				
Multicycle False Path Advanced	nstraints	of this kind are correct and	l valid.				
Multicycle * False Path Advanced Clock Source La All co	nstraints	of this kind are correct and	l valid.				
Multicycle * False Path Advanced Clock Source La All co Disable Timing	nstraints	of this kind are correct and	l valid.				
Multicycle * False Path Advanced Clock Source La All co Disable Timing	nstraints	of this kind are correct and	l valid.				
Multicycle * False Path Advanced Clock Source La All co Disable Timing	nstraints	of this kind are correct and	i valid.				
Multicycle * False Path Advanced Clock Source La All co Disable Timing	nstraints	of this kind are correct and	l vəlid.				
Multicycle * False Path Advanced Clock Source La All co Disable Timing	nstraints	of this kind are correct and	i valid.				

Figure 159 · False Path Constraints in the SmartTime Constraint Editor

 View the summary in the Maximum Delay Analysis View (Tools > Max Delay Analysis). Note that SmartTime now reports the maximum operating frequency as 586.17 MHz (as shown in the figure below).

Note: The maximum operating frequency may vary slightly with a different version of the Libero software.

2	🔉 🕒 😏 🍝 🛠 😕 📼 ≍									
um Dela	y Analysis View									
2	Analysis for scenario Primary	Design		false	nath					
MAX ▲ ⓒI Summary ▲ ✓ my_clk ← Register to Register External Setup			Family		tFusion2					
			Die		050					
			Package		BGA					
			Temperature Range		50					
	Clock to Output Register to Asynchronous	Voltage Ra			- 1.26 V					
External Recovery		Speed Grad			1.20 V					
4.5	Asynchronous to Register		Design State		Layout					
	Input to Output		Data source		uction					
2	User Sets		Min Operating Conditions		T - 1.26 V - 0 C					
			Max Operating Condition		ST - 1.14 V - 85 C					
			Scenario for Timing Analy							
		Summa	ry							
	Select a set of paths to see its slack distribution.	Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)
		my_clk	1.706	586.166	10.000	100.000	-0.025	0.753	5.117	9.781
Į			Min f)olay (nc) M	ax Delay (ns)					
	slack distribution(ns)	Input to Ou		N/						

Figure 160 · Maximum Delay Analysis View - Summary

11. Select the **Register to Register** set for my_clk. Observe that only one path is visible, from D2_reg: CLK to Q_reg:D. This is the only path that propagates a signal (as shown in the figure below).



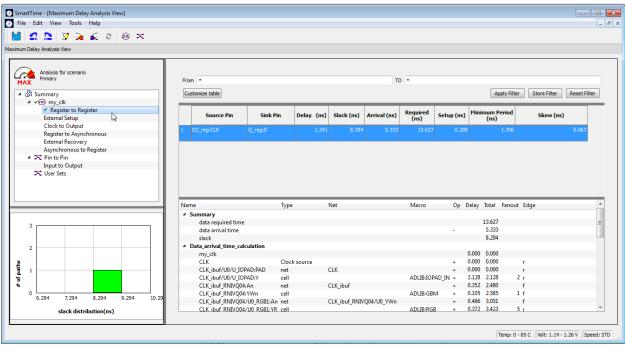


Figure 161 · Maximum Delay Analysis View - Register to Register

- 12. Close SmartTime.
- 13. Close Libero SoC.



Tutorial 5 - Cross Clock Domain Analysis

SmartTime performs inter-clock domain timing checks for designs that contain functional paths that cross two clock domains (the register launching the data and the register capturing the data are clocked by two different clock sources). Accurate specification of both clocks is required to allow a valid interclock domain timing check.

SmartTime analyzes each inter-clock domain by determining a common period equal to the least common multiple of the two clock periods.

For setup check, the tightest launch-capture time period is considered to ensure that the data arrives before the capture edge (as shown in the figure below). The hold check verifies that a setup relationship is not overwritten by a following data launch.

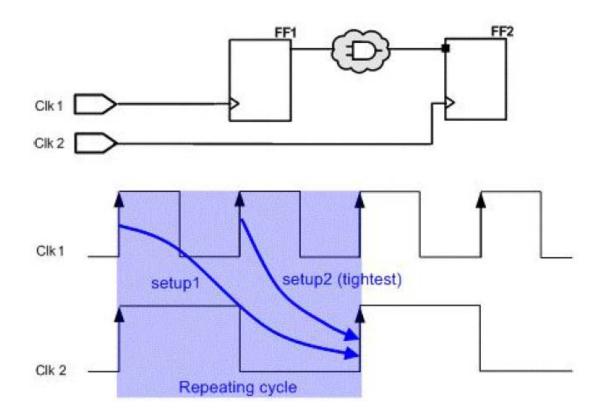


Figure 162 · Tightest Launch - Capture Relation for Setup Check in SmartTime

In this tutorial you will:

- 1. Create a new Libero project.
- 2. Import a Verilog source file for the design shown in the figure below.
- 3. Enter timing constraints for the two clock domains.
- 4. Use SmartTime to analyze the inter-clock domain timing.



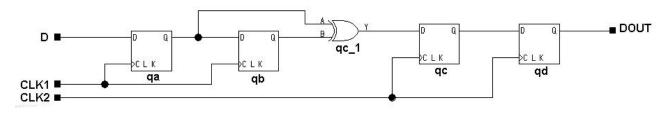


Figure 163 · Inter-Clock Domain Example Design Diagram

Set Up Your Cross Clock Domain Analysis Example Design Project

- 1. Open Libero and create a new project (from the Project menu choose New Project).
- 2. Name the project **multi_clocks** and set the project location according to your preferences. Enter the following values for your new project:
 - **Family**: SmartFusion2
 - Die: M2S050
 - Package: 484 FBGA
 - Speed: STD
 - Core Voltage: 1.2 V
 - Range: COM

Leave all other fields at their default values.

📀 New project								- • ×
Device selection Select a part for your project	from the part number list						Selected part	M25050-FG484
Project Details	Part filter Family: SmartFu Speed: STD	sion2 🔻		M2S050 1.2	Packag Rang	e: COM	• • et filters	
Device Settings	Search part:							
Design Template	Part Number M2S050-FG484	4LUT 56340	DFF 56340	User I/Os 267	uSRAM 1K 72	LSRAM 18K 69	Math (18x18) 72	PLLs and 6
Add HDL Sources								
Add Constraints								
Liberoo System-on-Chip	•							4
Help					< E	Back Next	> Finish	Cancel

Figure 164 · multi_clocks Project Settings

3. Click Finish to create the new project.



Import Verilog Source File and Run Compile for Cross Clock Domain Analysis Example

You must import the multi_clk.v file into your design for this tutorial. Download the design files from the Microsemi website.

To import and constrain the Verilog source file:

- 1. From the File menu choose Import > HDL Source Files
- 2. Choose HDL Source Files from the file type dropdown list in the Import Files dialog box.
- 3. Browse to the location of the **multi_clk.v** file you have downloaded and select it. Click **Open** to import the file.
- 4. Verify that the file appears in the Design Hierarchy window of your project (as shown in the figure below).

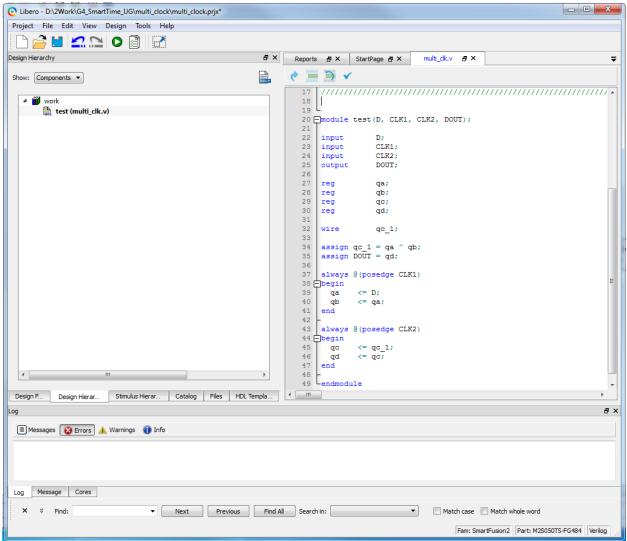


Figure 165 · multi_clocks Design in the Design Hierarchy Window and HDL Editor

5. Double-click **Compile** in the Design Flow window to run Synthesis first and then Compile with default settings.

A green check mark appears next to Compile when it has run successfully (as shown in the figure below).



Design Flow	1		₽×
test		D) ø
T	ool		*
	4) (Create Design	
		🔓 System Builder	
	4	💪 Configure MSS	
	s	Create SmartDesign	
		Create HDL	
	S	🖁 Create SmartDesign Testbench	-
		Create HDL Testbench	=
	•	🗇 Generate Memory Map	
	⊿	Verify Pre-Synthesized Design	
		Simulate	
4		Create Constraints	
		E I/O Constraints	
	_ ⊿ (Timing Constraints	
		Synthesis\test_sdc.sdc	
	1	Floorplan Constraints	
		mplement Design	
V		Synthesize	
	⊿	Verify Post-Synthesis Implementation	
_	_	Simulate	
		Compile	
		Configure Flash*Freeze	
	2	Place and Route	
	⊿	Edit Constraints	
		➡ I/O Constraints	
		Diming Constraints	
		💱 Floorplan Constraints	
	⊿	Verify Post Layout Implementation	-
•		Concrete Pack Annotated Eller	•
Catalog	Desi	Design Hi Stimulus Hi Files	HDL Te

Figure 166 · Design Flow Window – Synthesize and Compile Successful

Enter Timing Constraints for the Cross Clock Domain Analysis Example

To add a clock constraint to your example design:

- 1. In the Design Flow window, expand **Edit Constraints**. Right-click Timing Constraints and choose **Open Interactively**, to open the SmartTime Constraints Editor.
- 2. In the Constraint Browser, expand Requirements and double-click **Clock** to enter the following clock constraints:



- Clock Source: CLK1, Clock Name: my_clk1, Frequency:250 MHz
- Clock Source: CLK2, Clock Name: my_clk2, Frequency:100 MHz
- 3. Verify that your new constraints are listed in the Constraints Editor (as shown in the figure below).

🕒 SmartTime - [Constraints Editor for scenario Primary]												
🖸 File Edit View Constraints Tools Help												
Constraints Editor for scenario Primary												
······································												
Constraints A Requirements		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File	Comments
Clock Generated Clock	1	Click here to add a co					50.0000	rising 👻	0.000	0 0	GUI	
Input Delay	2	٣	my_dk1					rising 👻	0.000			
Output Delay =	3	٣	my_dk2	CLK2	10.000	100.000	50.0000	risina 👻	0.000	0 5	GUI	
A Exceptions		X		CERE								
Max Delay												
Min Delay Multicycle												
False Path												
4 Advanced												
Clock Source Latency +												
<												
											Temp: 0 - 85	5 C Volt: 1.14 - 1.26 V Speed: STD

Figure 167 · Clock Constraints in the SmartTime Constraints Editor

- 4. Click Save to save your constraints.
- 5. Open the Max Delay Analysis View (Tools > Max Delay Analysis).
- Choose Tools > Options. Ensure that the checkbox to Include inter-Clock domain analysis in calculations for timing analysis is enabled (default) as shown in the figure below.

SmartTime Options	
Option Categories Select a category: General Analysis Advanced	General Operating Conditions Perform maximum delay analysis based on WORST case Perform minimum delay analysis based on BEST case Clock Domains Include inter-clock domains in calculations for timing analysis. Enable recovery and removal checks. Restore Defaults
Help	OK Cancel

Figure 168 · Inter-Clock Domain Analysis Enabled in the SmartTime Options Dialog Box

7. Exit SmartTime (File > Exit).



Place and Route Your Cross Clock Domain Analysis Example

To run Place and Route on multi_clocks:

- 1. Right-click Place and Route in the Design Flow window.and choose Configure Options.
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings (as shown in the figure below).
- 3. Click OK to close the Layout Options dialog box.
- 4. Right-click Place and Route and choose **Run**.

A green check mark appears next to Place and route when it completes successfully.

Layout Options	? X							
Timing-driven								
Power-driven								
High Effort Layout								
Repair Minimum Delay Violations								
 Incremental Layout Use Multiple Passes Configure 								
Comgue								
Help ОК	Cancel							

Figure 169 · Layout Options - multi_clocks

Analyze Inter-Clock Domain Timing

Inter-clock domain timing enables you to analyze timing for designs that contain functional paths that cross two clock domains.

To analyze inter-clock domain timing:

- 1. Right-click Verify Timing and choose Open Interactively to open the Maximum Delay Analysis View.
- 2. Expand the my_clk2 path in the Maximum Delay Analysis View. Click to select the my_clk1 to my_clk2 path and observe the inter-clock domain path timing (as shown in the figure below).



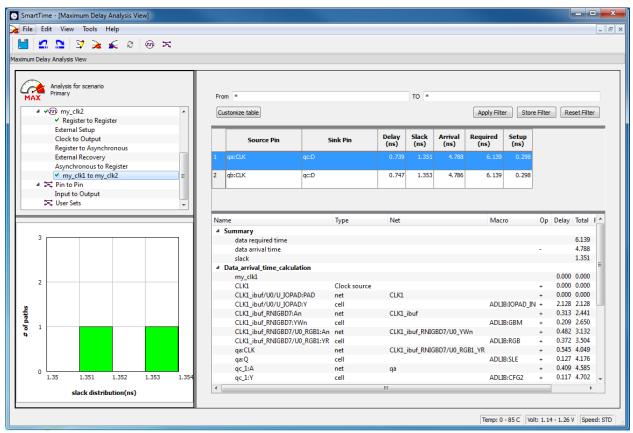
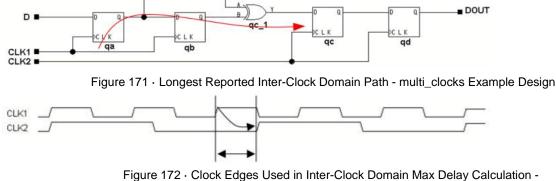


Figure 170 · Maximum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design

The Paths list shows the detailed timing analysis. The longest reported path is from qa:clk to qc:d (as shown in the figure below). This path has a slack of 1.351 ns. The clock edges used in the calculation are shown in the timing diagram below.

Note: The actual slack value may vary with different die size and different Libero SoC versions.



gure 172 · Clock Edges Used in Inter-Clock Domain Max Delay Calculation multi_clocks Example Design

- 3. Click Tools and choose Minimum Delay Analysis.
- 4. Expand the CLK2 paths in the Minimum Delay Analysis View. Click to select my_clk1 to_my_clk2 path and observe the inter-clock domain path timing (as shown in the figure below).



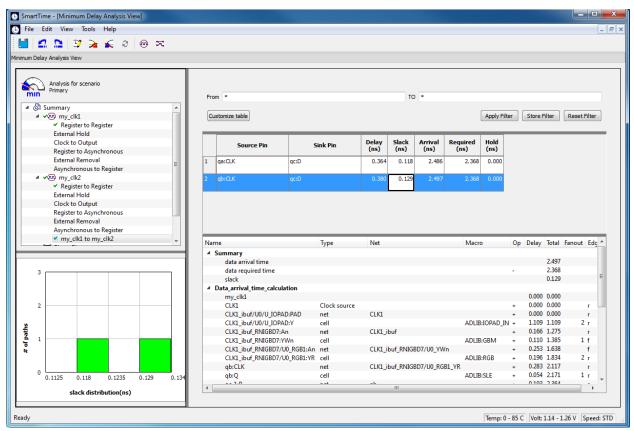


Figure 173 · Minimum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design

The Paths list shows the detailed timing analysis. The shortest reported path is from qb:clk to qc:d (as shown in the figure below). This path has a positive slack of 0.129 ns. The clock edges used in the calculation are shown in the Figure 68.

Note: The actual slack value may vary with different die size and different versions of Libero SoC.

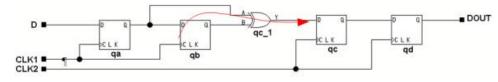


Figure 174 · Shortest Reported Inter-Clock Domain Path - multi_clocks Example Design

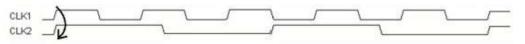


Figure 175 · Clock Edges Used in Inter-Clock Domain Min Delay Calculation - multi_clocks Example Design

- 5. Exit SmartTime (File > Exit).
- 6. Exit Libero (Project > Exit).



Tcl Commands

all_inputs

Tcl command; returns an object representing all input and inout pins in the current design.

all_inputs

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Exceptions

You can only use this command as part of a –from, -to, or –through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path</u>, and <u>set false path</u>.

Examples

set_max_delay -from [all_inputs] -to [get_clocks ck1]

See Also

Tcl documentation conventions Designer Tcl Command Reference

all_outputs

Tcl command; returns an object representing all output and inout pins in the current design.

all_outputs

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Exceptions

You can only use this command as part of a -from, -to, or -through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path, and set false path.</u>

Examples

set_max_delay 1.2 -from [all_inputs] -to [all_outputs]

See Also

Tcl documentation conventions



Designer Tcl Command Reference

all_registers

Tcl command; returns an object representing register pins or cells in the current scenario based on the given parameters.

```
all_registers [-clock clock_name]
[-async_pins][-output_pins][-data_pins][-clock_pins]
```

Arguments

-clock clock_name

Specifies the name of the clock domain to which the registers belong. If no clock is specified, all registers in the design will be targeted.

-async_pins

Lists all register pins that are async pins for the specified clock (or all registers asynchronous pins in the design).

-output_pins

Lists all register pins that are output pins for the specified clock (or all registers output pins in the design). -data pins

Lists all register pins that are data pins for the specified clock (or all registers data pins in the design). -clock_pins

Lists all register pins that are data pins for the specified clock (or all registers clock pins in the design).

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Exceptions

You can only use this command as part of a -from, -to, or -through argument in the following Tcl commands: <u>set min delay, set max delay, set multicycle path</u>, and <u>set false path</u>.

Examples

```
set_max_delay 2.000 -from { ff_m:CLK ff_s2:CLK } -to [all_registers -clock_pins -clock { ff_m:Q }]
```

See Also

Tcl documentation conventions Designer Tcl Command Reference

check_timing_constraints

Tcl command; checks all timing constraints in the current timing scenario for validity.

check_timing_constraints

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Examples

check_timing_constraints

See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

clone_scenario

Tcl command; creates a new timing scenario by duplicating an existing one. You must provide a unique name (that is, it cannot already be used by another timing scenario).

clone_scenario original new_scenario_name

Arguments

original

Specifies the name of the source timing scenario to clone (copy). The source must be a valid, existing timing scenario.

new_scenario_name

Specifies the name of the new scenario to be created.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

This command creates a timing scenario with the new_scenario_name ,

which includes a copy of all constraints in the original scenario. The new scenario is then added to the list of scenarios.

Example

clone_scenario primary my_new_scenario

See Also

create_scenario delete_scenario Tcl documentation conventions Designer Tcl Command Reference

create_clock

Tcl command; creates a clock constraint on the specified ports/pins, or a virtual clock if no source other than a name is specified.

```
create_clock -period period_value [-name clock_name]
[-waveform> edge_list][source_objects]
```

Arguments

-period period_value

Specifies the clock period in nanoseconds. The value you specify is the minimum time over which the clock waveform repeats. The period_value must be greater than zero. -name clock_name



Specifies the name of the clock constraint. You must specify either a clock name or a source.

-waveform edge_list

Specifies the rise and fall times of the clock waveform in ns over a complete clock period. There must be exactly two transitions in the list, a rising transition followed by a falling transition. You can define a clock starting with a falling edge by providing an edge list where fall time is less than rise time. If you do not specify -waveform option, the tool creates a default waveform, with a rising edge at instant 0.0 ns and a falling edge at instant (period_value/2)ns.

source_objects

Specifies the source of the clock constraint. The source can be ports, pins, or nets in the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing one. You must specify either a source or a clock name.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Creates a clock in the current design at the declared source and defines its period and waveform. The static timing analysis tool uses this information to propagate the waveform across the clock network to the clock pins of all sequential elements driven by this clock source.

The clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Examples

The following example creates two clocks on ports CK1 and CK2 with a period of 6, a rising edge at 0, and a falling edge at 3:

create_clock -name {my_user_clock} -period 6 CK1

create_clock -name {my_other_user_clock} -period 6 -waveform {0 3} {CK2}

The following example creates a clock on port CK3 with a period of 7, a rising edge at 2, and a falling edge at 4:

create_clock -period 7 -waveform {2 4} [get_ports {CK3}]

See Also

create_generated_clock Tcl Command Documentation Conventions Designer Tcl Command Reference

create_generated_clock

Tcl command; creates an internally generated clock constraint on the ports/pins and defines its characteristics.

```
create_generated_clock [-name name] -source reference_pin [-divide_by divide_factor] [-
multiply_by multiply_factor] [-invert] source
```

Arguments

-name name

Specifies the name of the clock constraint.

-source reference_pin

Specifies the reference pin in the design from which the clock waveform is to be derived. -divide_by <u>divide_factor</u>



Specifies the frequency division factor. For instance if the *divide_factor* is equal to 2, the generated clock period is twice the reference clock period.

-multiply_by multiply_factor

Specifies the frequency multiplication factor. For instance if the *multiply_factor* is equal to 2, the generated clock period is half the reference clock period.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

source

Specifies the source of the clock constraint on internal pins of the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing clock. Only one source is accepted. Wildcards are accepted as long as the resolution shows one pin.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

Creates a generated clock in the current design at a declared source by defining its frequency with respect to the frequency at the reference pin. The static timing analysis tool uses this information to compute and propagate its waveform across the clock network to the clock pins of all sequential elements driven by this source.

The generated clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Examples

The following example creates a generated clock on pin U1/reg1:Q with a period twice as long as the period at the reference port CLK.

create_generated_clock -name {my_user_clock} -divide_by 2 -source [get_ports
{CLK}] U1/reg1:Q

The following example creates a generated clock at the primary output of myPLL with a period ³/₄ of the period at the reference pin clk.

create_generated_clock -divide_by 3 -multiply_by 4 -source clk [get_pins {myPLL:CLK1}]

See Also

<u>create_clock</u> <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

create_scenario

Tcl command; creates a new timing scenario with the specified name. You must provide a unique name (that is, it cannot already be used by another timing scenario).

create_scenario name

Arguments

name

Specifies the name of the new timing scenario.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.



Description

A timing scenario is a set of timing constraints used with a design. Scenarios enable you to easily refine the set of timing constraints used for Timing-Driven Place-and-Route, so as to achieve timing closure more rapidly.

This command creates an empty timing scenario with the specified name and adds it to the list of scenarios.

Example

create_scenario scenario_A

See Also

<u>clone_scenario</u> <u>Tcl Command Documentation Conventions</u> Designer Tcl Command Reference

get_cells

Tcl command; returns an object representing the cells (instances) that match those specified in the pattern argument.

get_cells pattern

Arguments

pattern

Specifies the pattern to match the instances to return. For example, "get_cells U18*" returns all instances starting with the characters "U18", where "*" is a wildcard that represents any character string.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

This command returns a collection of instances matching the pattern you specify. You can only use this command as part of a –from, -to, or –through argument in the following Tcl commands: <u>set_max delay</u>, <u>set_multicycle_path</u>, and <u>set_false_path</u>.

Examples

set_max_delay 2 -from [get_cells {reg*}] -to [get_ports {out}]
set_false_path -through [get_cells {Rblock/muxA}]

See Also

get_clocks get_nets get_pins get_ports <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

get_clocks

Tcl command; returns an object representing the clock(s) that match those specified in the pattern argument in the current timing scenario.



get_clocks pattern

Arguments

pattern

Specifies the pattern to use to match the clocks set in SmartTime or Timer.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

- If this command is used as a -from argument in either the set maximum (<u>set_max_delay</u>), or set minimum delay (<u>set_min_delay</u>), false path (<u>set_false_path</u>), and multicycle constraints (<u>set_multicycle_path</u>), the clock pins of all the registers related to this clock are used as path start points.
- If this command is used as a -to argument in either the set maximum (<u>set_max_delay</u>), or set minimum delay (<u>set_min_delay</u>), false path (<u>set_false_path</u>), and multicycle constraints (<u>set_multicycle_path</u>), the synchronous pins of all the registers related to this clock are used as path endpoints.

Example

set_max_delay -from [get_ports datal] -to \
[get_clocks ck1]

See Also

create_clock create_generated_clock Tcl Command Documentation Conventions Designer Tcl Command Reference

get_current_scenario

Tcl command; returns the name of the current timing scenario.

get_current_scenario

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

get_current_scenario

See Also

set_current_scenario Tcl documentation conventions Designer Tcl Command Reference



get_nets

Tcl command; returns an object representing the nets that match those specified in the pattern argument.

get_nets pattern

Arguments

pattern

Specifies the pattern to match the names of the nets to return. For example, "get_nets N_255*" returns all nets starting with the characters "N_255", where "*" is a wildcard that represents any character string.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

This command returns a collection of nets matching the pattern you specify. You can only use this command as source objects in create clock (create_clock) or create generated clock (create_generated clock) constraints and as -through arguments in the set false path, set minimum delay, set maximum delay, and set multicycle path constraints.

Examples

set_max_delay 2 -from [get_ports RDATA1] -through [get_nets {net_chkp1 net_chkqi}]
set_false_path -through [get_nets {Tblk/rm/n*}]
create_clock -name mainCLK -period 2.5 [get_nets {cknet}]

See Also

create_clock create_generated_clock set_false_path set_min_delay set_max_delay set_multicycle_path Tcl documentation conventions Designer Tcl Command Reference

get_pins

Tcl command; returns an object representing the pin(s) that match those specified in the pattern argument.

get_pins pattern

Arguments

pattern

Specifies the pattern to match the pins to return. For example, "get_pins clock_gen*" returns all pins starting with the characters "clock_gen", where "*" is a wildcard that represents any character string.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Example

create_clock -period 10 [get_pins clock_gen/reg2:Q]

See Also

create_clock create_generated_clock set_clock_latency set_false_path set_min_delay set_max_delay set_multicycle_path Tcl documentation conventions Designer Tcl Command Reference

get_ports

Tcl command; returns an object representing the port(s) that match those specified in the pattern argument.

get_portspattern

Argument

```
pattern
```

Specifies the pattern to match the ports.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Example

create_clock -period 10 [get_ports CK1]

See Also

create_clock set_clock_latency set_input_delay set_output_delay set_min_delay set_max_delay set_false_path set_multicycle_path Tcl documentation conventions Designer Tcl Command Reference

list_clock_latencies

Tcl command; returns details about all of the clock latencies in the current timing constraint scenario.

list_clock_latencies



Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Examples

puts [list_clock_latencies]

See Also

set_clock_latency remove_clock_latency Tcl documentation conventions Designer Tcl Command Reference

list_clock_uncertainties

Tcl command; returns details about all of the clock uncertainties in the current timing constraint scenario.

```
list_clock_uncertainties
```

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

list_clock_uncertainties

See Also

set_clock_uncertainty
remove_clock_uncertainty
Designer Tcl Command Reference

list_clocks

Tcl command; returns details about all of the clock constraints in the current timing constraint scenario.

list_clocks

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

puts [list_clocks]



See Also

create_clock remove_clock Tcl documentation conventions Designer Tcl Command Reference

list_disable_timings

Tcl command; returns the list of disable timing constraints for the current scenario.

list_disable_timings

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Example

list_disable_timings

See Also

Designer Tcl Command Reference

list_false_paths

Tcl command; returns details about all of the false paths in the current timing constraint scenario.

list_false_paths

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

puts [list_false_paths]

See Also

set_false_path remove_false_path Tcl documentation conventions Designer Tcl Command Reference

list_generated_clocks

Tcl command; returns details about all of the generated clock constraints in the current timing constraint scenario.

list_generated_clocks



Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

puts [list_generated_clocks]

See Also

create_generated_clock remove_generated_clock Tcl documentation conventions Designer Tcl Command Reference

list_input_delays

Tcl command; returns details about all of the input delay constraints in the current timing constraint scenario.

list_input_delays

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Examples

puts [list_input_delays]

See Also

set_input_delay remove_input_delay Tcl documentation conventions Designer Tcl Command Reference

list_max_delays

Tcl command; returns details about all of the maximum delay constraints in the current timing constraint scenario.

list_max_delays

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Examples

```
puts [list_max_delays]
```

See Also

set_max_delay remove_max_delay Tcl documentation conventions Designer Tcl Command Reference

list_min_delays

Tcl command; returns details about all of the minimum delay constraints in the current timing constraint scenario.

list_min_delays

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

puts [list_min_delays]

See Also

set_min_delay remove_min_delay Tcl documentation conventions Designer Tcl Command Reference

list_multicycle_paths

Tcl command; returns details about all of the multicycle paths in the current timing constraint scenario.

list_multicycle_paths

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Examples

puts [list_multicycle_paths]

See Also

set_multicycle_path
remove_multicycle_path
Tcl documentation conventions



Designer Tcl Command Reference

list_objects

Tcl command; returns a list of object matching the parameter. Objects can be nets, pins, ports, clocks or instances.

list_objects <object>

Arguments

Any timing constraint parameter.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Example

The following example lists all the inputs in your design: list_objects [all_inputs] You can also use wildcards to filter your list, as in the following command: list_objects [get_ports a*]

See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

list_output_delays

Tcl command; returns details about all of the output delay constraints in the current timing constraint scenario.

list_output_delays

Arguments

None

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Examples

puts [list_output_delays]

See Also

set_output_delay remove_output_delay Tcl documentation conventions Designer Tcl Command Reference



list_paths

Tcl command; returns a list of the *n* worst paths matching the arguments. The number of paths returned can be changed using the set_options -limit_max_paths <value> command.

```
list_paths
-analysis <max | min>
-format <csv | text>
-set <name>
-clock <clock name>
-type <set_type>
-from_clock <clock name>
-to_clock <clock name>
-in_to_out
-from <port/pin pattern>
-to <port/pin pattern>
```

Arguments

-analysis <max | min>

Specifies whether the timing analysis is done for max-delay (setup check) or min-delay (hold check). Valid values are: max or min.

```
-format < text | csv >
```

Specifies the list format. It can be either text (default) or csv (comma separated values). Text format is better for display and csv format is better for parsing.

-set <<u>name</u>>

Returns a list of paths from the named set. You can either use the -set option to specify a user set by its name or use both -clock and -type to specify a set.

-clock <*clock name*>

Returns a list of paths from the specified clock domain. This option requires the -type option.

```
-type <set_type>
```

Specifies the type of paths to be included. It can only be used along with -clock. Valid values are:

reg_to_reg -- Paths between registers

external_setup -- Path from input ports to data pins of registers

external_hold -- Path from input ports to data pins of registers

clock_to_out -- Path from registers to output ports

reg_to_async -- Path from registers to asynchronous pins of registers

external_recovery -- Path from input ports to asynchronous pins of registers

external_removal -- Path from input ports to asynchronous pins of registers

async_to_reg -- Path from asynchronous pins to registers

-from_clock < clock name>

Used along with -to_clock to get the list of paths of the inter-clock domain between the two clocks.

-to_clock < clock name >

Used along with -from_clock to get the list of paths of the inter-clock domain between the two clocks. -in_to_out

Used to get the list of path between input and output ports.

-from <port/pin pattern>

Filter the list of paths to those starting from ports or pins matching the pattern.

-to <port/pin pattern>

Filter the list of paths to those ending at ports or pins matching the pattern.



Example

The following command displays the list of register to register paths of clock domain clk1:

```
puts [ list_paths -clock clk1 -type reg_to_reg ]
```

See Also

create_set expand_path set_options

list_scenarios

Tcl command; returns a list of names of all of the available timing scenarios.

list_scenarios

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Examples

list_scenarios

See Also

get_current_scenario Tcl documentation conventions Designer Tcl Command Reference

read_sdc

The read_sdc Tcl command evaluate an SDC file, adding all constraints to the specified scenario (or the current/default one if none is specified). Existing constraints are removed if -add is not specified.

```
read_sdc
-add
-scenario scenario_name
-netlist (user | optimized)
-pin_separator (: | /)
file name
```

Arguments

-add

Specifies that the constraints from the SDC file will be added on top of the existing ones, overriding them in case of a conflict. If not used, the existing constraints are removed before the SDC file is read.

-scenario scenario_name

Specifies the scenario to add the constraints to. The scenario is created if none exists with this name. -netlist (user | optimized)

Specifies whether the SDC file contains object defined at the post-synthesis netlist (user) level or physical (optimized) netlist (used for timing analysis).



-pin_separator sep Specify the pin separator used in the SDC file. It can be either ':' or '/'. file name Specify the SDC file name.

Example

The following command removes all constraints from the current/default scenario and adds all constraints from design.sdc file to it: read_sdc design.sdc

See Also

write_sdc

remove_all_constraints

Tcl command; removes all timing constraints from analysis.

remove_all_constraints

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Example

remove_all_constraints

See Also

remove_scenario

remove_clock

Tcl command; removes the specified clock constraint from the current timing scenario.

remove_clock -name clock_name | -id constraint_ID

Arguments

-name clock_name

Specifies the name of the clock constraint to remove from the current scenario. You must specify either a clock name or an ID.

-id constraint_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either an ID or a clock name that exists in the current scenario.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.



Description

Removes the specified clock constraint from the current scenario. If the specified name does not match a clock constraint in the current scenario, or if the specified ID does not refer to a clock constraint, this command fails.

Do not specify both the name and the ID.

Exceptions

You cannot use wildcards when specifying a clock name.

Examples

The following example removes the clock constraint named "my_user_clock": remove_clock -name my_user_clock The following example removes the clock constraint using its ID: set clockId [create_clock -name my_user_clock -period 2] remove_clock -id \$clockId

See Also

<u>create_clock</u> <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

remove_clock_latency

Tcl command; removes a clock source latency from the specified clock and from all edges of the clock.

remove_clock_latency {-source clock_name_or_source |-id constraint_ID}

Arguments

-source clock_name_or_source

Specifies either the clock name or source name of the clock constraint from which to remove the clock source latency. You must specify either a clock or source name or its constraint ID.

-id constraint_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either a clock or source name or its constraint ID.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

Removes a clock source latency from the specified clock in the current scenario. If the specified source does not match a clock with a latency constraint in the current scenario, or if the specified ID does not refer to a clock with a latency constraint, this command fails. Do not specify both the source and the ID.

Exceptions

You cannot use wildcards when specifying a clock name.

Examples

The following example removes the clock source latency from the specified clock.



remove_clock_latency -source my_clock

See Also

set_clock_latency Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_clock_uncertainty

Tcl command; removes a clock-to-clock uncertainty from the current timing scenario by specifying either its exact arguments or its ID.

```
remove_clock_uncertainty -from | -rise_from | -fall_from from_clock_list -to | -rise_to| -
fall_to to_clock_list -setup {value} -hold {value}
remove_clock_uncertainty -id constraint_ID
```

Arguments

-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. Only one of the *-from*, *-rise_from*, or *-fall_from* arguments can be specified for the constraint to be valid.

-rise_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. Only one of the -from, -rise_from, or -fall_from arguments can be specified for the constraint to be valid. -fall_from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. Only one of the <code>-from</code>, <code>-rise_from</code>, <code>or -fall_from</code> arguments can be specified for the constraint to be valid.

from_clock_list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. Only one of the -to, -rise_to, or -fall_to arguments can be specified for the constraint to be valid.

-rise_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. Only one of the -to, -rise_to, or -fall_to arguments can be specified for the constraint to be valid. -fall_to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. Only one of the -to, -rise_to, or -fall_to arguments can be specified for the constraint to be valid. to_clock_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-id constraint_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either the exact parameters to set the constraint or its constraint ID.



Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes a clock-to-clock uncertainty from the specified clock in the current scenario. If the specified arguments do not match clocks with an uncertainty constraint in the current scenario, or if the specified ID does not refer to a clock-to-clock uncertainty constraint, this command fails. Do not specify both the exact arguments and the ID.

Examples

```
remove_clock_uncertainty -from Clk1 -to Clk2
remove_clock_uncertainty -from Clk1 -fall_to { Clk2 Clk3 } -setup
remove_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
remove_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3
Clk4 } -setup
remove_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
remove_clock_uncertainty -id $clockId
```

See Also

remove_clock
remove_generated_clock
set_clock_uncertainty
Designer Tcl Command Reference

remove_disable_timing

Tcl command; removes a disable timing constraint by specifying its arguments, or its ID. If the arguments do not match a disable timing constraint, or if the ID does not refer to a disable timing constraint, the command fails.

remove_disable_timing -from value -to value name -id name

Arguments

-from from_port

Specifies the starting port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

-to *to_port*

Specifies the ending port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

name

Specifies the cell name where the disable timing constraint will be removed. It is an error to supply both a cell name and a constraint ID, as they are mutually exclusive. No wildcards are allowed when specifying a clock name, either alone or in an accessor command1.

-id name

Specifies the constraint name where the disable timing constraint will be removed. It is an error to supply both a cell name and a constraint ID, as they are mutually exclusive. No wildcards are allowed when specifying a clock name, either alone or in an accessor command1.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Example

remove_disable_timing -from port1 -to port2 -id new_constraint
Designer Tcl Command Reference

remove_false_path

Tcl command; removes a false path from the current timing scenario by specifying either its exact arguments or its ID.

```
remove_false_path [-from from_list] [-to to_list] [-through through_list] [-id constraint_ID]
remove_false_path -id constraint_ID
```

Arguments

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint_ID

Specifies the ID of the false path constraint to remove from the current scenario. You must specify either the exact false path to remove or the constraint ID that refers to the false path constraint to remove.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes a false path from the specified clock in the current scenario. If the arguments do not match a false path constraint in the current scenario, or if the specified ID does not refer to a false path constraint, this command fails.

Do not specify both the false path arguments and the constraint ID.

Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an Accessor command such as get_pins or get_ports.

Examples

The following example specifies all false paths to remove:

remove_false_path -through U0/U1:Y

The following example removes the false path constraint using its id:

```
set fpId [set_false_path -from [get_clocks c*] -through {topx/reg/*} -to [get_ports
out15] ]
```

remove_false_path -id \$fpId

See Also

set_false_path Tcl Command Documentation Conventions Designer Tcl Command Reference



remove_generated_clock

Tcl command; removes the specified generated clock constraint from the current scenario.

```
remove_generated_clock {-name clock_name | -id constraint_ID }
```

Arguments

-name clock_name

Specifies the name of the generated clock constraint to remove from the current scenario. You must specify either a clock name or an ID.

-id constraint_ID

Specifies the ID of the generated clock constraint to remove from the current scenario. You must specify either an ID or a clock name that exists in the current scenario.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes the specified generated clock constraint from the current scenario. If the specified name does not match a generated clock constraint in the current scenario, or if the specified ID does not refer to a generated clock constraint, this command fails.

Do not specify both the name and the ID.

Exceptions

You cannot use wildcards when specifying a generated clock name.

Examples

The following example removes the generated clock constraint named "my_user_clock": remove_generated_clock -name my_user_clock

See Also

create_generated_clock Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_input_delay

Tcl command; removes an input delay a clock on a port by specifying both the clocks and port names or the ID of the input_delay constraint to remove.

```
remove_input_delay -clock clock_name port_pin_list
remove_input_delay -id constraint_ID
```

Arguments

-clock clock_name

Specifies the clock name to which the specified input delay value is assigned. *port_pin_list* Specifies the port names to which the specified input delay value is assigned. -id *constraint_ID*



Specifies the ID of the clock with the input_delay value to remove from the current scenario. You must specify either both a clock name and list of port names or the input_delay constraint ID.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes an input delay from the specified clocks and port in the current scenario. If the clocks and port names do not match an input delay constraint in the current scenario, or if the specified ID does not refer to an input delay constraint, this command fails.

Do not specify both the clock and port names and the constraint ID.

Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

Examples

The following example removes the input delay from CLK1 on port data1:

remove_input_delay -clock [get_clocks CLK1] [get_ports data1]

See Also

set_input_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_max_delay

Tcl command; removes a maximum delay constraint from the current timing scenario by specifying either its exact arguments or its ID.

```
remove_max_delay [-from from_list] [-to to_list] [-through through_list]
remove_max_delay -id constraint_ID
```

Arguments

-from *from_list*

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint_ID

Specifies the ID of the maximum delay constraint to remove from the current scenario. You must specify either the exact maximum delay arguments to remove or the constraint ID that refers to the maximum delay constraint to remove.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Description

Removes a maximum delay value from the specified clock in the current scenario. If the arguments do not match a maximum delay constraint in the current scenario, or if the specified ID does not refer to a maximum delay constraint, this command fails.

Do not specify both the maximum delay arguments and the constraint ID.

Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an Accessor command.

Examples

The following example specifies a range of maximum delay constraints to remove: remove_max_delay -through U0/U1:Y

See Also

set_max_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_min_delay

Tcl command; removes a minimum delay constraint in the current timing scenario by specifying either its exact arguments or its ID.

```
remove_min_delay [-from from_list] [-to to_list] [-through through_list]
remove_min_delay -id constraint_ID
```

Arguments

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to*to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint_ID

Specifies the ID of the minimum delay constraint to remove from the current scenario. You must specify either the exact minimum delay arguments to remove or the constraint ID that refers to the minimum delay constraint to remove.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes a minimum delay value from the specified clock in the current scenario. If the arguments do not match a minimum delay constraint in the current scenario, or if the specified ID does not refer to a minimum delay constraint, this command fails.

Do not specify both the minimum delay arguments and the constraint ID.



Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

Examples

The following example specifies a range of minimum delay constraints to remove: remove_min_delay -through U0/U1:Y

See Also

set_min_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_multicycle_path

Tcl command; removes a multicycle path constraint in the current timing scenario by specifying either its exact arguments or its ID.

```
remove_multicycle_path [-from from_list] [-to to_list] [-through through_list]
remove multicycle_path -id constraint_ID
```

Arguments

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to*to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-id constraint_ID

Specifies the ID of the multicycle path constraint to remove from the current scenario. You must specify either the exact multicycle path arguments to remove or the constraint ID that refers to the multicycle path constraint to remove.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes a multicycle path from the specified clock in the current scenario. If the arguments do not match a multicycle path constraint in the current scenario, or if the specified ID does not refer to a multicycle path constraint, this command fails.

Do not specify both the multicycle path arguments and the constraint ID.

Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

Examples

The following example removes all paths between reg1 and reg2 to 3 cycles for setup check. remove_multicycle_path -from [get_pins {reg1}] -to [get_pins {reg2}]



See Also

set_multicycle_path <u>Tcl Command Documentation Conventions</u> <u>Designer Tcl Command Reference</u>

remove_output_delay

Tcl command; removes an ouput delay by specifying both the clocks and port names or the ID of the output_delay constraint to remove.

remove_output_delay -clock clock_name port_pin_list
remove_output_delay -id constraint_ID

Arguments

-clock clock_name

Specifies the clock name to which the specified output delay value is assigned.

port_pin_list

Specifies the port names to which the specified output delay value is assigned.

-id constraint_ID

Specifies the ID of the clock with the output_delay value to remove from the current scenario. You must specify either both a clock name and list of port names or the output_delay constraint ID.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Removes an output delay from the specified clocks and port in the current scenario. If the clocks and port names do not match an output delay constraint in the current scenario, or if the specified ID does not refer to an output delay constraint, this command fails.

Do not specify both the clock and port names and the constraint ID.

Exceptions

You cannot use wildcards when specifying a clock name, either alone or in an accessor command.

Examples

The following example removes the output delay from CLK1 on port out1:

remove_output_delay -clock [get_clocks CLK1] [get_ports out1]

See Also

set_output_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

remove_scenario

Tcl command; removes a scenario from the constraint database.

remove_scenario <name>



Arguments

name

Specifies the name of the scenario to delete.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Example

The following command removes the scenario named my_scenario: remove_scenario my_scenario

See Also

create_scenario

remove_set

Tcl command; removes a set of paths from analysis. Only user-created sets can be deleted.

remove_set -name name

Parameters

-name *nam*e

Specifies the name of the set to delete.

Example

The following command removes the set named my_set: remove_set -name my_set

See Also

create_set

rename_scenario

Tcl command; renames an existing timing scenario to a new name. You must provide a unique name (that is, it cannot already be used by another timing scenario) for the new name. rename_scenario old_name new_name

Arguments

old_name

Specifies the name of the existing timing scenario to be renamed.

new_name

Specifies the new name for the scenario.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

This command renames an existing scenario name to a new name.



Example

rename_scenario my_old_scenario my_new_scenario

See Also

<u>create_scenario</u> <u>delete_scenario</u> <u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

save

Tcl command; saves all changes made prior to this command. This includes changes made on constraints, options and sets.

save

Arguments

None

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Example

The following script sets the maximum number of paths reported by list_paths to 10, reads an SDC file, and save both the option and the constraints into the design project:

```
set_options -limit_max_paths 10
read_sdc somefile.sdc
save
```

See Also

set_options

set_clock_latency

Tcl command; defines the delay between an external clock source and the definition pin of a clock within SmartTime.

set_clock_latency -source [-rise][-fall][-early][-late] delay clock

Arguments

-source

Specifies the source latency on a clock pin, potentially only on certain edges of the clock.

-rise

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-fall

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.



-late

Optional. Specifies that the latency is late bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

-early

Optional. Specifies that the latency is early bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

delay

Specifies the latency value for the constraint.

clock

Specifies the clock to which the constraint is applied. This clock must be constrained.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint. You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

Examples

The following example sets an early clock source latency of 0.4 on the rising edge of main_clock. It also sets a clock source latency of 1.2, for both the early and late values of the falling edge of main_clock. The late value for the clock source latency for the falling edge of main_clock remains undefined.

set_clock_latency -source -rise -early 0.4 { main_clock }
set_clock_latency -source -fall 1.2 { main_clock }

See Also

<u>create_clock</u> <u>create_generated_clock</u> <u>Tcl Command Documentation Conventions</u> Designer Tcl Command Reference

set_clock_uncertainty

Tcl command; specifies a clock-to-clock uncertainty between two clocks (from and to) and returns the ID of the created constraint if the command succeeded.

```
set_clock_uncertainty uncertainty -from | -rise_from | -fall_from from_clock_list -to | -
rise_to | -fall_to to_clock_list -setup {value} -hold {value}
```

Arguments

uncertainty

Specifies the time in nanoseconds that represents the amount of variation between two clock edges.



-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. Only one of the -from, -rise_from, or -fall_from arguments can be specified for the constraint to be valid.

-rise_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. Only one of the -from, -rise_from, or -fall_from arguments can be specified for the constraint to be valid. -fall_from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. Only one of the -from, -rise_from, or -fall_from arguments can be specified for the constraint to be valid. from clock list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. Only one of the -to, -rise_to, or -fall_to arguments can be specified for the constraint to be valid.

-rise_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. Only one of the -to, -rise_to, or -fall_to arguments can be specified for the constraint to be valid. -fall_to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. Only one of the -to, $-rise_to$, or $-fall_to$ arguments can be specified for the constraint to be valid.

```
to_clock_list
```

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

The set_clock_uncertainty command sets the timing uncertainty between two clock waveforms or maximum clock skew. Timing between clocks have no uncertainty unless you specify it.

Examples

```
set_clock_uncertainty 10 -from Clk1 -to Clk2
set_clock_uncertainty 0 -from Clk1 -fall_to { Clk2 Clk3 } -setup
set_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
set_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3 Clk4 }
-setup
set_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
```

See Also

create_clock
create_generated_clock
remove_clock_uncertainty
Designer Tcl Command Reference



set_current_scenario

Tcl command; specifies the timing scenario for the Timing Analyzer to use. All commands that follow this command will apply to the specified timing scenario.

set_current_scenario name

Arguments

name

Specifies the name of the timing scenario to which to apply all commands from this point on.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

A timing scenario is a set of timing constraints used with a design. If the specified scenario is already the current one, this command has no effect.

After setting the current scenario, constraints can be listed, added, or removed, the checker can be invoked on the set of constraints, and so on.

This command uses the specified timing scenario to compute timing analysis.

Example

set_current_scenario scenario_A

See Also

get_current_scenario Tcl Command Documentation Conventions Designer Tcl Command Reference

set_disable_timing

Tcl command; disables timing arcs within a cell and returns the ID of the created constraint if the command succeeded.

```
set_disable_timing -from value -to value name
```

Arguments

-from from_port

Specifies the starting port. The -from and -to arguments must either both be present or both omitted for the constraint to be valid.

-to to_port

Specifies the ending port. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

name

Specifies the cell name where the timing arcs will be disabled.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Example

set_disable_timing -from A -to Y a2

See Also

Tcl documentation conventions Designer Tcl Command Reference

set_false_path

Tcl command; identifies paths that are considered false and excluded from the timing analysis in the current timing scenario.

set_false_path [-from from_list] [-through through_list] [-to to_list]

Arguments

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to *to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

The set_false_path command identifies specific timing paths as being false. The false timing paths are paths that do not propagate logic level changes. This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins, and the path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints. If more than one object is specified within one -through option, the path can pass through any objects.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

Examples

The following example specifies all paths from clock pins of the registers in clock domain clk1 to data pins of a specific register in clock domain clk2 as false paths:

set_false_path -from [get_clocks {clk1}] -to reg_2:D

The following example specifies all paths through the pin U0/U1:Y to be false:

set_false_path -through U0/U1:Y

See Also

Tcl Command Documentation Conventions Designer Tcl Command Reference



set_input_delay

Tcl command; creates an input delay on a port list by defining the arrival time of an input relative to a clock in the current scenario.

set_input_delay delay_value -clock clock_ref [-max] [-min] [-clock_fall] input_list

Arguments

delay_value

Specifies the arrival time in nanoseconds that represents the amount of time for which the signal is available at the specified input after a clock edge.

-clock clock_ref

Specifies the clock reference to which the specified input delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay_value refers to the longest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-min

Specifies that delay_value refers to the shortest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-clock_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. *input_list*

Provides a list of input ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.and IGLOOe, except ProASIC3 nano and ProASIC3L

Description

The set_input_delay command sets input path delays on input ports relative to a clock edge. This usually represents a combinational path delay from the clock pin of a register external to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds input delay to path delay for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be:

- a single port name used as source for a clock constraint
- a single pin name used as source for a clock constraint; for instance reg1:CLK. This name can be hierarchical (for instance toplevel/block1/reg2:CLK)
- an object accessor that will refer to one clock: [get_clocks {clk}]

Examples

The following example sets an input delay of 1.2ns for port data1 relative to the rising edge of CLK1: set_input_delay 1.2 -clock [get_clocks CLK1] [get_ports data1]

The following example sets a different maximum and minimum input delay for port IN1 relative to the falling edge of CLK2:

```
set_input_delay 1.0 -clock_fall -clock CLK2 -min {IN1}
set_input_delay 1.4 -clock_fall -clock CLK2 -max {IN1}
```



See Also

set_output_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

set_max_delay

Tcl command; specifies the maximum delay for the timing paths in the current scenario.

set_max_delay delay_value [-from from_list] [-to to_list] [-through through_list]

Arguments

delay_value

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the timing paths must pass.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

This command specifies the required maximum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.

The timing engine automatically derives the individual maximum delay targets from clock waveforms and port input or output delays.

The maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.



Examples

The following example sets a maximum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set_max_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}

The following example sets a maximum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set_max_delay 3.8 -to [get_ports out*]

See Also

set_min_delay remove_max_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

set_min_delay

Tcl command; specifies the minimum delay for the timing paths in the current scenario.

set_min_delay delay_value [-from from_list] [-to to_list] [-through through_list]

Arguments

delay_value

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-to *to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the timing paths must pass.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

This command specifies the required minimum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.



The timing engine automatically derives the individual minimum delay targets from clock waveforms and port input or output delays.

The minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

Examples

The following example sets a minimum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set_min_delay 5 -from {ff1a:CLK ff1b:CLK} -to {ff2e:D}

The following example sets a minimum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set_min_delay 3.8 -to [get_ports out*]

See Also

set_max_delay remove_min_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

set_multicycle_path

Tcl command; defines a path that takes multiple clock cycles in the current scenario.

```
set_multicycle_path ncycles [-setup] [-hold] [-from from_list[-through_list[-to
to_list
```

Arguments

ncycles

Specifies an integer value that represents a number of cycles the data path must have for setup or hold check. The value is relative to the starting point or ending point clock, before data is required at the ending point.

-setup

Optional. Applies the cycle value for the setup check only. This option does not affect the hold check. The default hold check will be applied unless you have specified another set_multicycle_path command for the hold value.

-hold

Optional. Applies the cycle value for the hold check only. This option does not affect the setup check.

Note: Note: If you do not specify "-setup" or "-hold", the cycle value is applied to the setup check and the default hold check is performed (*ncycles* -1).

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through *through_list* Specifies a list of pins or ports through which the multiple cycle paths must pass.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.



Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

Setting multiple cycle paths constraint overrides the single cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks. If you change the multiplier, it affects both the setup and hold checks.

False path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

If you specify more than one object within one -through option, the path passes through any of the objects.

You must specify at least one of the -from, -to, or -through arguments for this constraint to be valid.

Exceptions

Multiple priority management is not supported in Microsemi SoC designs. All multiple cycle path constraints are handled with the same priority.

Examples

The following example sets all paths between reg1 and reg2 to 3 cycles for setup check. Hold check is measured at the previous edge of the clock at reg2.

set_multicycle_path 3 -from [get_pins {reg1}] -to [get_pins {reg2}]

The following example specifies that four cycles are needed for setup check on all paths starting at the registers in the clock domain ck1. Hold check is further specified with two cycles instead of the three cycles that would have been applied otherwise.

set_multicycle_path 4 -setup -from [get_clocks {ck1}]
set_multicycle_path 2 -hold -from [get_clocks {ck1}]

See Also

remove_multicycle_path Tcl Command Documentation Conventions Designer Tcl Command Reference

set_options

SmartTime-specific Tcl command; sets options for timing analysis. Some options will also affect timingdriven place-and-route. The same parameters can be changed in the SmartTime Options dialog box in the SmartTime GUI.

set_options

```
[-max_opcond value ]
[-min_opcond value]
[-interclockdomain_analysis value]
[-use_bibuf_loopbacks value]
[-enable_recovery_removal_checks value]
[-break_at_async value]
[-filter_when_slack_below value]
[-filter_when_slack_above value]
[-remove_slack_filters]
[-limit_max_paths value]
[-expand_clock_network value]
[-expand_parallel_paths value]
[-analysis_scenario value]
```



[-tdpr_scenario value] [-reset]

Arguments

-max_opcond value

Sets the operating condition to use for Maximum Delay Analysis. The following table shows the acceptable values for this argument. Default is *worst*.

Value	Description			
worst	Use Worst Case conditions for Maximum Delay Analysis			
typical	Use Typical conditions for Maximum Delay Analysis			
best	Use Best Case conditions for Maximum Delay Analysis			

-min_opcond value

Sets the operating condition to use for Minimum Delay Analysis. The following table shows the acceptable values for this argument. Default is *best*.

Value	Description		
best	Use Best Case conditions for Minimum Delay Analysis		
typical	Use Typical conditions for Minimum Delay Analysis		
worst	Use Worst Case conditions for Minimum Delay Analysis		

-interclockdomain_analysis value

Enables or disables inter-clock domain analysis. Default is yes.

Value	Description		
yes	Enables inter-clock domain analysis		
no	Disables inter-clock domain analysis		

-use_bibuf_loopbacks value

Instructs the timing analysis whether to consider loopback path in bidirectional buffers (D->Y, E->Y)as false-path {no}. Default is *yes*; i.e., loopback are false paths.

Value	Description		
yes	Enables loopback in bibufs		
no	Disables loopback in bibufs		

-enable_recovery_removal_checks value

Enables recovery checks to be included in max-delay analysis and removal checks in min-delay analysis. Default is *yes*.



Value	Description		
yes	Enables recovery and removal checks		
no	Disables recovery and removal checks		

-break_at_async value

Specifies whether or not timing analysis is allowed to cross asynchronous pins (clear, reset of sequential elements). Default is *no*.

Value Description	
yes	Enables breaking paths at asynchronous ports
no	Disables breaking paths at asynchronous ports

-filter_when_slack_below value

Specifies a minimum slack value for paths reported by list_paths. Not set by default. -filter_when_slack_above value

Specifies a maximum slack value for paths reported by list_paths. Not set by default. -remove slack filters

Removes the slack minimum and maximum set using -filter_when_slack_below and filter_when_slack_above.

-limit_max_paths value

Specifies the maximum number of paths reported by list_paths. Default is 100. -expand_clock_network value

Specify whether or not clock network details are reported in expand_path. Default is yes.

Value	Description	
yes	Enables expanded clock network information in paths	
no	Disables expanded clock network information in paths	

-expand_parallel_paths value

Specify the number of parallel paths {paths with the same ends} to include in expand_path. Default is 1. -analysis_scenario value

Specify the constraint scenario to be used for timing analysis. Default is *Primary*, the default scenario. -tdpr_scenario value

Specify the constraint scenario to be used for timing-driven place-and-route. Default is Primary, the default scenario.

-reset

Reset all options to the default values, except those for analysis and TDPR scenarios, which remain unchanged.

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



Examples

The following script commands the timing engine to use best operating conditions for both max-delay analysis and min-delay analysis:

set_options -max_opcond {best} -min_opcond {best}

The following script changes the scenario used by timing-driven place-and-route and saves the change in the Libero project for place-and-route tools to see the change.

set_options -tdpr_scenario {My_TDPR_Scenario}

See Also

save

set_output_delay

Tcl command; defines the output delay of an output relative to a clock in the current scenario.

set_output_delay delay_value -clock clock_ref [-max] [-min] [-clock_fall] output_list

Arguments

delay_value

Specifies the amount of time before a clock edge for which the signal is required. This represents a combinational path delay to a register outside the current design plus the library setup time (for maximum output delay) or hold time (for minimum output delay).

-clock clock_ref

Specifies the clock reference to which the specified output delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay_value refers to the longest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

-min

Specifies that delay_value refers to the shortest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

-clock_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. *output_list*

Provides a list of output ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

Description

The set_output_delay command sets output path delays on output ports relative to a clock edge. Output ports have no output delay unless you specify it. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds output delay to path delay for paths ending at primary outputs.

Examples

The following example sets an output delay of 1.2ns for port OUT1 relative to the rising edge of CLK1: set_output_delay 1.2 -clock [get_clocks CLK1] [get_ports OUT1]



The following example sets a different maximum and minimum output delay for port OUT1 relative to the falling edge of CLK2:

```
set_output_delay 1.0 -clock_fall -clock CLK2 -min {OUT1}
set_output_delay 1.4 -clock_fall -clock CLK2 -max {OUT1}
```

See Also

remove_output_delay set_input_delay Tcl Command Documentation Conventions Designer Tcl Command Reference

write_sdc

Tcl command; writes timing constraints into an SDC file. If multiple constraint scenarios are defined, - scenario allows the user to specify which scenario to write. By default, the current scenario is written.

```
write_sdc
-scenario scenario name
-pin_separator (: | /)
file name
```

Arguments

-scenario scenario name Specify the scenario to write. By default the current scenario is used. -pin_separator sep Specify the pin separator used in the SDC file. It can be either ':' or '/'. file name Specify the SDC file name.

Example

The following script merges two SDC files and writes the result into a third SDC file: read_sdc first.sdc read_sdc -add second.sdc write_sdc merged.sdc

See Also

read_sdc, set_current_scenario VERIFYTIMING (SmartFusion2 and IGLOO2)



Constraints by File Format - SDC Command Reference



About Synopsys Design Constraints (SDC) Files

Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi tools use a subset of the SDC format to capture supported timing constraints. Any timing constraint that you can enter using Designer tools can also be specified in an SDC file.

Use the SDC-based flow to share timing constraint information between Microsemi tools and third-party EDA tools.

Command	Action	
create_clock	Creates a clock and defines its characteristics	
create_generated_clock	Creates an internally generated clock and defines its characteristics	
remove_clock_uncertainty	Removes a clock-to-clock uncertainty from the current timing scenario.	
set_clock_latency	Defines the delay between an external clock source and the definition pin of a clock within SmartTime	
set clock uncertainty	Defines the timing uncertainty between two clock waveforms or maximum skew	
<u>set false path</u>	Identifies paths that are to be considered false and excluded from the timing analysis	
set_input_delay	Defines the arrival time of an input relative to a clock	
set_load	Sets the load to a specified value on a specified port	
<u>set max delay</u>	Specifies the maximum delay for the timing paths	
<u>set_min_delay</u>	Specifies the minimum delay for the timing paths	
set_multicycle_path	Defines a path that takes multiple clock cycles	
set output delay	Defines the output delay of an output relative to a clock	

See Also

Constraint Entry SDC Syntax Conventions Importing Constraint Files



SDC Syntax Conventions

The following table shows the typographical conventions that are used for the SDC command syntax.

Syntax Notation	Description
command - argument	Commands and arguments appear in Courier New typeface.
variable	Variables appear in blue, italic <i>Courier New</i> typeface. You must substitute an appropriate value for the variable.
[-argument value]	Optional arguments begin and end with a square bracket.

Note: SDC commands and arguments are case sensitive.

Example

The following example shows syntax for the create_clock command and a sample command:

```
create_clock -period period_value [-waveform edge_list] source
```

create_clock -period 7 -waveform {2 4}{CLK1}

Wildcard Characters

You can use the following wildcard characters in names used in the SDC commands:

Wildcard	What it does		
١	Interprets the next character literally		
*	Matches any string		

Note: The matching function requires that you add a backslash (\) before each slash in the pin names in case the slash does not denote the hierarchy in your design.

Special Characters ([], { }, and \)

Square brackets ([]) are part of the command syntax to access ports, pins and clocks. In cases where these netlist objects names themselves contain square brackets (for example, buses), you must either enclose the names with curly brackets ({}) or precede the open and closed square brackets ([]) characters with a backslash (\). If you do not do this, the tool displays an error message.

For example:

```
create_clock -period 3 clk\[0\]
set_max_delay 1.5 -from [get_pins ffl\[5\]:CLK] -to [get_clocks {clk[0]}]
```

Although not necessary, Microsemi recommends the use of curly brackets around the names, as shown in the following example:

set_false_path -from {data1} -to [get_pins {reg1:D}]

In any case, the use of the curly bracket is mandatory when you have to provide more than one name. For example:

```
set_false_path -from {data3 data4} -to [get_pins {reg2:D reg5:D}]
```



Entering Arguments on Separate Lines

If a command needs to be split on multiple lines, each line except the last must end with a backslash (\) character as shown in the following example:

```
set_multicycle_path 2 -from \
[get_pins {reg1*}] \
-to {reg2:D}
```

See Also

About SDC Files



create_clock

SDC command; creates a clock and defines its characteristics.

create_clock -name name -period period_value [-waveform edge_list] source

Arguments

-name *nam*e

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

-period period_value

Specifies the clock period in nanoseconds. The value you specify is the minimum time over which the clock waveform repeats. The period_value must be greater than zero.

-waveform edge_list

Specifies the rise and fall times of the clock waveform in ns over a complete clock period. There must be exactly two transitions in the list, a rising transition followed by a falling transition. You can define a clock starting with a falling edge by providing an edge list where fall time is less than rise time. If you do not specify -waveform option, the tool creates a default waveform, with a rising edge at instant 0.0 ns and a falling edge at instant (period_value/2)ns.

source

Specifies the source of the clock constraint. The source can be ports or pins in the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing one. Only one source is accepted. Wildcards are accepted as long as the resolution shows one port or pin.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Creates a clock in the current design at the declared source and defines its period and waveform. The static timing analysis tool uses this information to propagate the waveform across the clock network to the clock pins of all sequential elements driven by this clock source.

The clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Exceptions

None

Examples

The following example creates two clocks on ports CK1 and CK2 with a period of 6, a rising edge at 0, and a falling edge at 3:

create_clock -name {my_user_clock} -period 6 CK1

create_clock -name {my_other_user_clock} -period 6 -waveform {0 3} {CK2}

The following example creates a clock on port CK3 with a period of 7, a rising edge at 2, and a falling edge at 4:

create_clock -period 7 -waveform {2 4} [get_ports {CK3}]

Microsemi Implementation Specifics

• The -waveform in SDC accepts waveforms with multiple edges within a period. In Microsemi design implementation, only two waveforms are accepted.



- SDC accepts defining a clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The source argument in SDC create_clock command is optional. This is in conjunction with the -name argument in SDC to support the concept of virtual clocks. In Microsemi implementation, source is a mandatory argument as -name and virtual clocks concept is not supported.
- The -domain argument in the SDC create_clock command is not supported.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Clock Definition Create Clock Create a New Clock Constraint



create_generated_clock

SDC command; creates an internally generated clock and defines its characteristics.

```
create_generated_clock -name {name -source reference_pin [-divide_by divide_factor] [-
multiply_by multiply_factor] [-invert] source -pll_output pll_feedback_clock -pll_feedback
pll_feedback_input
```

Arguments

-name name

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

-source *reference_pin*

Specifies the reference pin in the design from which the clock waveform is to be derived.

-divide_bydivide_factor

Specifies the frequency division factor. For instance if the *divide_factor* is equal to 2, the generated clock period is twice the reference clock period.

-multiply_by multiply_factor

Specifies the frequency multiplication factor. For instance if the *multiply_factor* is equal to 2, the generated clock period is half the reference clock period.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

source

Specifies the source of the clock constraint on internal pins of the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing clock. Only one source is accepted. Wildcards are accepted as long as the resolution shows one pin.

-pll_output pll_feedback_clock

Specifies the output pin of the PLL which is used as the external feedback clock. This pin must drive the feedback input pin of the PLL specified using the -pll_feedback option. The PLL will align the rising edge of the reference input clock to the feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

-pll_feedback pll_feedback_input

Specifies the feedback input pin of the PLL. This pin must be driven by the output pin of the PLL specified using the -pll_output option. The PLL will align the rising edge of the reference input clock to the external feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Creates a generated clock in the current design at a declared source by defining its frequency with respect to the frequency at the reference pin. The static timing analysis tool uses this information to compute and propagate its waveform across the clock network to the clock pins of all sequential elements driven by this source.

The generated clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Examples

The following example creates a generated clock on pin U1/reg1:Q with a period twice as long as the period at the reference port CLK.



create_generated_clock -name {my_user_clock} -divide_by 2 -source [get_ports
{CLK}] U1/reg1:Q

The following example creates a generated clock at the primary output of myPLL with a period ³/₄ of the period at the reference pin clk.

create_generated_clock -divide_by 3 -multiply_by 4 -source clk [get_pins {myPLL:CLK1}] The following example creates a generated clock named system_clk on the GL2 output pin of FCCC_0 with a period equal to half the period of the source clock. The constraint also identifies GL2 output pin as the external feedback clock source and CLK2 as the feedback input pin for FCCC_0.

```
create_generated_clock -name { system_clk } \
-multiply_by 2 \
-source { FCCC_0/CCC_INST/INST_CCC_IP:CLK3_PAD } \
-pll_output { FCCC_0/CCC_INST/INST_CCC_IP:GL2 } \
-pll_feedback { FCCC_0/CCC_INST/INST_CCC_IP:CLK2 } \
{ FCCC_0/CCC_INST/INST_CCC_IP:GL2 }
```

Microsemi Implementation Specifics

- SDC accepts either –multiply_by or –divide_by option. In Microsemi design implementation, both are
 accepted to accurately model the PLL behavior.
- SDC accepts defining a generated clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The -duty_cycle ,-edges and -edge_shift options in the SDC create_generated_clock command are not supported in Microsemi design implementation.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Create Generated Clock Constraint (SDC)

remove_clock_uncertainty

SDC command; Removes a clock-to-clock uncertainty from the current timing scenario.

```
remove_clock_uncertainty -from | -rise_from | -fall_from from_clock_list -to | -rise_to| -
fall_to to_clock_list -setup {value} -hold {value}
remove_clock_uncertainty -id constraint_ID
```

Arguments

-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. You can specify only one of the *-from*, *-rise_from*, or *-fall_from* arguments for the constraint to be valid.

```
-rise_from
```

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. You can specify only one of the *-from*, *-rise_from*, or *-fall_from* arguments for the constraint to be valid. *-fall_from*

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. You can specify only one of the -from, -rise_from, or -fall_from arguments for the constraint to be valid.

from_clock_list

Specifies the list of clock names as the uncertainty source.

-to



Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. You can specify only one of the -to, $-rise_to$, or $-fall_to$ arguments for the constraint to be valid.

-rise_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. You can specify only one of the -to, -rise_to, or -fall_to arguments for the constraint to be valid. -fall to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. You can specify only one of the -to, $-rise_to$, or $-fall_to$ arguments for the constraint to be valid.

to_clock_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-hold

Specifies that the uncertainty applies only to hold checks. If none or both -setup and -hold are present, the uncertainty applies to both setup and hold checks.

-id constraint_ID

Specifies the ID of the clock constraint to remove from the current scenario. You must specify either the exact parameters to set the constraint or its constraint ID.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Removes a clock-to-clock uncertainty from the specified clock in the current scenario. If the specified arguments do not match clocks with an uncertainty constraint in the current scenario, or if the specified ID does not refer to a clock-to-clock uncertainty constraint, this command fails. Do not specify both the exact arguments and the ID.

Exceptions

None

Examples

```
remove_clock_uncertainty -from Clk1 -to Clk2
remove_clock_uncertainty -from Clk1 -fall_to { Clk2 Clk3 } -setup
remove_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
remove_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3
Clk4 } -setup
remove_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
remove_clock_uncertainty -id $clockId
```

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions set clock uncertainty



set_clock_latency

SDC command; defines the delay between an external clock source and the definition pin of a clock within SmartTime.

set_clock_latency -source [-rise][-fall][-early][-late] delay clock

Arguments

-source

Specifies a clock source latency on a clock pin.

-rise

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-fall

Specifies the edge for which this constraint will apply. If neither or both rise are passed, the same latency is applied to both edges.

-invert

Specifies that the generated clock waveform is inverted with respect to the reference clock.

-late

Optional. Specifies that the latency is late bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

-early

Optional. Specifies that the latency is early bound on the latency. The appropriate bound is used to provide the most pessimistic timing scenario. However, if the value of "-late" is less than the value of "-early", optimistic timing takes place which could result in incorrect analysis. If neither or both "-early" and "-late" are provided, the same latency is used for both bounds, which results in the latency having no effect for single clock domain setup and hold checks.

delay

Specifies the latency value for the constraint.

clock

Specifies the clock to which the constraint is applied. This clock must be constrained.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Clock source latency defines the delay between an external clock source and the definition pin of a clock within SmartTime. It behaves much like an input delay constraint. You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which SmartTime propagates through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

Exceptions

None



Examples

The following example sets an early clock source latency of 0.4 on the rising edge of main_clock. It also sets a clock source latency of 1.2, for both the early and late values of the falling edge of main_clock. The late value for the clock source latency for the falling edge of main_clock remains undefined.

set_clock_latency -source -rise -early 0.4 { main_clock }
set_clock_latency -source -fall 1.2 { main_clock }

Microsemi Implementation Specifics

SDC accepts a list of clocks to -set_clock_latency. In Microsemi design implementation, only one clock pin can have its source latency specified per command.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

set_clock_to_output

SDC command; defines the timing budget available inside the FPGA for an output relative to a clock.

set_clock_to_output delay_value -clock clock_ref [-max] [-min] [-clock_fall] output_list

Arguments

delay_value

Specifies the clock to output delay in nanoseconds. This time represents the amount of time available inside the FPGA between the active clock edge and the data change at the output port.

-clock clock_ref

Specifies the reference clock to which the specified clock to output is related. This is a mandatory argument.

-max

Specifies that delay_value refers to the maximum clock to output at the specified output. If you do not specify -max or -min options, the tool assumes maximum and minimum clock to output delays to be equal.

-min

Specifies that delay_value refers to the minimum clock to output at the specified output. If you do not specify -max or -min options, the tool assumes maximum and minimum clock to output delays to be equal.

-clock_fall

Specifies that the delay is relative to the falling edge of the reference clock. The default is the rising edge. *output_list*

Provides a list of output ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The set_clock_to_output command specifies the clock to output maximum and minimum delays on output ports relative to a clock edge. This usually represents a combinational path delay from a register internal to



the current design to the output port. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool uses clock to output delays for paths ending at primary outputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be an object accessor that will refer to one clock. For example:

```
[get_clocks {system_clk}]
[get_clocks {sys*_clk}]
```

Examples

The following example sets a maximum clock to output delay of 12 ns and a minimum clock to output delay of 6 ns for port data_out relative to the rising edge of CLK1:

set_clock_to_output 12 -clock [get_clocks CLK1] -max [get_ports data_out]
set_clock_to_output 6 -clock [get_clocks CLK1] -min [get_ports data_out]

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions

set_clock_uncertainty

SDC command; defines the timing uncertainty between two clock waveforms or maximum skew.

```
set_clock_uncertainty uncertainty (-from | -rise_from | -fall_from) from_clock_list (-to | -
rise_to | -fall_to) to_clock_list [-setup | -hold]
```

Arguments

uncertainty

Specifies the time in nanoseconds that represents the amount of variation between two clock edges. The value must be a positive floating point number.

-from

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. You can specify only one of the -from, -rise_from, or -fall_from arguments for the constraint to be valid. This option is the default.

-rise_from

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. You can specify only one of the -from, -rise_from, or -fall_from arguments for the constraint to be valid. -fall from

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. You can specify only one of the -from, -rise_from, or -fall_from arguments for the constraint to be valid.

from_clock_list

Specifies the list of clock names as the uncertainty source.

-to

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. You can specify only one of the -to, -rise_to, or -fall_to arguments for the constraint to be valid.

-rise_to

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. You can specify only one of the -to, -rise_to, or -fall_to arguments for the constraint to be valid. -fall_to

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. You can specify only one of the -to, -rise_to, or -fall_to arguments for the constraint to be valid.



to_clock_list

Specifies the list of clock names as the uncertainty destination.

-setup

Specifies that the uncertainty applies only to setup checks. If you do not specify either option (-setup or -hold) or if you specify both options, the uncertainty applies to both setup and hold checks.

Specifies that the uncertainty applies only to hold checks. If you do not specify either option (-setup or -hold) or if you specify both options, the uncertainty applies to both setup and hold checks.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Clock uncertainty defines the timing between an two clock waveforms or maximum clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.

Exceptions

None

Examples

The following example defines two clocks and sets the uncertainty constraints, which analyzes the interclock domain between clk1 and clk2.

```
create_clock -period 10 clk1
create_generated_clock -name clk2 -source clk1 -multiply_by 2 sclk1
set_clock_uncertainty 0.4 -rise_from clk1 -rise_to clk2
```

Microsemi Implementation Specifics

• SDC accepts a list of clocks to -set_clock_uncertainty.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions create_clock (SDC) create_generated_clock (SDC) remove_clock_uncertainty

set_disable_timing

SDC command; disables timing arcs within the specified cell and returns the ID of the created constraint if the command succeeded.

set_disable_timing [-from from_port] [-to to_port] cell_name



Arguments

-from from_port

Specifies the starting port.

```
-to to_port
```

Specifies the ending port.

cell_name

Specifies the name of the cell in which timing arcs will be disabled.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command disables the timing arcs in the specified cell, and returns the ID of the created constraint if the command succeeded. The –from and –to arguments must either both be present or both omitted for the constraint to be valid.

Examples

The following example disables the arc between a2:A and a2:Y.

set_disable_timing -from port1 -to port2 cellname
This command ensures that the arc is disabled within a cell instead of between cells.

Microsemi Implementation Specifics

None

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

set_external_check

SDC command; defines the external setup and hold delays for an input relative to a clock.

```
set_external_check delay_value -clock clock_ref [-setup] [-hold] [-clock_fall] input_list
```

Arguments

delay_value

Specifies the external setup or external hold delay in nanoseconds. This time represents the amount of time available inside the FPGA for the specified input after a clock edge.

-clock clock_ref

Specifies the reference clock to which the specified external check is related. This is a mandatory argument.

-setup



Specifies that delay_value refers to the setup check at the specified input. This is a mandatory argument if –hold is not used. You must specify either -setup or -hold option.

-clock_fall

Specifies that the delay is relative to the falling edge of the reference clock. The default is the rising edge. *input_list*

Provides a list of input ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The set_external_check command specifies the external setup and hold times on input ports relative to a clock edge. This usually represents a combinational path delay from the input port to the clock pin of a register internal to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool uses external setup and external hold times for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be an object accessor that will refer to one clock. For example:

```
[get_clocks {system_clk}]
[get_clocks {sys*_clk}]
```

Examples

The following example sets an external setup check of 12 ns and an external hold check of 6 ns for port data_in relative to the rising edge of CLK1:

set_external_check 12 -clock [get_clocks CLK1] -setup [get_ports data_in]
set_external_check 6 -clock [get_clocks CLK1] -hold [get_ports data_in]

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions



set_false_path

SDC command; identifies paths that are considered false and excluded from the timing analysis.

set_false_path [-from from_list] [-through through_list] [-to to_list]

Arguments

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The set_false_path command identifies specific timing paths as being false. The false timing paths are paths that do not propagate logic level changes. This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins, and the path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints. If more than one object is specified within one -through option, the path can pass through any objects.

Examples

The following example specifies all paths from clock pins of the registers in clock domain clk1 to data pins of a specific register in clock domain clk2 as false paths:

set_false_path -from [get_clocks {clk1}] -to reg_2:D

The following example specifies all paths through the pin U0/U1:Y to be false:

set_false_path -through U0/U1:Y

Microsemi Implementation Specifics

SDC accepts multiple -through options in a single constraint to specify paths that traverse multiple points in the design. In Microsemi design implementation, only one –through option is accepted.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set False Path Constraint



set_input_delay

SDC command; defines the arrival time of an input relative to a clock.

set_input_delay delay_value -clock clock_ref [-max] [-min] [-clock_fall] input_list

Arguments

delay_value

Specifies the arrival time in nanoseconds that represents the amount of time for which the signal is available at the specified input after a clock edge.

-clock clock_ref

Specifies the clock reference to which the specified input delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay_value refers to the longest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-min

Specifies that delay_value refers to the shortest path arriving at the specified input. If you do not specify - max or -min options, the tool assumes maximum and minimum input delays to be equal.

-clock_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge.

input_list

Provides a list of input ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion and IGLOOe, except ProASIC3 nano and ProASIC3L

Description

The set_input_delay command sets input path delays on input ports relative to a clock edge. This usually represents a combinational path delay from the clock pin of a register external to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds input delay to path delay for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be:

- a single port name used as source for a clock constraint
- a single pin name used as source for a clock constraint; for instance reg1:CLK. This name can be hierarchical (for instance toplevel/block1/reg2:CLK)
- an object accessor that will refer to one clock: [get_clocks {clk}]

Examples

The following example sets an input delay of 1.2ns for port data1 relative to the rising edge of CLK1: set_input_delay 1.2 -clock [get_clocks CLK1] [get_ports data1]

The following example sets a different maximum and minimum input delay for port IN1 relative to the falling edge of CLK2:

set_input_delay 1.0 -clock_fall -clock CLK2 -min {IN1}
set_input_delay 1.4 -clock_fall -clock CLK2 -max {IN1}



Microsemi Implementation Specifics

In SDC, the -clock is an optional argument that allows you to set input delay for combinational designs. Microsemi Implementation currently requires this argument.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Input Delay



set_load

SDC command; sets the load to a specified value on a specified port.

set_load capacitance port_list

Arguments

capacitance
Specifies the capacitance value that must be set on the specified ports.
port_list
Specifies a list of ports in the current design on which the capacitance is to be set.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The load constraint enables the Designer software to account for external capacitance at a specified port. You cannot set load constraint on the nets. When you specify this constraint on the output ports, it impacts the delay calculation on the specified ports.

Examples

The following examples show how to set output capacitance on different output ports:

set_load	35	out_p
set_load	40	{01 02}
set_load	25	[get_ports out]

Microsemi Implementation Specifics

• In SDC, you can use the set_load command to specify capacitance value on nets. Microsemi Implementation only supports output ports.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Load on Port



set_max_delay (SDC)

SDC command; specifies the maximum delay for the timing paths.

set_max_delay delay_value [-from from_list] [-to to_list]

Arguments

delay_value

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command specifies the required maximum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.

The tool automatically derives the individual maximum delay targets from clock waveforms and port input or output delays. For more information, refer to the <u>create clock</u>, <u>set input delay</u>, and <u>set output delay</u> commands.

The maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

Examples

The following example sets a maximum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

set_max_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}

The following example sets a maximum delay by constraining all paths to output ports whose names start by "out" with a delay less than 3.8 ns:

set_max_delay 3.8 -to [get_ports out*]

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



Microsemi Implementation Specifics

The -through option in the set_max_delay SDC command is not supported.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Max Delay



set_min_delay

SDC command; specifies the minimum delay for the timing paths.

set_min_delay delay_value [-from from_list] [-to to_list]

Arguments

delay_value

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-to *to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command specifies the required minimum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.

The tool automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. For more information, refer to the <u>create_clock</u>, <u>set_input_delay</u>, and <u>set_output_delay</u> commands.

The minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

Examples

The following example sets a minimum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:



set_min_delay 5 -from {ffla:CLK fflb:CLK} -to {ff2e:D}
The following example sets a minimum delay by constraining all paths to output ports whose names start by
"out" with a delay less than 3.8 ns:

set_min_delay 3.8 -to [get_ports out*]

Microsemi Implementation Specifics

The -through option in the set_min_delay SDC command is not supported.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions



set_multicycle_path

SDC command; defines a path that takes multiple clock cycles.

```
set_multicycle_path ncycles [-setup] [-hold] [-from from_list] [-through through_list] [-to
to_list]
```

Arguments

ncycles

Specifies an integer value that represents a number of cycles the data path must have for setup or hold check. The value is relative to the starting point or ending point clock, before data is required at the ending point.

-setup

Optional. Applies the cycle value for the setup check only. This option does not affect the hold check. The default hold check will be applied unless you have specified another set_multicycle_path command for the hold value.

-hold

Optional. Applies the cycle value for the hold check only. This option does not affect the setup check.

Note: If you do not specify "-setup" or "-hold", the cycle value is applied to the setup check and the default hold check is performed (*ncycles* -1).

-from from_list

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

-through through_list

Specifies a list of pins or ports through which the multiple cycle paths must pass.

-to to_list

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Setting multiple cycle paths constraint overrides the single cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks. If you change the multiplier, it affects both the setup and hold checks.

False path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

If you specify more than one object within one -through option, the path passes through any of the objects.

Examples

The following example sets all paths between reg1 and reg2 to 3 cycles for setup check. Hold check is measured at the previous edge of the clock at reg2.

set_multicycle_path 3 -from [get_pins {reg1}] -to [get_pins {reg2}]

The following example specifies that four cycles are needed for setup check on all paths starting at the registers in the clock domain ck1. Hold check is further specified with two cycles instead of the three cycles that would have been applied otherwise.

set_multicycle_path 4 -setup -from [get_clocks {ck1}]



set_multicycle_path 2 -hold -from [get_clocks {ck1}]

Microsemi Implementation Specifics

• SDC allows multiple priority management on the multiple cycle path constraint depending on the scope of the object accessors. In Microsemi design implementation, such priority management is not supported. All multiple cycle path constraints are handled with the same priority.

See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Multicycle Path



set_output_delay

SDC command; defines the output delay of an output relative to a clock.

set_output_delay delay_value -clock clock_ref [-max] [-min] [-clock_fall] output_list

Arguments

delay_value

Specifies the amount of time before a clock edge for which the signal is required. This represents a combinational path delay to a register outside the current design plus the library setup time (for maximum output delay) or hold time (for minimum output delay).

-clock clock_ref

Specifies the clock reference to which the specified output delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

-max

Specifies that delay_value refers to the longest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

Specifies that delay_value refers to the shortest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

-clock_fall

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge. output_list

Provides a list of output ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The set_output_delay command sets output path delays on output ports relative to a clock edge. Output ports have no output delay unless you specify it. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds output delay to path delay for paths ending at primary outputs.

Examples

The following example sets an output delay of 1.2ns for port OUT1 relative to the rising edge of CLK1:

set_output_delay 1.2 -clock [get_clocks CLK1] [get_ports OUT1]

The following example sets a different maximum and minimum output delay for port OUT1 relative to the falling edge of CLK2:

set_output_delay 1.0 -clock_fall -clock CLK2 -min {OUT1}
set_output_delay 1.4 -clock_fall -clock CLK2 -max {OUT1}

Microsemi Implementation Specifics

• In SDC, the -clock is an optional argument that allows you to set the output delay for combinational designs. Microsemi Implementation currently requires this option.



See Also

Constraint Support by Family Constraint Entry Table SDC Syntax Conventions Set Output Delay

Design Object Access Commands

Design object access commands are SDC commands. Most SDC constraint commands require one of these commands as command arguments.

Design Object	Access Command
Cell	<u>get_cells</u>
Clock	<u>get_clocks</u>
Net	<u>get_nets</u>
Port	<u>get_ports</u>
Pin	<u>get pins</u>
Input ports	all_inputs
Output ports	all outputs
Registers	all_registers

Microsemi software supports the following SDC access commands:

See Also

About SDC Files



all_inputs

Design object access command; returns all the input or inout ports of the design.

all_inputs

Arguments

None

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Exceptions

None

Example

set_max_delay -from [all_inputs] -to [get_clocks ck1]

Microsemi Implementation Specifics

None

See Also



all_outputs

Design object access command; returns all the output or inout ports of the design.

all_outputs

Arguments

None

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Exceptions

None

Example

set_max_delay -from [all_inputs] -to [all_outputs]

Microsemi Implementation Specifics

None

See Also



all_registers

<u>Design object access command</u>; returns either a collection of register cells or register pins, whichever you specify.

```
all_registers [-clock clock_name] [-cells] [-data_pins ]
[-clock_pins] [-async_pins] [-output_pins]
```

Arguments

-clock clock_name

Creates a collection of register cells or register pins in the specified clock domain.

-cells

Creates a collection of register cells. This is the default. This option cannot be used in combination with any other option.

-data_pins

Creates a collection of register data pins.

-clock_pins

Creates a collection of register clock pins.

-async_pins

Creates a collection of register asynchronous pins.

-output_pins

Creates a collection of register output pins.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command creates either a collection of register cells (default) or register pins, whichever is specified. If you do not specify an option, this command creates a collection of register cells.

Exceptions

None

Examples

```
set_max_delay 2 -from [all_registers] -to [get_ports {out}]
set_max_delay 3 -to [all_registers -async_pins]
set_false_path -from [all_registers -clock clk150]
set_multicycle_path -to [all_registers -clock c* -data_pins
-clock_pins]
```

Microsemi Implementation Specifics

None

See Also



get_cells

Design object access command; returns the cells (instances) specified by the pattern argument.

get_cells pattern

Arguments

pattern

Specifies the pattern to match the instances to return. For example, "get_cells U18*" returns all instances starting with the characters "U18", where "*" is a wildcard that represents any character string.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command returns a collection of instances matching the pattern you specify. You can only use this command as part of a –from, -to, or –through argument for the following constraint exceptions: set_max delay, set_multicycle_path, and set_false_path design constraints.

Exceptions

None

Examples

set_max_delay 2 -from [get_cells {reg*}] -to [get_ports {out}]
set_false_path -through [get_cells {Rblock/muxA}]

Microsemi Implementation Specifics

None

See Also



get_clocks

Design object access command; returns the specified clock.

get_clocks pattern

Arguments

pattern

Specifies the pattern to match to the SmartTime on which a clock constraint has been set.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

- If this command is used as a -from argument in maximum delay (set_max_path_delay), false path (set_false_path), and multicycle constraints (set_multicycle_path), the clock pins of all the registers related to this clock are used as path start points.
- If this command is used as a -to argument in maximum delay (set_max_path_delay), false path (set false path), and multicycle constraints (set multicycle path), the synchronous pins of all the registers related to this clock are used as path endpoints.

Exceptions

None

Example

set_max_delay -from [get_ports datal] -to \
[get_clocks ck1]

Microsemi Implementation Specifics

None

See Also



get_pins

Design object access command; returns the specified pins.

get_pins pattern

Arguments

pattern Specifies the pattern to match the pins.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Exceptions

None

Example

create_clock -period 10 [get_pins clock_gen/reg2:Q]

Microsemi Implementation Specifics

None

See Also



get_nets

Design object access command; returns the named nets specified by the pattern argument.

get_nets *pattern*

Arguments

pattern

Specifies the pattern to match the names of the nets to return. For example, "get_nets N_255*" returns all nets starting with the characters "N_255", where "*" is a wildcard that represents any character string.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command returns a collection of nets matching the pattern you specify. You can only use this command as source objects in create clock (<u>create_clock</u>) or create generated clock (<u>create_generated_clock</u>) constraints and as -through arguments in set false path (<u>set_false_path</u>), set minimum delay (set_min_delay), set maximum delay (<u>set_max_delay</u>), and set multicycle path (<u>set_multicycle_path</u>) constraints.

Exceptions

None

Examples

set_max_delay 2 -from [get_ports RDATA1] -through [get_nets {net_chkpl net_chkqi}]
set_false_path -through [get_nets {Tblk/rm/n*}]
create_clcok -name mainCLK -per 2.5 [get_nets {cknet}]

Microsemi Implementation Specifics

None

See Also



get_ports

Design object access command; returns the specified ports.

get_ports *pattern*

Argument

pattern

Specifies the pattern to match the ports. This is equivalent to the macros \$in()[<pattern>] when used as – from argument and \$out()[<pattern>] when used as –to argument or \$ports()[<pattern>] when used as a – through argument.

Supported Families

SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion

Exceptions

None

Example

create_clock -period 10[get_ports CK1]

Microsemi Implementation Specifics

None

See Also



Glossary

arrival time

Actual time in nanoseconds at which the data arrives at a sink pin when considering the propagation delays across the path.

asynchronous

Two signals that are not related to each other. Signals not related to the clock are usually asynchronous.

capture edge

The clock edge that triggers the capture of data at the end point of a path.

clock

A periodic signal that captures data into sequential elements.

critical path

A path with the maximum delay between a starting point and an end point. In the presence of a clock constraint, the worst critical path between registers in this clock domain is the path with the worst slack.

dynamic timing analysis

The standard method for verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface.

exception

See timing exception.

explicit clock

Clock sources that can be traced back unambiguously from the clock pin of the registers they deserve, including the output of a DLL or PLL.

filter

A set of limitations applied to object names in timing analysis to generate target specific sets.

launch edge

The clock edge that triggers the release of data from a starting point to be captured by another clock edge at an end point.

minimum period

Timing characteristic of a path between two registers. It indicates how fast the clock will run when this path is the most critical one. The minimum period value takes into consideration both the skew and the setup on the receiving register.

parallel paths

Paths that run in parallel between a given source and sink pair.



path

A sequence of elements in the design that identifies a logical flow starting at a source pin and ending at a sink pin.

path details

An expansion of the path that shows all the nets and cells between the source pin and the sink pin.

path set

A collection of paths.

paths list

Same as path set.

post-layout

The state of the design after you run Layout. In post-layout, the placement and routing information are available for the whole design.

potential clock

Pins or ports connected to the clock pins of sequential elements that the Static Timing Analysis (STA) tool cannot determine whether they are is enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks.

pre-layout

The state of the design before you run Layout. In pre-layout, the placement and routing information are not available.

recovery time

The amount of time before the active clock edge when the de-activation of asynchronous signals is not allowed.

removal time

The amount of time after the active clock edge when the de-activation of asynchronous signals is not allowed.

required time

The time at which the data must be at a sink pin to avoid being in violation.

requirement

See timing requirement.

scenario (timing constraints scenario)

Set of timing constraints defined by the user.

setup time

The time in nanoseconds relative to a clock edge during which the data at the input to a sequential element must remain stable.



sink pin

The pin located at the end of the timing path. This pin is usually the one where arrival time and required time are evaluated for path violation.

skew

The difference between the clock insertion delay to the clock pin of a sink register and the insertion delay to the clock pin of a source register.

slack

The difference between the arrival time and the required time at a specific pin, generally at the data pin of a sequential component.

slew rate

The time needed for a signal to transition from one logic level to another.

source pin

The pin located at the beginning of a timing path.

STA

See static timing analysis.

standard delay format (SDF)

Standard Delay Format, a standard file format used to store design data suited for back-annotation.

static timing analysis

An efficient technique to identify timing violations in a design and to ensure that all timing requirements are met. It is well suited for traditional synchronous designs. The main advantages are that it does not require input vectors, and it exclusively covers all possible paths in the design in a relatively short run-time.

synopsys design constraint (SDC)

A standard file format for timing constraints. Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi SoC tools use a subset of the SDC format to capture supported timing constraints. You can import or export an SDC file from the Designer software. Any timing constraint that you can enter using Designer tools, can also be specified in an SDC file.

timing constraint

A requirement or limitation on the design to be satisfied during the design implementation.

timing exception

An exception to a general requirement usually applied on a subset of the objects on which the requirement is applied.

timing requirement

A constraint on the design usually determined by the specifications at the system level.



virtual clock

A virtual clock is a clock with no source associated to it. It is used to describe clocks outside the FPGA that have an impact on the timing analysis inside the FPGA. For example, if the I/Os are synchronous to an external clock.

WLM

Wire Load Model. A timing model used in pre-layout to estimate a net delay based on the fan-out.



Product Support

The Microsemi SoC Products Group backs its products with various support services including a Customer Technical Support Center and Non-Technical Customer Service. This appendix contains information about contacting the SoC Products Group and using these support services.

Contacting the Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.800.262.1060

Phone (International): +1 650.318.4460

Email: soc_tech@microsemi.com

ITAR Technical Support

Microsemi customers can receive ITAR technical support on Microsemi SoC products by calling ITAR Technical Support Hotline: Monday through Friday, from 9 AM to 6 PM Pacific Time. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.888.988.ITAR

Phone (International): +1 650.318.4900

Email: soc_tech_itar@microsemi.com

Non-Technical Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

Microsemi's customer service representatives are available Monday through Friday, from 8 AM to 5 PM Pacific Time, to answer non-technical questions.

Phone: +1 650.318.2470



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