Total Ionizing Dose Test Report

No. 14T-RTSX72SU-CQ256-D1RCS1

May 19, 2014

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CK Huang and J.J. Wang

(408) 643-6136, (408) 643-6302

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

Parameter	Tolerance
1.Gross Functionality	Passed 100 krad (SiO2)
2.Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO2)
3.Input Threshold (VIL/VIH)	Passed 100 krad (SiO2)
4.Output Drive (VOL/VOH)	Passed 100 krad (SiO2)
5.Propagation Delay	Passed 100 krad (SiO2) for 10% degradation criterion
6.Transition Characteristics	Passed 100 krad (SiO2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a 1K Ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1RCS1
Quantity Tested	6
Serial Number	40 krad(SiO2): 3685, 3695 60 krad(SiO2): 3719, 3819 100 krad(SiO2): 3822, 3827
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

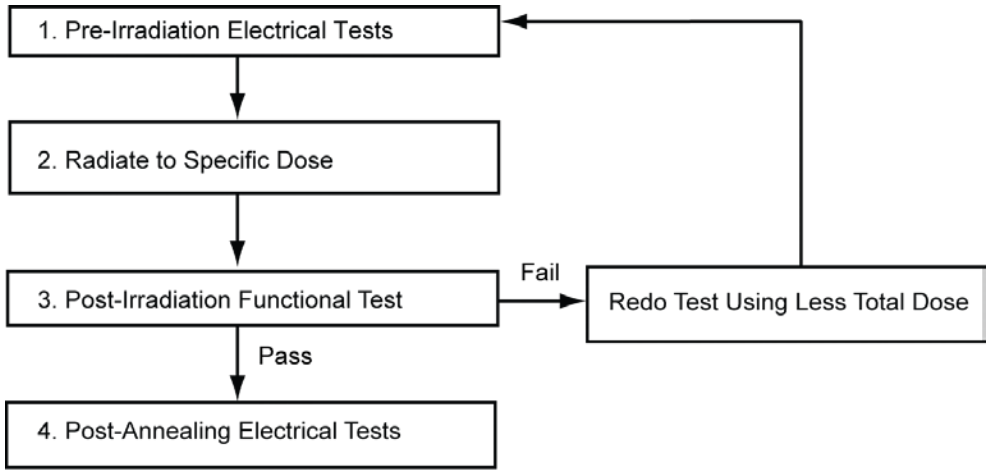


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging or rebound test mentioned in TM1019.8 is unnecessary, because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at CLOCK input to the time of switching state at output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1.Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2.ICC (ICCA/ICCI)	DUT power supply
3.Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4.Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5.Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6.Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
3685	40 krad	1.28	3	1	0.74	1	1
3695	40 krad	1.36	5	3	0.81	3	2
3719	60 krad	1.23	24	28	0.76	78	15
3819	60 krad	1.32	22	24	0.73	26	14
3822	100 krad	3.08	287	209	8.23	231	78
3827	100 krad	1.50	333	199	5.07	239	86

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test is defined as the highest ICCA/ICCI in the RTSXSU spec sheet of 25 mA.

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT.

There are unexpected ICCI increases during irradiation as shown. In Figures 3 through 7 the ICCI shows more noises at some points of time. The suspect is an intermittent continuity problem of the socket on the test board.

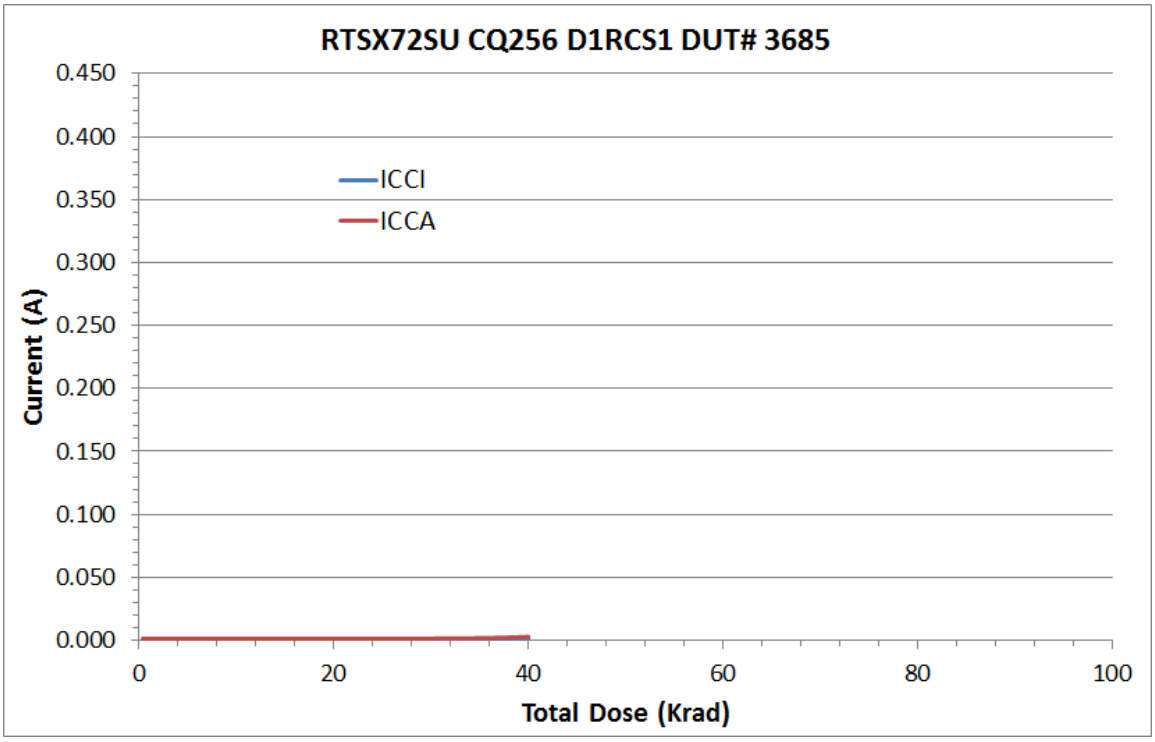


Figure 2 DUT 3685 Influx ICCA and ICCI

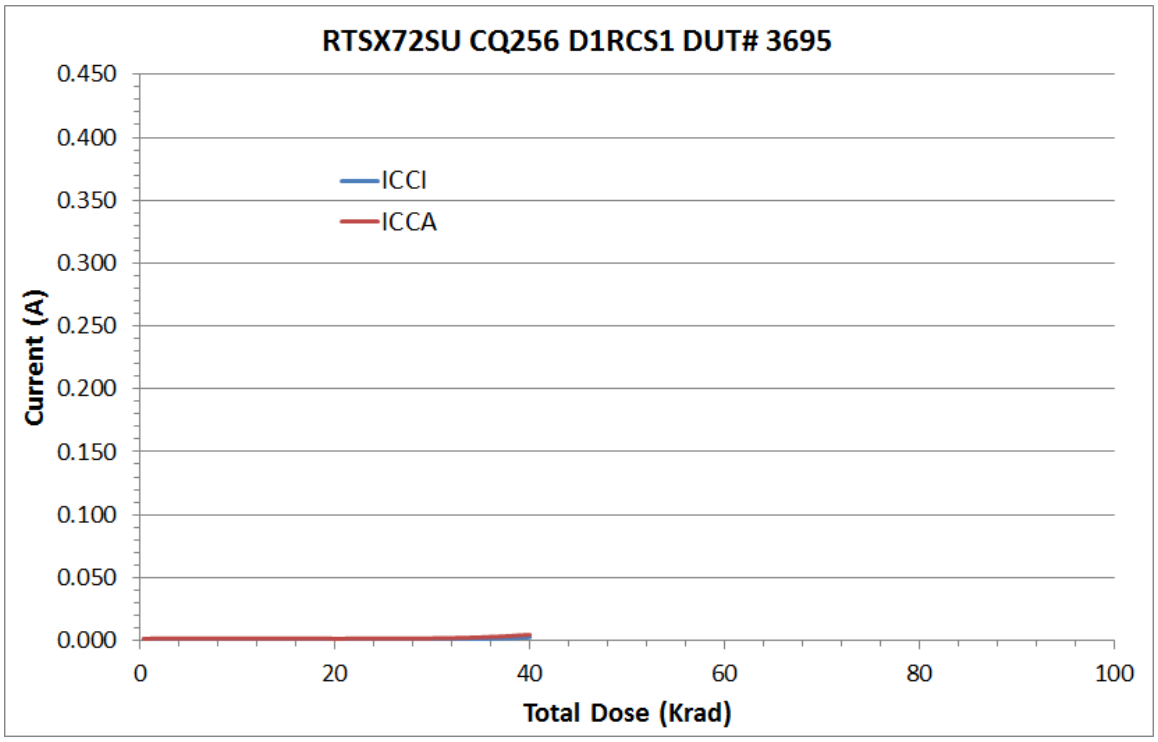


Figure 3 DUT 3695 Influx ICCA and ICCI

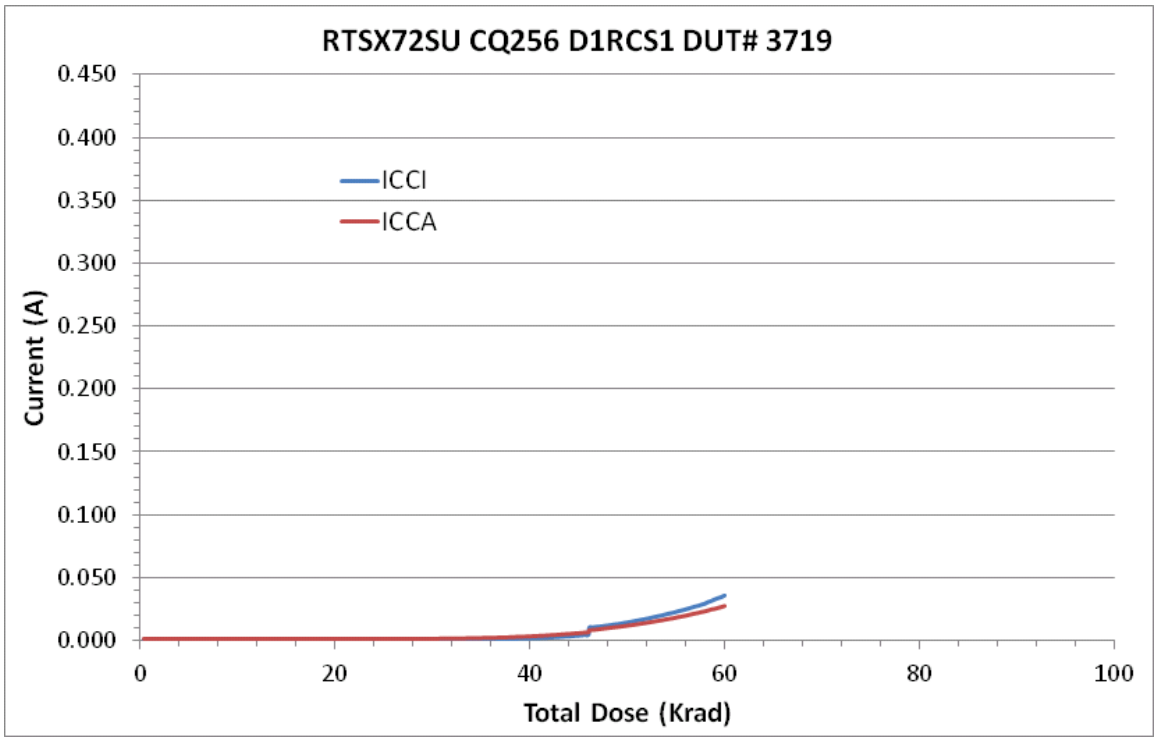


Figure 4 DUT 3719 Influx ICCA and ICCI

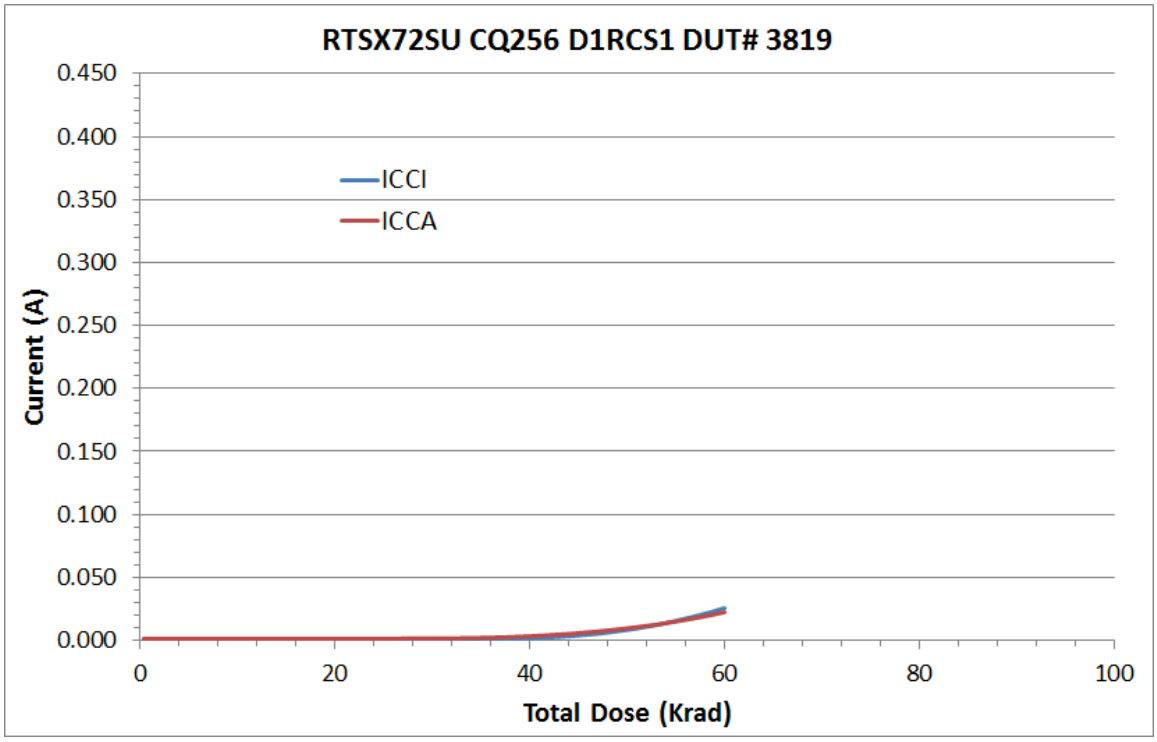


Figure 5 DUT 3819 Influx ICCA and ICCI

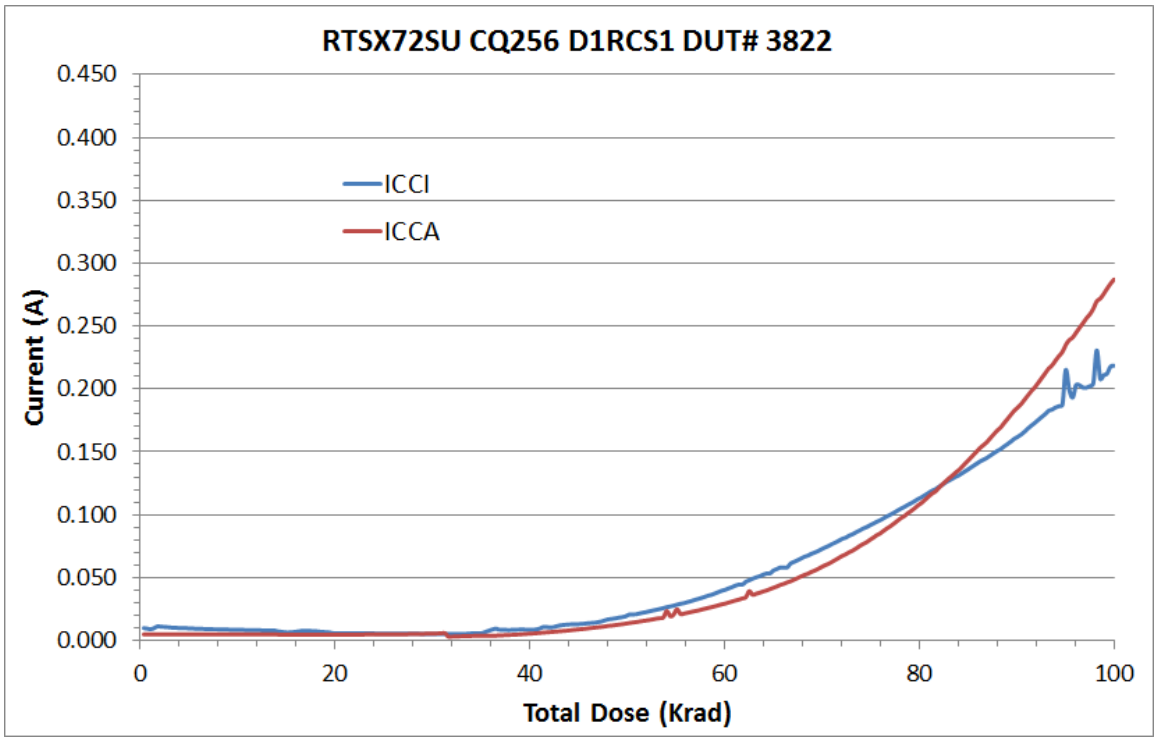


Figure 6 DUT 3822 Influx ICCA and ICCI

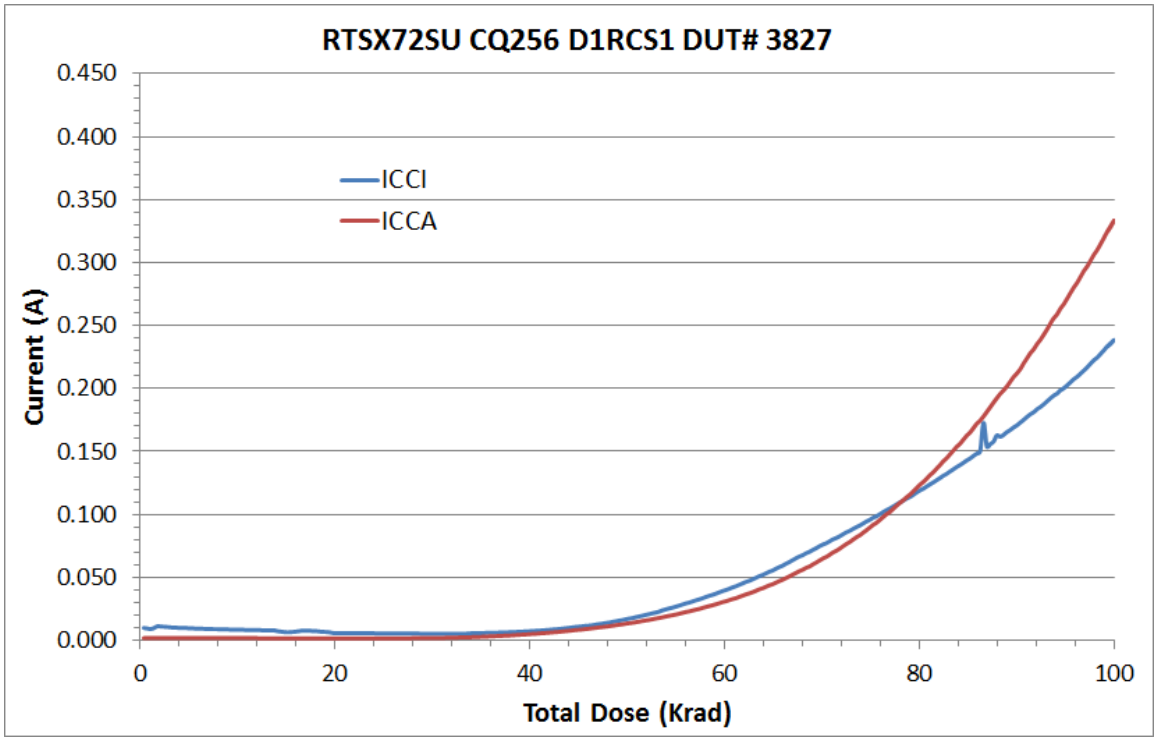


Figure 7 DUT 3827 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds.

Some parameters of certain samples show more post-annealing shift, which could be caused by measurement sensitivity from the setup, as no obvious dose dependence is seen.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	3685 (40 krad)				3695 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1150	1500	1085	1530	1160	1550	1095	1525
DAH/QA0H	1425	1435	1425	1410	1460	1465	1445	1400
ENCNTRH/YO0H	1490	1965	1510	1980	1490	1925	1530	1985
IDII0/IDIO0	1385	1460	1360	1425	1475	1450	1380	1405
IDII1/IDIO1	1470	1440	1490	1390	1535	1490	1495	1395
IDII2/IDIO2	1270	1400	1305	1390	1410	1430	1300	1395
IDII3/IDIO3	1400	1420	1455	1380	1515	1450	1455	1390
IDII4/IDIO4	1460	1400	1445	1425	1470	1410	1455	1460
IDII5/IDIO5	1280	1505	1410	1360	1300	1435	1420	1370
IDII6/IDIO6	1450	1425	1380	1405	1435	1460	1365	1390
IDII7/IDIO7	1450	1440	1430	1380	1440	1475	1440	1385

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	3719 (60 krad)				3819 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1335	1480	1170	1480	1295	1475	1115	1540
DAH/QA0H	1490	1495	1440	1425	1455	1450	1450	1425
ENCNTRH/YO0H	910	1945	840	1965	870	1970	840	1990
IDII0/IDIO0	1415	1480	1360	1415	1465	1435	1440	1425
IDII1/IDIO1	1535	1490	1480	1380	1425	1450	1495	1390
IDII2/IDIO2	1440	1430	1285	1395	1330	1415	1300	1485
IDII3/IDIO3	1550	1455	1455	1380	1515	1440	1460	1400
IDII4/IDIO4	1460	1410	1440	1420	1365	1450	1450	1430
IDII5/IDIO5	1405	1435	1470	1350	1455	1500	1480	1465
IDII6/IDIO6	1475	1445	1355	1385	1435	1460	1380	1415
IDII7/IDIO7	1460	1480	1465	1395	1470	1425	1440	1385

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	3822 (100 krad)				3827 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1255	1480	1160	1555	1225	1530	1190	1595
DAH/QA0H	1450	1445	1460	1445	1515	1500	1515	1520
ENCNTRH/YO0H	895	1950	840	1985	960	1935	1495	1990
IDII0/IDIO0	1395	1450	1375	1415	1380	1500	1425	1470
IDII1/IDIO1	1440	1455	1510	1425	1465	1520	1520	1440
IDII2/IDIO2	1245	1425	1420	1405	1425	1450	1490	1445
IDII3/IDIO3	1515	1450	1395	1405	1545	1475	1495	1425
IDII4/IDIO4	1475	1415	1440	1420	1470	1470	1440	1420
IDII5/IDIO5	1445	1525	1405	1360	1245	1575	1380	1360
IDII6/IDIO6	1405	1440	1450	1425	1455	1500	1440	1435
IDII7/IDIO7	1440	1440	1490	1405	1470	1505	1505	1430

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	3685 (40 krad)		3695 (40 krad)		3719 (60 krad)		3819 (60 krad)		3822 (100 krad)		3827 (100 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	10	10	10	10	10	10	10	10	11	10	11
12 mA	116	119	117	120	117	120	118	120	115	119	116	119
20 mA	193	197	195	200	195	199	196	200	192	198	193	198
50 mA	484	496	490	501	489	500	492	501	483	497	485	498
100 mA	990	1014	1004	1026	1001	1023	1006	1026	989	1016	994	1018

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	3685 (40 krad)		3695 (40 krad)		3719 (60 krad)		3819 (60 krad)		3822 (100 krad)		3827 (100 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4978	4976	4978	4976	4978	4978	4978	4978	4978	4979	4978	4979
8 mA	4842	4835	4845	4837	4843	4839	4844	4839	4846	4842	4843	4840
20 mA	4604	4587	4611	4594	4606	4595	4607	4596	4612	4602	4606	4597
50 mA	3953	3912	3974	3932	3957	3929	3966	3936	3979	3952	3962	3938
100 mA	2399	2243	2489	2345	2414	2330	2460	2371	2528	2460	2457	2394

F. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion; take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Anneal (µs)	Degradation (%)
3685	40 krad	1.39	1.38	-0.36%
3695	40 krad	1.40	1.40	-0.36%
3719	60 krad	1.36	1.36	0.00%
3819	60 krad	1.34	1.35	0.75%
3822	100 krad	1.36	1.40	2.94%
3827	100 krad	1.37	1.40	2.20%

G. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

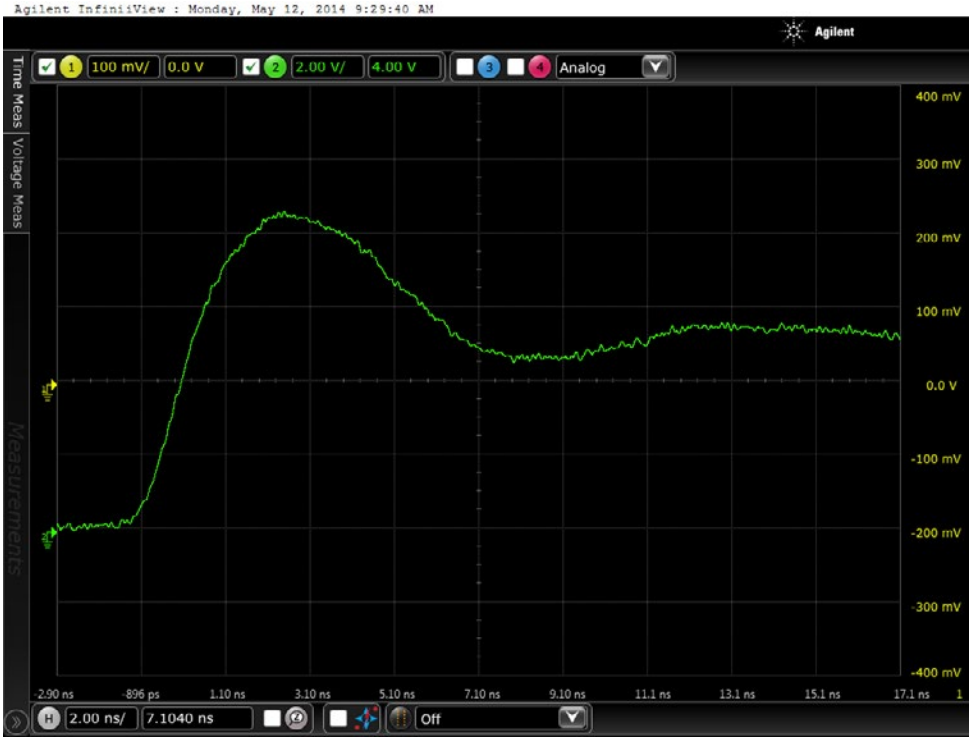


Figure 9a DUT 3685 Pre-Irradiation Rising Edge

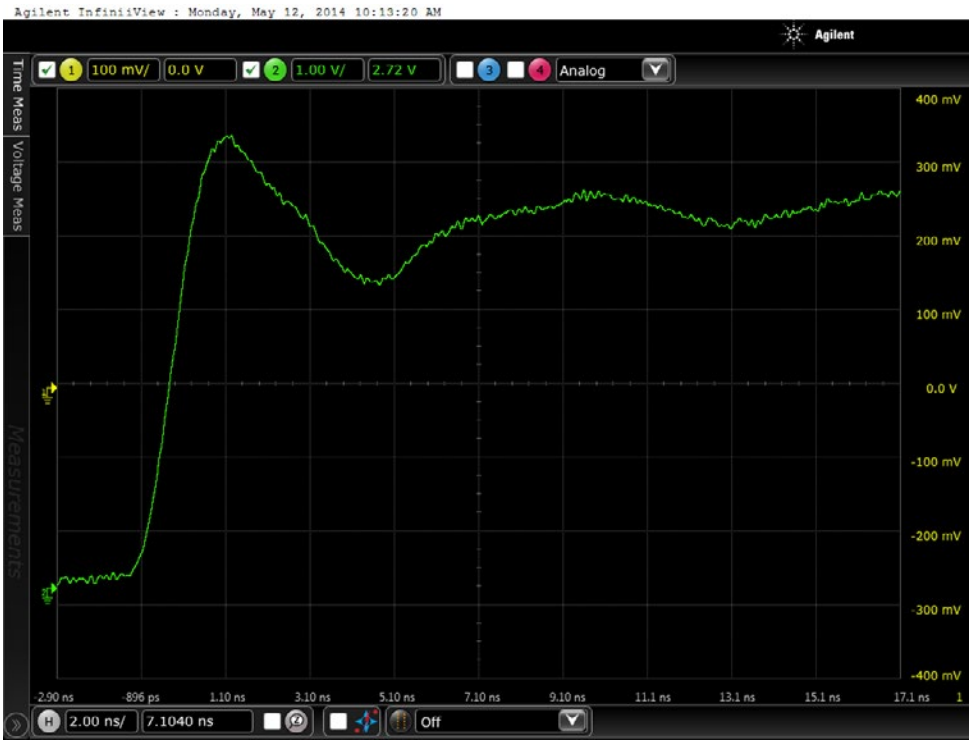


Figure 9b DUT 3685 Post-Annealing Rising Edge

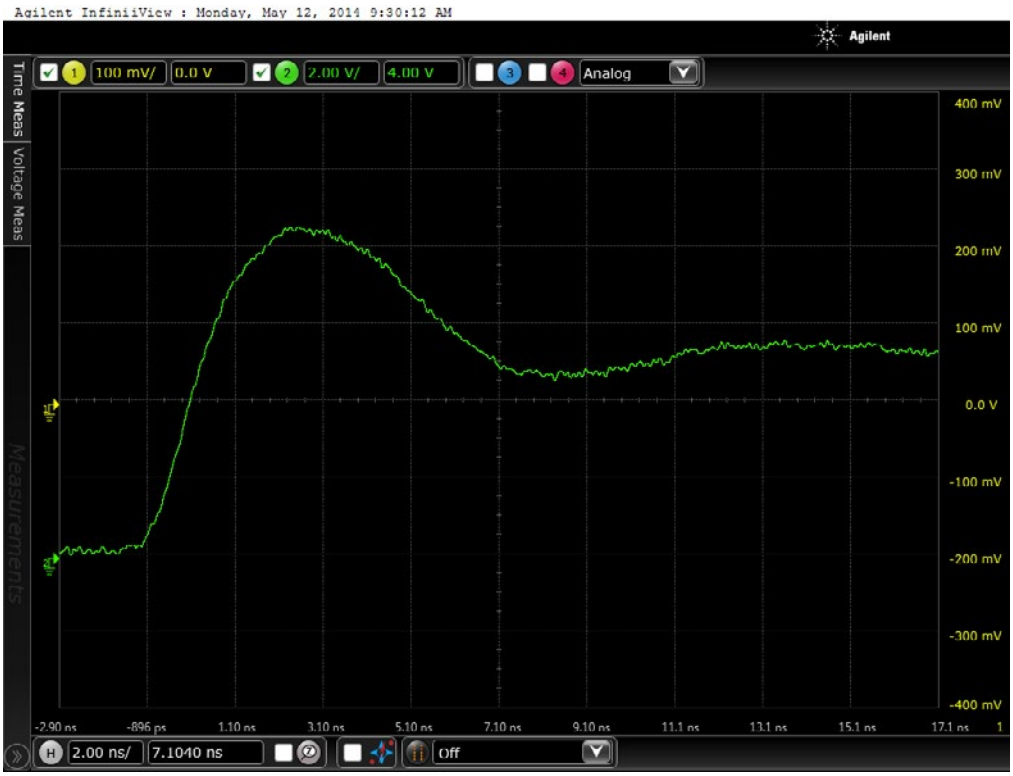


Figure 10a DUT 3695 Pre-Irradiation Rising Edge

Figure 10b DUT 3695 Post-Annealing Rising Edge

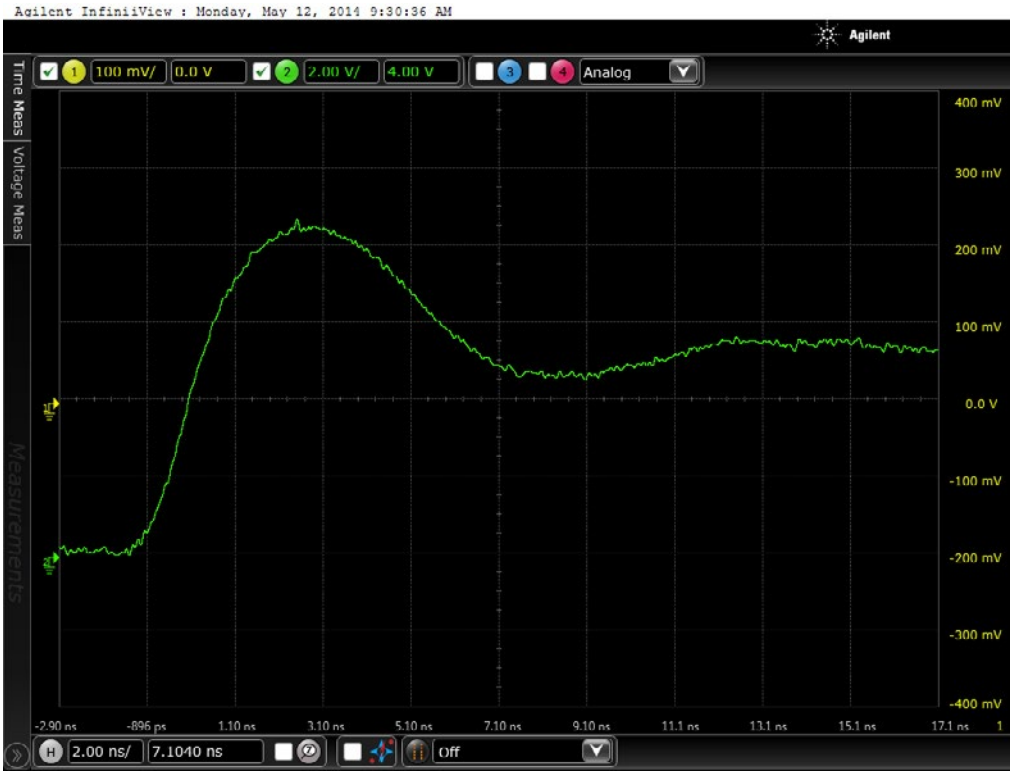


Figure 11a DUT 3719 Pre-Radiation Rising Edge

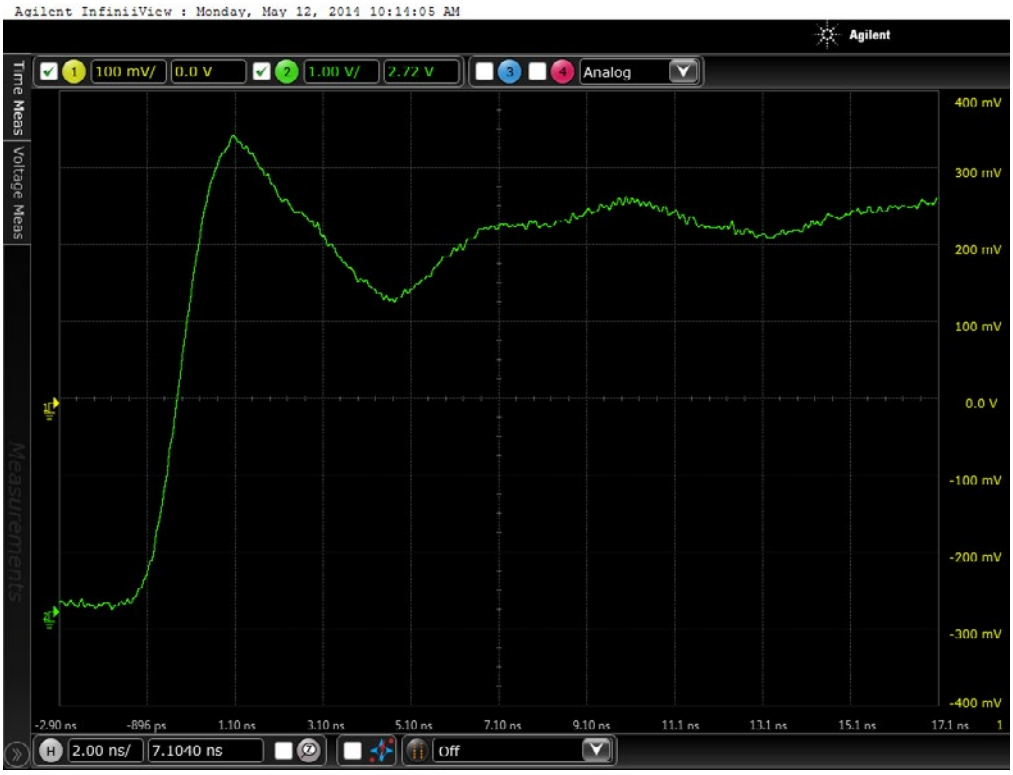


Figure 11b DUT 3719 Post-Annealing Rising Edge

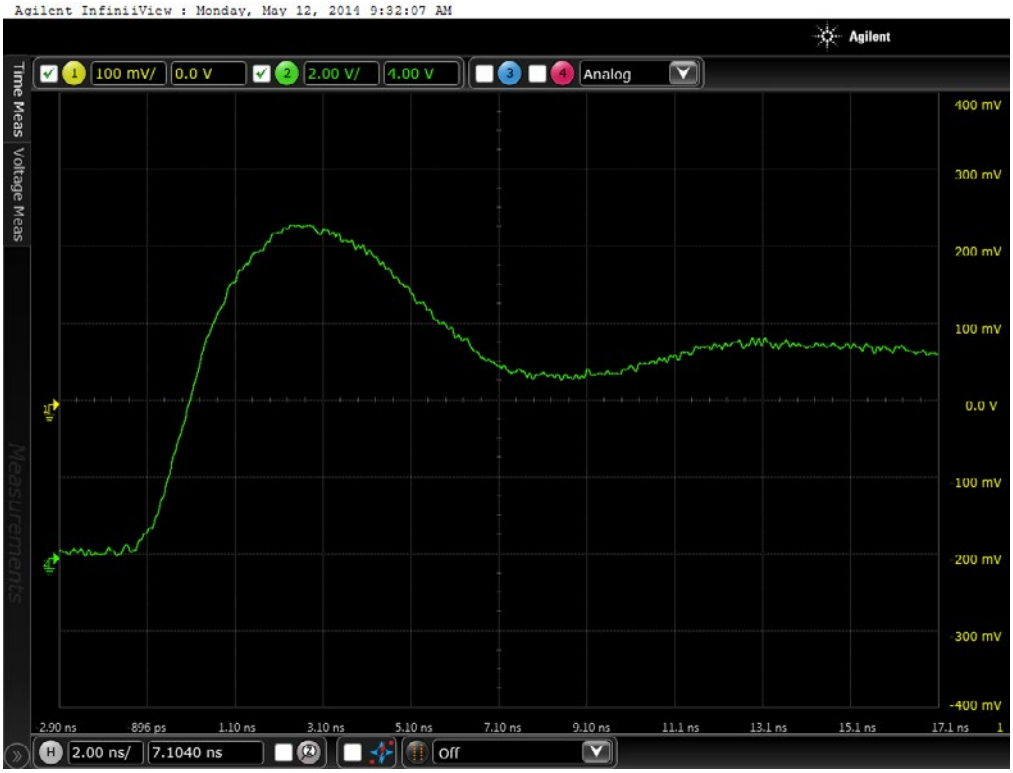


Figure 12a DUT 3819 Pre-Irradiation Rising Edge

Figure 12b DUT 3819 Post-Annealing Rising Edge

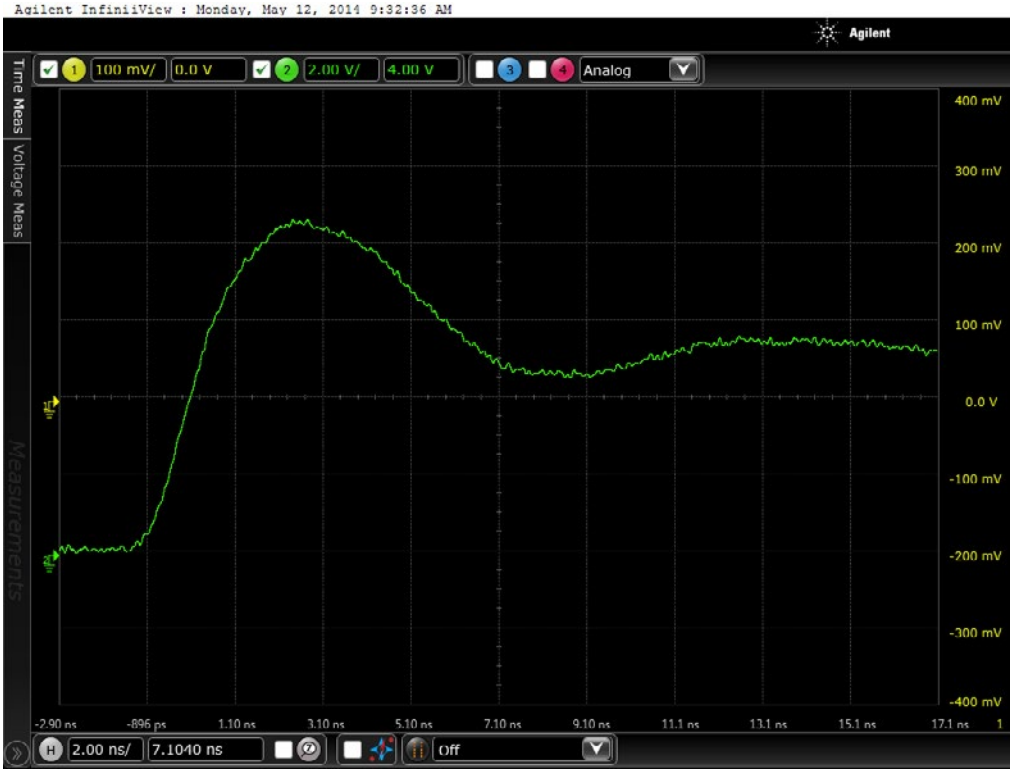


Figure 13a DUT 3822 Pre-Irradiation Rising Edge

Figure 13b DUT 3822 Post-Annealing Rising Edge

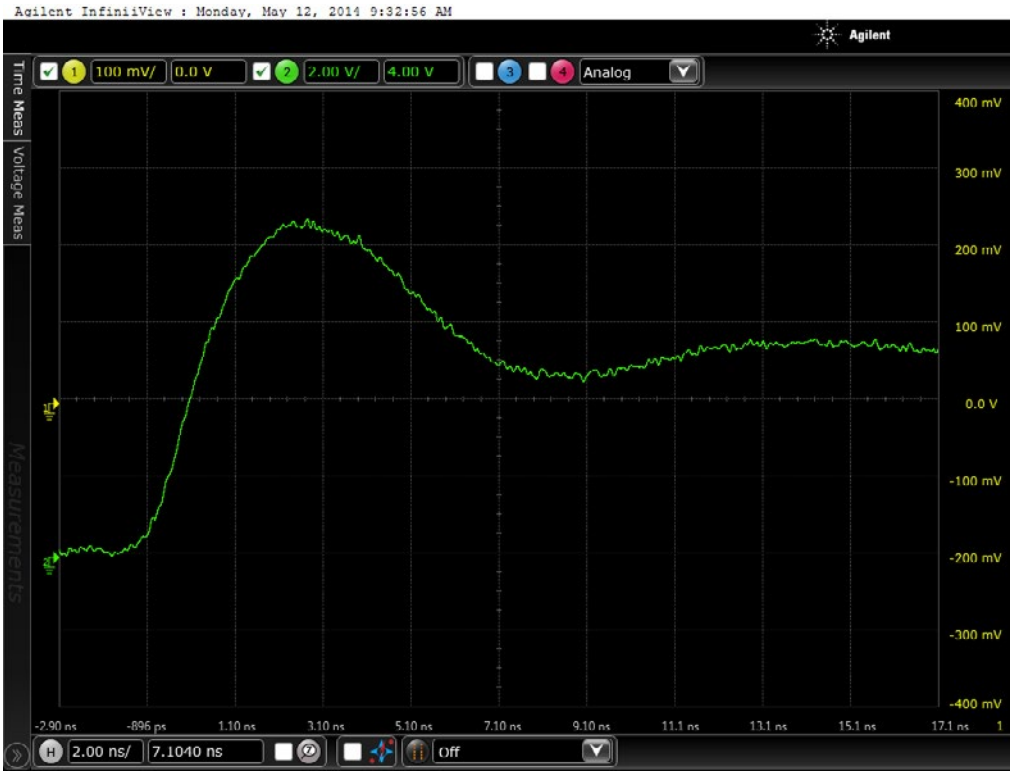


Figure 14a DUT 3827 Pre-Irradiation Rising Edge

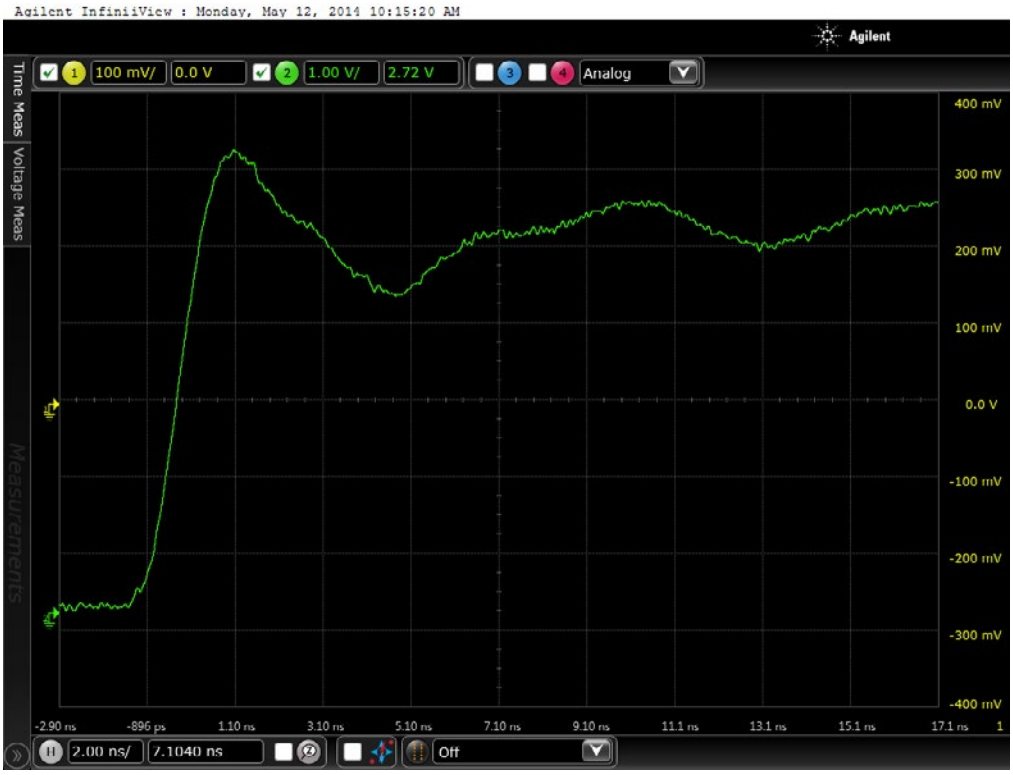


Figure 14b DUT 3827 Post-Annealing Rising Edge

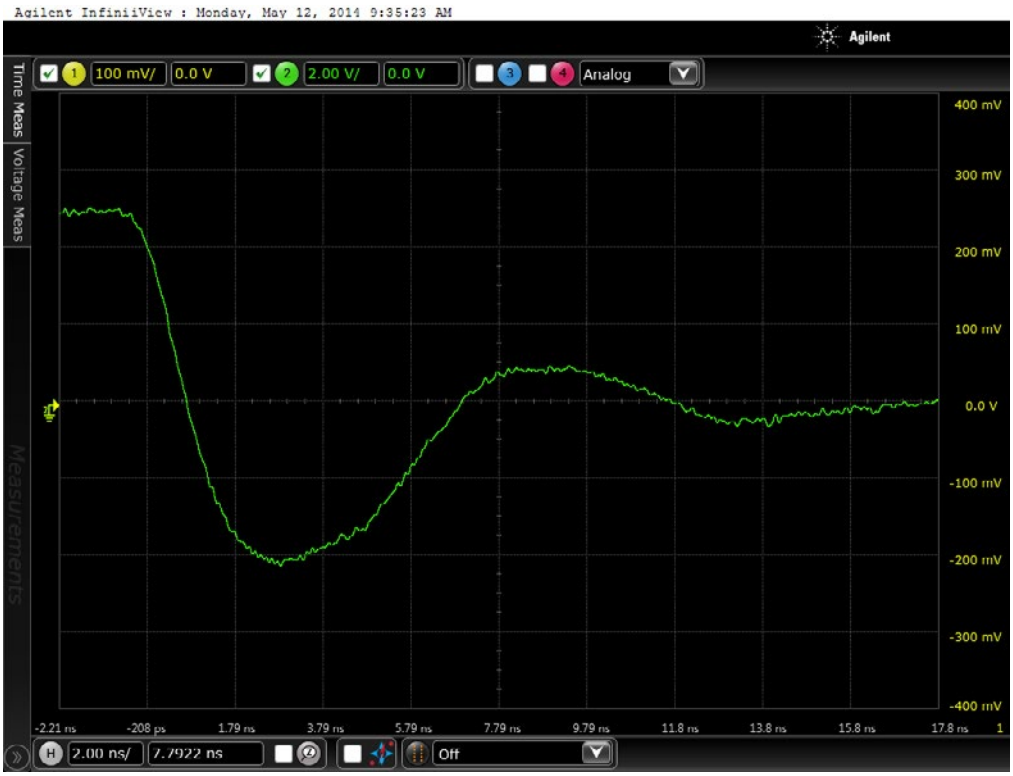


Figure 15a DUT 3685 Pre-Radiation Falling Edge

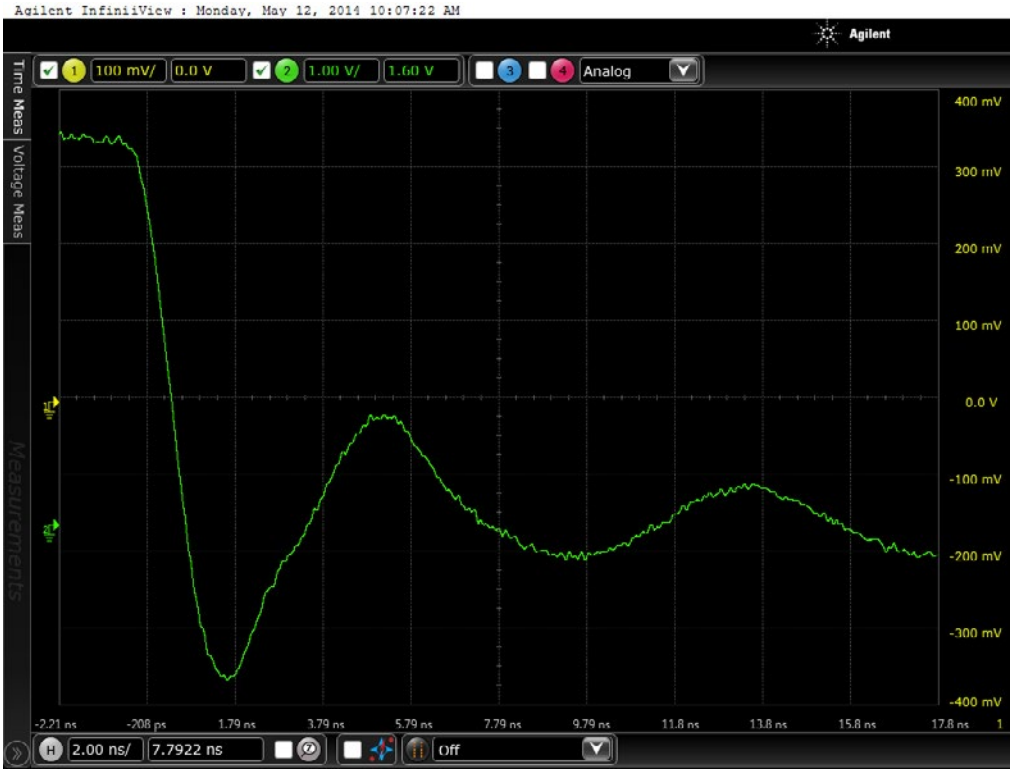


Figure 15b DUT 3685 Post-Annealing Falling Edge

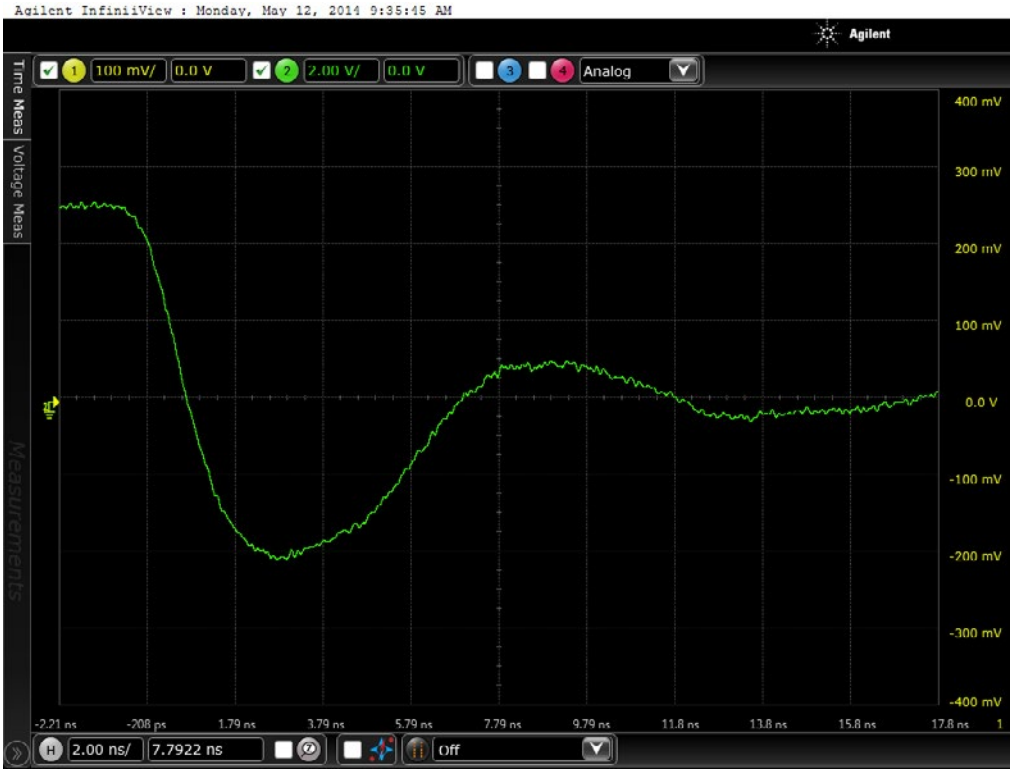


Figure 16a DUT 3695 Pre-Irradiation Falling Edge

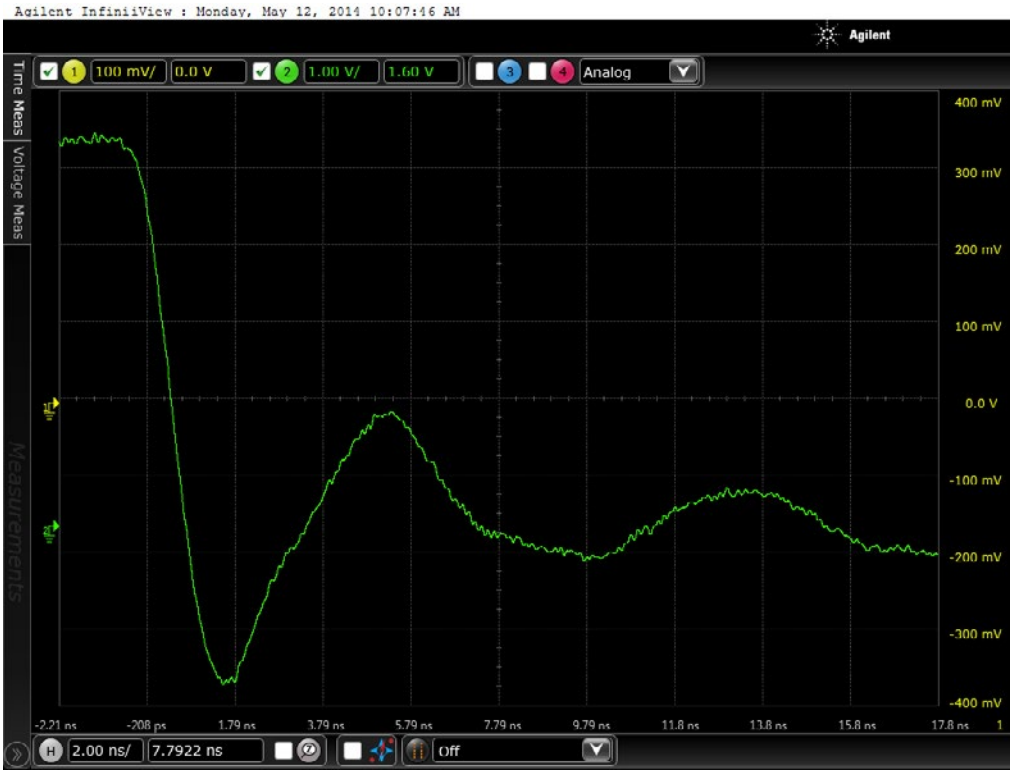


Figure 16b DUT 3695 Post-Annealing Falling Edge

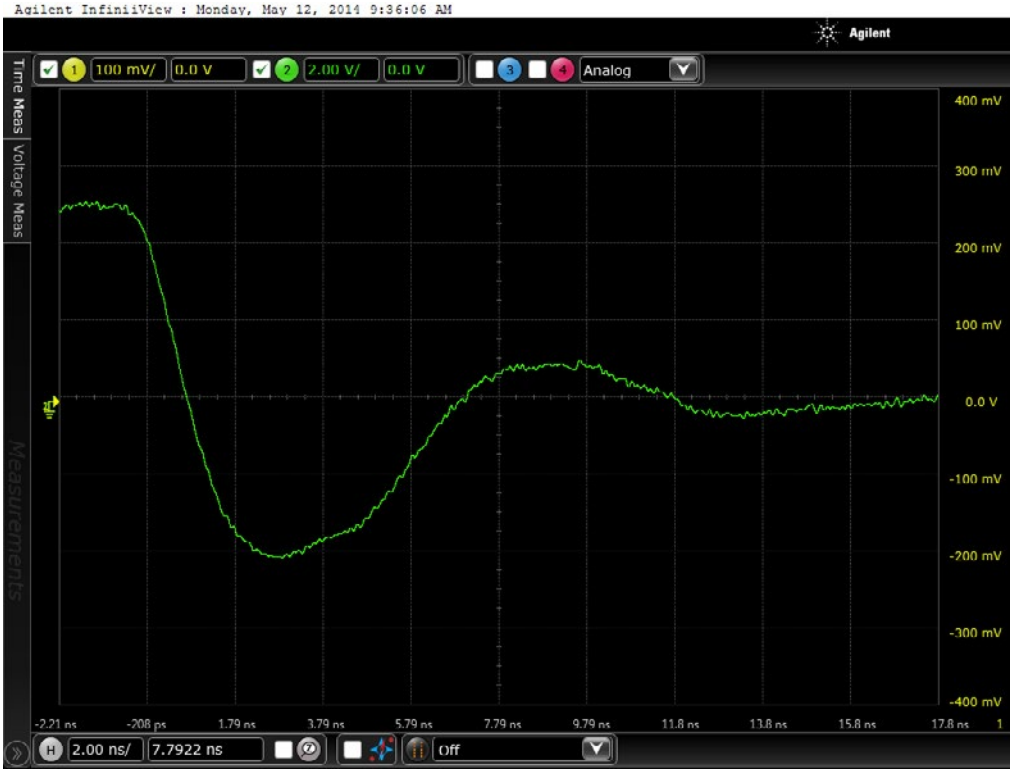


Figure 17a DUT 3719 Pre-Irradiation Falling Edge

Figure 17b DUT 3719 Post-Annealing Falling Edge

Figure 18a DUT 3819 Pre-Irradiation Falling Edge

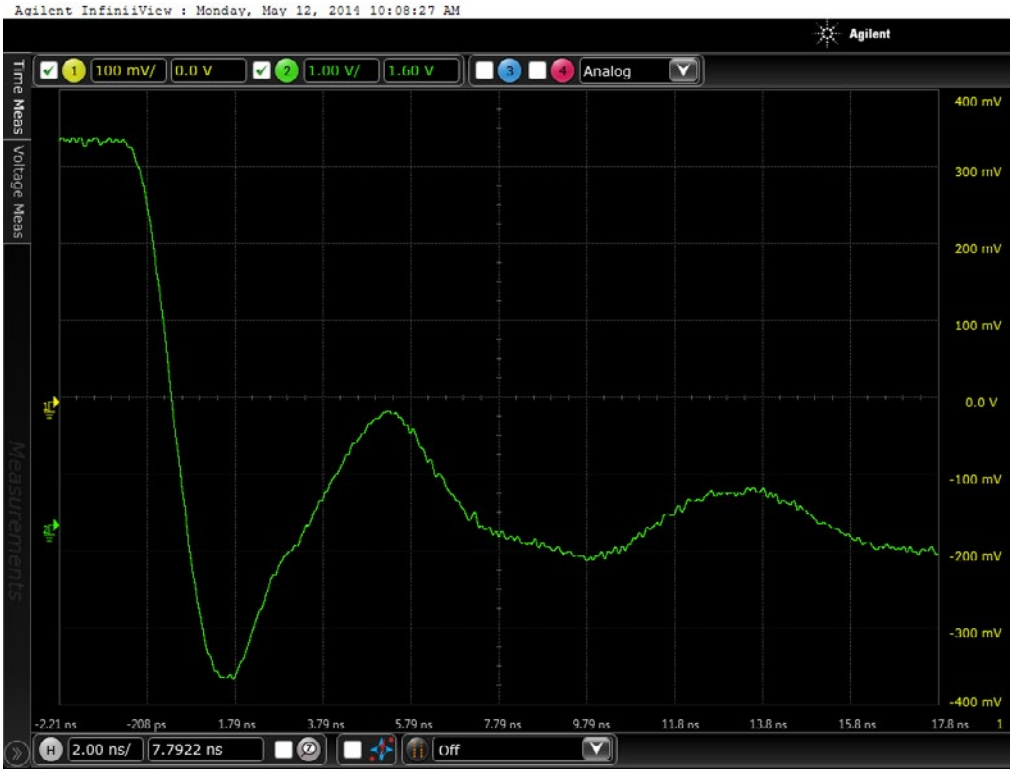


Figure 18b DUT 3819 Post-Annealing Falling Edge

Figure 19a DUT 3822 Pre-Irradiation Falling Edge

Figure 19b DUT 3822 Post-Annealing Falling Edge

Figure 20a DUT 3827 Pre-Irradiation Falling Edge

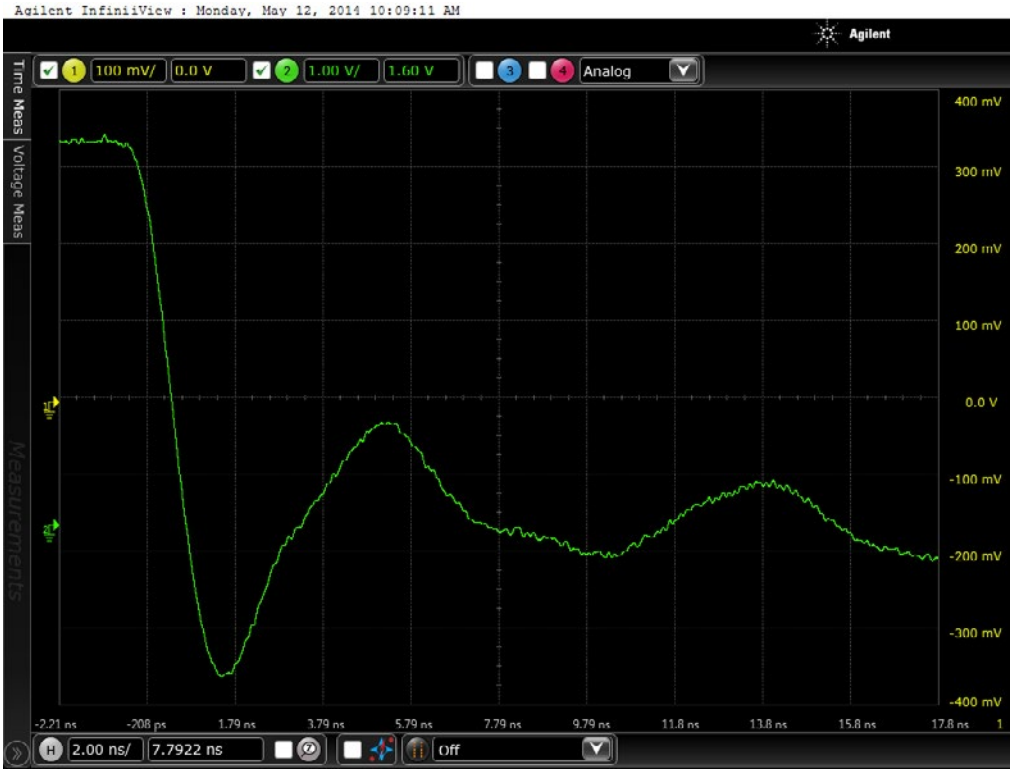


Figure 20b DUT 3827 Post-Annealing Falling Edge

Appendix A: DUT Bias

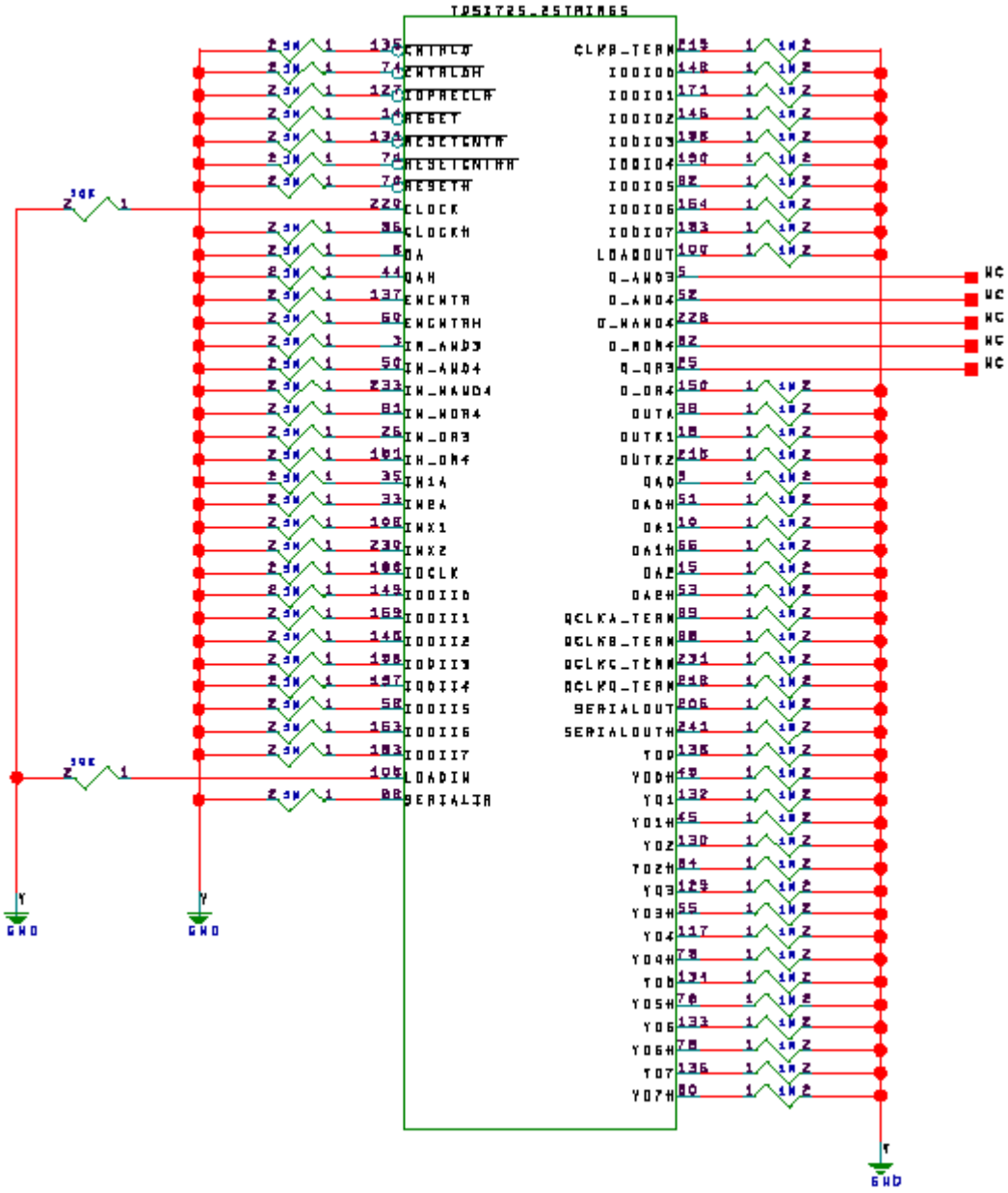


Figure A1 I/O Bias During Irradiation

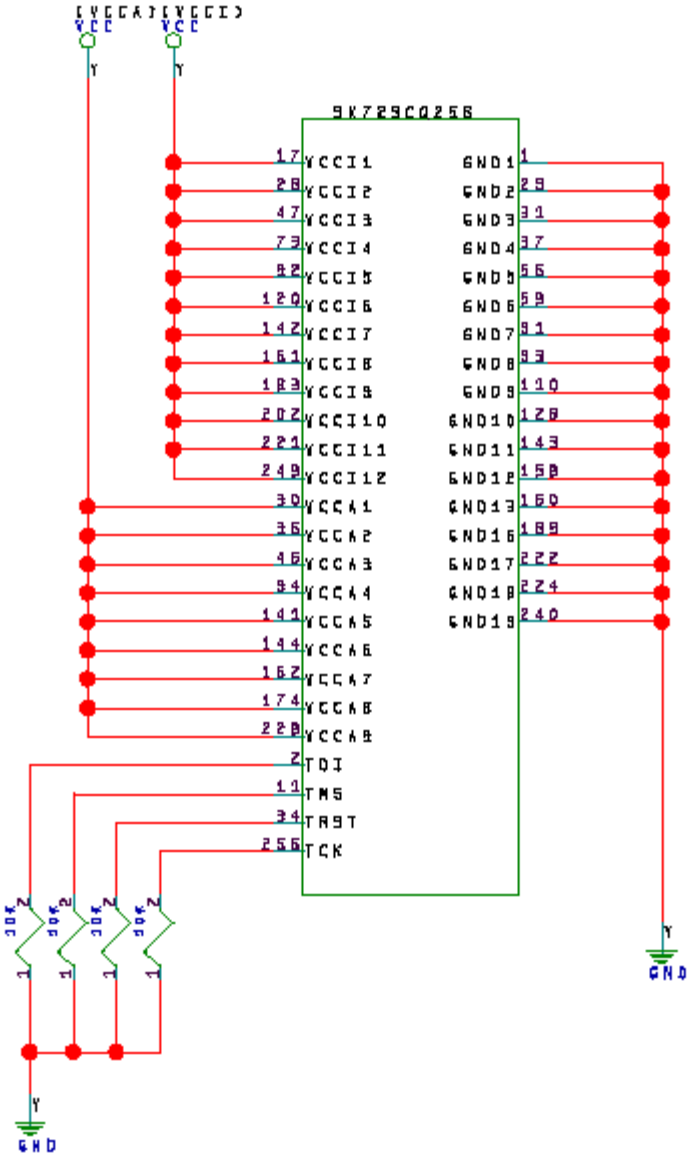
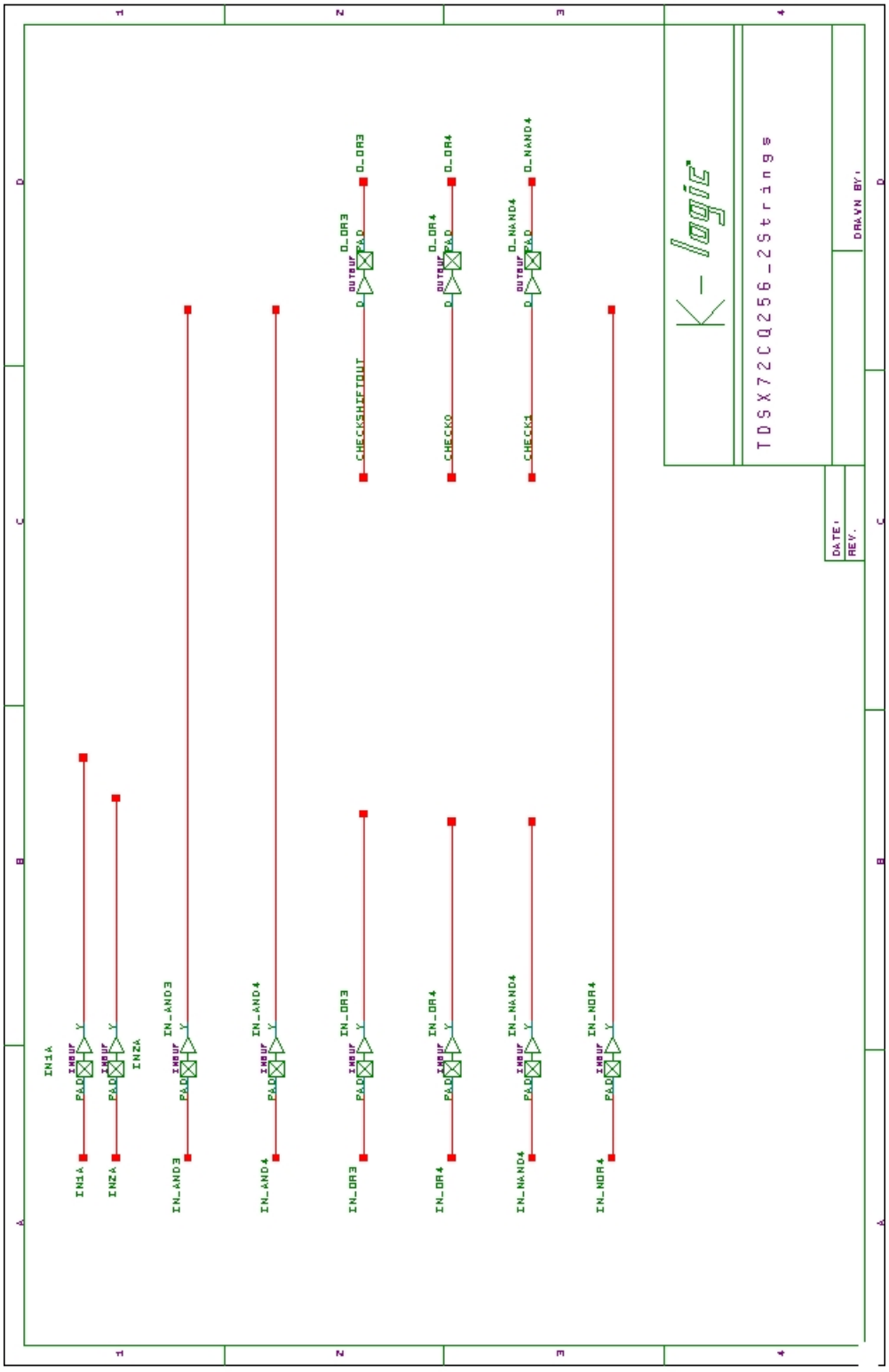
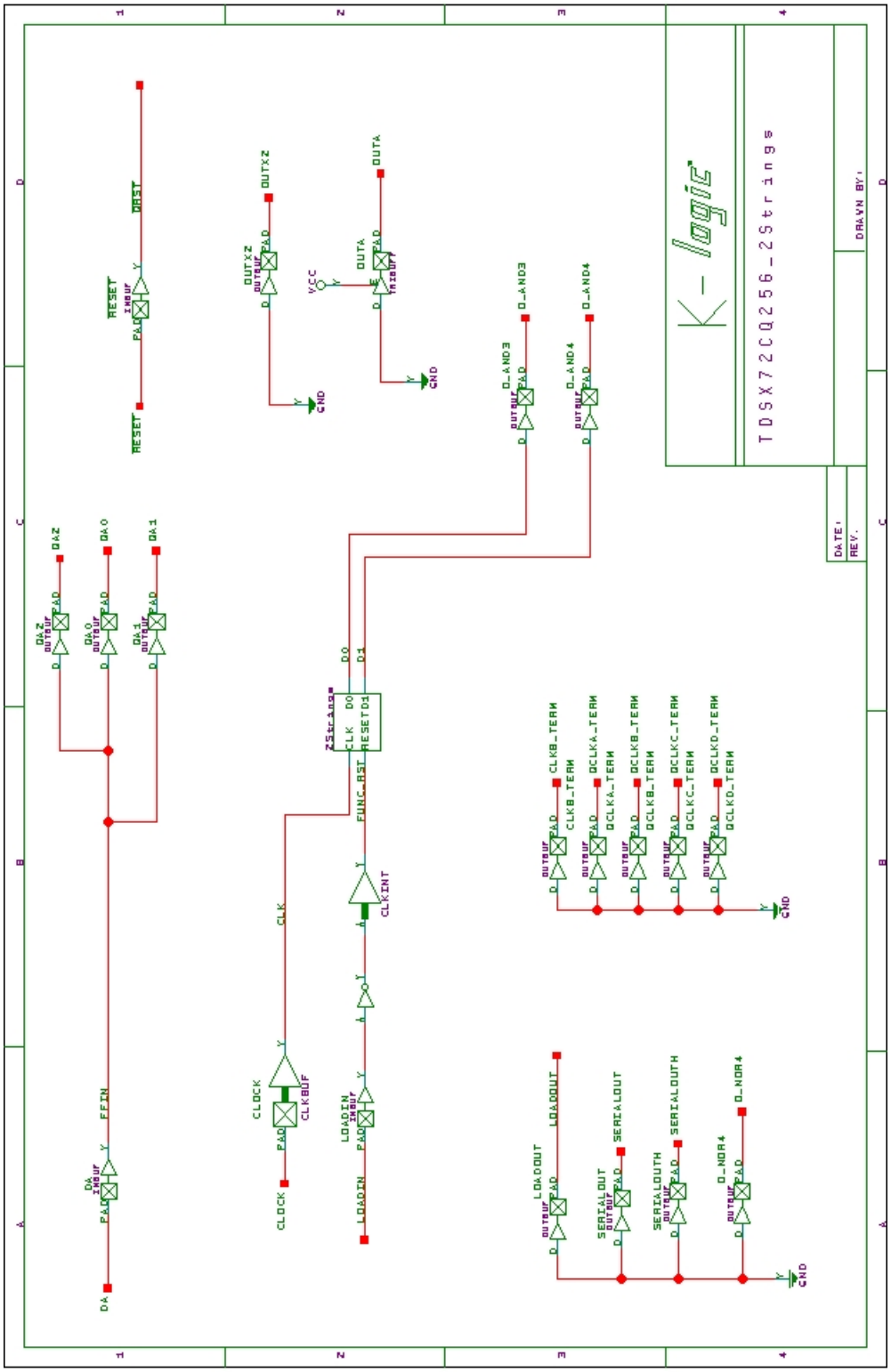
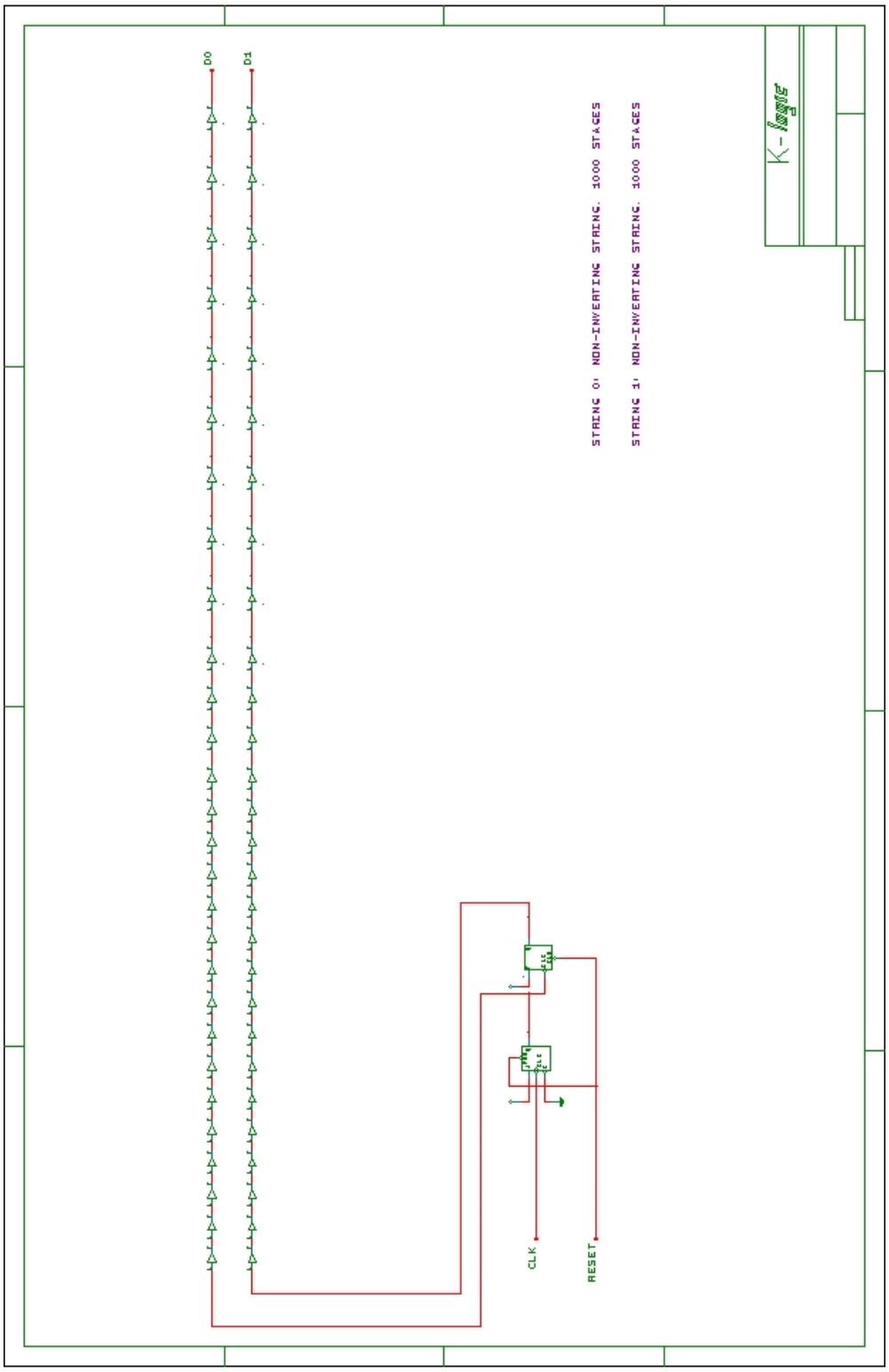


Figure A2 Power Supply, Ground, and Special Pins Bias During Irradiation

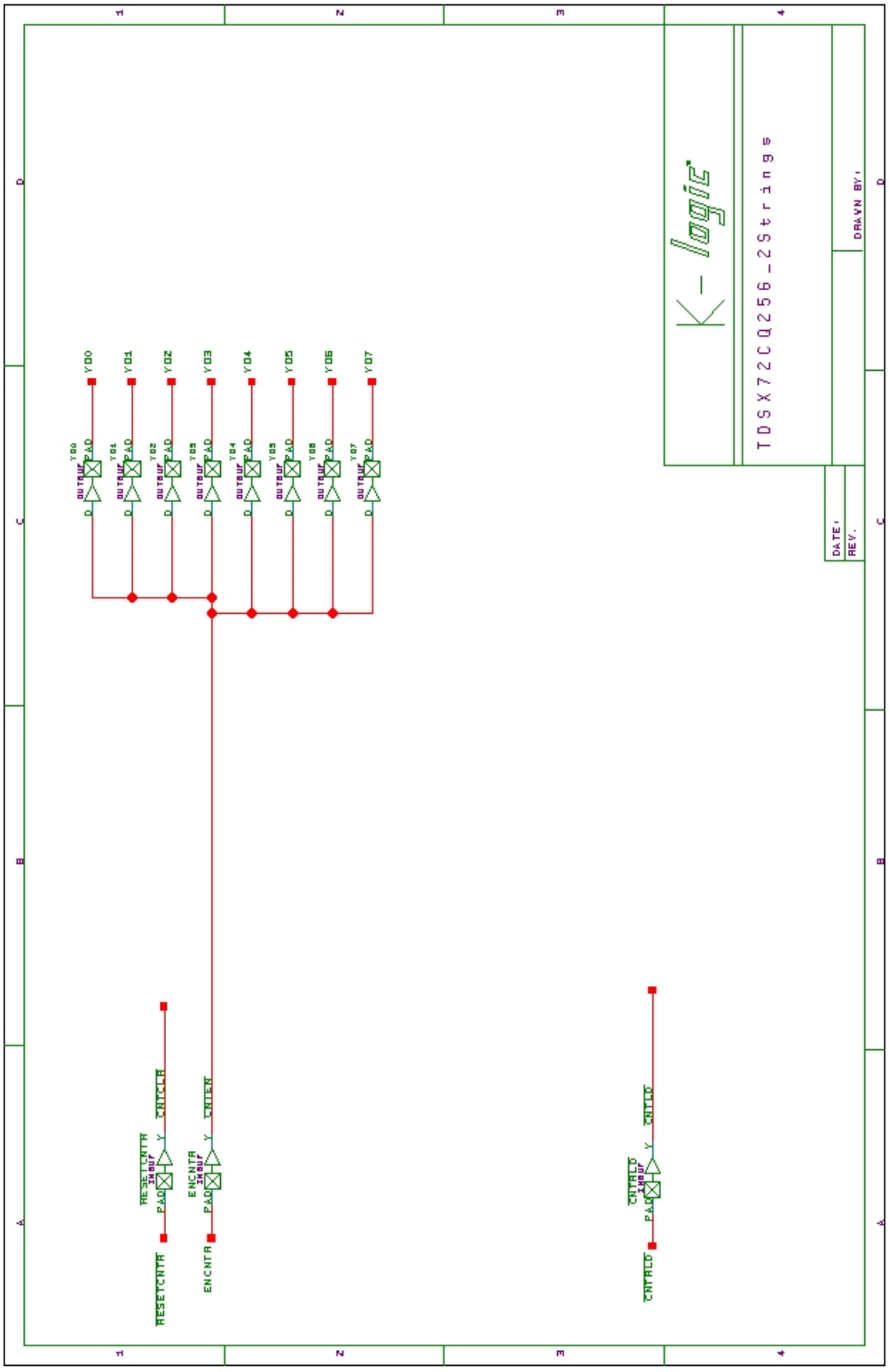
Appendix B: DUT Design Schematics

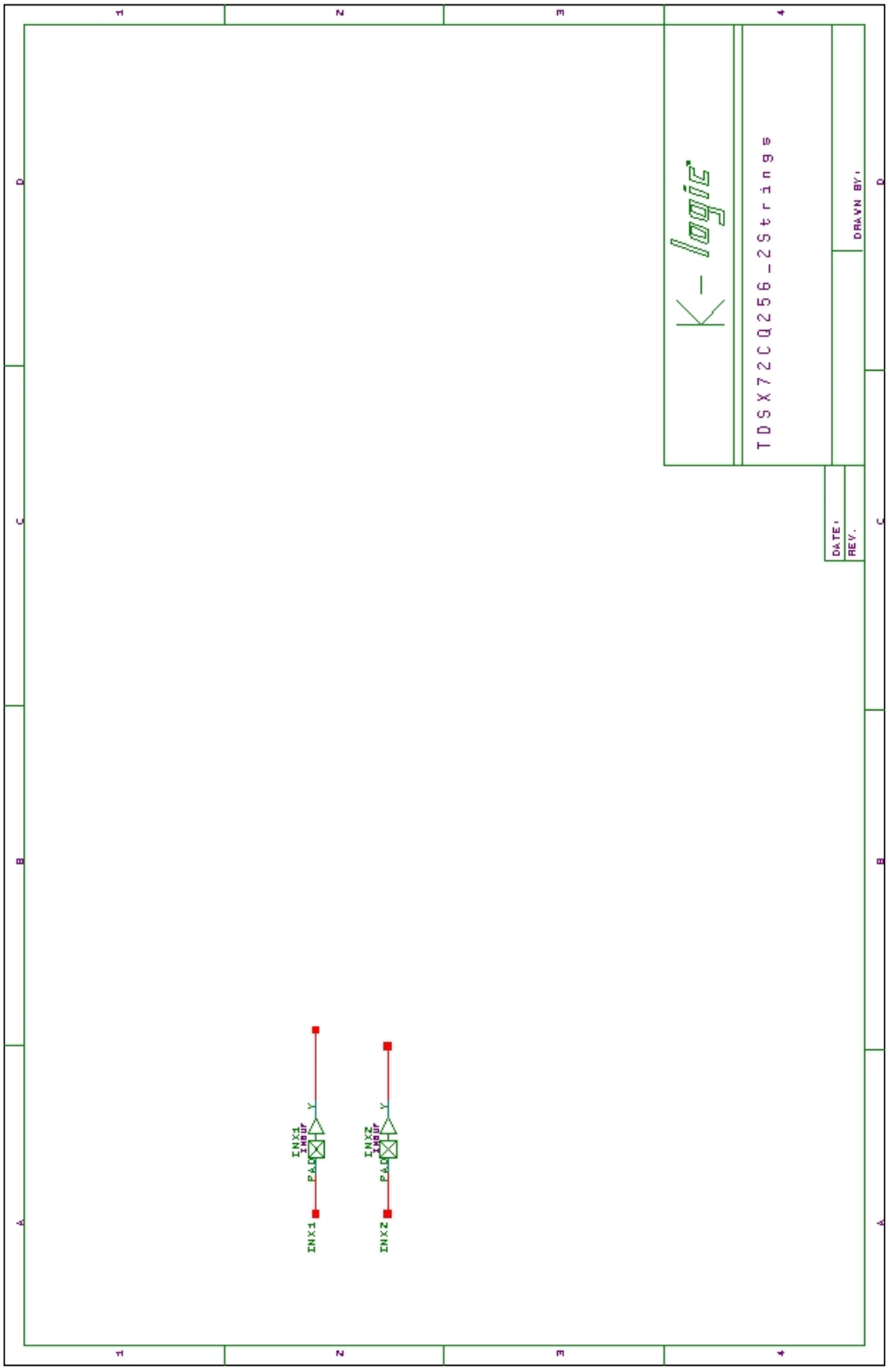


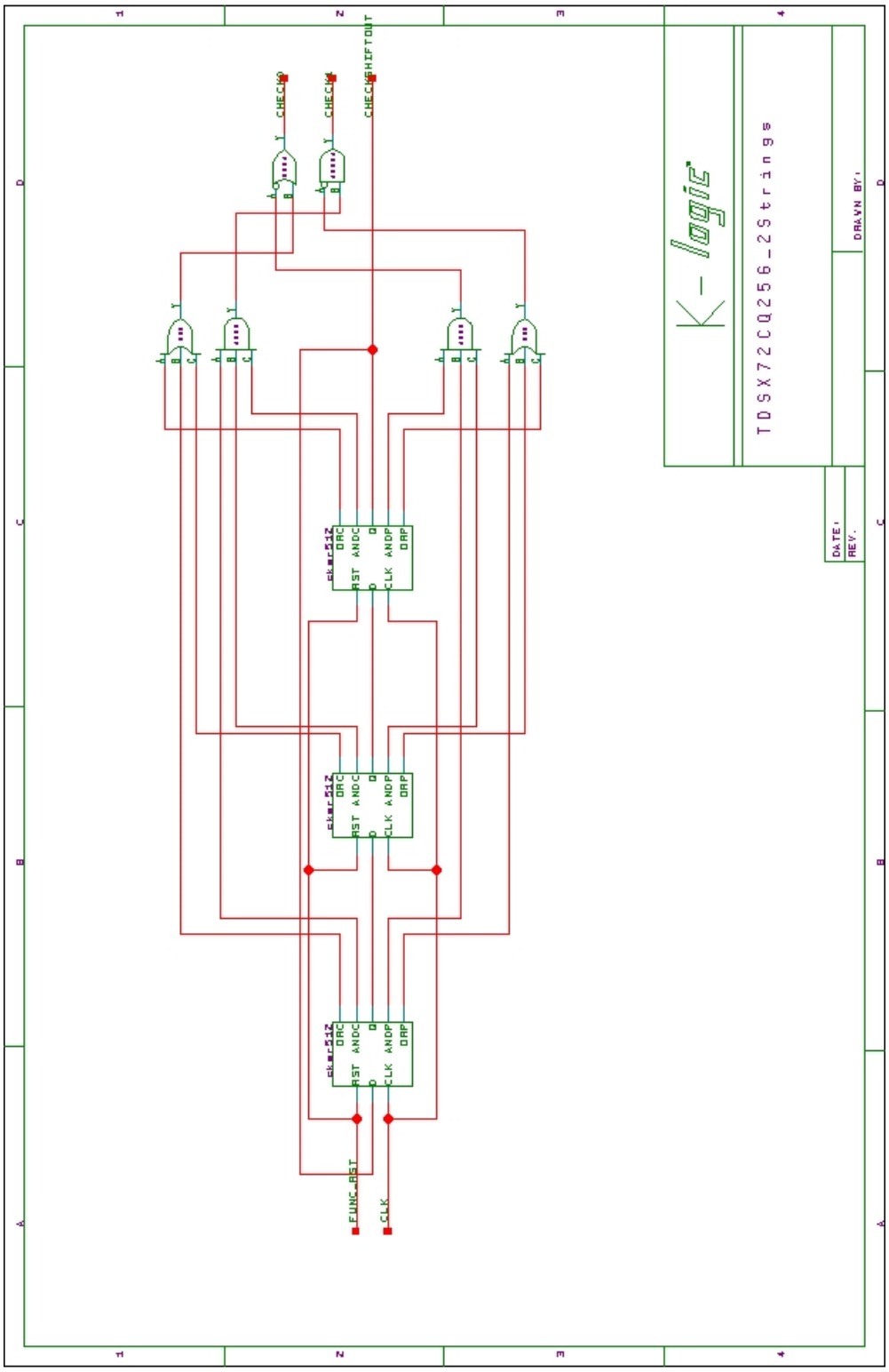

TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
RESET
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
PAD
INBUF
OUTBUF

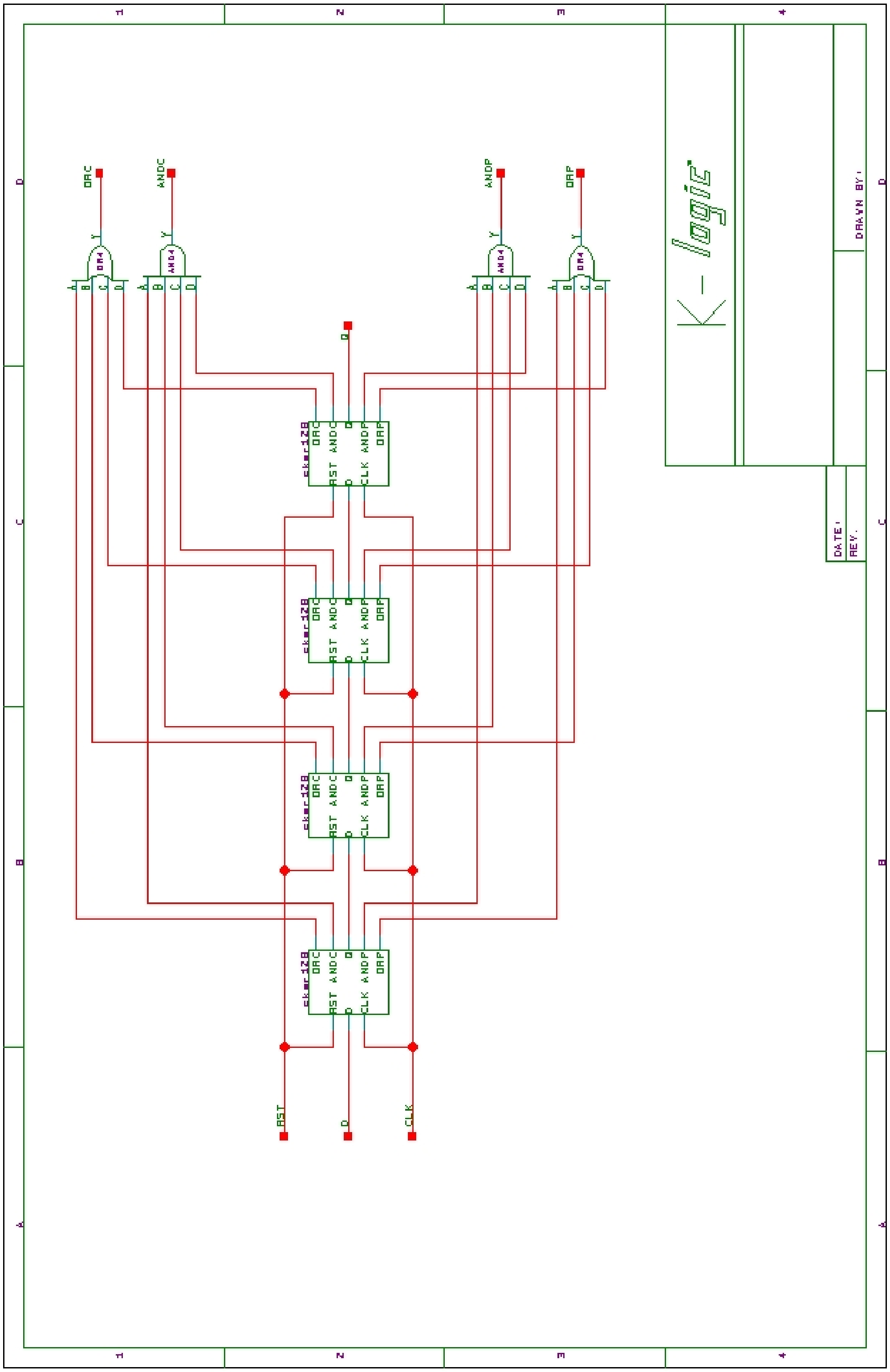

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Logic
CLK
RESET

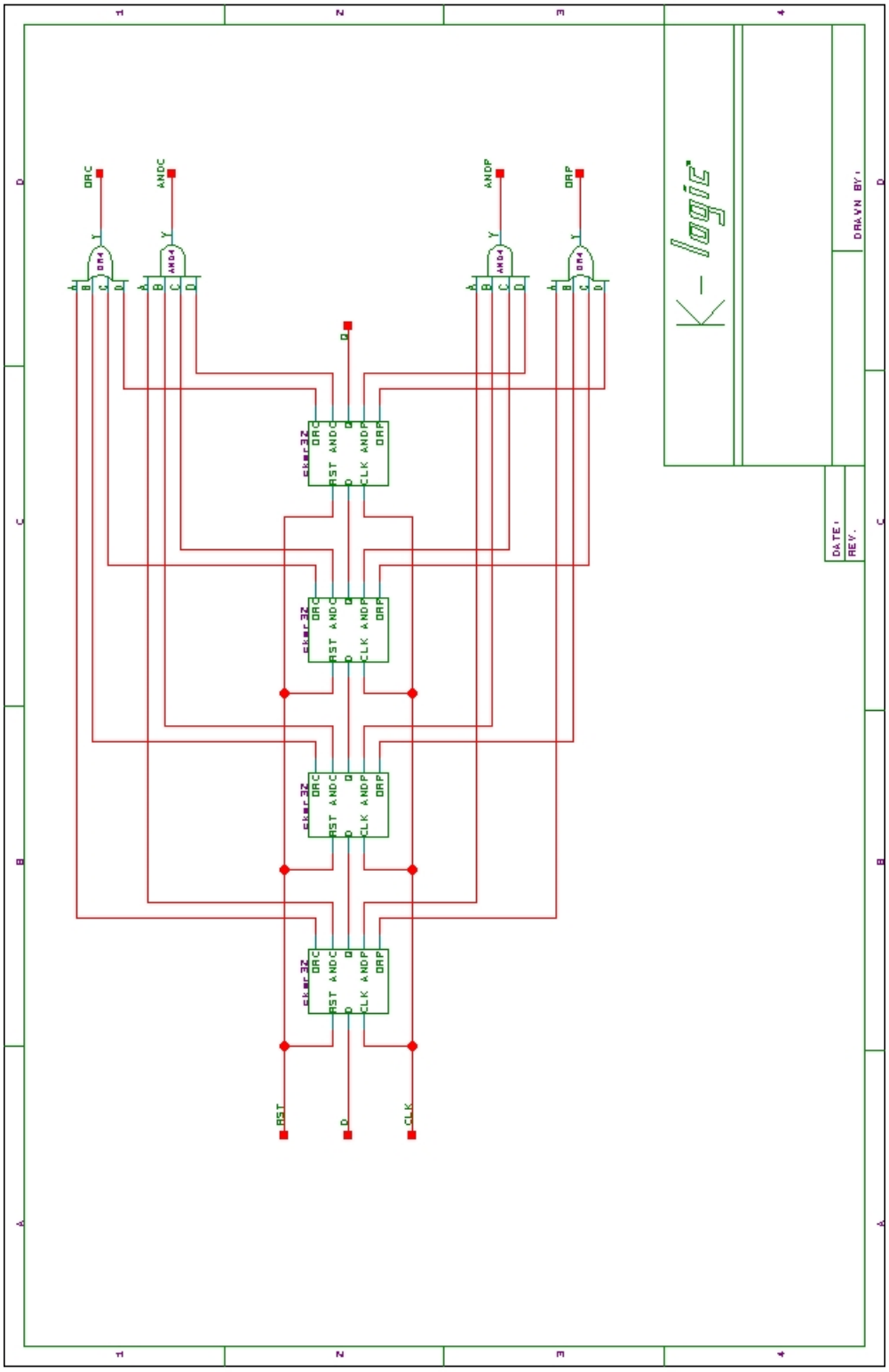

K- logic
T54CT35XCQ\BUF50NINV
DRAWN BY: RBK
DATE:
REV.
PRESERVE

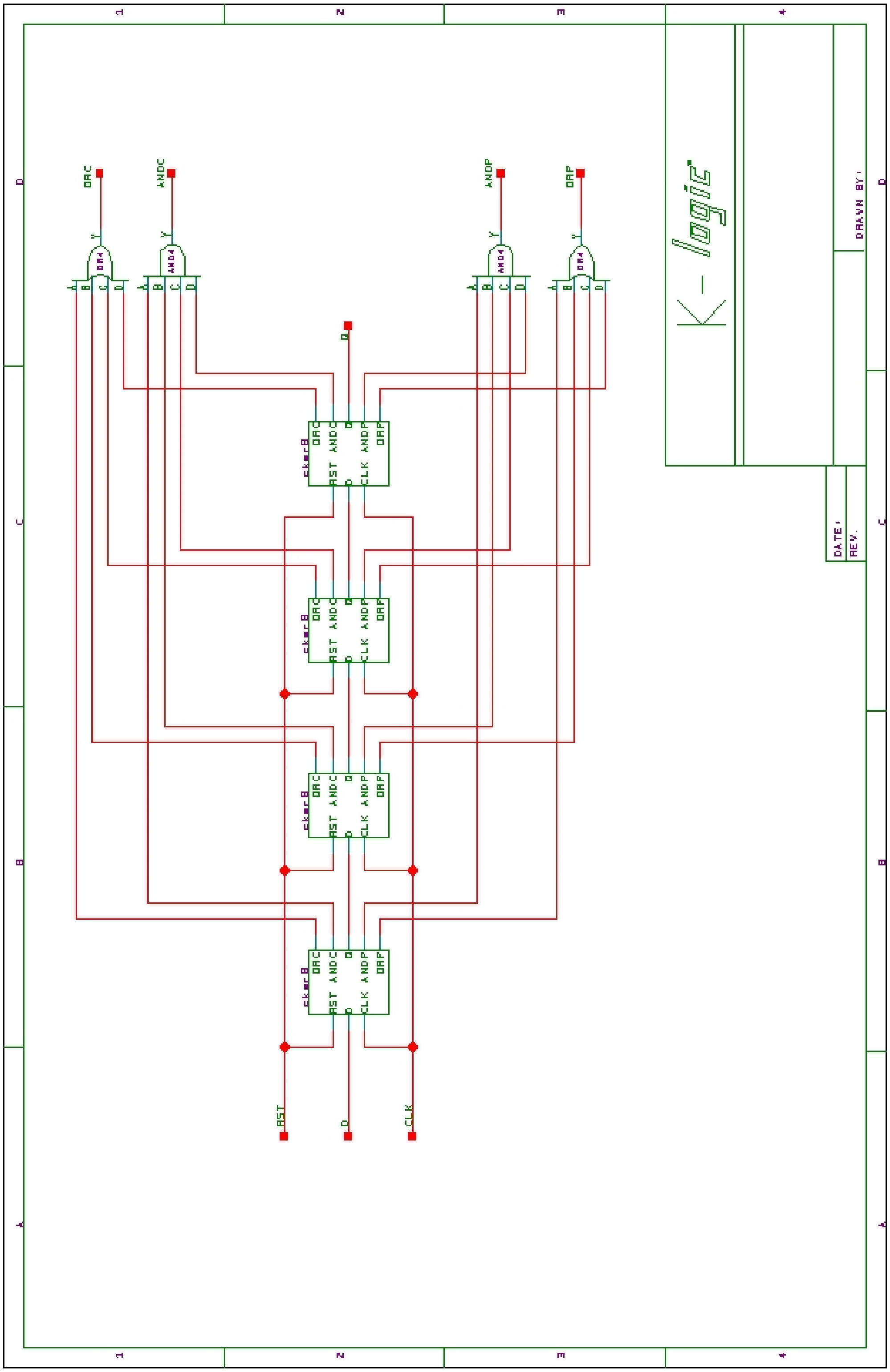

K-logic
TDSX72CQ256-25strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRCLR
CNTEN
CNTRCLD

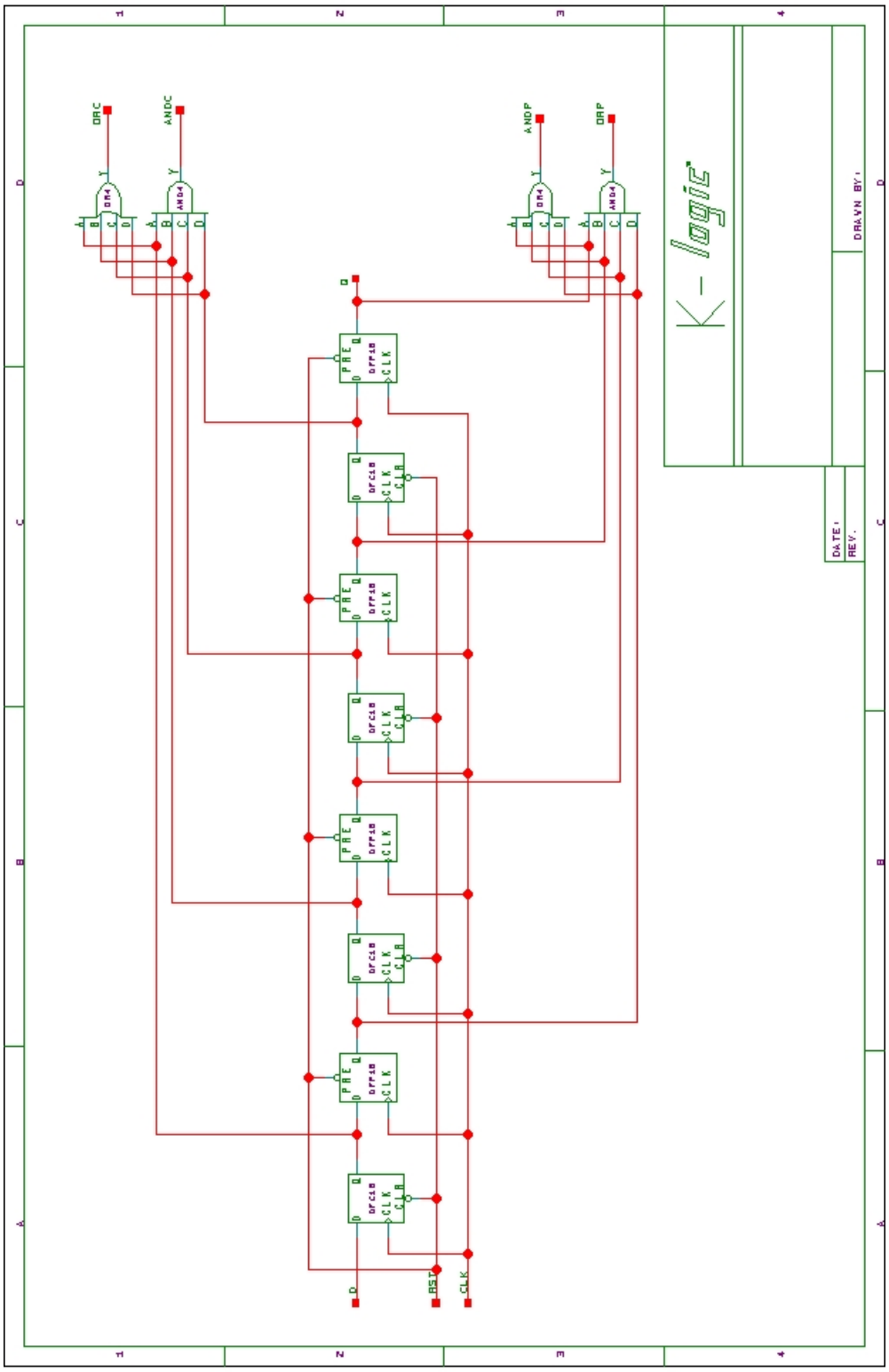

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
1
2
3
4
A
B
C
D
INX1
INX2

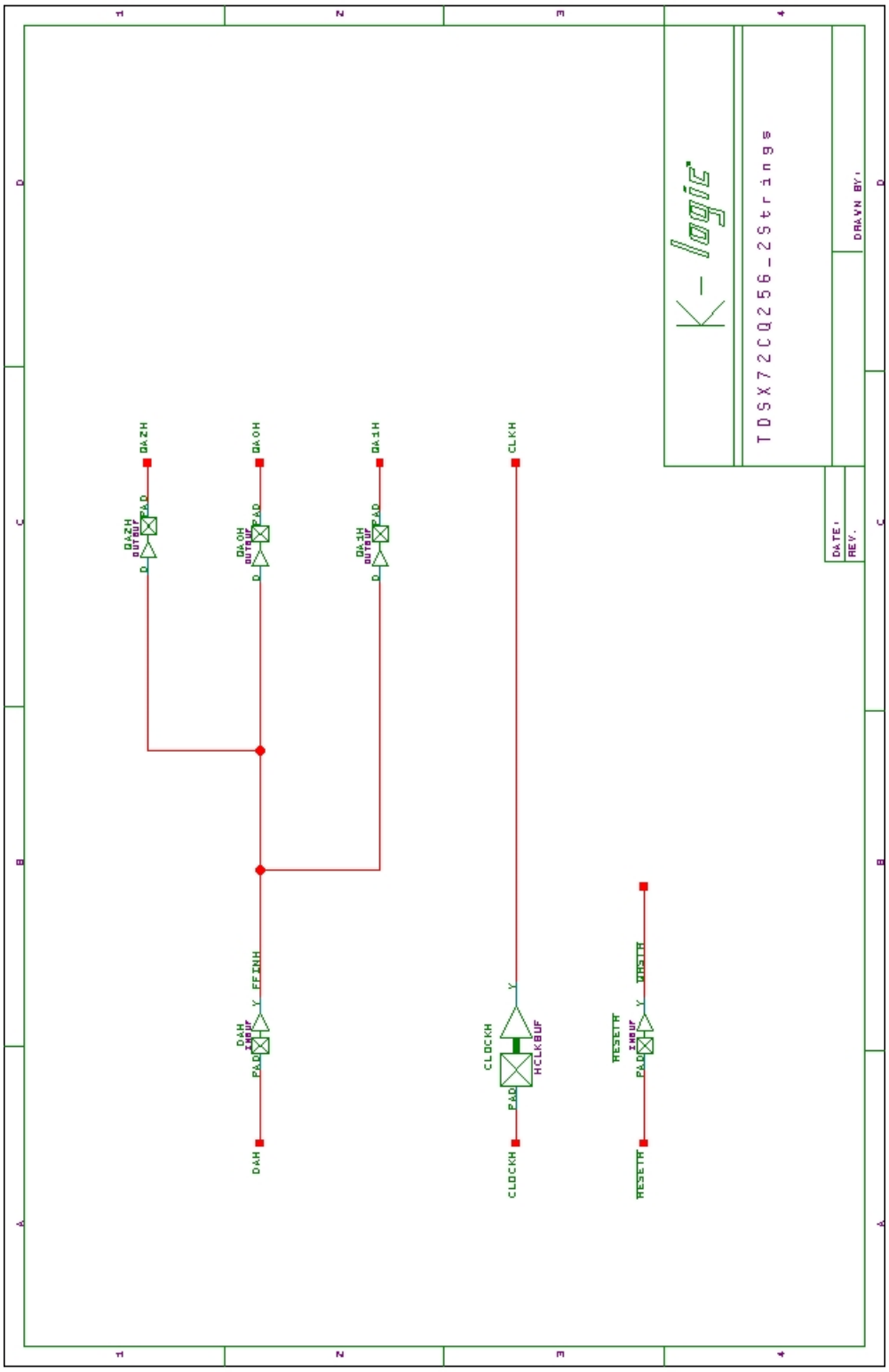

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

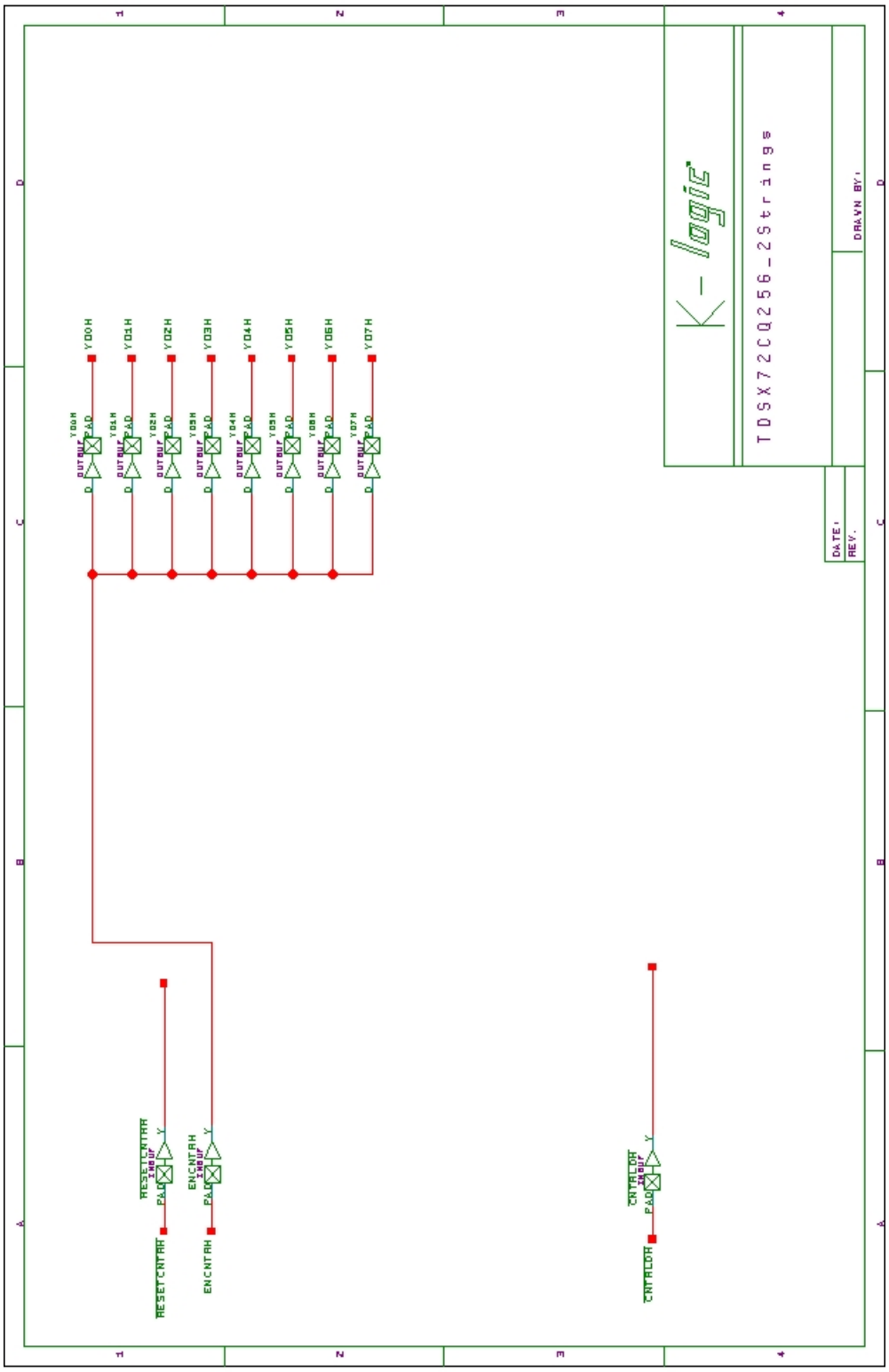

ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
K – logic
DRAWN BY:
DATE:
REV.

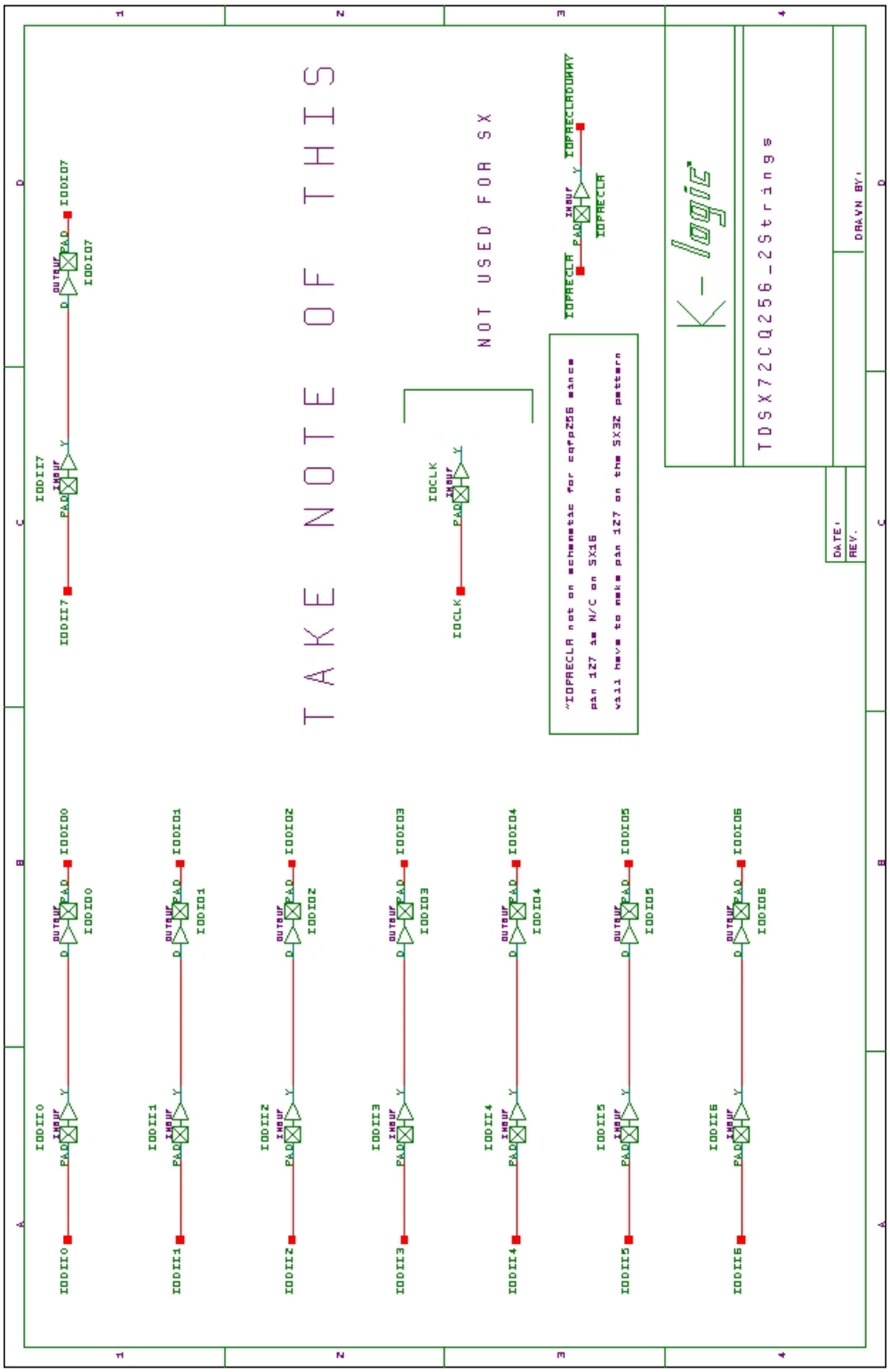

DRC
ANDC
ANDP
DRP
AND4
AND4
AND4
DFN4
K-logic
DRAWN BY:
DATE:
REV.
Fkmr32
DRC
ANDC
RST
D
ANDP
DRP
CLK
RST
D
CLK

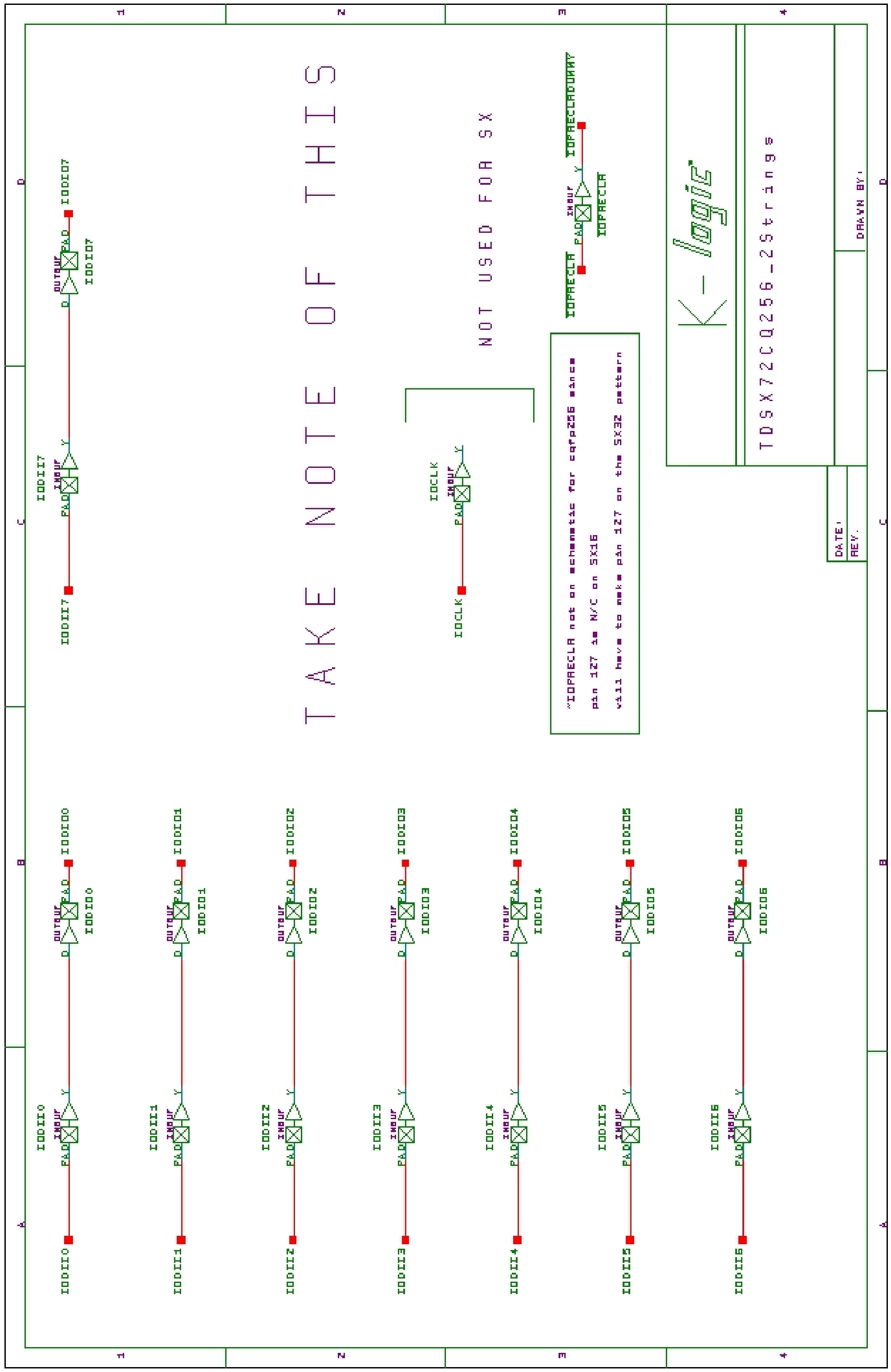

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DRAWN BY:
DATE:
REV.

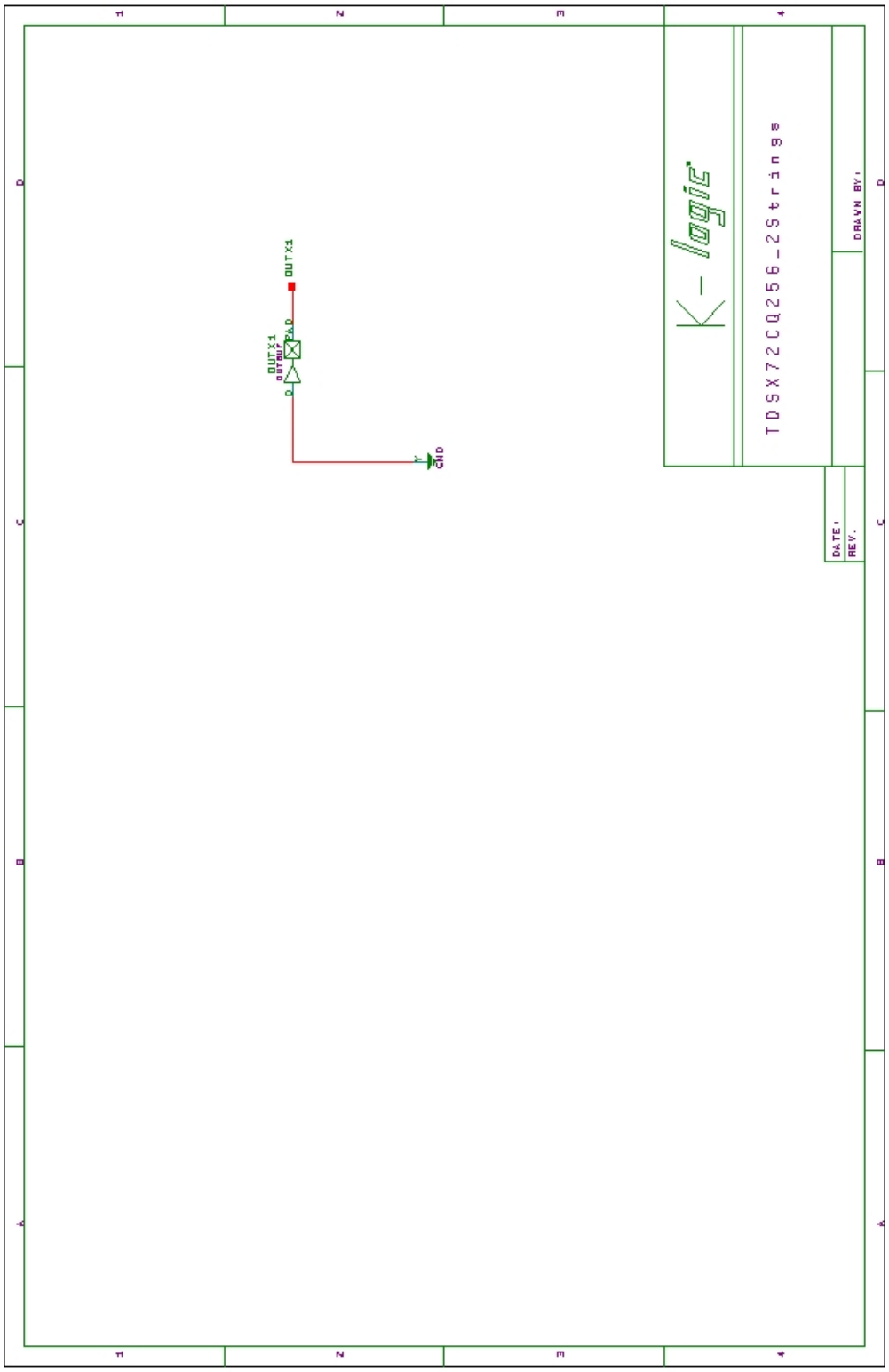

ORC
ANDC
ANDF
ORF
Q
D
RST
CLK
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DAH
RESETH
CLOCKH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
"IOPRECLR not on schematic for csfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
IOCLK
IOOII7
IOOIO7
IOOII0
IOOIO0
IOOII1
IOOIO1
IOOII2
IOOIO2
IOOII3
IOOIO3
IOOII4
IOOIO4
IOOII5
IOOIO5
IOOII6
IOOIO6


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


OUTX1
OUTX1
PAD
OUTPUT
GND
logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

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