Total Ionizing Dose Test Report

No. 14T-RTSX32SU-CQ256-D1RH41

March 9, 2014

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 100 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO_2)
5. Propagation Delay	Passed 100 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32S011104new
Die Lot Number	D1RH41
Quantity Tested	5
Serial Number	100 krad(SiO_2): 5388 60 krad(SiO_2): 5404, 5501 40 krad(SiO_2): 5608, 5629
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

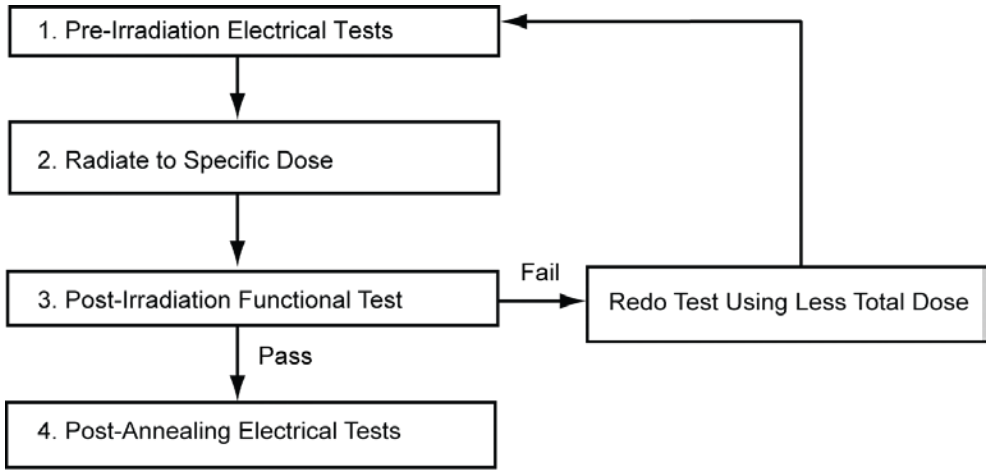

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX32SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32S011104,new) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
5388	100 krad	0.30	263	36	0.96	205	70
5501	60 krad	0.75	13	10	1.10	33	20
5504	60 krad	0.31	9	10	1.10	25	10
5608	40 krad	0.31	2	1	0.97	4	5
5629	40 krad	0.31	2	1	0.97	3	4

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test, is defined as the highest ICCA/ICCI in the RTSXSU spec sheet of 25 mA.

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT.

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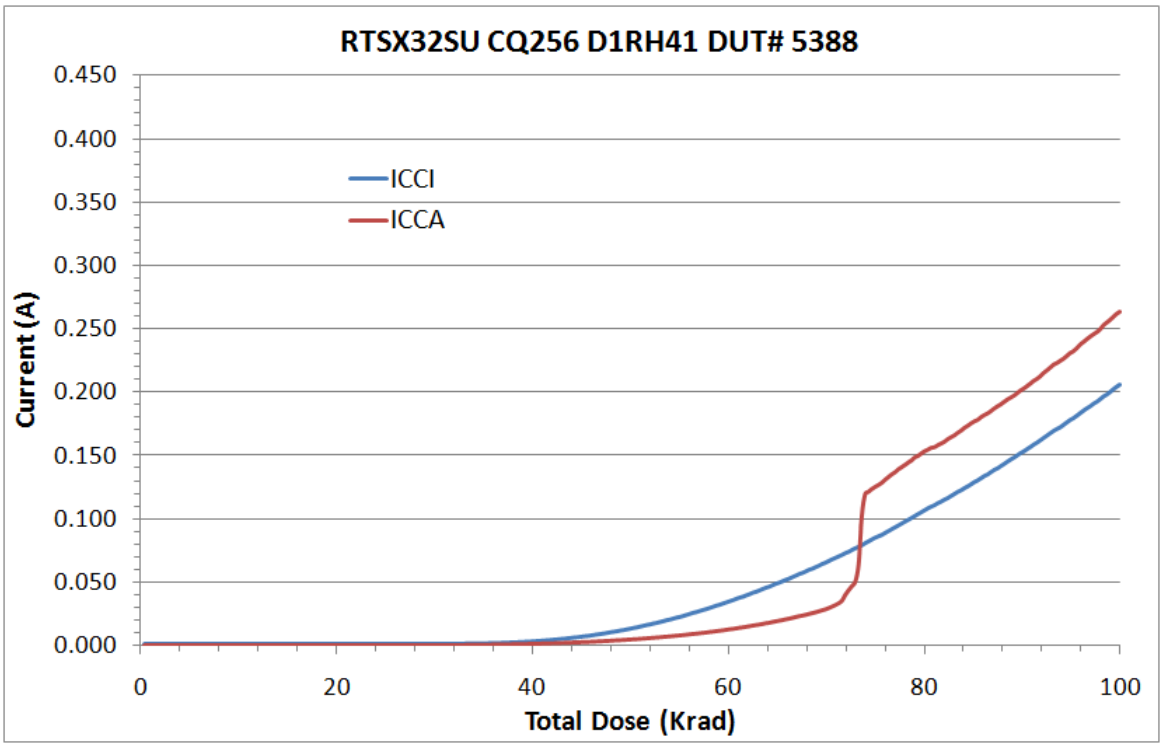


Figure 2 DUT 5388 Influx ICCA and ICCI

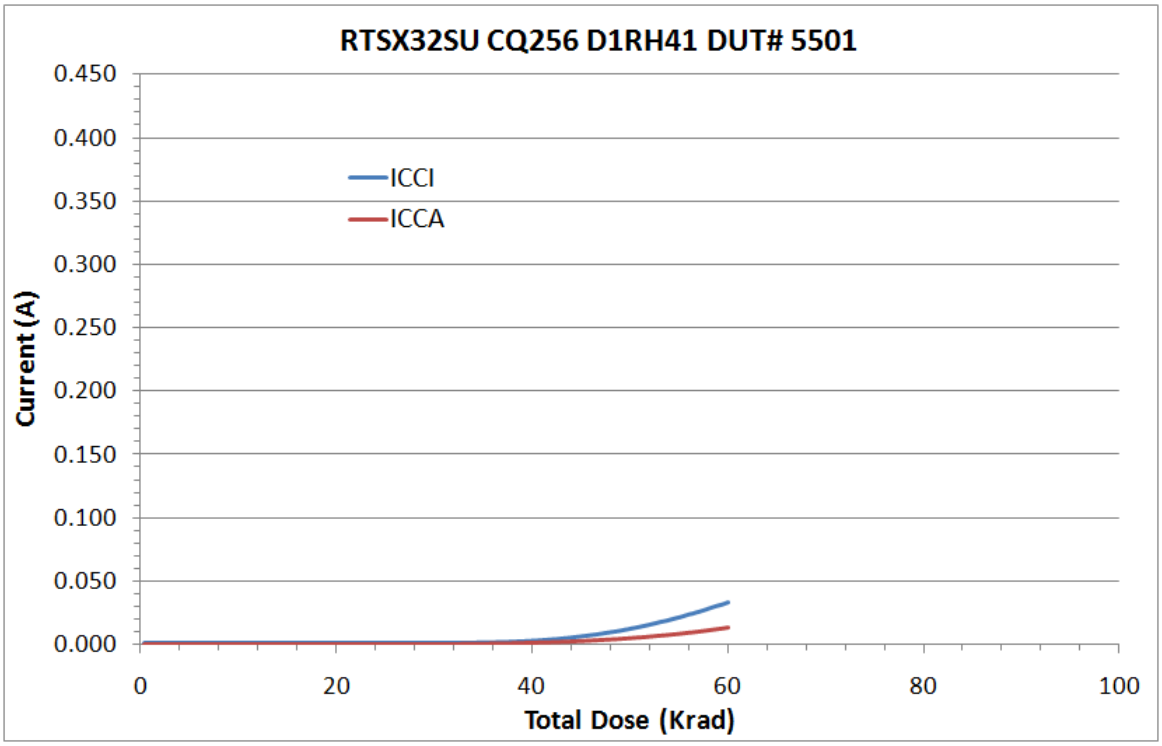


Figure 3 DUT 5501 Influx ICCA and ICCI

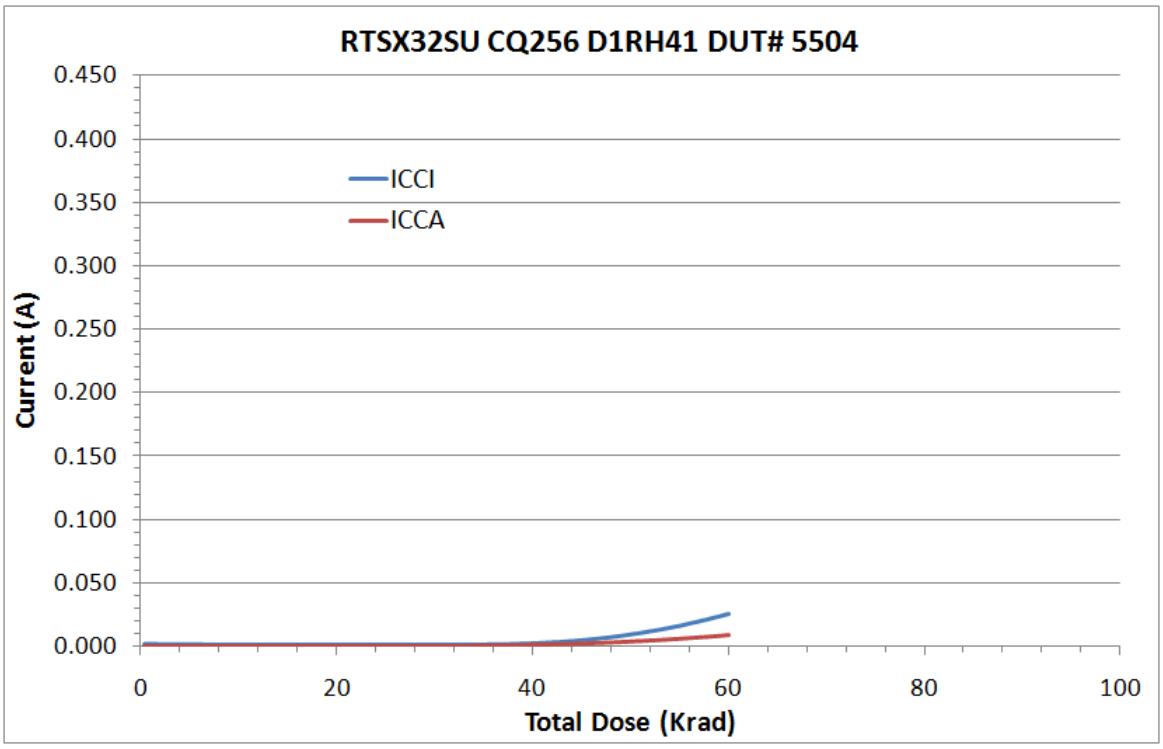


Figure 4 DUT 5504 Influx ICCA and ICCI

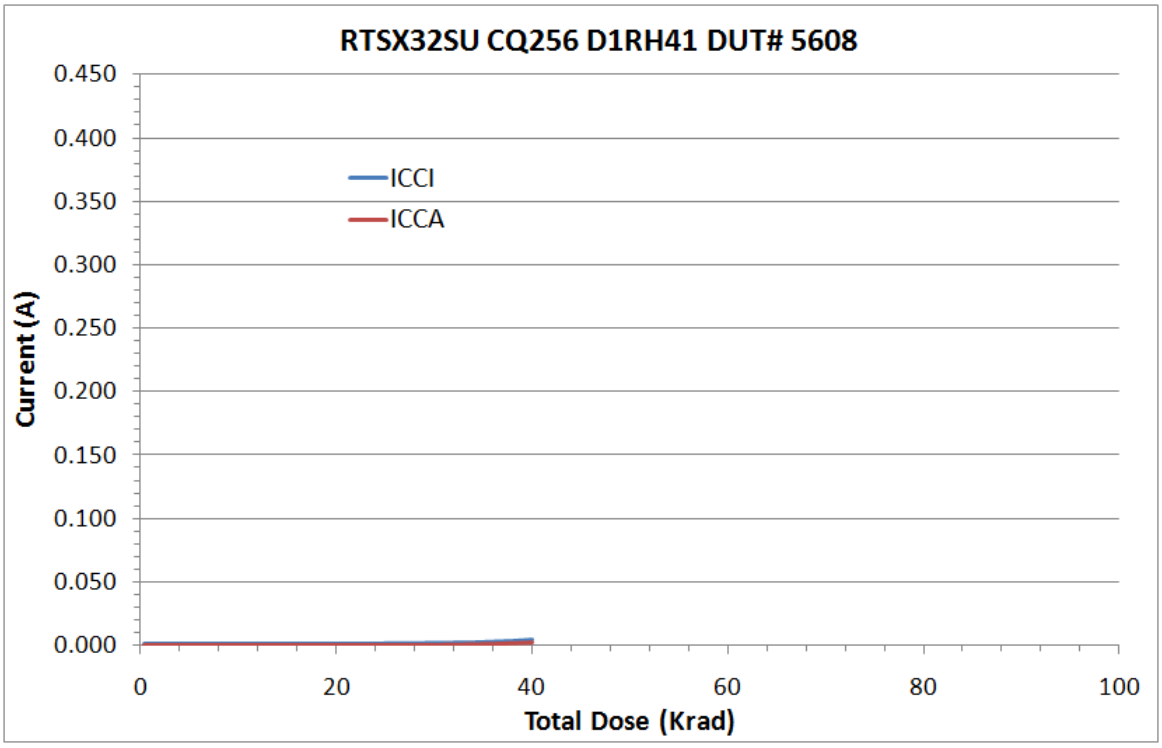


Figure 5 DUT 5608 Influx ICCA and ICCI

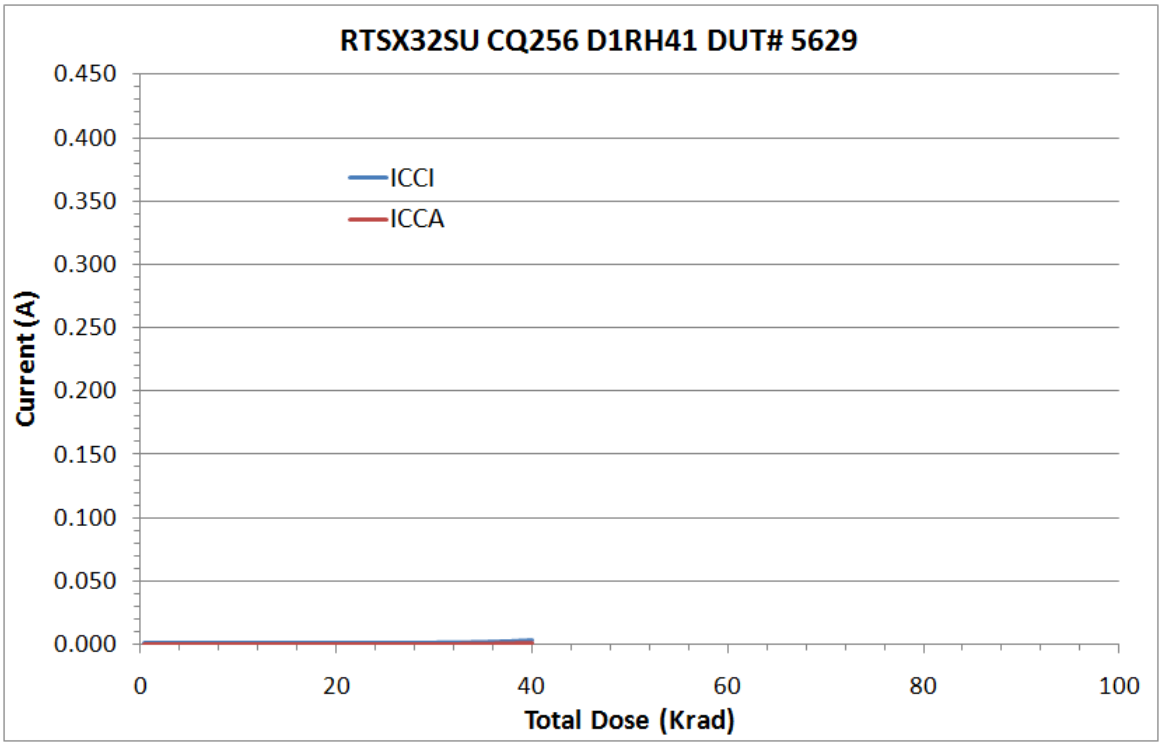


Figure 6 DUT 5629 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds. All data are within the specification limits. The post-annealing shift in every case is very small.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5388 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)	
DA/QA0	1415	1345	1415	1340
DAH/QA0H	1445	1375	1445	1435
ENCNTRH/YO0H	1460	1410	1460	1340
IDII0/IDIO0	1475	1360	1475	1335
IDII1/IDIO1	1285	1295	1285	1425
IDII2/IDIO2	1205	1185	1205	1450
IDII3/IDIO3	1450	1400	1450	1420
IDII4/IDIO4	1085	1025	1085	1585
IDII5/IDIO5	1360	1295	1360	1330
IDII6/IDIO6	1435	1375	1435	1310
IDII7/IDIO7	1380	1415	1380	1365

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5501 (60 krad)				5504 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1420	1345	1420	1320	1445	1365	1445	1535
DAH/QA0H	1370	1340	1370	1420	1375	1305	1375	1430
ENCNTRH/YO0H	1465	1385	1465	1340	1480	1385	1480	1340
IDII0/IDIO0	1455	1370	1455	1320	1460	1395	1460	1330
IDII1/IDIO1	1430	1360	1430	1425	1425	1240	1425	1425
IDII2/IDIO2	1200	1145	1200	1455	1210	1140	1210	1460
IDII3/IDIO3	1445	1385	1445	1420	1455	1390	1455	1420
IDII4/IDIO4	1085	1035	1085	1610	1095	1035	1095	1605
IDII5/IDIO5	1380	1295	1380	1345	1425	1305	1425	1335
IDII6/IDIO6	1425	1345	1425	1315	1425	1375	1425	1320
IDII7/IDIO7	1370	1410	1370	1315	1410	1410	1410	1315

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5608 (40 krad)				5629 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1440	1420	1440	1380	1455	1360	1455	1325
DAH/QA0H	1435	1385	1435	1460	1455	1335	1455	1425
ENCNTRH/YO0H	1380	1445	1380	1920	1440	1375	1440	1320
IDII0/IDIO0	1435	1410	1435	1380	1430	1380	1430	1320
IDII1/IDIO1	1300	1290	1300	1490	1420	1355	1420	1420
IDII2/IDIO2	1215	1170	1215	1475	1215	1130	1215	1445
IDII3/IDIO3	1450	1440	1450	1365	1480	1385	1480	1415
IDII4/IDIO4	1075	1070	1075	1665	1105	1035	1105	1595
IDII5/IDIO5	1395	1345	1395	1395	1385	1285	1385	1330
IDII6/IDIO6	1425	1425	1425	1360	1485	1360	1485	1370
IDII7/IDIO7	1380	1355	1380	1425	1395	1405	1395	1310

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	5388 (100 krad)		5501 (60 krad)		5504 (60 krad)		5608 (40 krad)		5629 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	10	10	10	10	10	10	10	10	10
12 mA	116	119	117	118	114	117	114	117	114	114
20 mA	193	197	194	196	190	194	190	194	190	190
50 mA	484	494	486	494	478	487	479	486	478	476
100 mA	992	1015	996	1015	979	1002	981	1000	980	975

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	5388 (100 krad)		5501 (60 krad)		5504 (60 krad)		5608 (40 krad)		5629 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4978	4614	4978	4613	4978	4614	4978	4614	4977	4977
8 mA	4849	4479	4847	4476	4850	4480	4852	4483	4848	4846
20 mA	4623	4240	4618	4235	4625	4243	4632	4253	4622	4619
50 mA	4014	3584	4000	3570	4019	3592	4042	3624	4010	4005
100 mA	2657	1851	2606	1764	2667	1883	2765	2088	2634	2611

F. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (ns)	Post-Anneal (ns)	Degradation (%)
5388	100 krad	25.14	24.19	-3.76%
5501	60 krad	24.99	23.78	-4.84%
5504	60 krad	24.64	23.44	-4.85%
5608	40 krad	25.59	23.85	-6.80%
5629	40 krad	24.97	23.68	-5.15%

G. Transition Characteristics

Figure 7a to Figure 16b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

Figure 7a DUT 5388 Pre-Irradiation Rising Edge

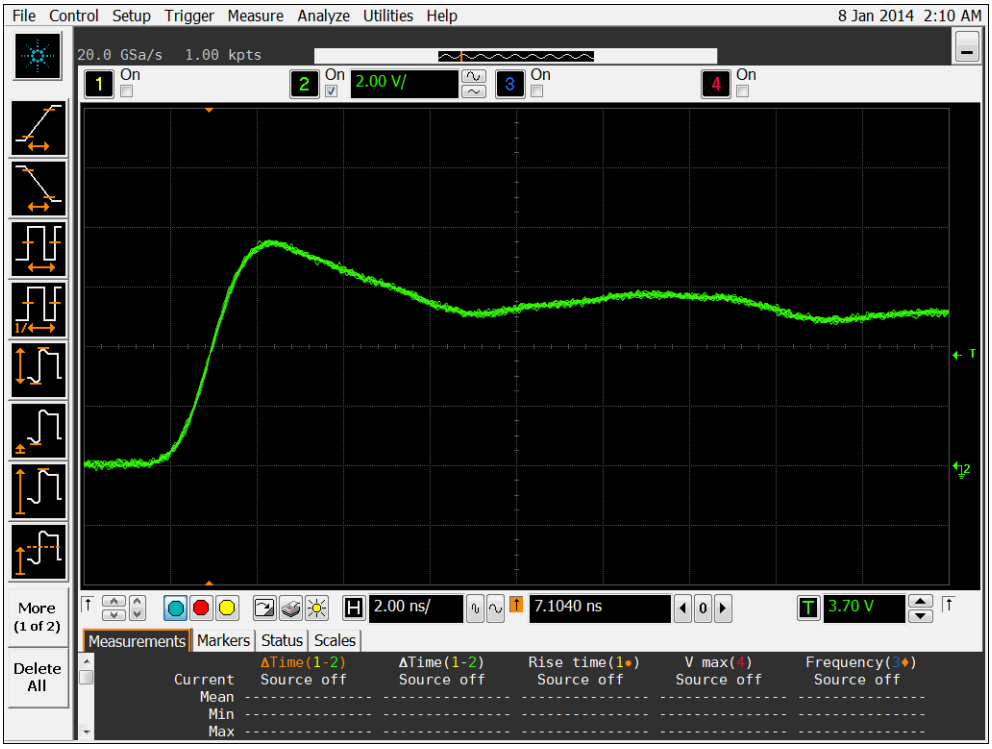


Figure 7b DUT 5388 Post-Annealing Rising Edge

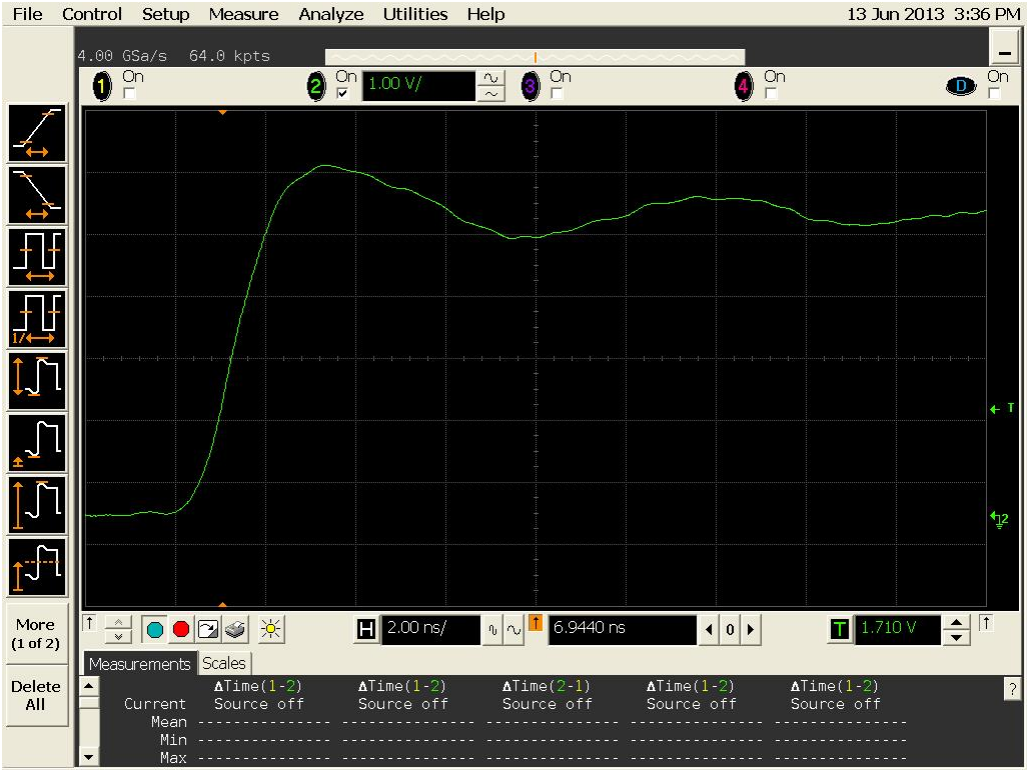


Figure 8a DUT 5501 Pre-Irradiation Rising Edge

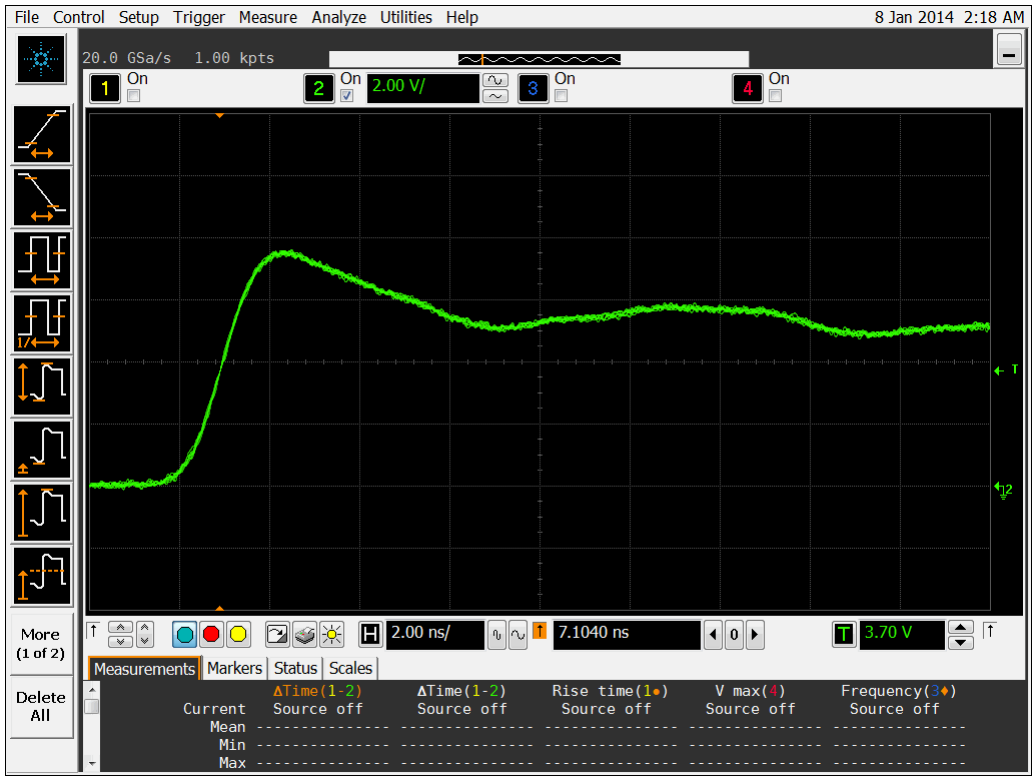


Figure 8b DUT 5501 Post-Annealing Rising Edge

Figure 9a DUT 5504 Pre-Radiation Rising Edge

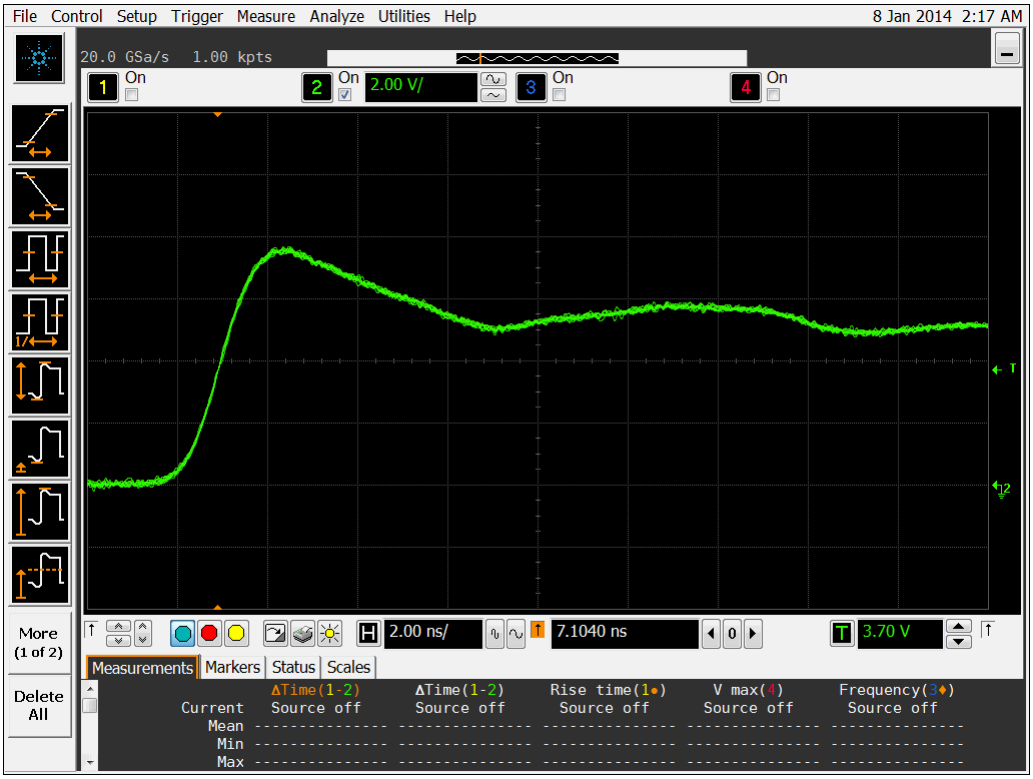


Figure 9b DUT 5504 Post-Annealing Rising Edge

Figure 10a DUT 5608 Pre-Irradiation Rising Edge

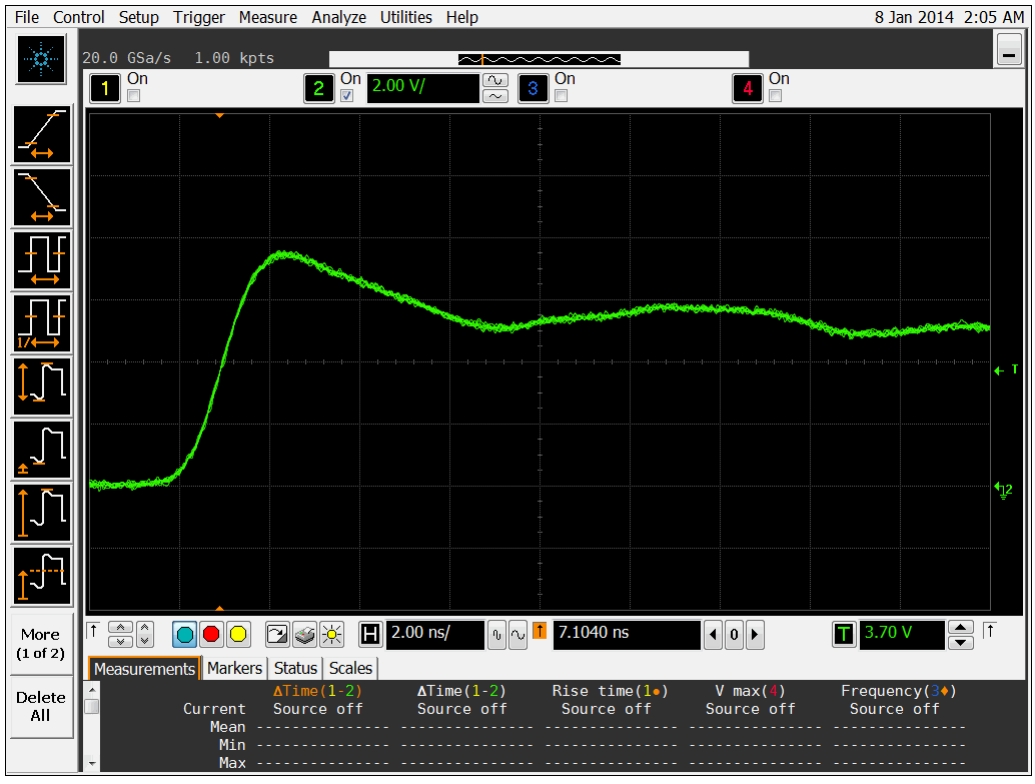


Figure 10b DUT 5608 Post-Annealing Rising Edge

Figure 11a DUT 5629 Pre-Irradiation Rising Edge

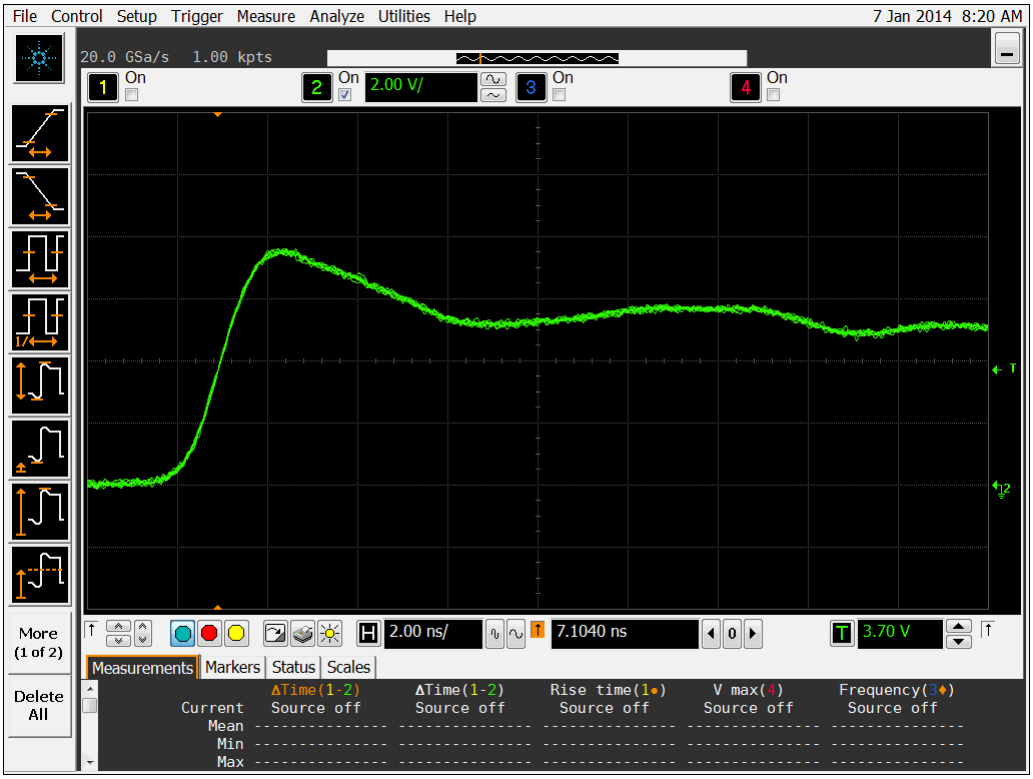


Figure 11b DUT 5629 Post-Annealing Rising Edge

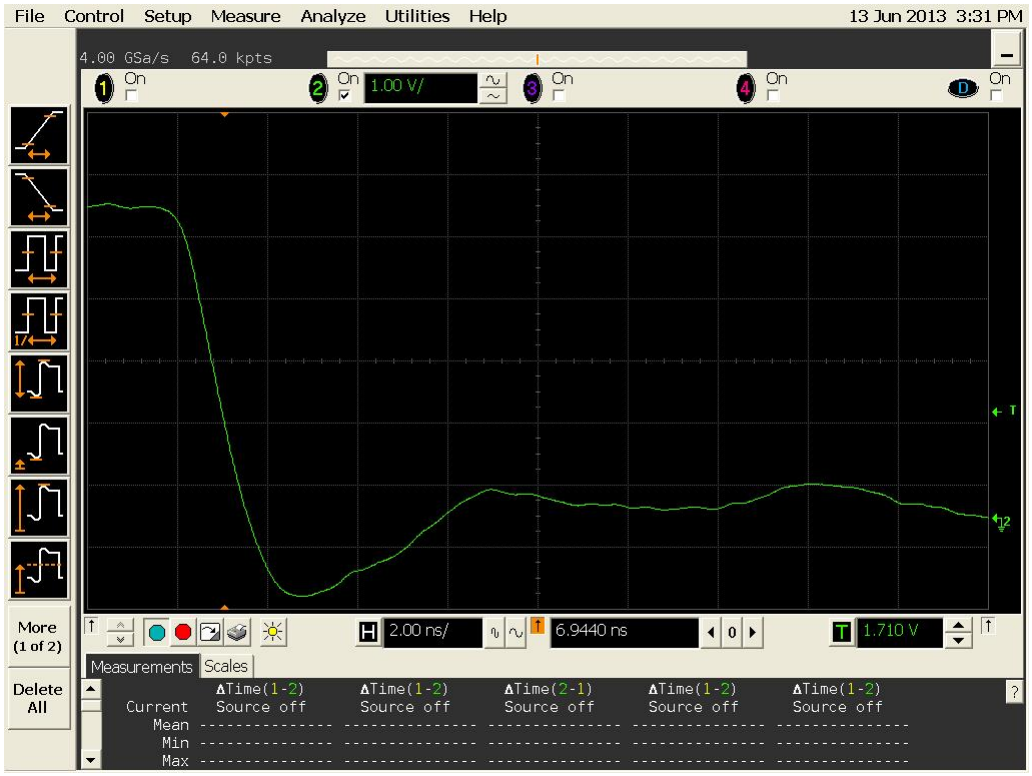


Figure 12a DUT 5388 Pre-Radiation Falling Edge

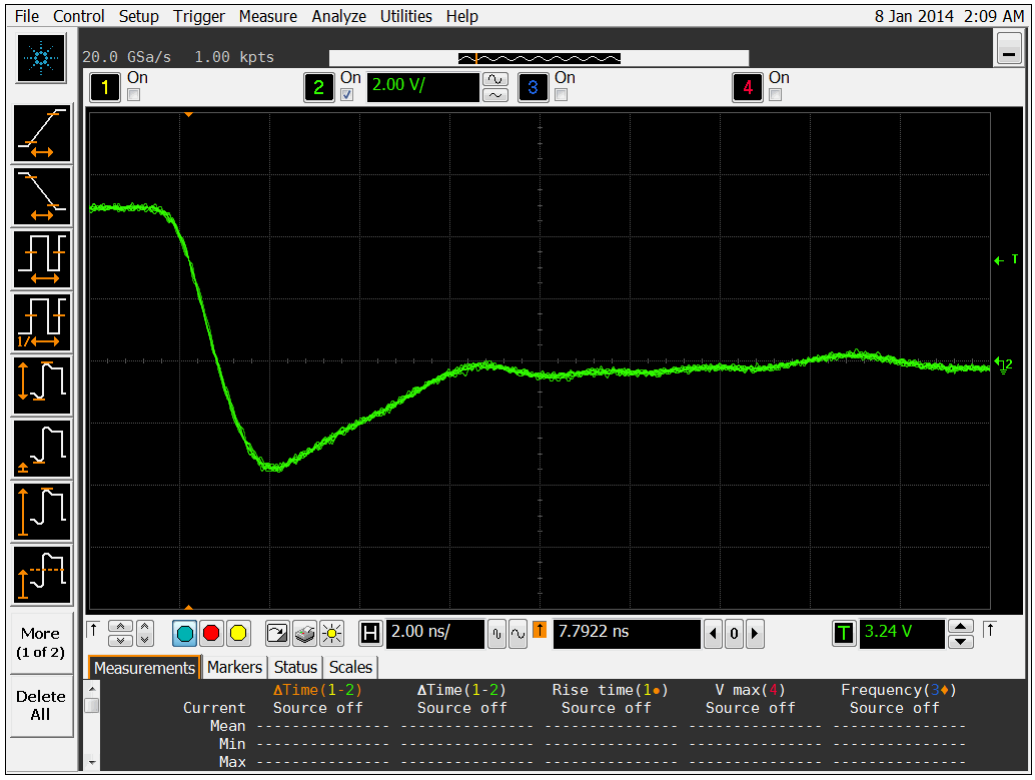


Figure 12b DUT 5388 Post-Annealing Falling Edge

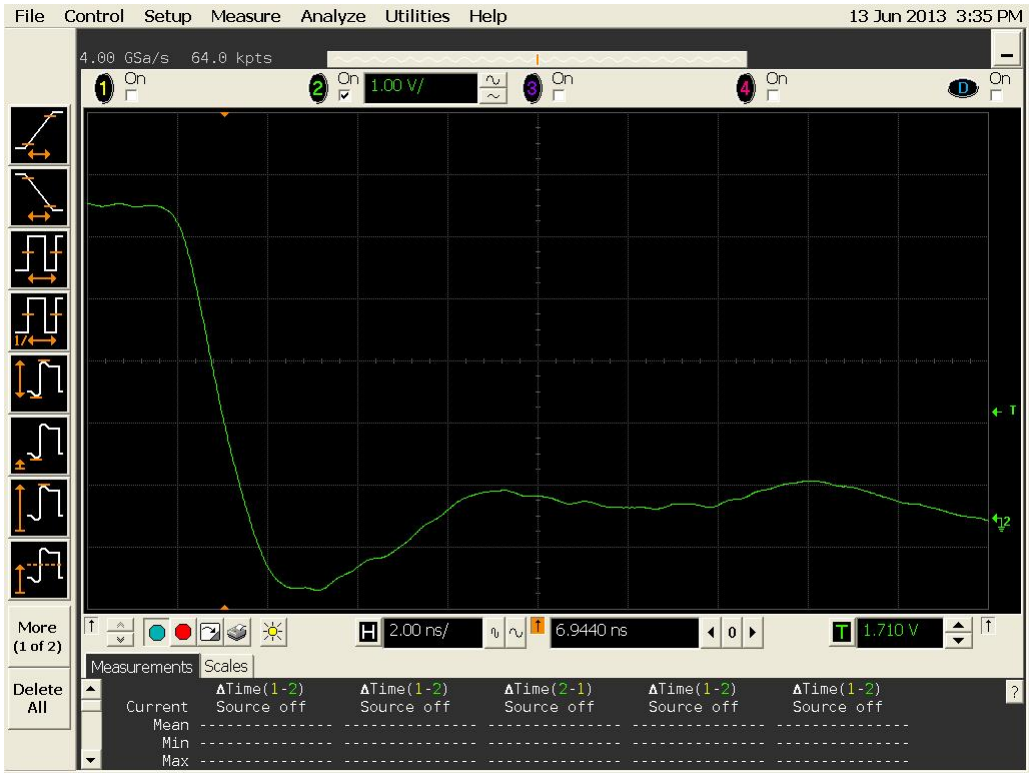


Figure 13a DUT 5501 Pre-Irradiation Falling Edge

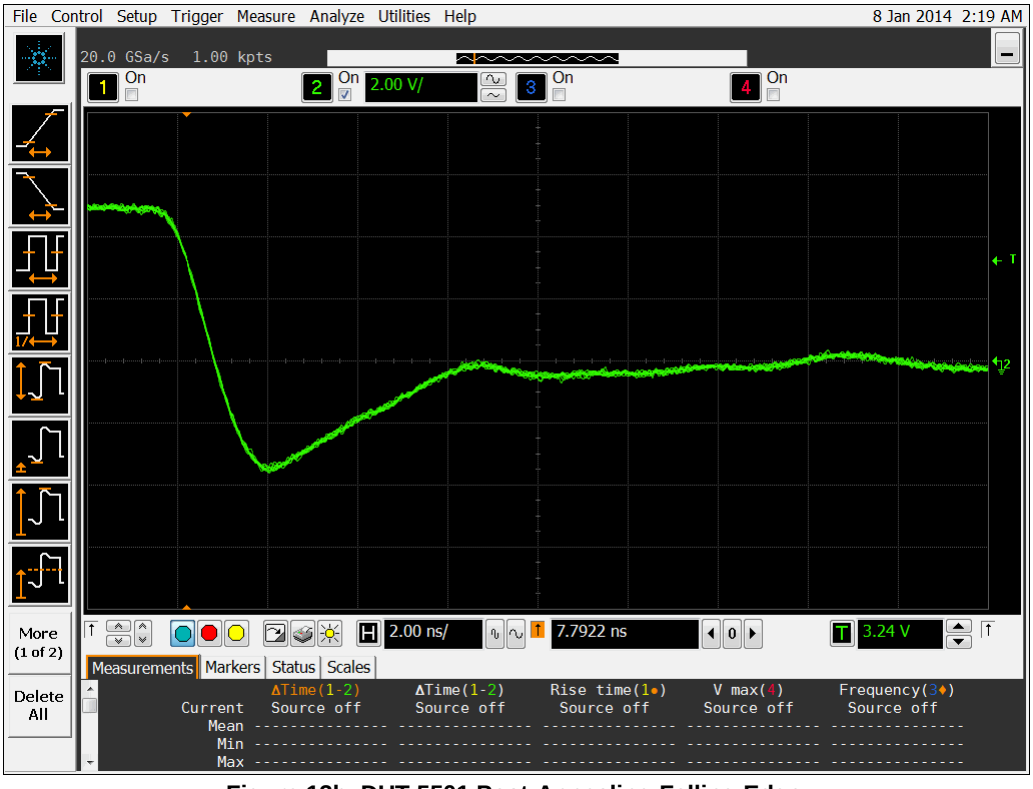


Figure 13b DUT 5501 Post-Annealing Falling Edge

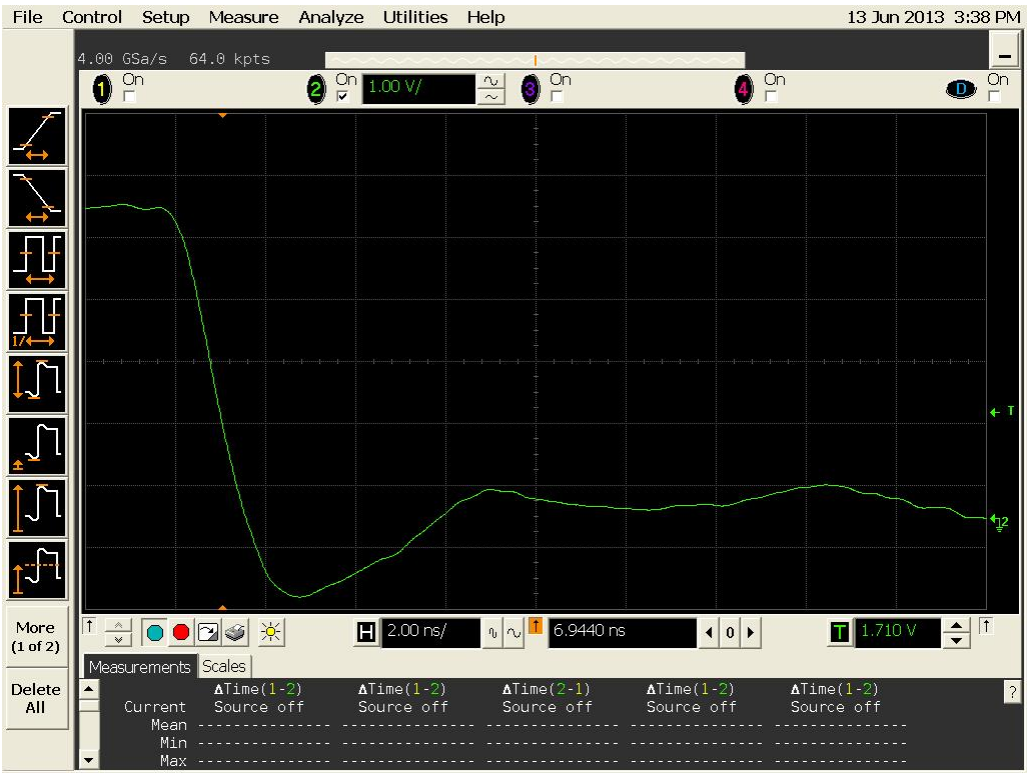


Figure 14a DUT 5504 Pre-Irradiation Falling Edge

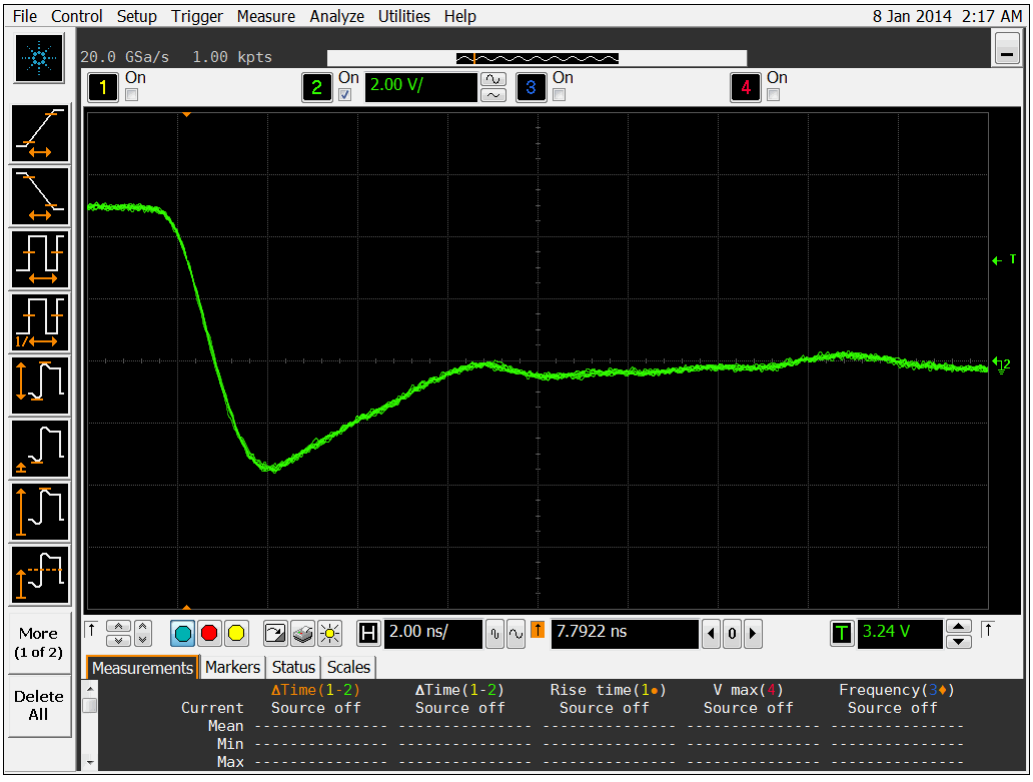


Figure 14b DUT 5504 Post-Annealing Falling Edge

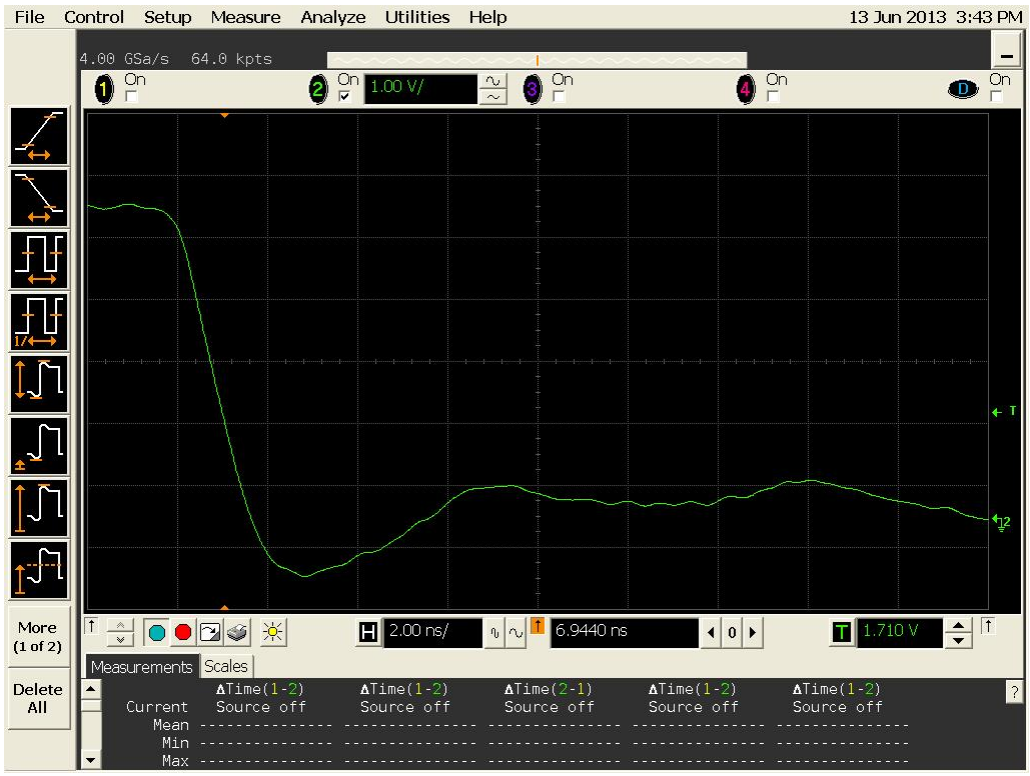


Figure 15a DUT 5608 Pre-Irradiation Falling Edge

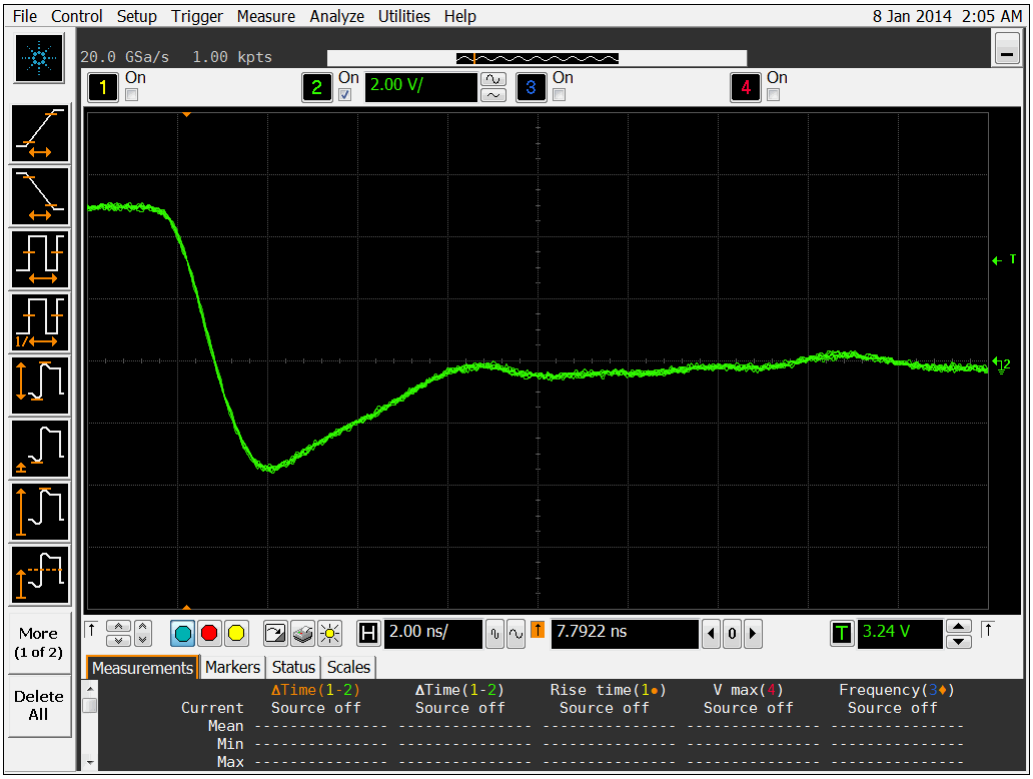


Figure 15b DUT 5608 Post-Annealing Falling Edge

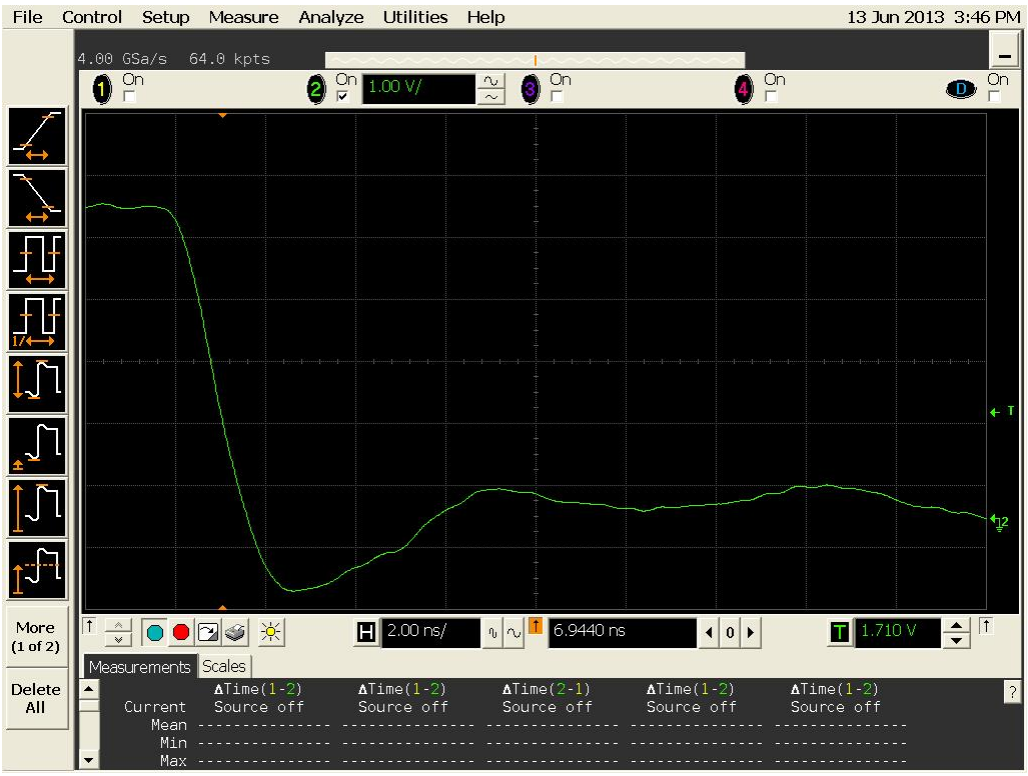


Figure 16a DUT 5629 Pre-Irradiation Falling Edge

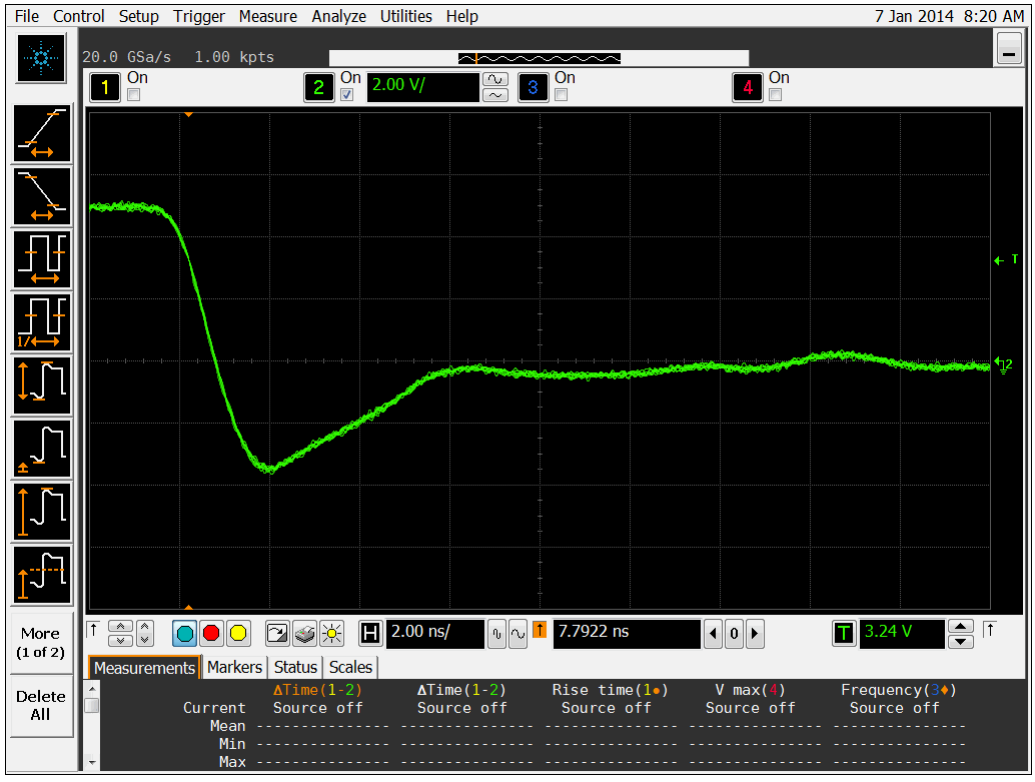


Figure 16b DUT 5629 Post-Annealing Falling Edge

Appendix A: DUT Bias

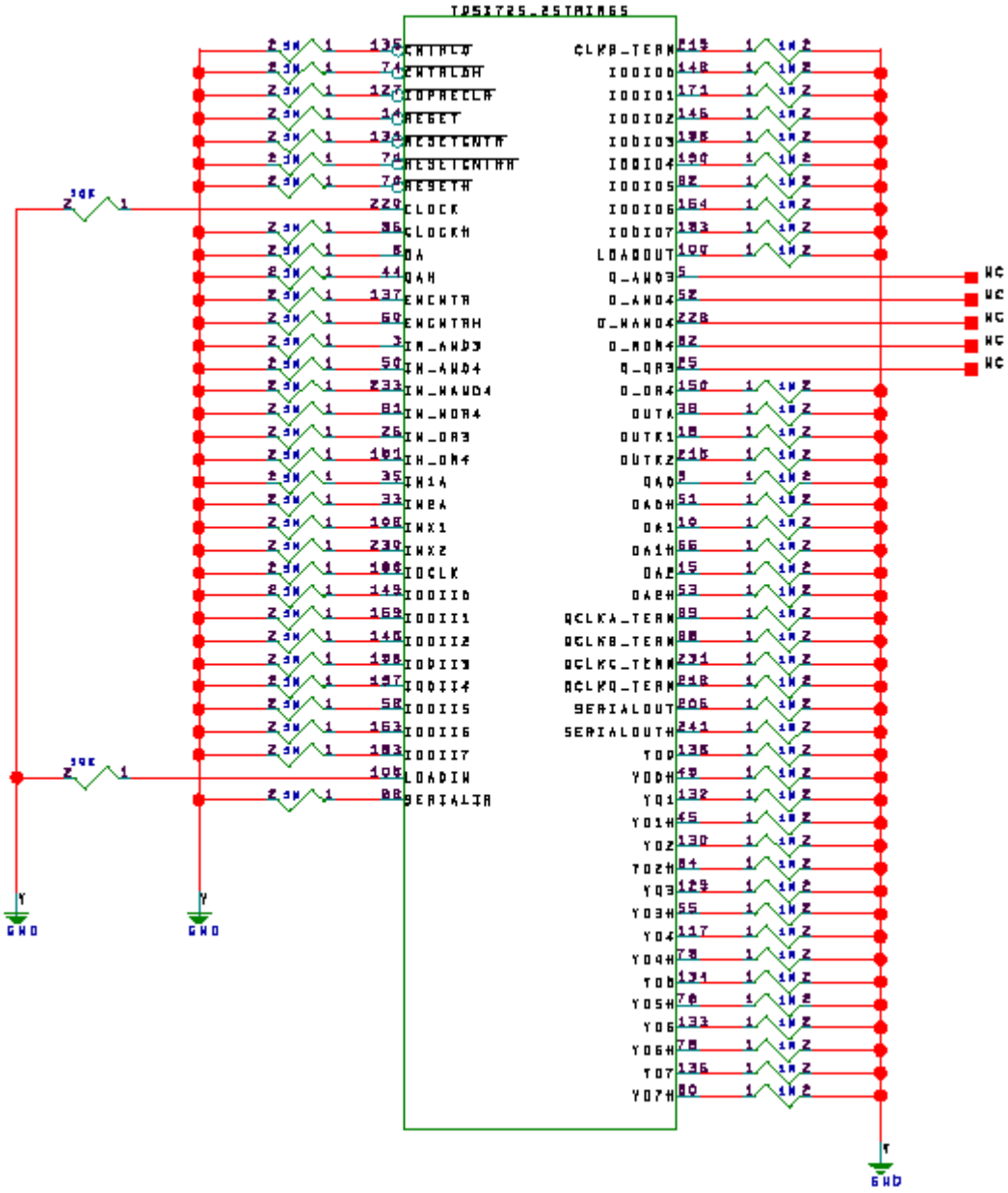


Figure A1 I/O Bias During Irradiation

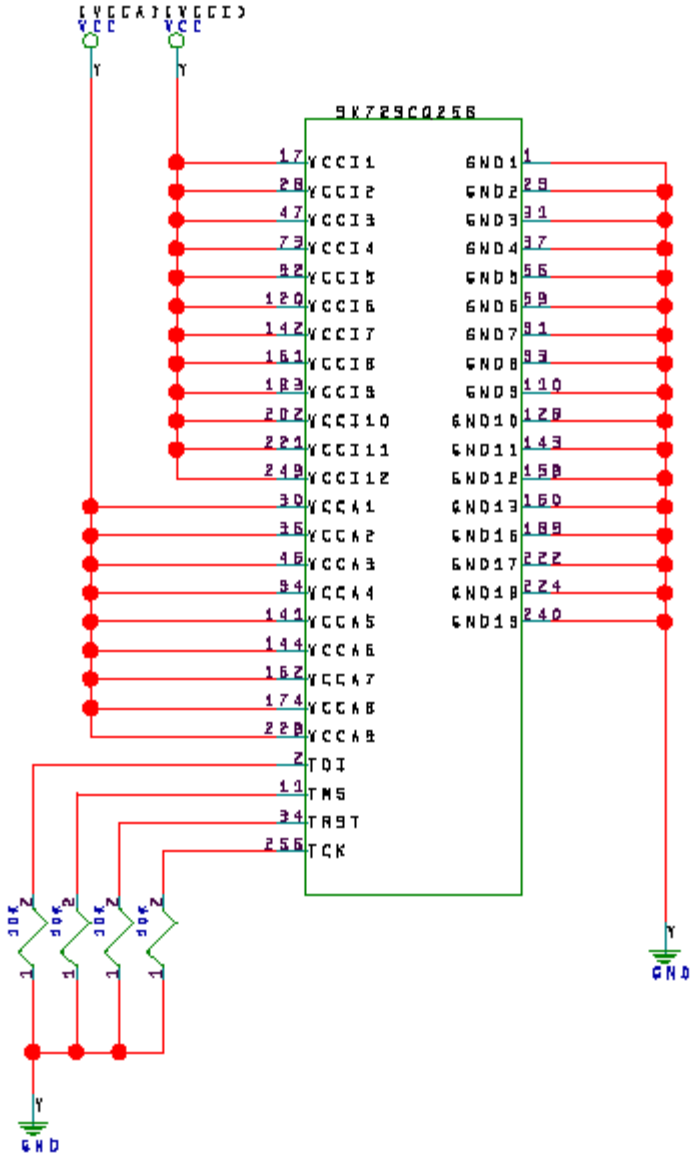
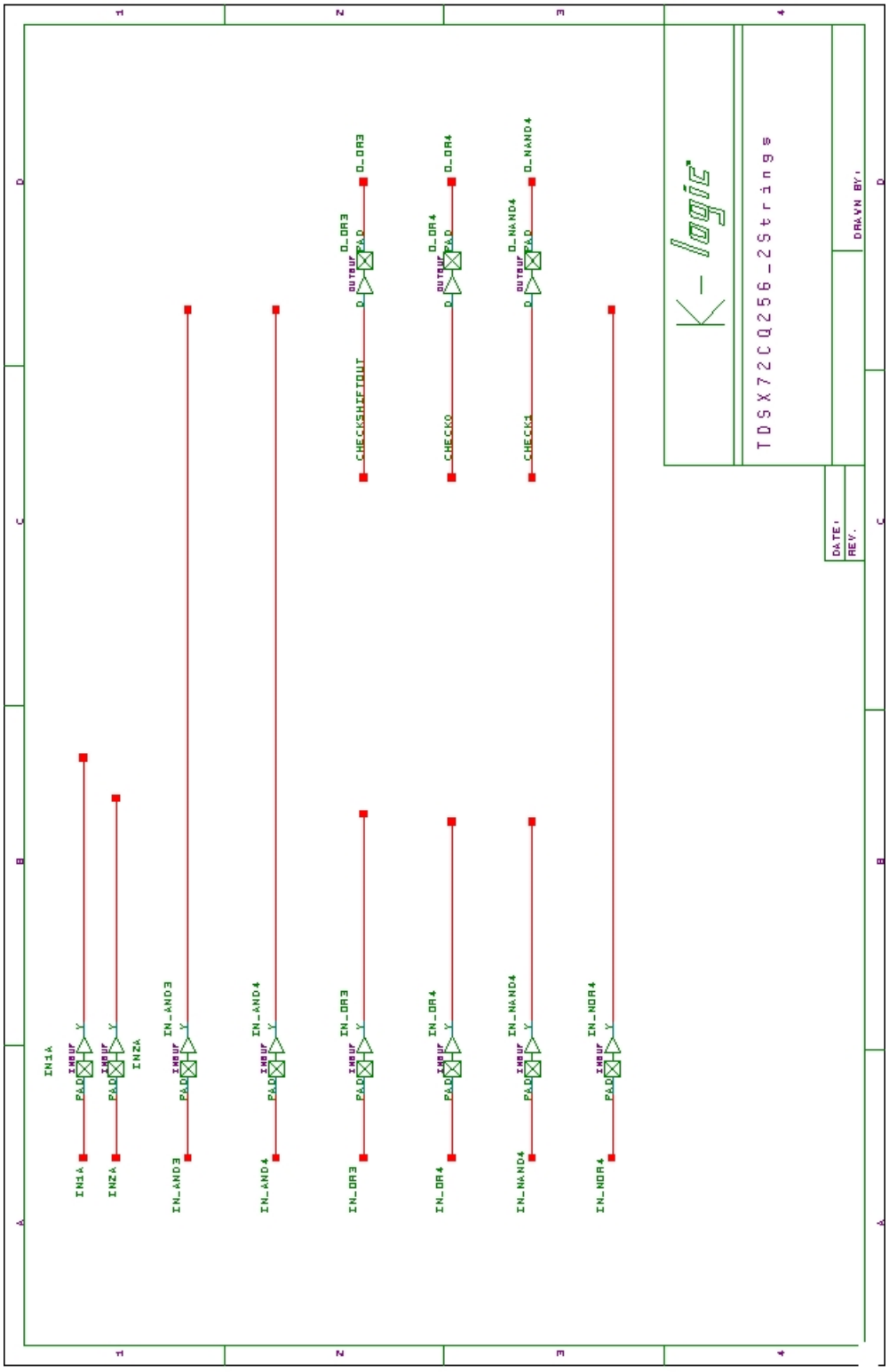
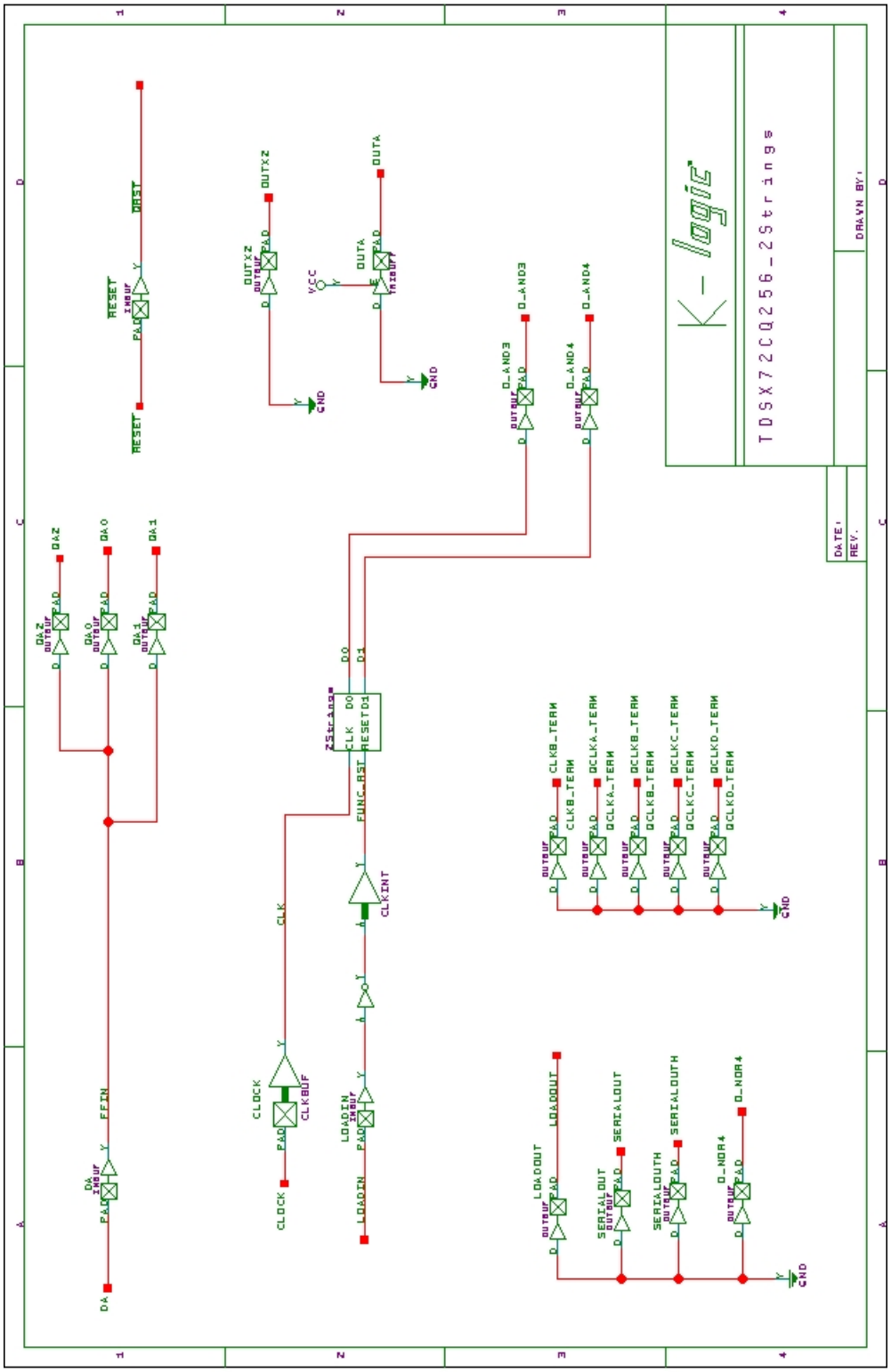


Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

Appendix B: DUT Design Schematics

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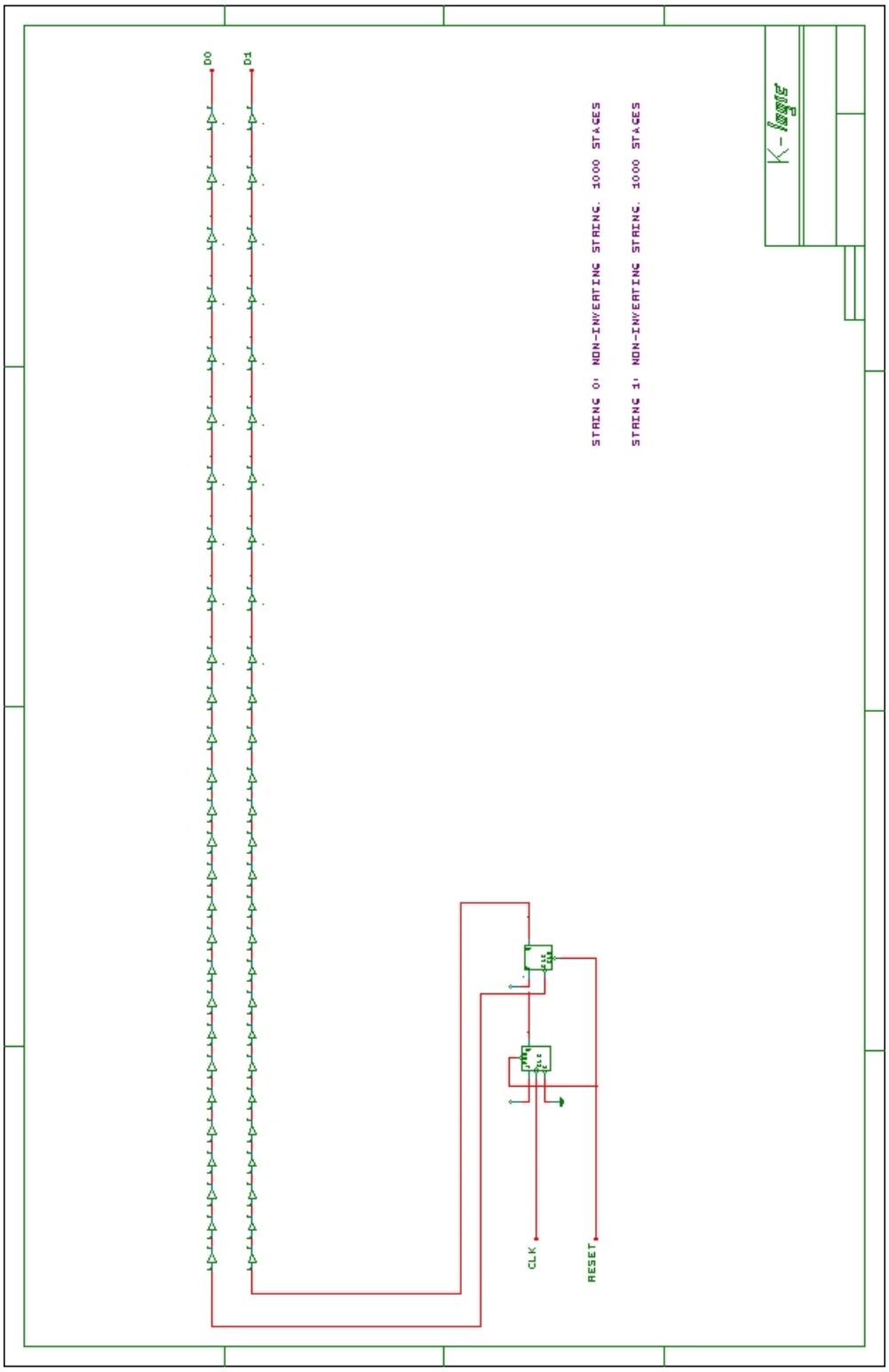
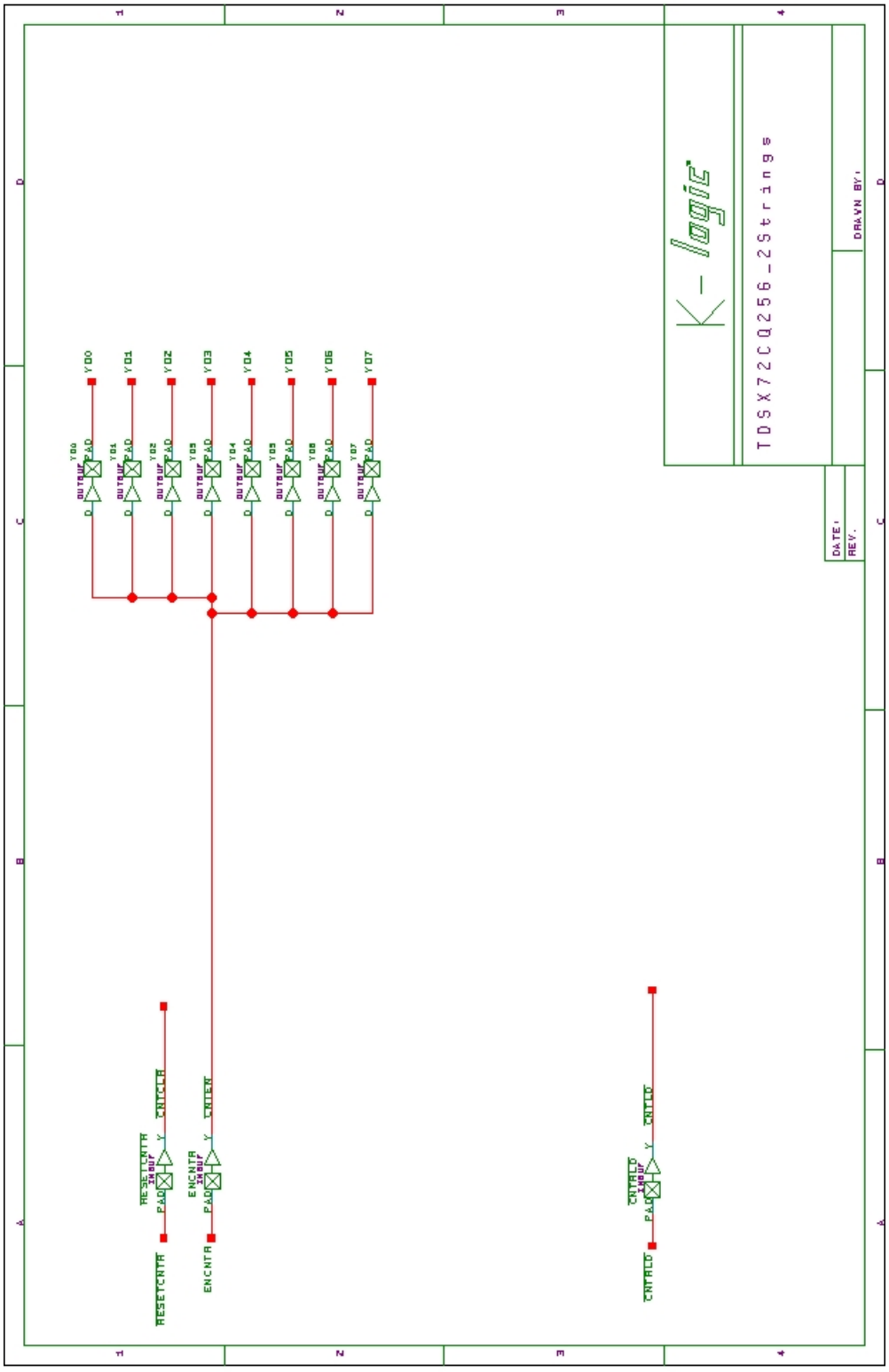
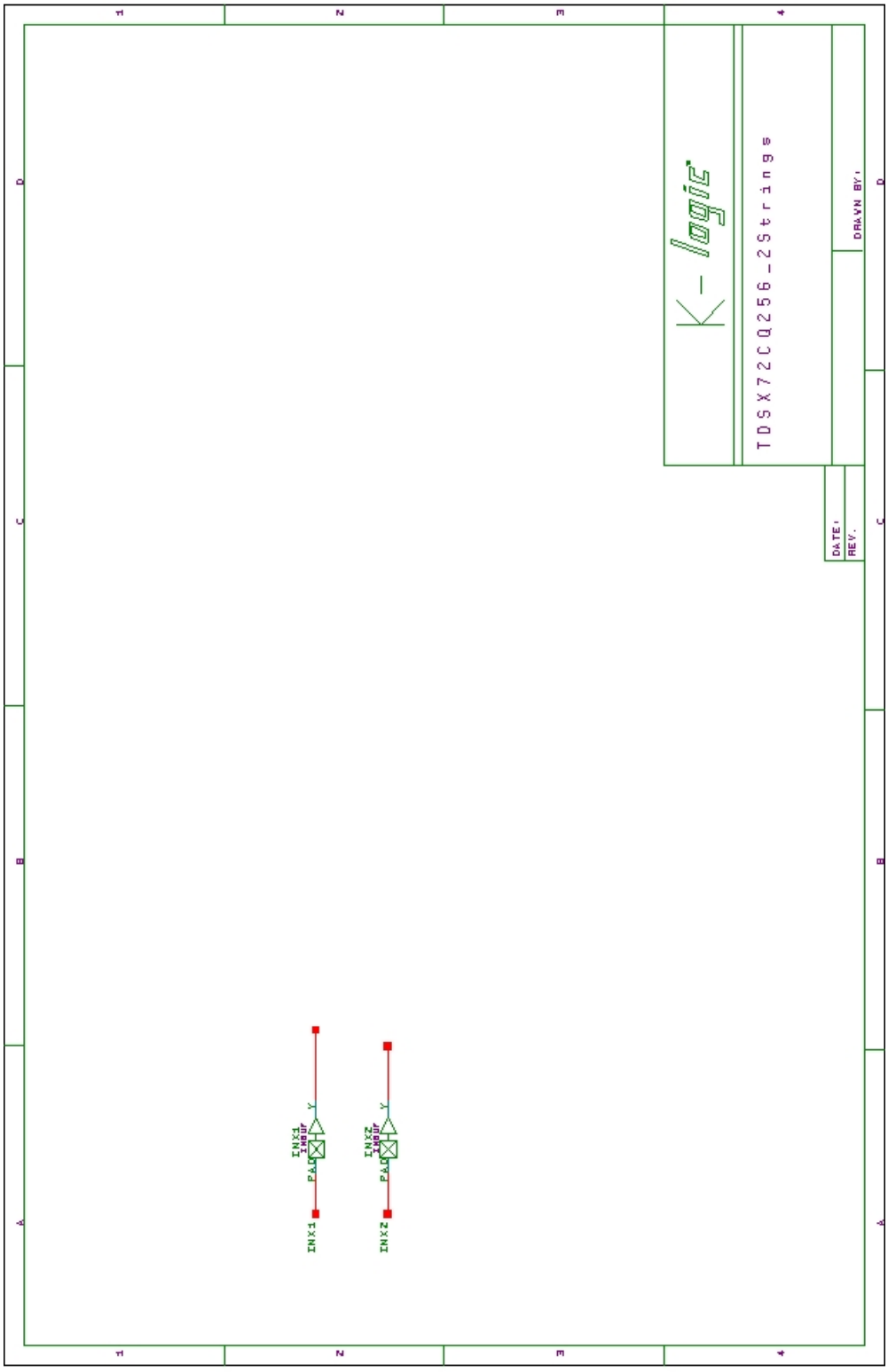
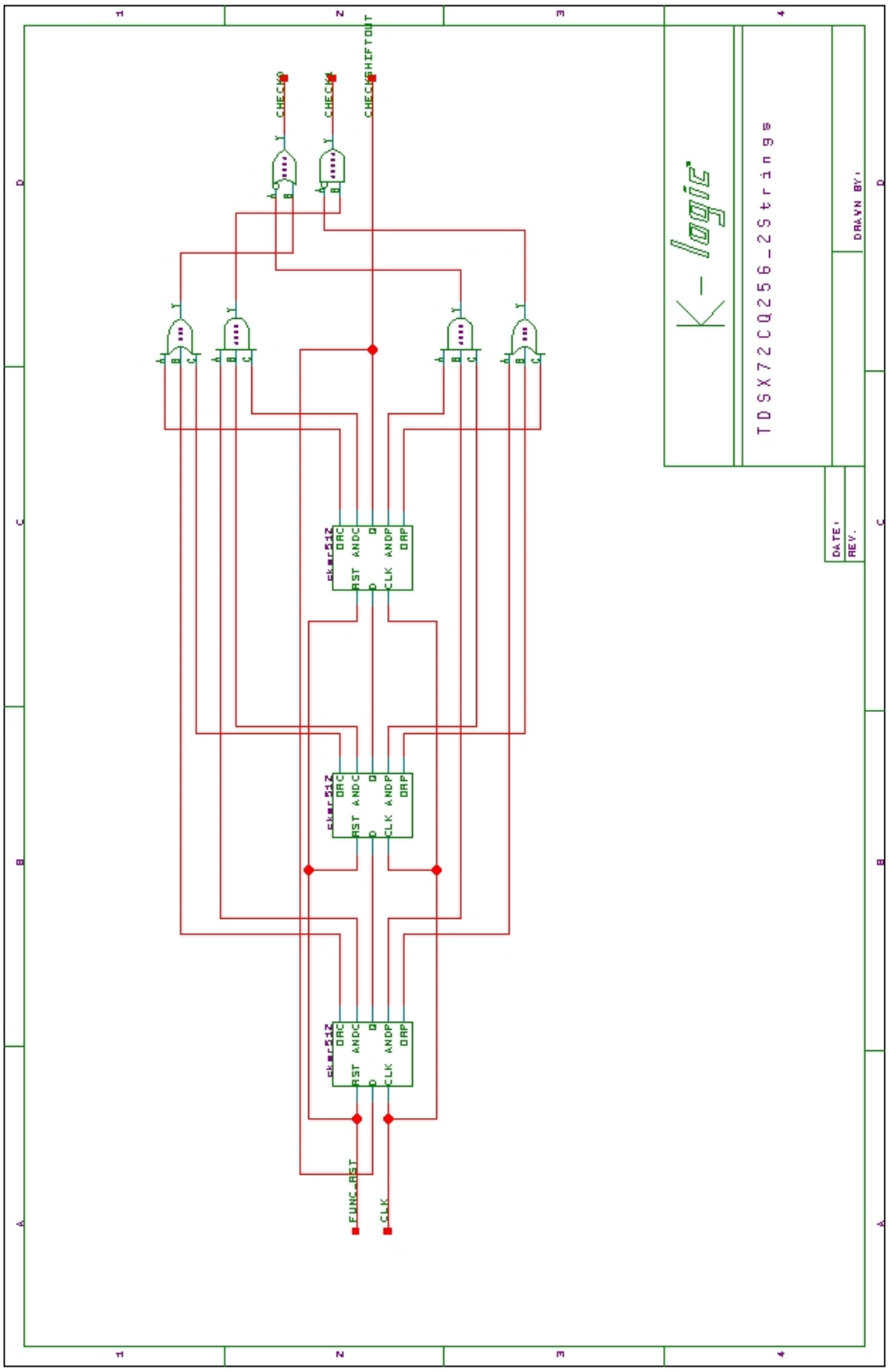
K-logic
DRAWN BY:
DATE:
REV.
RESET
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

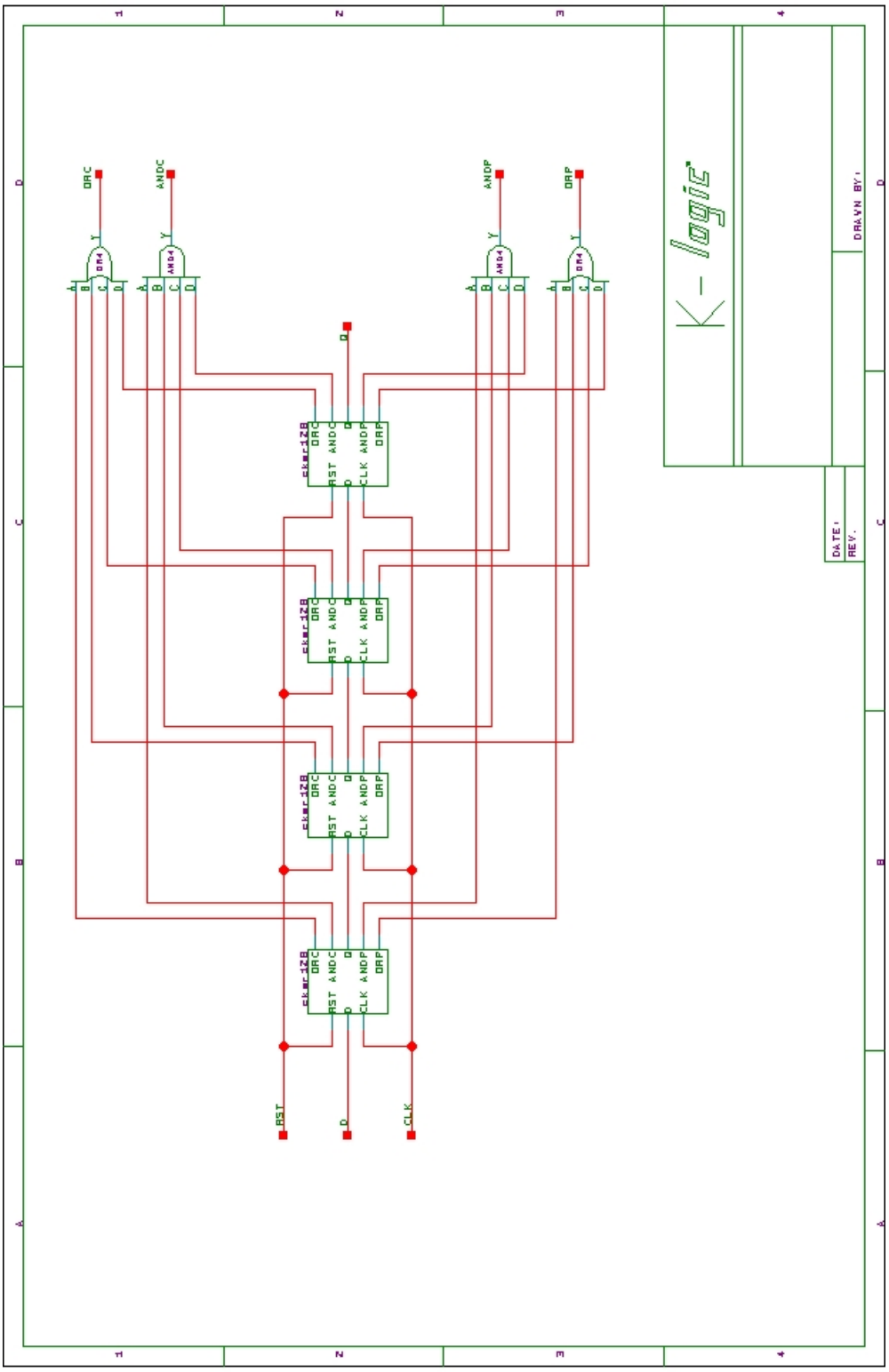

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Logic
CLK
RESET

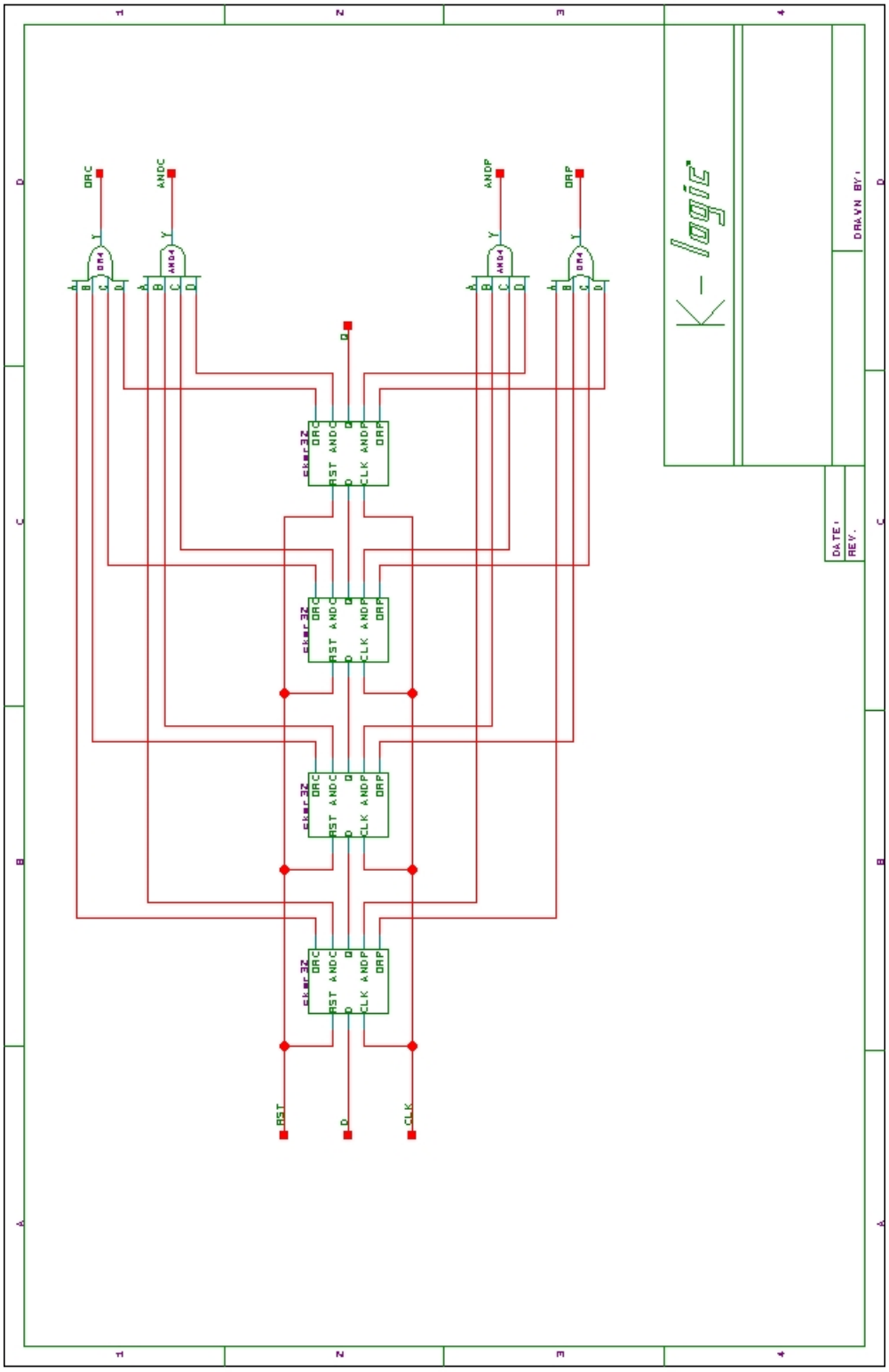

K- logic
T0ACT35XCQ\BUF50NINV
DRAWN BY: RBK
DATE:
REV.
PRESERVE

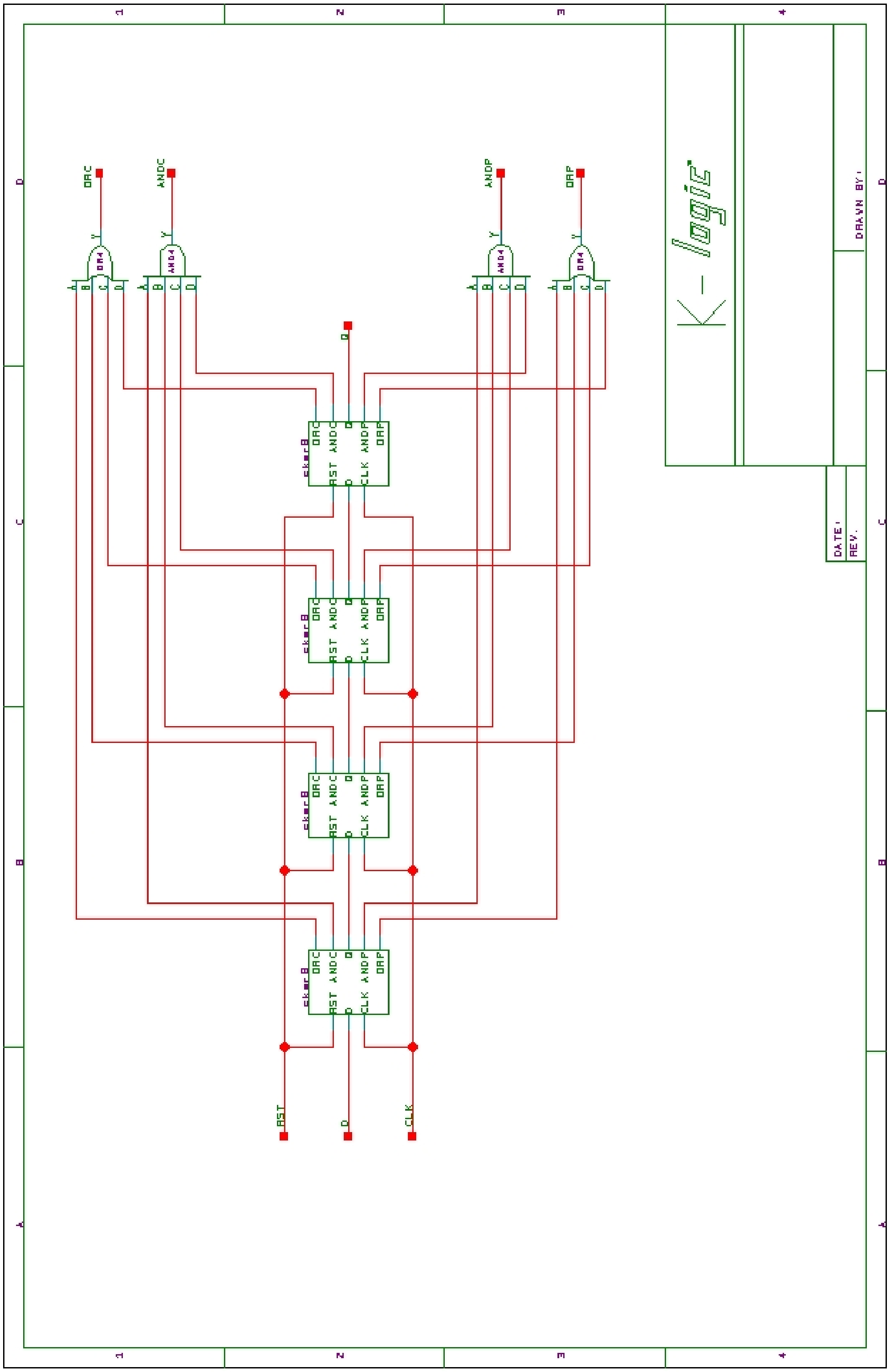

K-logic
TDSX72CQ256-25strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRCLR
CNTRCLD

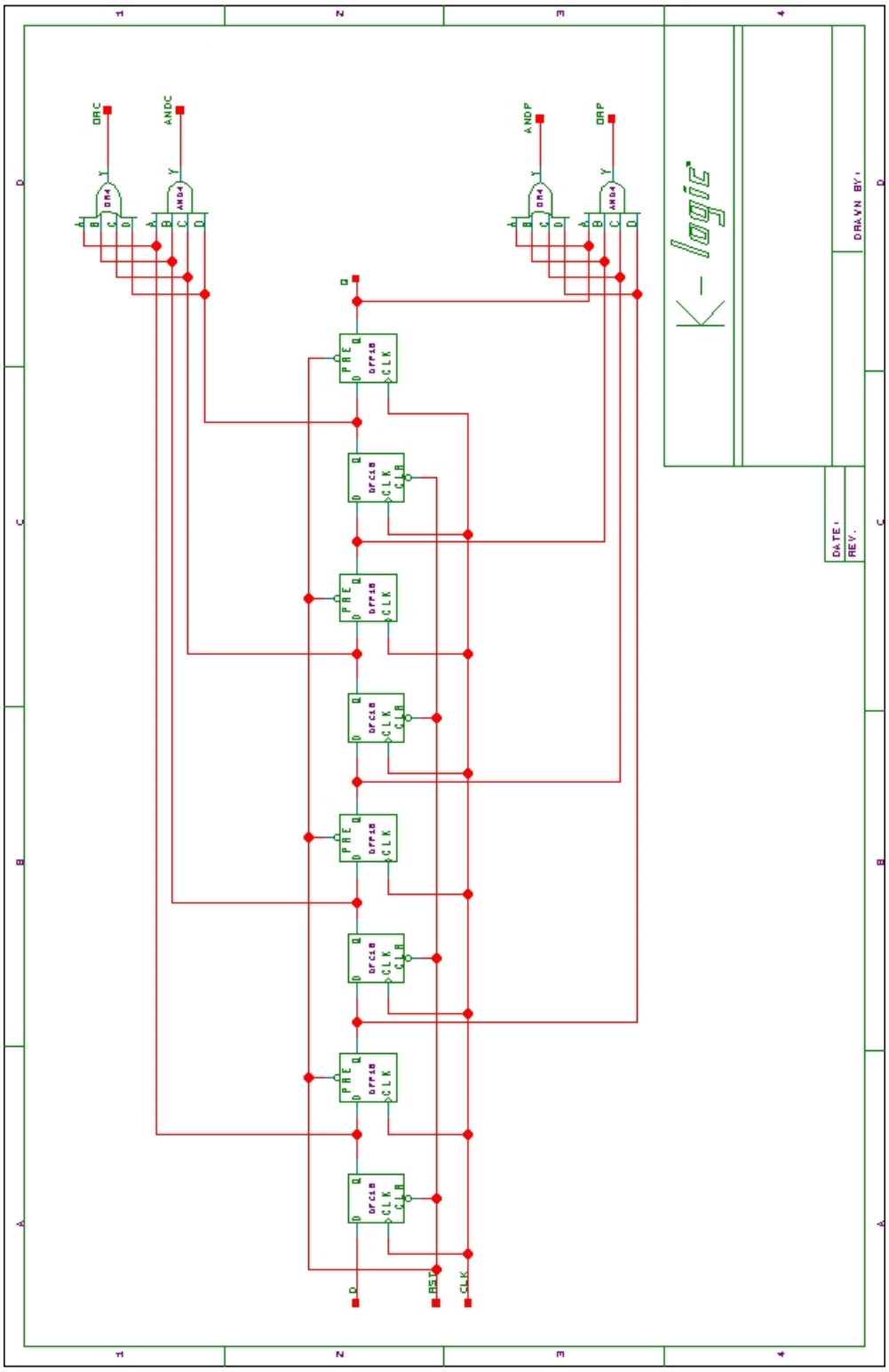

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

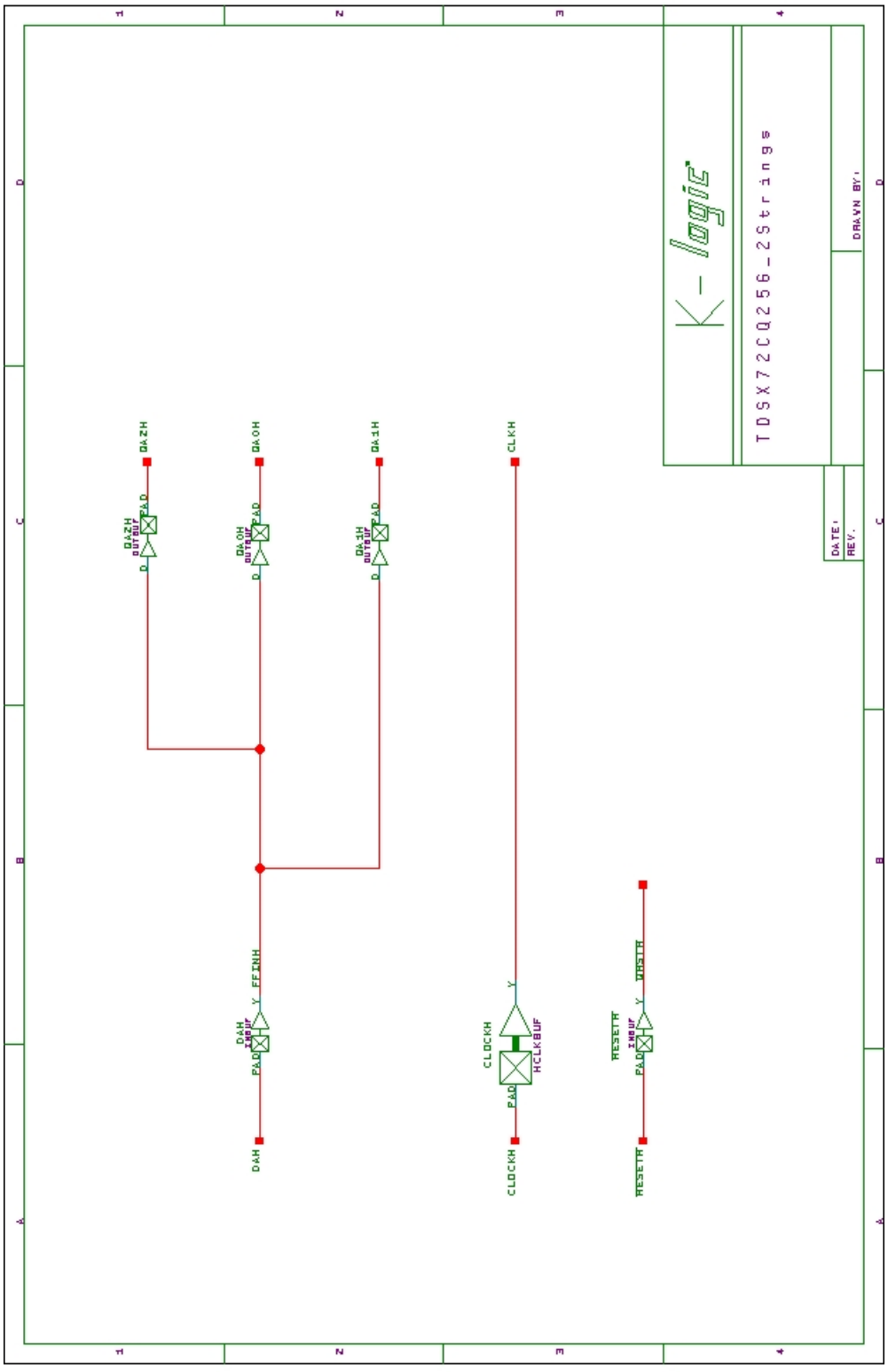

CHECK0
CHECK1
CHECKSHIFTOUT
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
FUNC_RST
CLK

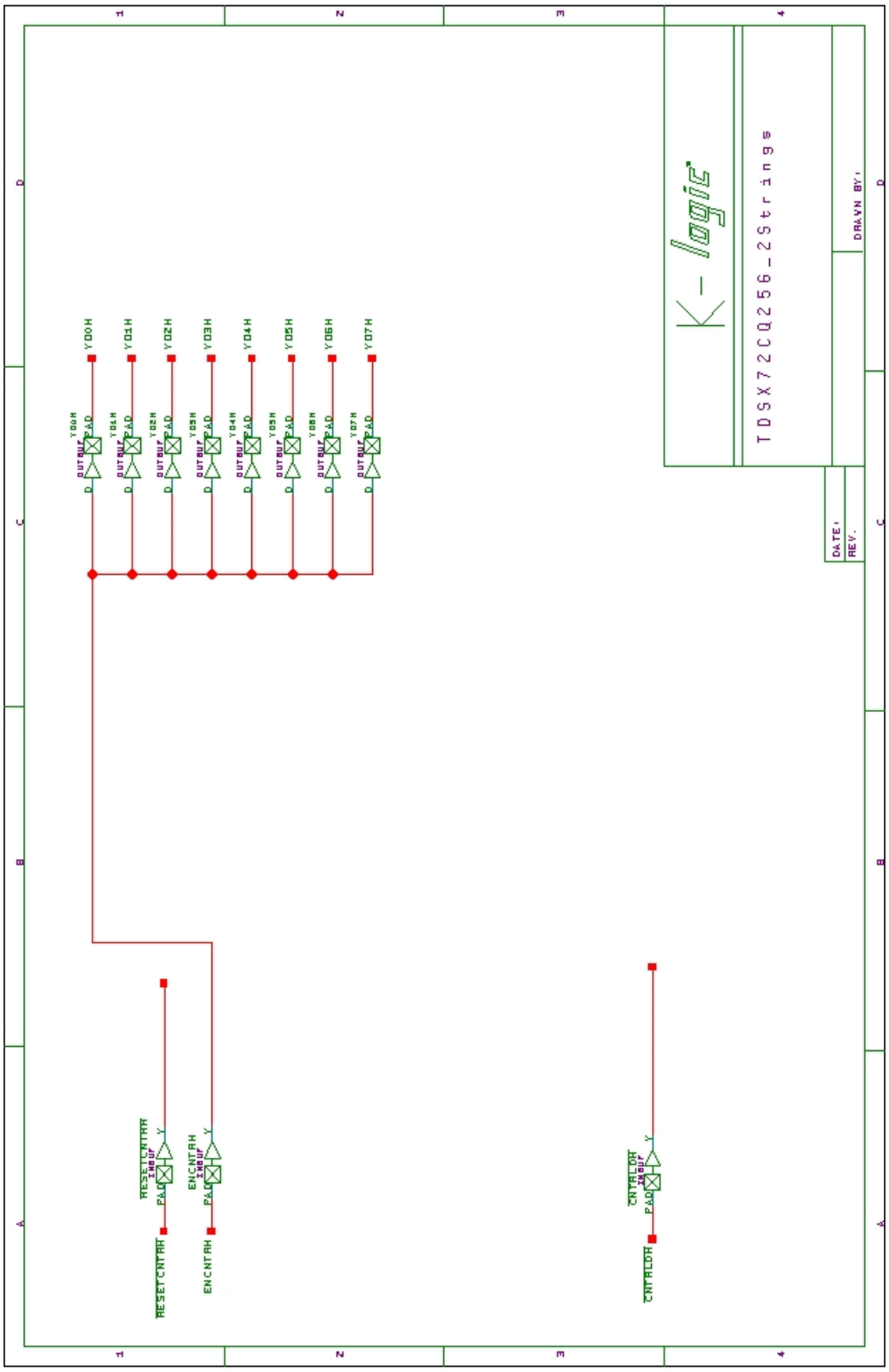

DRC
ANDC
ANDP
DRP
K-logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

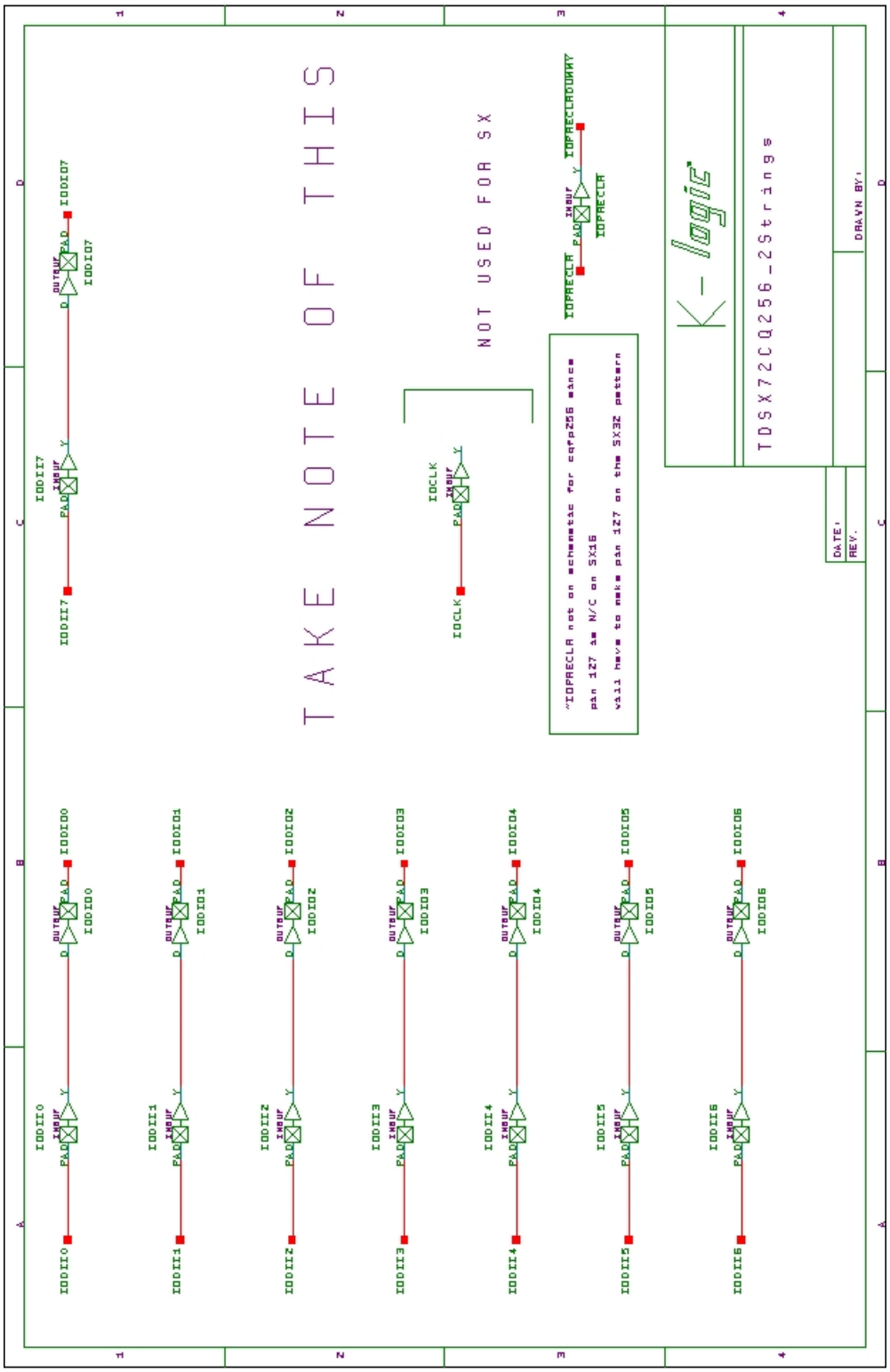

DRC
ANDC
ANDP
DRP
AND4
DRH
K-logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

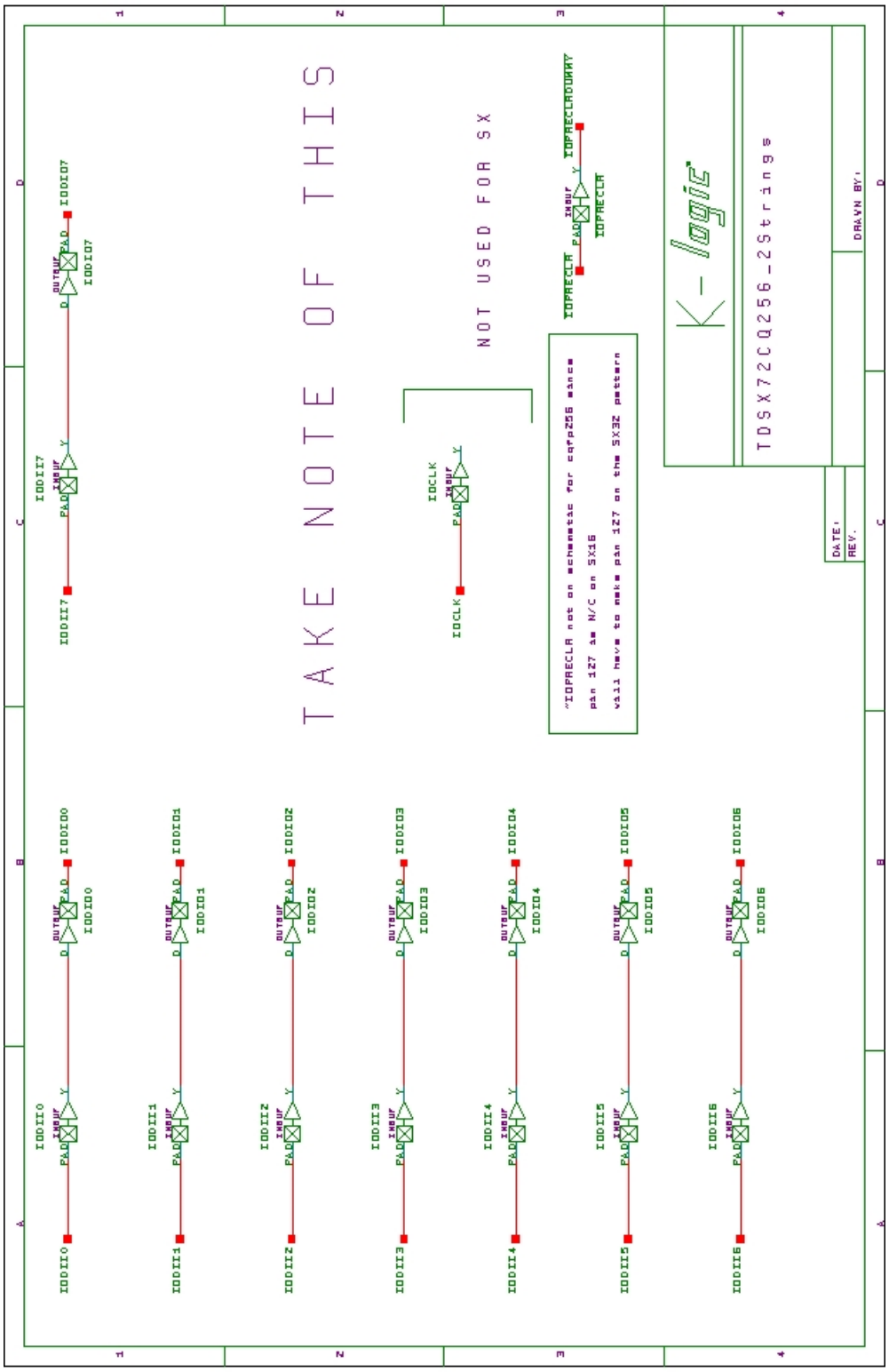

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DATE:
REV.
DRAWN BY:

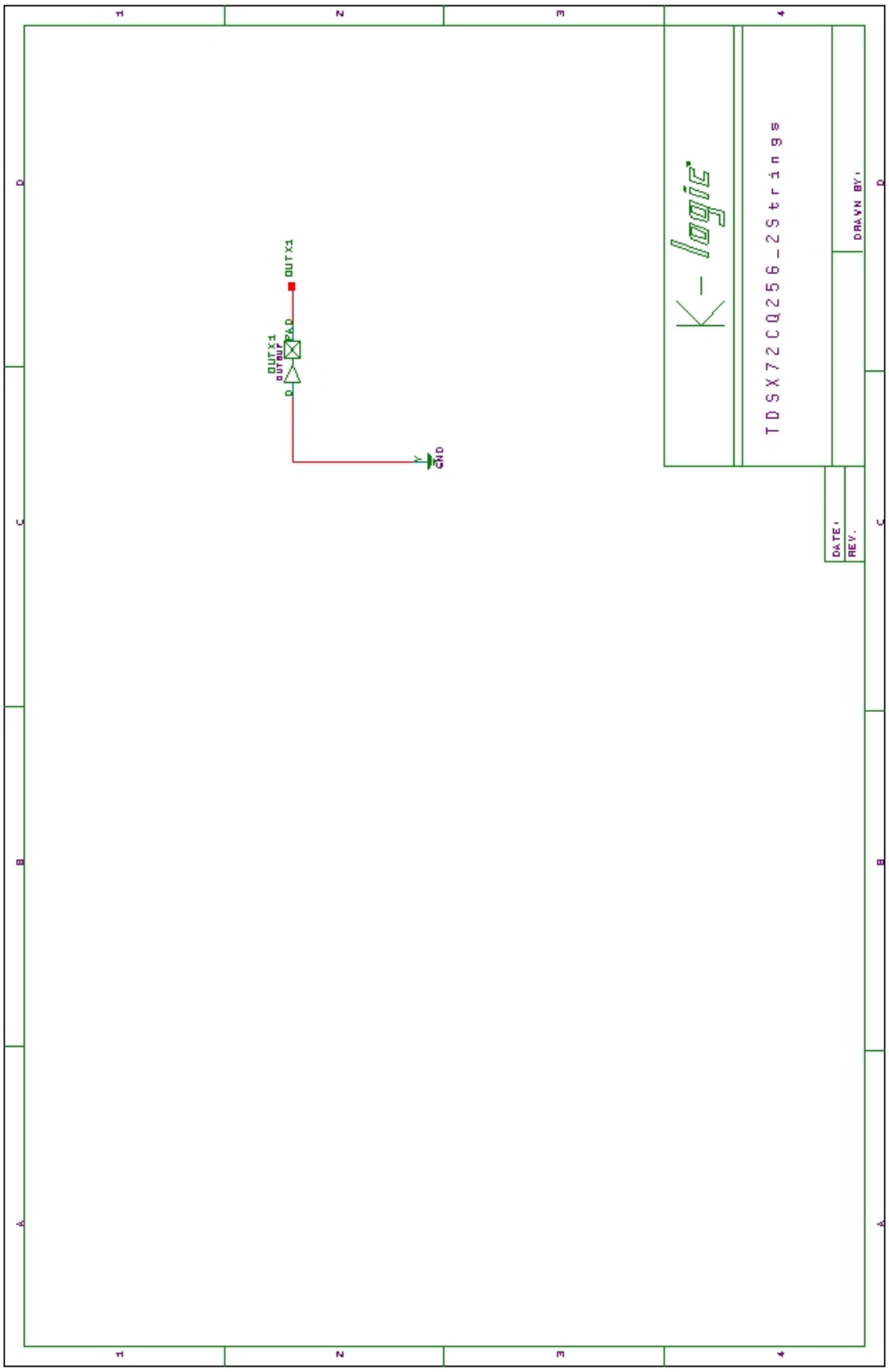

ORC
ANDC
ANDF
ORF
OR4
AND4
DFF1S
DFC1S
PRE
CLR
CLK
D
Q
RST
CLK
Logic
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DAH
RESETH
CLOCKH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
"IOPRECLR not on schematic for csp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


TAKE NOTE OF THIS
NOT USED FOR SX
IOCLK
IOPRECLR
IOPRECLRQUINAY
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
*IOPRECLR not on schematic for csfp256 sance
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


OUTX1
OUTX1
PAD
OUTPUT
GND
logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

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