

UG0646
User Guide
Image Enhancement IP



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The resource utilization reports were updated. For more information, see [Resource Utilization](#), page 5.

1.2 Revision 2.0

The following is a summary of changes made in this revision.

- Updated [Figure 1](#), page 3 and [Table 1](#), page 3. For more information, see [Figure 1](#), page 3.

1.3 Revision 1.0

The first publication of this document.

2 Introduction

Image Enhancement IP enables you to adjust the brightness, contrast and color balance of a final video Image according to personal preferences. These calculations are done in the RGB domain.

The inputs to Image Enhancement IP in terms of brightness and contrast are as follows:

$$R_CONST_I = (R_{gain} \times contrast_factor) / 10$$

$$G_CONST_I = (G_{gain} \times contrast_factor) / 10$$

$$B_CONST_I = (B_{gain} \times contrast_factor) / 10$$

$$COMMON_CONST_I = 128 \times (brightness - ((128 \times contrast_factor) / 10))$$

where,

$$contrast_factor = \frac{325 \times (contrast + 128)}{(387 - contrast) \times 32}$$

R_{gain} , G_{gain} , and B_{gain} are the red, green, and blue gain values.

The output RGB values are calculated from the above inputs based on the following equations:

$$R_{out} = COMMON_CONST_I + R_CONST_I \times R_{in}$$

$$G_{out} = COMMON_CONST_I + G_CONST_I \times G_{in}$$

$$B_{out} = COMMON_CONST_I + B_CONST_I \times B_{in}$$

Where,

R_{in} , G_{in} , and B_{in} are the red, green and blue values of input data.

R_{out} , G_{out} , and B_{out} are the red, green and blue values of output data.

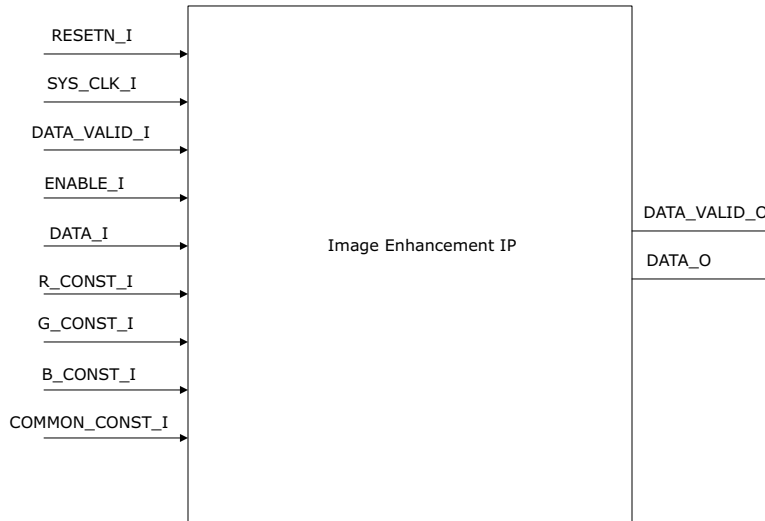
3 Hardware Implementation

This section describes the design description and inputs and outputs of the Image Enhancement IP.

3.1 Design Description

The following figure shows the block diagram of the Image Enhancement IP.

Figure 1 • Block Diagram



When the ENABLE_I and DATA_VALID_I signal goes high the R, G and B values of the output is computed from the inputs according to the formula given in introduction section. DATA_O is valid when DATA_VALID_O (which is equivalent to DATA_VALID_I with two clock cycle delay) goes high.

3.2 Inputs and Outputs

The following table lists the input and output ports of the Image Enhancement IP.

Table 1 • Inputs and Outputs

Port Name	Direction	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
DATA_VALID_I	Input	1 bit	Input data valid signal This signal is asserted high when the data is valid
ENABLE_I	Input	1 bit	Enable signal Should be '1' to enable image enhancement operation

Table 1 • Inputs and Outputs (continued)

Port Name	Direction	Width	Description
DATA_I	Input	3*G_PIXEL_WIDTH bits	Input RGB data DATA_I[3* G_PIXEL_WIDTH -1] to DATA_I[2*G_PIXEL_WIDTH] represents R input DATA_I[2* G_PIXEL_WIDTH -1] to DATA_I[G_PIXEL_WIDTH] represents G input DATA_I[G_PIXEL_WIDTH -1] to DATA_I[0] represents B input
R_CONST_I	Input	10 bits	Input constant to multiply with R data
G_CONST_I	Input	10 bits	Input constant to multiply with G data
B_CONST_I	Input	10 bits	Input constant to multiply with B data
COMMON_CONST_I	Input	20 bits	Input constant with brightness and contrast
DATA_VALID_O	Output	1 bit	Output data valid signal This signal is asserted high when the data is valid
DATA_O	Output	3*G_PIXEL_WIDTH bits	Enhanced RGB data DATA_O[3* G_PIXEL_WIDTH -1] to DATA_O[2*G_PIXEL_WIDTH] represents enhanced R output DATA_O[2* G_PIXEL_WIDTH -1] to DATA_O[G_PIXEL_WIDTH] represents enhanced G output DATA_O[G_PIXEL_WIDTH -1] to DATA_O[0] represents enhanced B output

3.3 Configuration Parameters

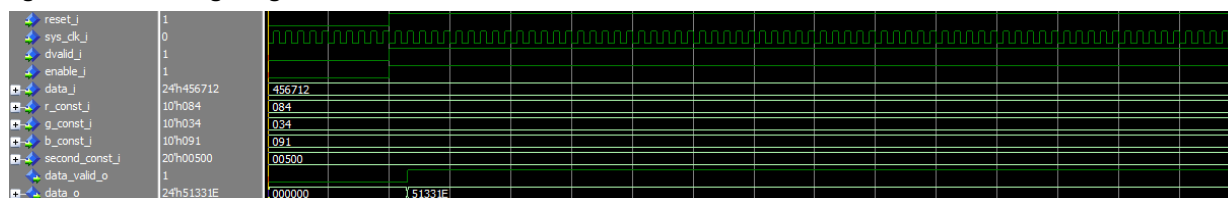
The following table lists the configuration parameters used in the hardware implementation of the Image Enhancement. These parameters are generic and can be varied based on the application requirement.

Table 2 • Configuration Parameter

Parameter Name	Description
G_PIXEL_WIDTH	Bit width of each pixel

3.4 Timing Diagrams

The following figure shows the timing diagram of the Image Enhancement IP.

Figure 2 • Timing Diagram

3.5 Resource Utilization

The Image Enhancement IP is implemented on SmartFusion[®]2 system-on-chip (SoC) field programmable gate array (FPGA) device (M2S150T-1152 FC package) and PolarFire[®] FPGA (MPF300TS-1FCG1152E package).

Table 3 • Resource Utilization on PolarFire¹

Resource	Usage
DFFs	173
4-input LUTs	139
MACC	3
RAM1Kx18	0
RAM64x18	0

1. For G_PIXEL_WIDTH = 8.

Table 4 • Resource Utilization on SmartFusion2¹

Resource	Usage
DFFs	173
4-input LUTs	141
MACC	3
RAM1Kx18	0
RAM64x18	0

1. For G_PIXEL_WIDTH = 8.