

3.5A 12V E-Fuse with Hot-Swap and Voltage Surge Protection

Description

The LX8204 is a fast acting eFuse switch designed both to protect circuitry connected to its output (VOUT) from transient input voltage surges on its input (VCC), and to protect VCC from overload current events coming from the load on VOUT.

Voltage protection features include under-voltage lockout (UVLO), and over-voltage clamping. This clamp limits VOUT voltage allowing continued circuit operation during an input over-voltage transient condition, while UVLO ensures that VOUT remains off until VCC reaches its minimum operating threshold. On the current side, the LX8204 protects the input from a output short circuit and/or over current condition with a 3.5A current limit circuit. Additionally, the LX8204 protects the subsequent systems from hot-swap condition.

Another protection feature is latching thermal shutdown of VOUT, with a fault flag output on the combined EN/FAULT pin. Once thermal shutdown threshold is reached and the eFuse switch opens, the tristate EN/FAULT pin will be pulled to about 1.6V signaling to the system and potentially other connected eFuse switches that a fault has occurred.

Features

- Protected from Hot-Swap Condition.
- 50mΩ(typ.) R_{dson} Internal eFuse FET Protected from 24V
- Up to 24V Transient Input Range
- < 15V Output Voltage Clamp including Dynamic Transient
- Continuous Operation During VCC Surge
- 3.5A Current Limit at Overloading
- Over-Temperature Protection
- 13mS and 1.4ms Softstart Rise Time
- Current Limit During Vout Softstart
- UVLO Detection
- 3mm x 3mm DFN Available

Applications

- Hard-Disk Drive
- Solid-State Drive
- Hot Swap
- PC Cards

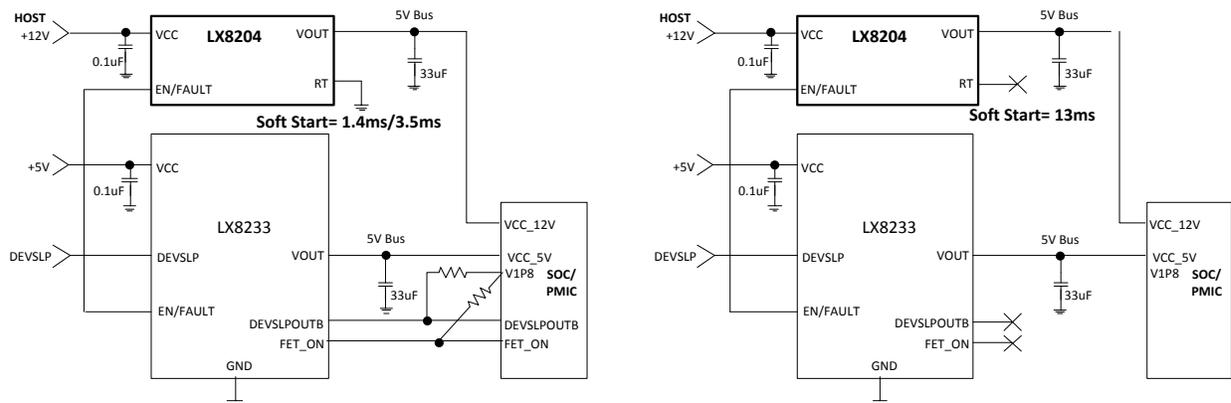
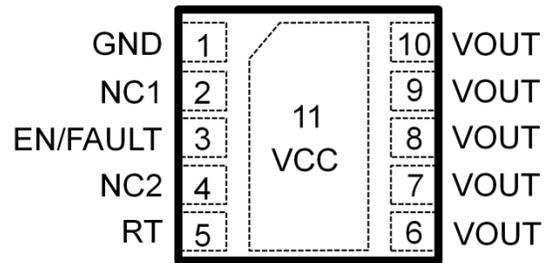


Figure 1 · Typical Application of LX8204

Pin Configuration and Pinout



3mmx3mm WDFN

Figure 2 · Pinout Top View

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant, Pb-free	WDFN 3X3 10L	LX8204-135ILD LX8204-xyyILD*	Bulk / Tube
			LX8204-135ILD-TR LX8204-xyyILD-TR*	Tape and Reel

Consult Factory for other options of “x” and “yy”

“x” is the soft start time with RT = GND (1 = 1.4ms, 3 = 3.5ms)

“yy” is the current limit (20 is 2Amps, 25 = 2.5Amps,30 = 3Amps,35 = 3.5Amps)

Pin Description

Pin Number	Pin Designator	Input/Output	Description																				
1	GND	-	Ground Pin																				
2,4	NC1,2	-	Do Not Connect.																				
3	EN/FAULT	Input/Output	<p>The EN/FAULT pin is a tri-state, bidirectional interface. It can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.</p> <table border="1"> <thead> <tr> <th>Symbol</th> <th>Description</th> <th>EN/FAULT</th> <th>eFuse State</th> <th>Latching</th> </tr> </thead> <tbody> <tr> <td>UVLO</td> <td>Under Voltage Lock Out. This UVLO condition must be applied even VCC is under Hi-Z or grounded.</td> <td>VL</td> <td>Off</td> <td>No</td> </tr> <tr> <td>THsd</td> <td>Thermal Shutdown</td> <td>VM</td> <td>Off</td> <td>Yes</td> </tr> <tr> <td></td> <td>Vcc>UVLO, No Fault</td> <td>VH</td> <td>On</td> <td>n/a</td> </tr> </tbody> </table>	Symbol	Description	EN/FAULT	eFuse State	Latching	UVLO	Under Voltage Lock Out. This UVLO condition must be applied even VCC is under Hi-Z or grounded.	VL	Off	No	THsd	Thermal Shutdown	VM	Off	Yes		Vcc>UVLO, No Fault	VH	On	n/a
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THsd	Thermal Shutdown	VM	Off	Yes																			
	Vcc>UVLO, No Fault	VH	On	n/a																			
5	RT	Input	<p>When RT is floating, the VOUT rise time will be 10ms. When RT is grounded, the VOUT rise time will be longer than 1.4ms. or 3.5ms. LX8204-1yy: 1.4ms VOUT rise time. LX8204-3yy: 3.5ms VOUT rise time.</p>																				
6-10	VOUT	Output	Output of the device, connect to circuitry to be protected.																				
11* (exposed pad)	VCC	Input	Input of the device. Positive input to the device (Bottom exposed pad)																				

Block Diagram

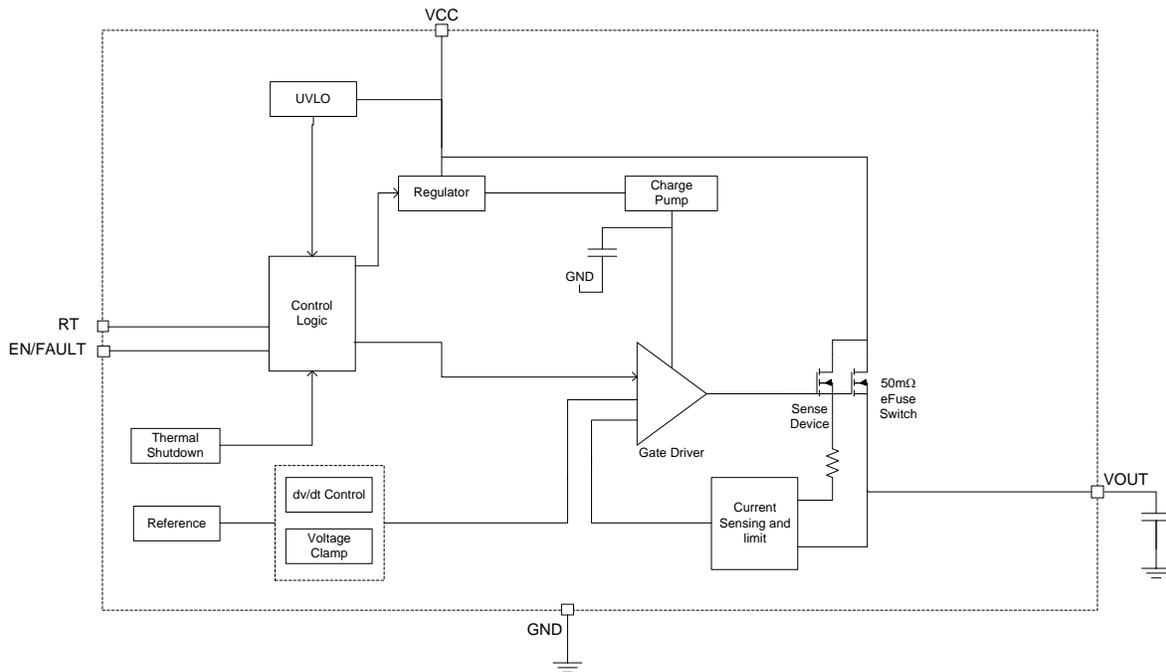


Figure 3 - Simplified Block Diagram of LX8204

Absolute Maximum Ratings

Parameter	Min	Max	Units
VCC to GND (Steady-State)	-0.6	18	V
VCC to GND (Transient 100ms)	-0.6	25	V
EN/FAULT to GND	-0.3	6	V
ESD (Human Body Model)	2000 ^(Note2)		V
ESD (Charged Device Model)	1000		V
Power Dissipation		2.5	W
Storage Temperature	-65	150	°C

Note: 1. Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

2. All pins meet +2000/-2000V HBM ESD rating, except pin 4 which meets +2000/-1500V.

Operating Ratings

	Min	Typ	Max	Units
VCC	10.8	12	13.2	V
I(VCC)			3.5	A
Junction Temperature	-40		125	°C

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	65	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Unless otherwise specified, the following specifications apply over the operating ambient temperature of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ except where otherwise noted with the following test conditions: $V_{IN}=12\text{V}$. Typical parameter refers to $T_J=25^{\circ}\text{C}$

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
eFuse FET						
T_{ONDLY}	Turn-on Delay Time	Enable by EN/FAULT with load current 100mA and 50pF load		100		μs
R_{DSON}	On Resistance	$T_A = 25^{\circ}\text{C}$, (Note 2)	51	59	68	$\text{m}\Omega$
		$T_J = 80^{\circ}\text{C}$, (Note 1)		75	90	$\text{m}\Omega$
I_{OFF}	Off State Output Leakage Current	$CC = 12V_{\text{DC}}$, EN/FAULT = GND, VOUT = GND Measure I(VOUT)			1	μA
I_{DC}	Continuous Current	$T_A = 25^{\circ}\text{C}$		2		A
T_{RISE}	VOUT Rise Time	RT = Float	8	11	12	ms
		RT = GND (LX8204-1yy)		1.4	2	ms
		RT = GND (LX8204-3yy)		3.5		ms
Thermal Shutdown						
T_{SD}	Shutdown Temperature	VOUT is latched off once thermal shutdown is triggered. It can be reset two ways. 1) EN/FAULT is pulled low then let float. 2) VCC is recycled. (Note 1)	140	150	160	$^{\circ}\text{C}$
Under/Over Voltage Protection						
V_{CLAMP}	Output Clamping Voltage	VCC = 18V	13.2		14.2	V
	Maximum Overshoot During Transient	VCC transient from 12V to the higher than 24V at $40\text{V}/\mu\text{s}$ with $I_{\text{VOUT}} = 0\text{A}$. (Note 1)			15.7	V
	Minimum Undershoot During Transient	VCC transient from 12V to the higher than 24V at $40\text{V}/\mu\text{s}$ with $I(\text{VOUT}) = 2\text{A}$. (Note 1)	7.35			V
$V_{\text{UVLO_TH}}$	Under-Voltage Lock-Out Threshold	Turn-on and voltage increases	7.5		9.5	V
$V_{\text{UVLO_HYS}}$	Under-Voltage Lock-Out Hysteresis			1.5		V
Current Protection						
$I_{\text{SC_LIM}}$	Short Circuit Current Limit	VOUT is $<1\text{V}$ from GND.		1.6		A
$I_{\text{AVG_LIM}}$	Overloading Current Limit	VOUT is 0.5V lower than the nominal VOUT.	yy = 20		24	
			yy = 25		2.5	
			yy = 30		3	
			yy = 35	3	3.5	
EN/FAULT						
$V_{\text{EN_DISIL}}$	Disable Logic Input Level Low	Output disabled			0.4	V
$V_{\text{EN_MIDIL}}$	Thermal Fault Input	EN/FAULT pin is driven by the other			1.0	V

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	Logic Level Low	eFuse. Thermal Fault, Output Disabled.				
VEN _{MIDIH}	Thermal Fault Input Logic Level Low	EN/FAULT pin is driven by the other eFuse. Thermal Fault, Output Disabled.	2.1			V
VEN _{ENIH}	Enable Logic Input Level High	Output Enabled	3.3			V
	High State Max Voltage	(Note 1)			5.4	V
VEN _{MIDOL}	Thermal Fault Output Logic Level Low	LX8233 drives EN/FAULT pin. Thermal Fault, Output Disabled,	1.1			V
VEN _{MIDOH}	Thermal Fault Output Logic Level Low	LX8233 drives EN/FAULT pin. Thermal Fault, Output Disabled			1.9	V
I _L _{EN/FAULT}	Logic Low Input Sink Current	V _{EN} = GND at the normal operation		10		μA
		V _{EN} = GND at the thermal shutdown		20		μA
I _H _{EN/FAULT}	Logic High Leakage Current	V _{EN} = 4.3V			3	μA
RT (Note 3)						
	Input leakage current	FET_ON = GND			1	μA
Total Device						
I _Q _{OP}	Bias Current	Operational		0.32	0.5	mA
I _Q _{DIS}		Disable (EN/FAULT = GND)		70		μA
I _Q _{FLT}		Thermal Fault Latch Off		0.1	1	mA
V _{MIN}	Minimum Operating Voltage	(Note 4)			7.6	V
I _{INRUSH}	In-Rush Current	at the slew rate of 12V/10ns (Note 1)		1.5		A

Note: 1. Guaranteed by Design

Note: 2. Pulse test: Pulse width = 300μs, Duty cycle = 2%.

Note: 3. Total pin capacitance must be ≤50pf to be considered floating by the chip.

Note: 4. Device may shut down prior to reaching this level based on actual UVLO trip point.

Theory of Operation / Application Information

EN/FAULT Operation

EN/FAULT is typically floated and connected as common node between the parallel connected devices. There is an a weak (~430kΩ) internal pull-up resistor, so the EN/FAULT pin goes to ~4.3V when VCC = 12V. However when parallel connected the actual voltage depends on the mismatch between the internal regulator supply voltages. To disable VOUT using the EN/FAULT pin you must use an external pull-down device, however the internal pull-up resistor will enable VOUT without any external signal.

If the IC's junction temperature passes the thermal shutdown threshold the LX8204 will pull down the EN/FAULT pin to the mid-level fault logic condition. As shown in the simplified schematic below an internal switch (thermal latch) engages at thermal shutdown driving the EN/FAULT pin to approximately 1.6V with pulldown capability to drive several parallel connected devices. Thus if LX8204 reaches thermal shutdown it will latch off all the parallel connected devices on the same node. It remains at 1.6V until either the Enable Pin is pulled low or there is a VCC power recycle.

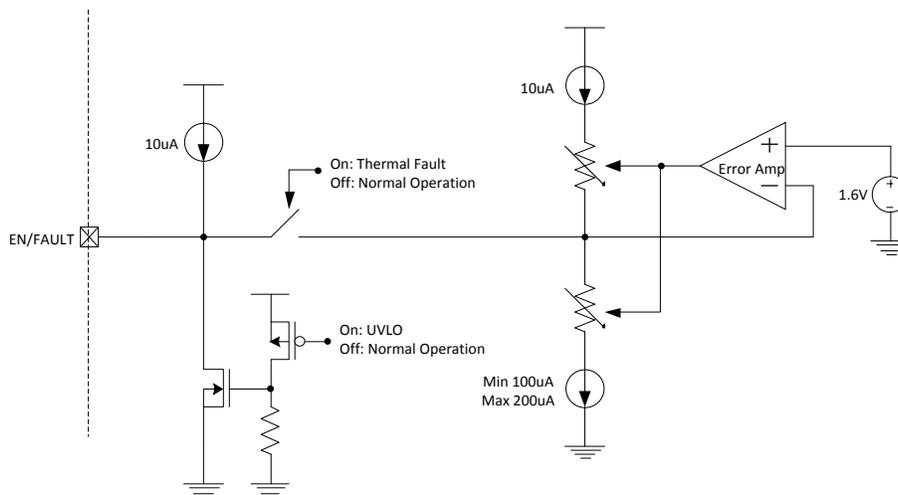


Figure 4 · Simplified EN/FAULT circuitry

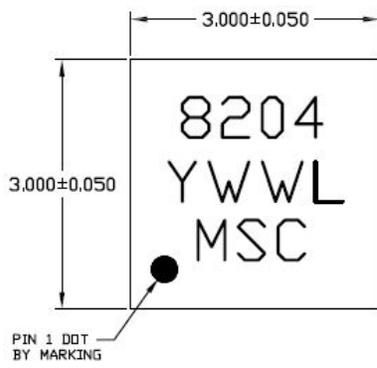
EN/FAULT node is share with a secondary eFuse in order to shutdown the secondary eFuse for the case, thermal fault and UVLO condition. It will guarantee the secondary eFuse never turns on when LX8204 is under the specific condition like thermal fault and UVLO conditions. The EN/FAULT responses are listed in the following table. UVLO condition is applied even when VCC is in Hi-Z or grounded.

	eFuse	EN/FAULT as OUTPUT	Effect on the secondary part
UVLO	eFuse is turned off.	Ground. Drive EN/FAULT is lower than 0.4V	Disable the secondary part.
Thermal Fault	eFuse is turned off. The thermal shutdown is latched off. It can be reset by VIN recycle. EN/FAULT toggle.	Mid point. Drive EN/FAULT lower than 1.9V higher than 1.1V	Disable the secondary part.

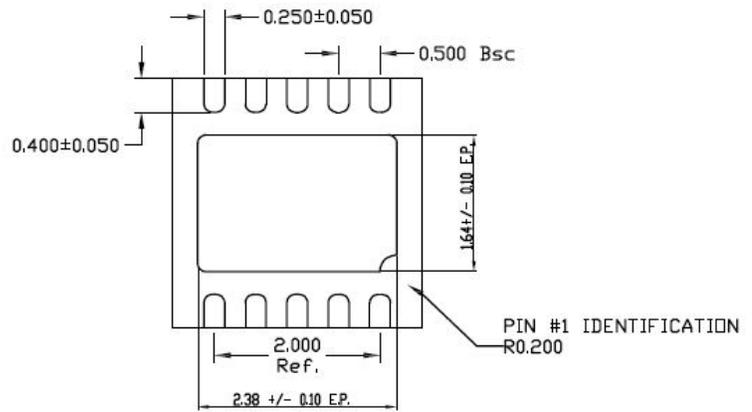
DV/DT (Rise time programming)

The rise time is programmed by either connecting or grounding the RT pin. When the RT pin is floating, the rise time is 13mS (typ). When the RT pin is grounded, the soft start time depends on the order code. For example with order code LX8204-330, the soft start time will be 3.5mS (typ) when the RT pin is floating.

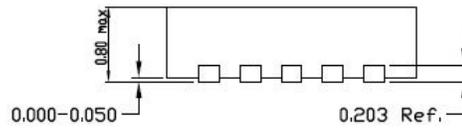
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW



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