IGLOO2 Device Errata

ER0198 v1.4 - July 2016

This Errata sheet contains information about known Errata specific to the IGLOO®2 device family listed in Table 2 and provides available fixes and solutions.

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Table 1: **Revision History**

Date	Version	Changes
July 2016	1.4	Updated text for item 19.
April 2016	1.3	Added Errata items 20. and 21.
December 2015	1.2	Updated Table 3 to include the M2GL010 revision 3 device.
		Added errata item 19.
		Updated Table 7 to include the M2GL010 (T, TS) device
		Added solution to item 14.
August 2015	1.1	Updated M2GL060 Revision from ES to Rev 0.
June 2015	1.0	Combined M2GL005, M2GL010, M2GL025, M2GL060, M2GL090 and M2GL150 devices and die revisions to one centralized document. Created a separate Errata for the M2GL050 device.

Table 2: **Revisions Released per Device**

Silicon Devices	Revisions	Device Status
M2GL005 (S)	All Temperature Grades	Production
M2GL010 (S, T, TS)	All Temperature Grades	Production
M2GL025 (T, TS)	All Temperature Grades	Production
M2GL060 (T, TS)	All Temperature Grades	Production
M2GL090 (T, TS)	All Temperature Grades	Production
M2GL150 (T, TS)	All Temperature Grades	Production

Errata for IGLOO2 Devices

Table 3 lists the specific device Errata and the affected IGLOO2 devices. Refer to the Marking Specification Details in the *PB0121: IGLOO2 FPGA Product Brief* for this Die revision part marking specification.

Table 3: **Summary of IGLOO2 Device Errata**

Errata No.	Errata	Silicon Revision(s) Affected													Software Errata
		M2GL005		M2GL010			M2GL025		M2GL060	M2GL090			M2GL150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
1.	VPP must be set to 2.5 V when programming or writing the eNVM at Industrial temperature range	X		X			X								
2.	Over-voltage support on MSIOs during Flash*Freeze mode	X		X			X								
3.	Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure	X		X			X								
4.	DDR_OUT and I/O-Reg functional Errata due to a software bug														X
5.	Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug														X
6.	Power-up digest is not supported	X		X			X			X			X		

Notes:

- *An "X" means that the Errata exists for that particular device and revision number.*
- *A blank box means that the Errata does not exist or the feature does not exist for that particular device and revision number.*
- *NS (Not Supported) means the Programming Recovery Mode is not available in this revision.*
- *Software Errata can be avoided by using Libero SoC v11.4 SPI or newer.*

Table 3: **Summary of IGLOO2 Device Errata (continued)**

Errata No.	Errata	Silicon Revision(s) Affected													Software Errata
		M2GL005		M2GL010			M2GL025		M2GL060	M2GL090			M2GL150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
7.	Programming of the eNVM must only occur as part of a bitstream containing the FPGA fabric														X
8.	Updating eNVM from the FPGA fabric requires changes in the FREQRNG register	X	X	X	X	X	X	X	X	X	X	X	X	X	
9.	SYSCTRL_RESET_STATUS macro is not supported	X		X			X			X			X		
10.	Zeroization is not supported	X		X			X			X	X		X		
11.	The System controller RC oscillator runs at 25 MHz after a programming recovery operation			NS	X					NS	X				
12.	ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported									X			X		
13.	Programming the FPGA fabric can occur only at room temperature									X			X		
14.	Programming the eNVM blocks needs to occur independent of the fabric									X			X		
15.	PCIe Hot Reset support requires a soft reset solution			X	X	X	X	X	X	X	X	X	X	X	
16.	eNVM1 becomes inaccessible to FPGA fabric master after executing SRAM-PUF services									X	X	X	X	X	

Notes:

- *An "X" means that the Errata exists for that particular device and revision number.*
- *A blank box means that the Errata does not exist or the feature does not exist for that particular device and revision number.*
- *NS (Not Supported) means the Programming Recovery Mode is not available in this revision.*
- *Software Errata can be avoided by using Libero SoC v11.4 SPI or newer.*

Table 3: **Summary of IGLOO2 Device Errata (continued)**

Errata No.	Errata	Silicon Revision(s) Affected												Software Errata
		M2GL005		M2GL010			M2GL025		M2GL060	M2GL090			M2GL150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
17.	After successful completion of 2-step IAP, user design/logic cannot access the fabric SRAM (LSRAM and uSRAM) blocks	X	X	X	X	X	X	X	X	X	X	X	X	X	
18.	SRAM-PUF system services may take two to three seconds to complete									X	X	X	X	X	
19.	The I/Os state during programming is changed from Z to weak pull-up	X		X			X						X		
20.	For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM	X	X	X	X	X	X	X	X	X	X	X	X	X	
21.	Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices								X	X	X	X	X	X	

Notes:

- *An "X" means that the Errata exists for that particular device and revision number.*
- *A blank box means that the Errata does not exist or the feature does not exist for that particular device and revision number.*
- *NS (Not Supported) means the Programming Recovery Mode is not available in this revision.*
- *Software Errata can be avoided by using Libero SoC v11.4 SPI or newer.*

For more information, contact *Microsemi SoC Technical Support*. To order a specific die, contact your local Microsemi sales office.

Errata Descriptions and Solutions

1. VPP must be set to 2.5 V when programming or writing the eNVM at Industrial temperature range

VPP can be set to 2.5 V or 3.3 V. However, when writing or programming the eNVM of Revision 0 of the M2GL005, M2GL010, and M2GL025 devices below 0°C, VPP must be set to 2.5 V.

Refer to the *DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet* for VPP minimum and maximum settings. The eNVM reading with VPP set to 3.3 V or 2.5 V operates as intended.

2. Over-voltage support on MSIOs during Flash*Freeze mode

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in Flash*Freeze mode.

3. Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure

Standalone verification (STAPL VERIFY action) should be run at temperatures lower than 50°C. If a VERIFY action is run at temperatures higher than 50°C, a false verify failure may be reported. The Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

4. DDR_OUT and I/O-Reg functional Errata due to a software bug

This Errata is applicable only if you have created or updated the design using Libero® SoC v11.1 SP1 or v11.1 SP2.

The corresponding I/O does not function properly in the silicon due to the wrong software implementation of the I/O macro, If you have one of the following in the design:

- If you use DDR_OUT macro in the design.
- If you combine an output or output enable register with an I/O using the PDC command set_io <portName> -register yes

Solution:

Both Errata are fixed in Libero SoC v11.1 SP3. Migrate the design to Libero SoC v11.1 SP3 or newer version, and re-run Compile and Layout.

5. Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug

If the design has a dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug, and the device fails during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This Errata exists when you choose the differential I/O option (dedicated differential I/O is used as CCC reference clock input).

This Errata cannot be detected in any functional simulation, and can only be detected in silicon testing.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to Libero SoC 11.1 SP3 or newer version, and re-run Compile and Layout.

6. Power-up digest is not supported

Workaround:

Use NVM Data Integrity Check System service after the device is switched ON, and check the data integrity.

7. Programming of the eNVM must only occur as part of a bitstream containing the FPGA fabric

The Bitstream Configuration Dialog Box in the Libero SoC allows the user to program the eNVM and the FPGA fabric separately. However, if Libero v11.1 SP2 or an older version is used, program the eNVM along with the FPGA fabric for the M2GL005, M2GL010, M2GL025, and M2GL050 devices. The fabric can be programmed separately, if needed.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to Libero SoC 11.1 SP3 or newer version, and re-run Compile and Layout.

8. Updating eNVM from the FPGA fabric requires changes in the FREQRNG register

When updating the eNVM from the FPGA fabric, the NV_FREQRNG register must be changed from 0x07(default) to 0x0F. eNVM reads are not affected.

9. SYSCTRL_RESET_STATUS macro is not supported

10. Zeroization is not supported

11. The System controller RC oscillator runs at 25 MHz after a programming recovery operation

After a programming recovery event, the system controller operates at 25 MHz. In general, the System controller must operate at 50 MHz after a programming recovery event.

Workaround:

For the system controller to operate at 50 MHz, contact soc_tech@microsemi.com.

12. ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported

13. Programming the FPGA fabric can occur only at room temperature

14. Programming the eNVM blocks needs to occur independent of the fabric

Customer using Revision 0 of M2GL090 or M2GL150 devices must Program the eNVM block independently in Libero v11.6 or older. Contact Microsemi SoC Technical Support, if you want to Program the eNVM block independently in Revision 0 of M2S090 and M2S150 devices using Libero v11.7.

15. PCIe Hot Reset support requires a soft reset solution

On IGLOO2 devices, a PCIe® Hot Reset requires a soft FPGA logic reset scheme, which clears the sticky bits of the PCI configuration space.

Workaround:

The application note *AC437: Implementing PCIe Reset Sequence in SmartFusion2 and IGLOO2 Devices* describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases.

- For the M2GL060/M2GL090T(S) devices there are no violations.
- For the M2GL010/M2GL025/M2GL150T(S) devices at Gen1 rates there are no violations.
- For the M2GL/M2GL025/M2GL150T(S) devices at Gen2 rates there are two PCIe CV violations.
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg)

16. eNVM1 becomes inaccessible to FPGA fabric master after executing SRAM-PUF services

In the IGLOO2 M2GL090/M2GL150 devices, the System Controller does not release the eNVM1 access after executing the following SRAM-PUF system services:

- Create User AC (Activation Code) service
- Delete User AC service
- Create User KC for an Intrinsic Key service
- Create User KC for an Extrinsic Key service
- Delete User KC service

The above system services are executed successfully. However, the eNVM1 is inaccessible to fabric master.

Any subsequent access to eNVM1 after this point, where eNVM1 is locked by the System Controller, results in a stall, and a Power on Reset (POR) is required to remove the stall.

Workaround:

Execute "Get Number of the Key Code (GET_NUMBER_OF_KC)" SRAM-PUF system services immediately after the above services.

- The additional GET_NUMBER_OF_KC services releases the eNVM1 access from the System Controller.
- The firmware code for running SRAM-PUF services workaround must be executed from eNVM0, eSRAM, or DDR memories only, as the Fabric master does not get access to the eNVM1 that time.

17. After successful completion of 2-step IAP, user design/logic cannot access the fabric SRAM (LSRAM and uSRAM) blocks

If LSRAM/uSRAM Read and Write access fails from the fabric path after performing 2-step IAP, perform a system reset or F*F Entry/Exit.

Workaround:

The user application must execute System Reset as soon as the IAP system service is completed. Otherwise, user write and read accesses to LSRAM/uRAM are not possible. The System Reset can be generated with the use of the tamper macro (availably in the Libero SoC Catalog). Immediately after the IAP service, the user logic checks the LSRAM/uRAM access. If access is denied, the user logic sends the reset request/interrupt to the system controller via the tamper macro (by enabling the RESET Function in the tamper macro configuration window) and then the system controller executes the system level reset.

For a design example on how to implement the workaround, contact at soc_tech@microsemi.com.

18. SRAM-PUF system services may take two to three seconds to complete

This Errata is fixed in the latest Date Code devices, where SRAM-PUF system services run fast. contact at soc_tech@microsemi.com for more information.

19. The I/Os state during programming is changed from Z to weak pull-up

The state of the I/O during programming is changed from Z to weak pull-up in the latest die revisions. Affected die revisions (marked with "X" in Table 3) have I/Os that are tristated during programming.

20. For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write, these regions are known as Protected 4 K Regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

21. Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices

For 060, 090, and 150 device densities: Each eNVM memory block has a user page lock bit (refer to PAGE_LOCK_SET register) to lock a page and prevent accidental writing. After the page lock is set in eNVM0 for the 060 device or eNVM1 for the 090/150 devices, the user will not be able to clear the lock for subsequent page updates later.

Workaround:

To use page lock feature, the user can use eNVM0 of 090/150 device and set/clear page lock using the master (for example, M3 or fabric). There is no workaround for the 060 device. User must contact SoC tech support if they already used page lock in the 060 device, which they need to unlock now.

Usage Guidelines for IGLOO2 Devices

1. Programming Support

There may be package dependencies that may not expose certain programming interfaces. Refer to the *PB0121: IGLOO2 FPGA Product Brief* for device/package specific features..

Table 4: **Revision 0 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	No	No	No	No
M2GL010 (S, T, TS)	Yes	Yes	No	No	No	No
M2GL025 (T, TS)	Yes	Yes	No	No	No	No
M2GL060 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	No	No	No	Yes*
M2GL150 (T, TS)	Yes	Yes	No	No	No	No
Note: **Refer to Errata item #11.*						

Table 5: **Revision 1 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL010 (S, T, TS)	Yes	Yes	Yes	Yes	Yes	Yes*
M2GL025 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes*
M2GL0150 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
Note: **Refer to Errata item #11.*						

Table 6: **Revision 2 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL010 (S, T, TS)	Yes	Yes	Yes	Yes	Yes	Yes*
M2GL025 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes*
M2GL150 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
Note: **Refer to Errata item #11.*						

Table 7: **Revision 3 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL010 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes

2. SHA-256 System Service

Microsemi recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion2 devices.

3. Accessing the PCIe Bridge Register in the High-speed Serial Interface

The PCIe Bridge registers must not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates that PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 us after the device is powered up. Wait for 200 us before accessing the PCIe Bridge registers.

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Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known Erratas and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit *http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support*.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group *home page*, at *http://www.microsemi.com/products/fpga-soc/fpga-and-soc*.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.The technical support email address is *soc_tech@microsemi.com*.

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ITAR Technical Support

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