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RTG4 Demo using RTG4 Development Kit

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Agenda

- SERDES Blocks Overview
- Demo Overview
- SERDES Configurators
- Run Demo
- Appendix

SERDES Blocks Overview

- The RTG4 devices include up to six integrated high-speed serial interface (SERDES) blocks with 4 bidirectional lanes each
- There are two types of SERDES blocks
  - A type that supports PCIe, XAUI and EPCS
    - Total SERDES blocks that support PCIe is two
  - A type that supports XAUI and EPCS (no PCIe support)
- Total number of SERDES blocks per RTG4 device

Feature	RT4G075	RT4G150
SERDES Blocks / Lanes / PCIe End Points	4 / 16 / 2	6 / 24 / 2

- Each SERDES block can be configured independently at power-up in a specific mode by using the SERDES block registers
  - These registers are used to configure different modes of the SERDES blocks
  - These registers can be accessed through the APB interface
  - SERDES parameters are loaded after power-up through the APB interface

SERDES Blocks Overview

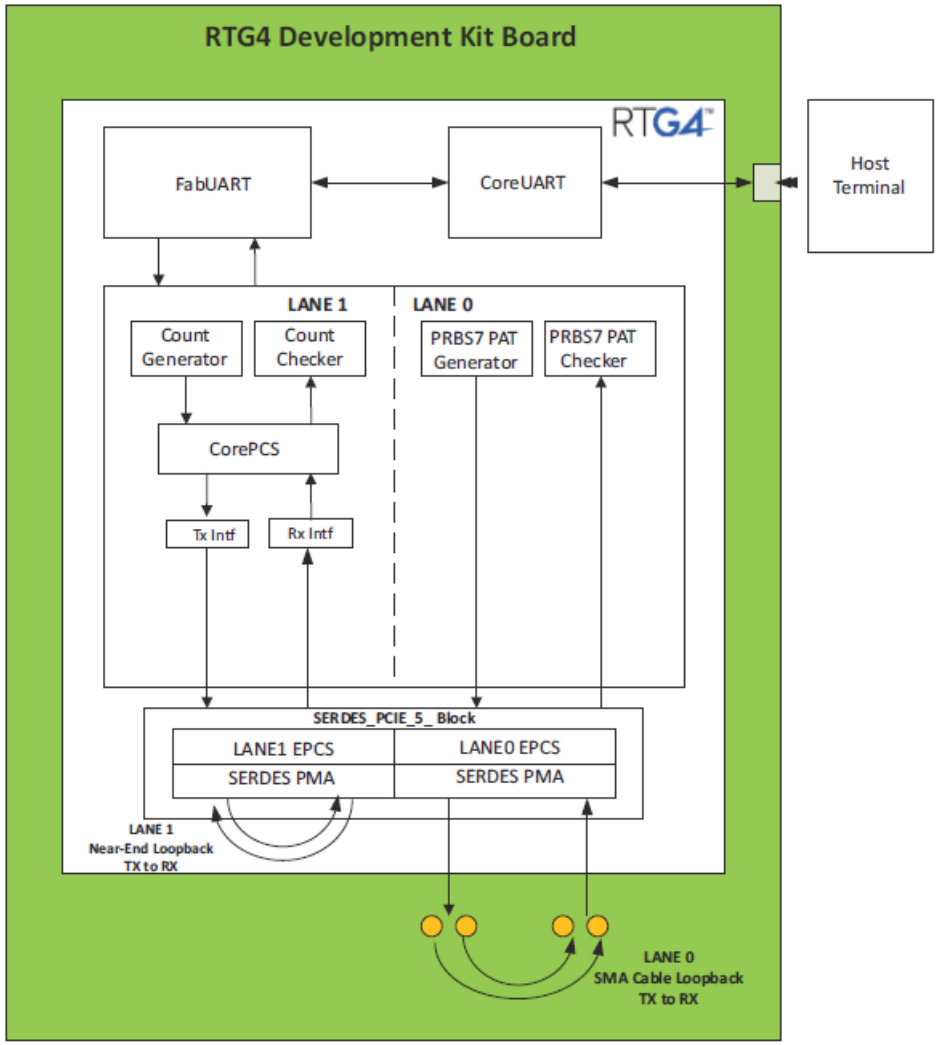
- Each SERDES block
  - Handles data rates between 1 Gbps and 3.125 Gbps
  - Includes four full-duplex differential channels and a fully implemented physical media attachment (PMA)
  - Based on the selected application, the data path includes:
    - A peripheral component interface express (PCIe) physical coding sublayer (PCS)
    - A 10 gigabit attachment unit interface (XAUI) extender
    - An External PCS (EPCS)
  - Option to generate Pseudo-Random Bit Sequences (PRBS) patterns
    - Commonly used to test the signal integrity of SERDES
- The PMA includes the TX and RX buffers, SERDES logic, clocking, and clock recovery circuitry
- Any unused SERDES block resources are automatically powered down

Demo Overview

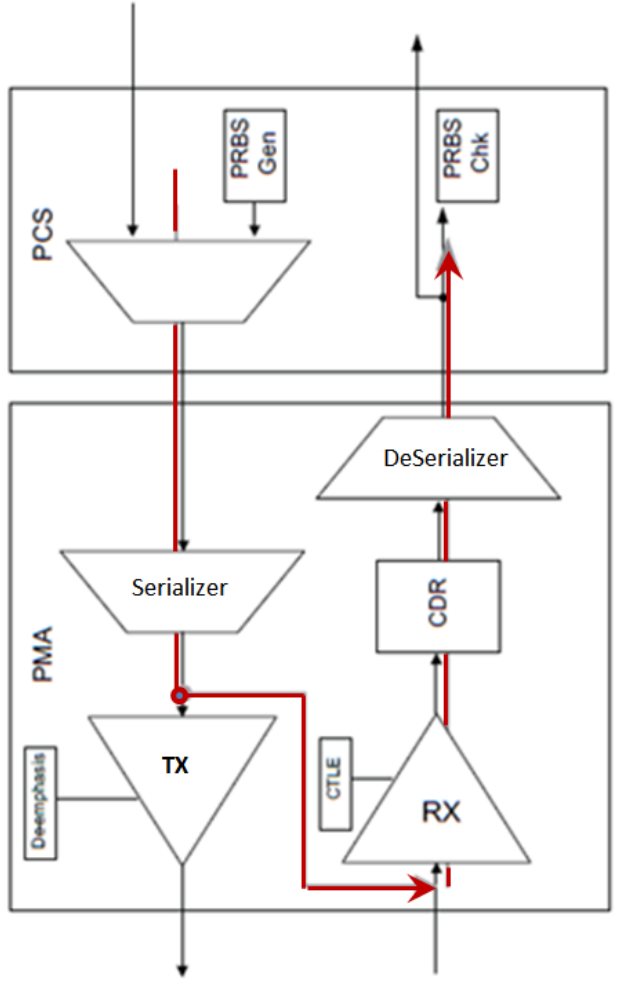
- This Demo will demonstrate the following:
  - Use of the EPCS interface of the RTG4 device
  - Use of DirectCore CorePCS IP for a customized application
  - In this design, the SERDESIF block is configured to be 20-bit wide, 125 MHz REFCLK, and 2.5 Gbps
  - Demo 1:
    - Generate PRBS pattern in the fabric
    - Send on Lane 0 directly from the fabric to the SERDES block and **off-chip**
    - Input SMA connectors are used to route the pattern back through the SERDES receiver pins
    - Check the returned data with a pattern checker in fabric
  - Demo 2:
    - Generate a counting pattern in the fabric
    - Send on Lane 1 through CorePCS IP (which provides simple 8b/10b encoding/decoding functionality)
    - The data is looped back onto itself inside the SERDES block (Near End Serial Loopback)
    - Check the looped back count pattern through the count checker in fabric

Demo Overview

- Demo Design Block Diagram



- Near-End Loopback Tx to Rx inside the device



Demo Overview

- SERDES Block Clock Network
  - Each SERDES block generates two dedicated Global clocks (GLOBAL_0/1_OUT)
  - Each SERDES block has 4 lanes
  - Each lane needs two clocks – RX and TX clocks
  - The source of the RX/TX clock can come from the GLOBAL_0/1_OUT
  - If ALL lanes are used together (using same RX/TX clock), then the two GLOBAL_0/1_OUT clock can drive the RX/TX clocks

- If lanes are not used together
  - Lanes require separate RX/TX clocks
  - The GLOBAL_0/1_OUT can be used only for 1 lane
  - The Other lanes RX/TX clocks need to be sourced localy from the fabric

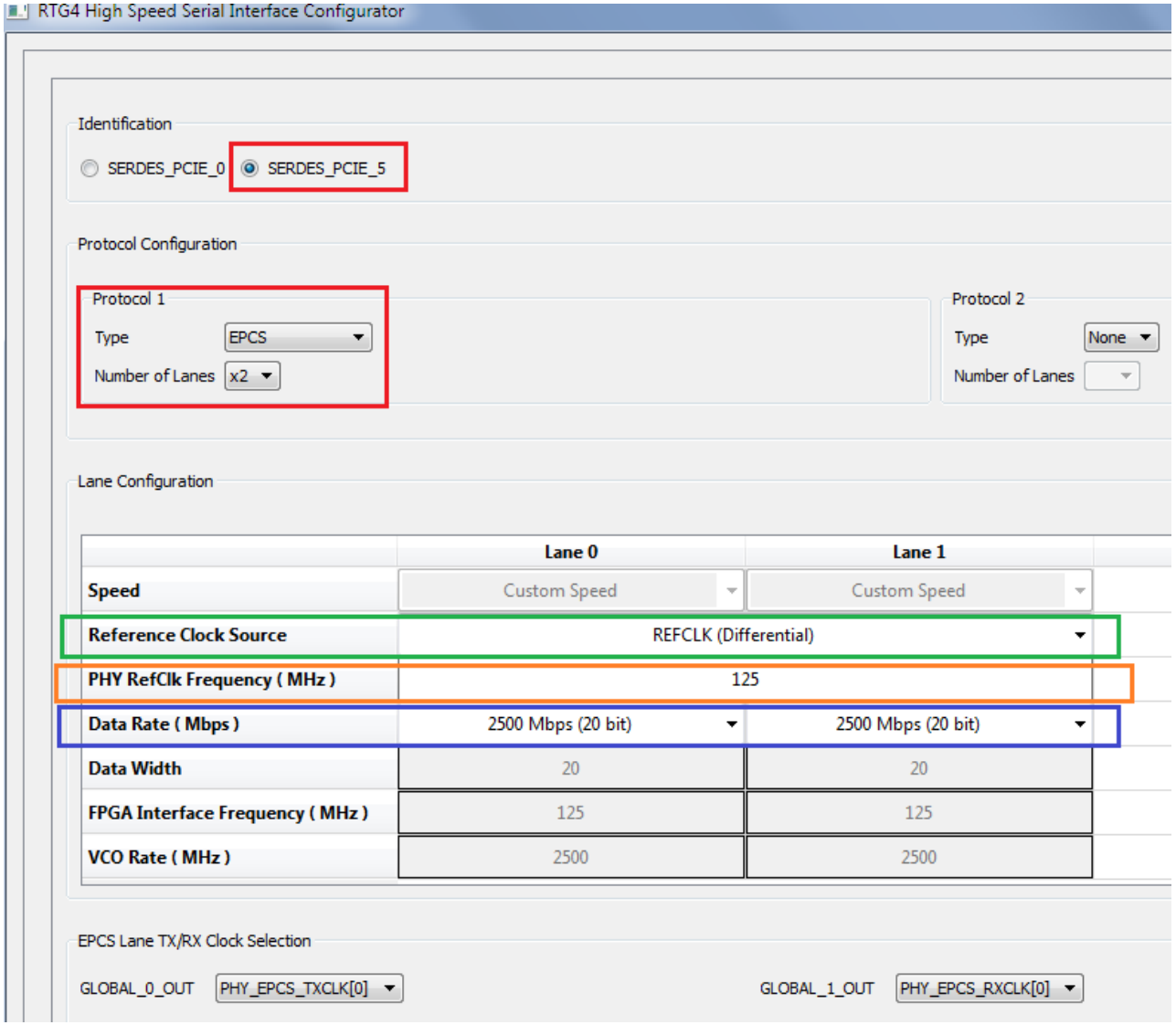
Demo Overview

- In this EPCS demo, since Lane0 and Lane 1 are used independently,
  - Lane 0 uses the dedicated global clock resource (GLOBAL_0/1_OUT) from SERDES
  - Lane 1 uses local fabric resources
    - As such, an additional tx and rx interface modules to manage the fabric interface timing is used

- RX and TX Interface blocks
  - RX and TX interfaces modules manage the timing relationships of the clock and data from the EPCS interface to the FPGA fabric when the global clocks are not used.

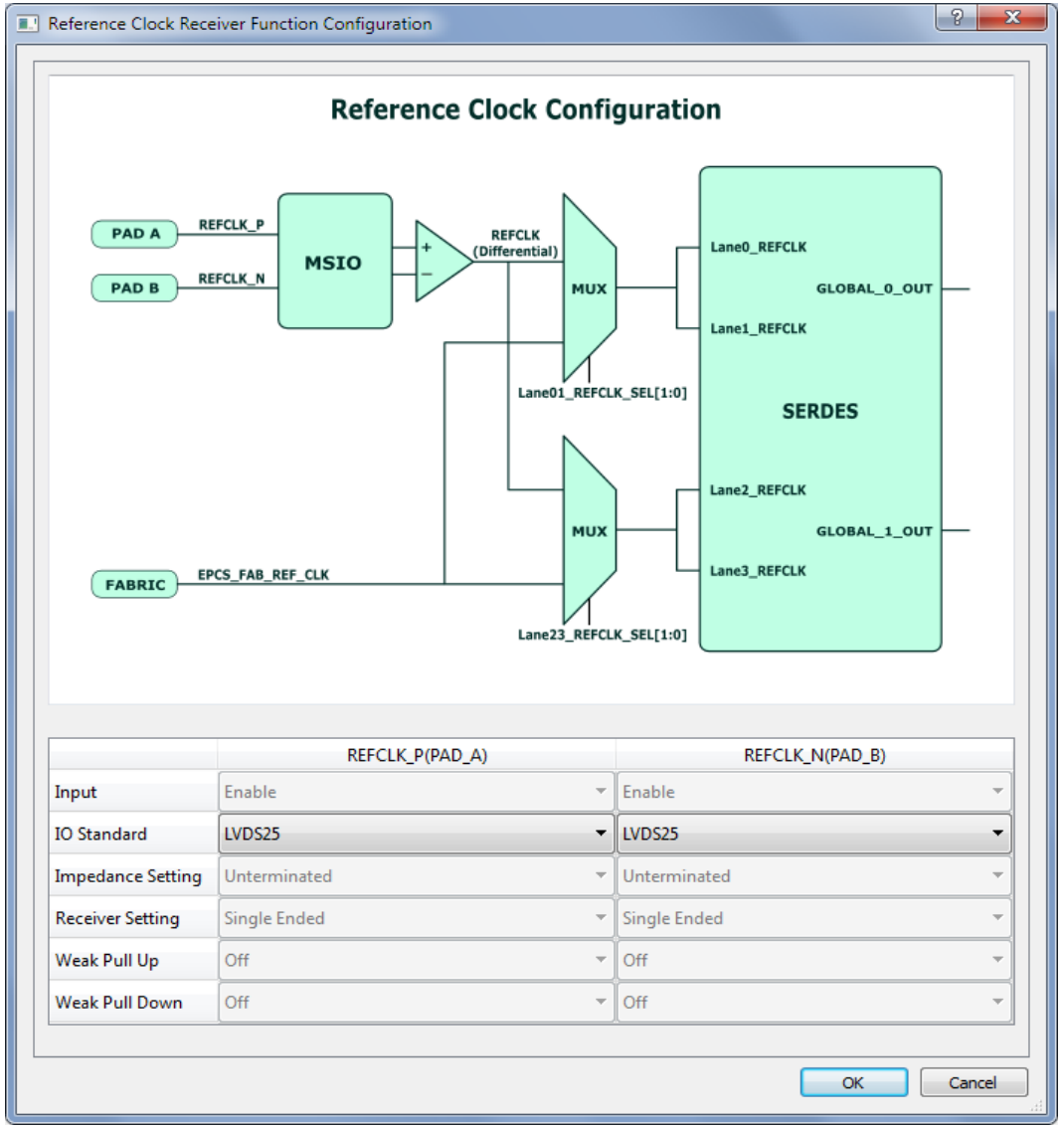
SERDES Block Configurator

- SERDES PCIE 5 block is used
- Protocol 1, EPCS, x2 (two lanes)
- Ref clock from dedicated differential REFCLK
- RefClk = 125 MHz
- Data Rate =2.5Gbps for both lanes



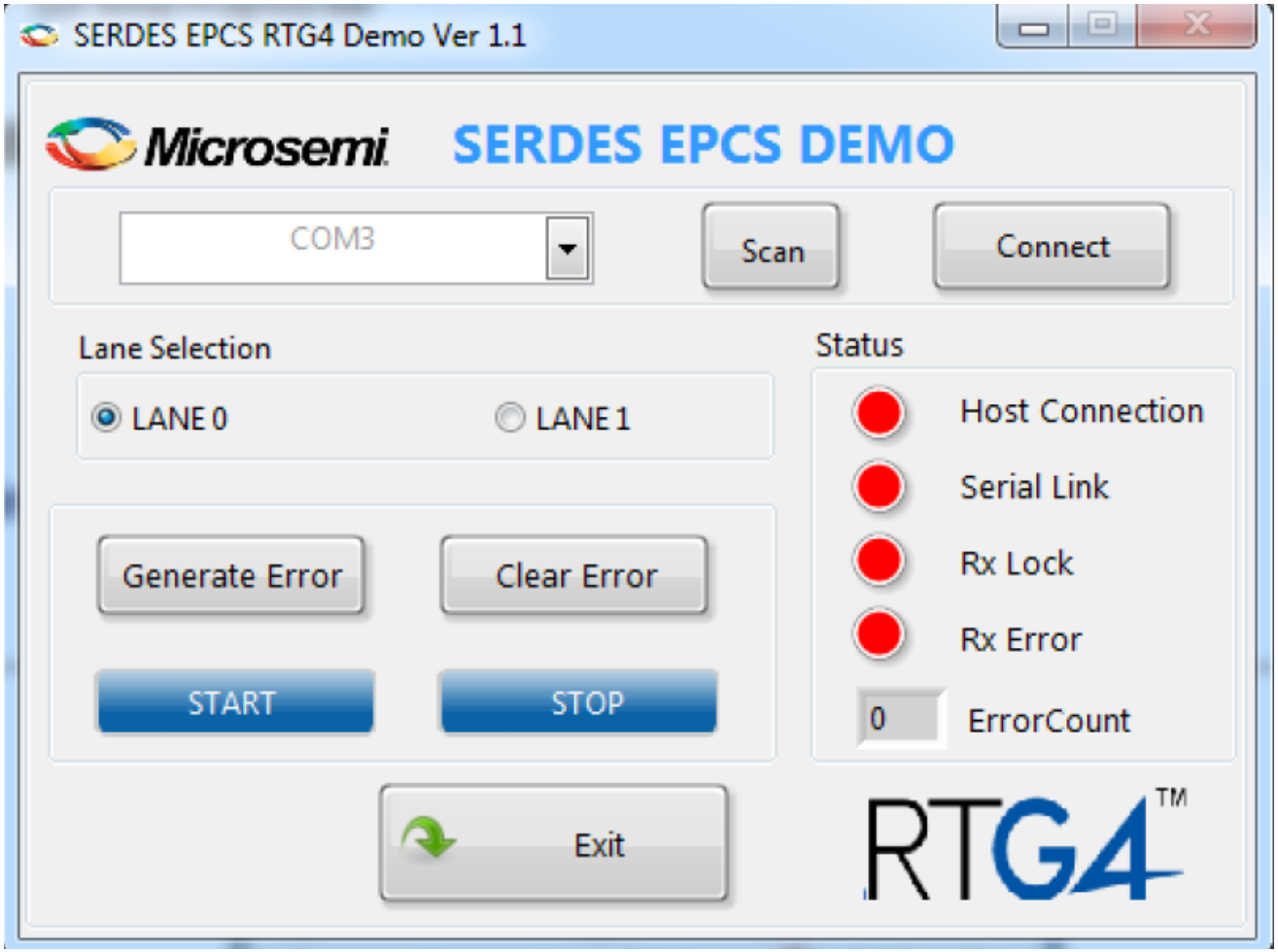
Reference Clock Configurator

- Multi-standard input reference clock
- Each SERDES has its dedicated REFCLK block
- Lanes ref clock source:
  - Dedicated REFCLK pads
  - Fabric (Only EPCS mode)
- REFCLK pads Settings:
  - I/O standards
  - Impedance
  - Receiver settings
  - Weak pull-up/pull-down



Run Demo

- EPCS Demo GUI Window



Appendix (1/3)

- SERDES is initialized through APB3 interface
- SmartTime shows APB hold violations on the APB3 bus interface
- An APB wrapper (apb_hold) is added to this demo to fix the hold violations
- This limitation will be fixed in the future Libero release.

Appendix (2/3)

- SERDES reference clocks
  - Dedicated clock inputs – Single Ended or Differential
  - Fabric clock available only for EPC protocols

- Dedicated reference clock inputs provide **two** reference clocks if configured as **single-ended**

- Dedicated reference clock inputs provide **one** reference clock if configured as **differential**

- The Ref clock is used by the TX PLL and CDR PLL to generate the clocks
  - Refer to the "Serializer/De-serializer" chapter on page 126 for more information on Tx and Rx clock generation through PLLs

Appendix (3/3)

- References
  - High Speed Serial Interface User Guide
  - High Speed Serial Interface Configurator User Guide within Libero SoC Software
  - RTG4 Dev Kit User Guide

- The demo design files include the following:
  - EPCS Demo GUI installer
  - Libero SoC project
  - Programming file
  - Source files

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Thank You

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