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RTG4 Reliability and Qualification

Microsemi Space Forum 2015

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Agenda

- RTG4 Reliability background
- Qualification and QML listing plans
- Production Test Methodology
- Burn-In Design highlights
- Preliminary Qualification Results
- Summary

RTG4 Reliability Background

- G4 product family is 65ηm Flash product fabricated at UMC, qualified per JEDEC47 for Commercial, Industrial & M-Temp application (plastic packages only).
  - G4 family includes : SmartFusion2 [M2S] & IGLOO2 [M2GL]

- RTG4 vs. G4 family (CMOS)
  - Same silicon design rules and fabrication technology.
  - Same LV/MV/HV oxide thickness.
  - Same UMC standard cell library used.
  - Same low voltage transistor bias (1.2V typical).
  - RTG4 shares features with qualified G4 products.
  - RTG4 added features include SpaceWire, EDAC SRAM, STMR FlipFlops, TMR PLL …
  - RTG4 device size (gate and IO counts) is larger than qualified G4 products.

- 65 ηm UMC Flash CMOS FPGA FIT = 3.22 (MTTF 3.11E+08), as of 6/30/2015
  - FIT per JESD85 (CI = 60%, Ea = 0.7eV, Tuse 55C), Life test performed on 4340 units from 12 lots

Device	SS	Test Tj	BI Hrs	BI Hrs @ 125C	Fail	Device Hrs	Comments
M2S050	244	138.6	1000	1962.9	0	478940	FP-178 Qualification Summary
M2S050	80	138.6	6000	11777.2	0	942177	FP-181 Qualification Summary
M2S050	19	146.8	2000	5772.3	0	109673	
M2S150	136	133.2	6000	9059.3	0	1232067	FP-185 Qualification Summary
M2S090	246	140	1000	2099	0	516276	FP-190 Qualification Summary
M2S090	3615	140.31	48	102	0	369576	FP-190 Qualification Summary
Total	**4340**				0	**3648710**	

883B Qualification Plans (1 of 3)

- Qualification Vehicle : RT4G150-LG1657
  - Ea studies to be completed prior to qualification approval
- Qualification plan : Group A, B, C & D per MIL-PRF-38535K
- Silicon Qualification Content

Stress Test	Reference	Abbv.	Test Conditions	# of Qual Lots	# Failures / Sample Size	Test Duration / Pull Point
Group A	MIL-PRF-38535		T_J = -55°C / 25°C / 125°C	1	0/116	Electrical test points
Group C	TM1005	HTOL	$T_J \geq$ 125°C * VDD = 1.26V VPP/VDDI/VDDPLL = 3.45V VDDI/SERDES_VDDPLL = 2.65V	3	0/45	168hr 500hr 1000hr
Human Body Model ESD	TM3015	HBM	HBM	1	0/3	Target >= 2000V
Latch-Up	JESD78	LU	Class I (25°C) and Class II (125°C)	1	0/3	Target > 200mA
Capacitance Test	TM3012		T_J = 25°C	1	0/3	< 8pF
Characterization		CHAR	T_J = -55°C to 125°C Bias = min to max operating condition	1	5	

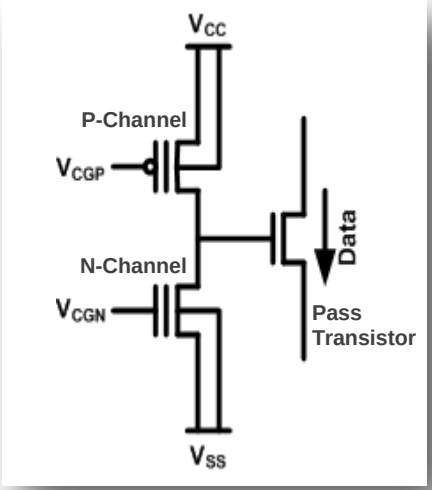
* Burn-In design activity increases junction temperature. Effective Tj will be greater than T_A

883B Qualification Plans (2 of 3)

- Group C
  - Pre group C
    - Endurance test – 220 erase/program cycles to exercise the worst user condition
    - Sample margining to record Vt of flash cells
  - Group C – 1000 cumulative hours of HTOL
  - Post Group C
    - Full electrical / functional test
    - Margining – monitor Vt shift (charge leakage) on sample flash cells
- Group B & Group D
  - Mechanical and Environmental tests per MIL-PRF-38535K
  - Package related tests per MIL-PRF-38535K

883B Qualification Plans (3 of 3)

- Additional NVM studies planned
  - Same Flash cell; New Push-Pull bit cell
  - Significantly more radiation tolerant structure
  - Enhanced HV devices used in programming circuits



Simplified view of Push-Pull Cell

Stress Test	Reference	Abbv.	Test Conditions	# of Qual Lots	# Failures / Sample Size	Test Duration / Pull Point
Non-Volatile Memory Cycling Endurance	JESD22-A117 1-04-12006	NVCE	25 °C and 85°C ≥Tj ≥ 55 °C	3	0/77	220 cycles
Nonvolatile Memory Post-cycling High Temperature Data Retention	JESD22-A117 1-04-12007	PCHTDR	Ta = 150°C	3	0/39	Cycles per NVCE (≥55 °C) / 100 hrs
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A117 1-04-12008	LTDR		3	0/38	Cycles per NVCE (25 °C) / 500 hrs
High Temperature Data Retention	JESD22-A117	HTR	Ta = 250C	3	0/39	NVM 220 cycles (25°C), 168 hrs / 0 Fail

QML listing Plans

- RTG4 technology Insertion
  - Product Introduction to DLA, NASA-JPL & Aerospace: **Completed [9/15/2014]**
  - Phase I: Class Q QML listing, Target End 2016 / Early 2017
  - Phase II: Class V QML listing, Targeting late 2017

  - Status
    - Reviews and direction check from DLA, NASA-JPL & Aerospace

    - Design, wafer fabrication, assembly and test certification review initiated on **3/5/2015**
      - Design methodologies section review and approval : **Completed**
      - Wafer fabrications and package/assembly flow reviewed. Action items identified
      - Manufacturing locations reviewed, audit plan/dates being finalized : ~Jan 2016

    - Next Steps (CY 2015)
      - Wafer fabrication and package/assembly flow reviews/approval [~Q3 CY2015]
      - Screening / Test Methodologies (Class Q and V Test flows) reviews/approval [~Q3 CY2015]
      - Physics-of-failure reliability assessment Plan reviews/approval [~Q4 CY2015]
      - Class Q Qualification and Characterization Plan reviews/approval [~Q4 CY2015]

- Qualification plan – Next slides

RTG4 Class Q Qualification – Phase I

- Process units from 3 wafer lots on Class Q Flow (SoC B Flow)
- Complete Group A, B, C & D per MIL-PRF-38535
- Group C – 1000hrs @ 125°C
  - 45 units (LTPD 5); Life test samples evenly distributed from 3 wafer lots
  - Assumptions: Ea = 0.7eV, Tj ≥ 125°C
- QML – Class Q approval
  - Complete Technology Insertion Plan reviews, SMD for Class Q part number only

Class Q (Microsemi SoC B Flow)
Wafer Sort
Package Assembly (B flow)
Internal Visual (Cond. B)
Serialization (RT only)
Temperature Cycling (10 Cycles)
Constant Acceleration
PIND (RT only)
Seal (Fine/Gross Leak Test)
Binning Circuit
Comm Temp Test
Dynamic Burn-in (160 Hrs @125C)
Post-BI-Test +25C
Final Test -55C
Final Test +125C
100% QA Electrical +25C
Visual Inspection

RTG4 Class V Qualification – Phase II

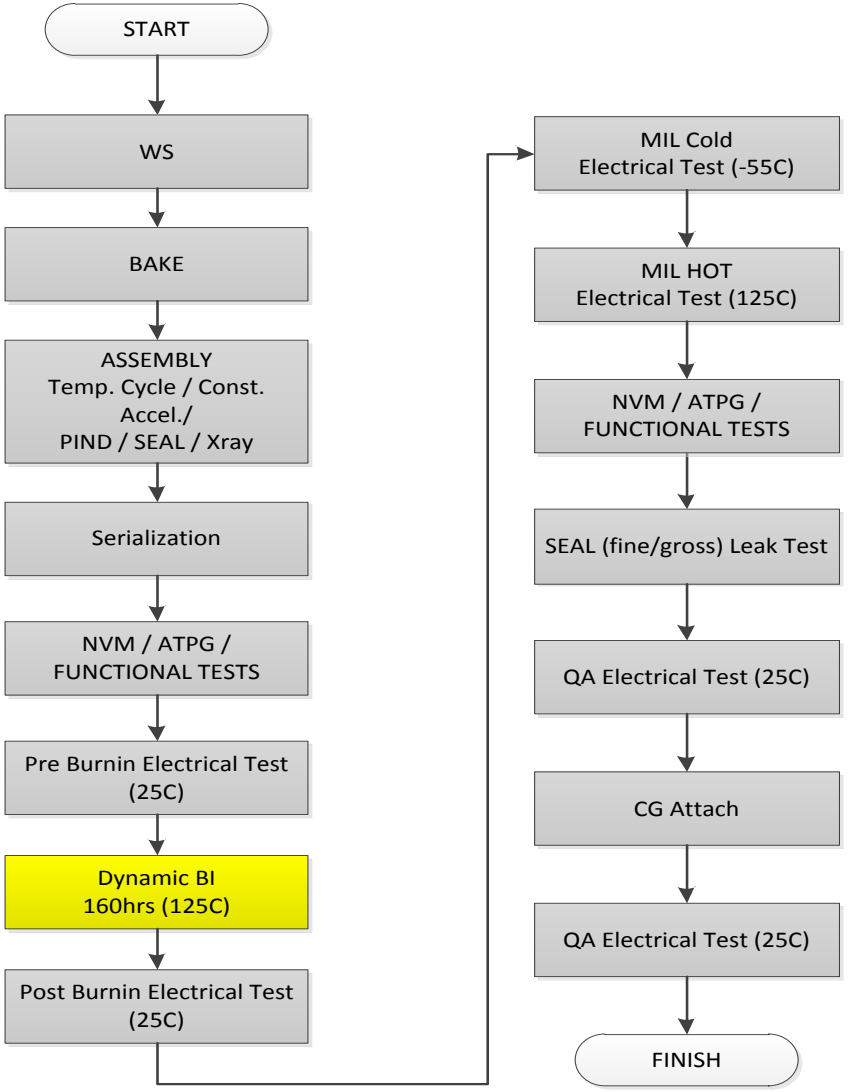
- Process units from 1 wafer lot on Class V Flow
- Complete Group A, B, C & D per MIL-PRF-38535
- Group C – 4000hrs @ 125°C
  - 45 units (LTPD 5); Life test samples from 1 wafer lot
  - Assumptions: Ea = 0.7eV, Tj ≥ 125°C
  - Life test may be modified based on the determination of failure mechanisms and activation energy (see TM 1016 for guidance with a goal of 15 years operating life at +65°C ≤ TJ ≤ 95°C
- QML – Class V approval
  - Update Technology Insertion plan & add Class V part numbers to SMD

Class V (Microsemi SoC V / EV Flow)
Wafer Sort
Package Assembly
Internal Visual (Cond. A)
Pre-Cap Source Inspection (Cond. A)
Serialization
Temperature Cycling (10 Cycles)
Constant Acceleration
PIND
Seal (Fine/Gross Leak Test)
X-Ray
Binning Circuit
Comm Temp Test
Pre Read and Record 25C (R&R)
Dynamic Burn-in (240 Hrs @125C)
Post-BI-Test 25C with R&R
Static Burn-in (144 Hrs @125C)
Post-BI Test +25C with R&R
Final Test -55C with R&R
Final Test +125C with R&R
Seal (Fine/Gross Leak Test)
100% QA Electrical +25C
Visual Inspection

RTG4 Production Test Flow (Class Q)

- Compliant with
  MIL-PRF-38535K

- Class V production flow adds
  - 240h dynamic burn-in @ 125 °C
  - 144h static burn-in @ 125 °C
  - Pre & Post Static and Dynamic BI RnR



RTG4 Burn-In Electrical Test

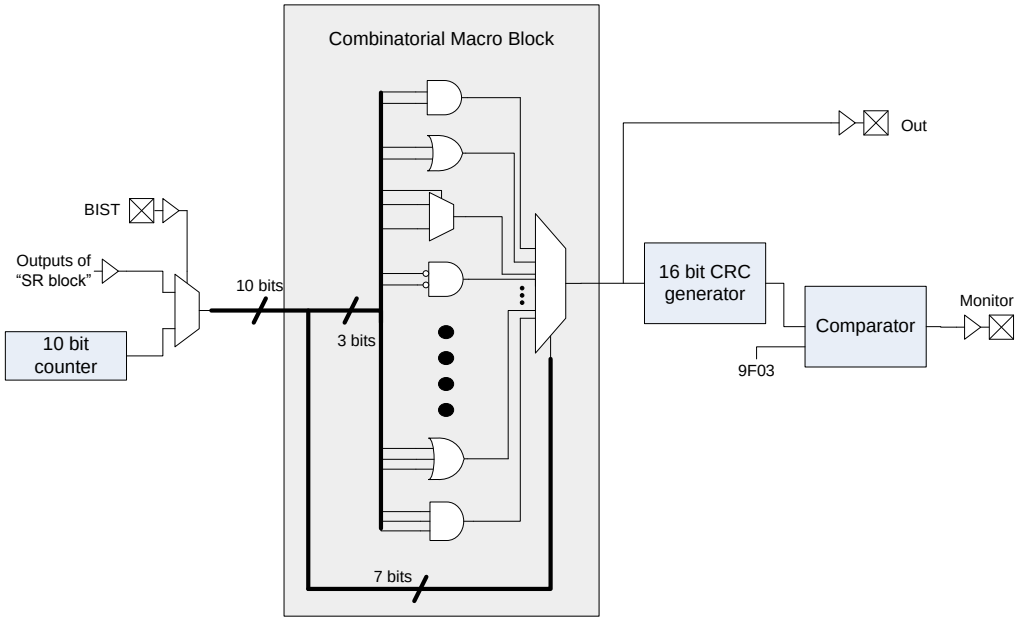
Dynamic BI

- High utilization Burn-In test design used in both production flow and qualification (Group C)
- Maximized toggle coverage using high fanout nets in FPGA
- Coverage of test
  - Electronic serialization based on Lot/Wafer/Die X,Y information
  - Standby Idd on individual power domains
  - Full DC parametric testing for all configurations on all user I/Os
  - Functional test for Burn-In design
  - PLL functional test
  - SERDES parametric and functional test
  - Delay Line Test (speed performance)

RTG4 Burn-In Design Overview (1 of 5)

Dynamic BI

- Clock Source
  - On Chip RCOSC 50MHz clock is fed into all 8 Fabric PLLs of the device
  - PLLs deliver the clock signals through global (low skew) networks

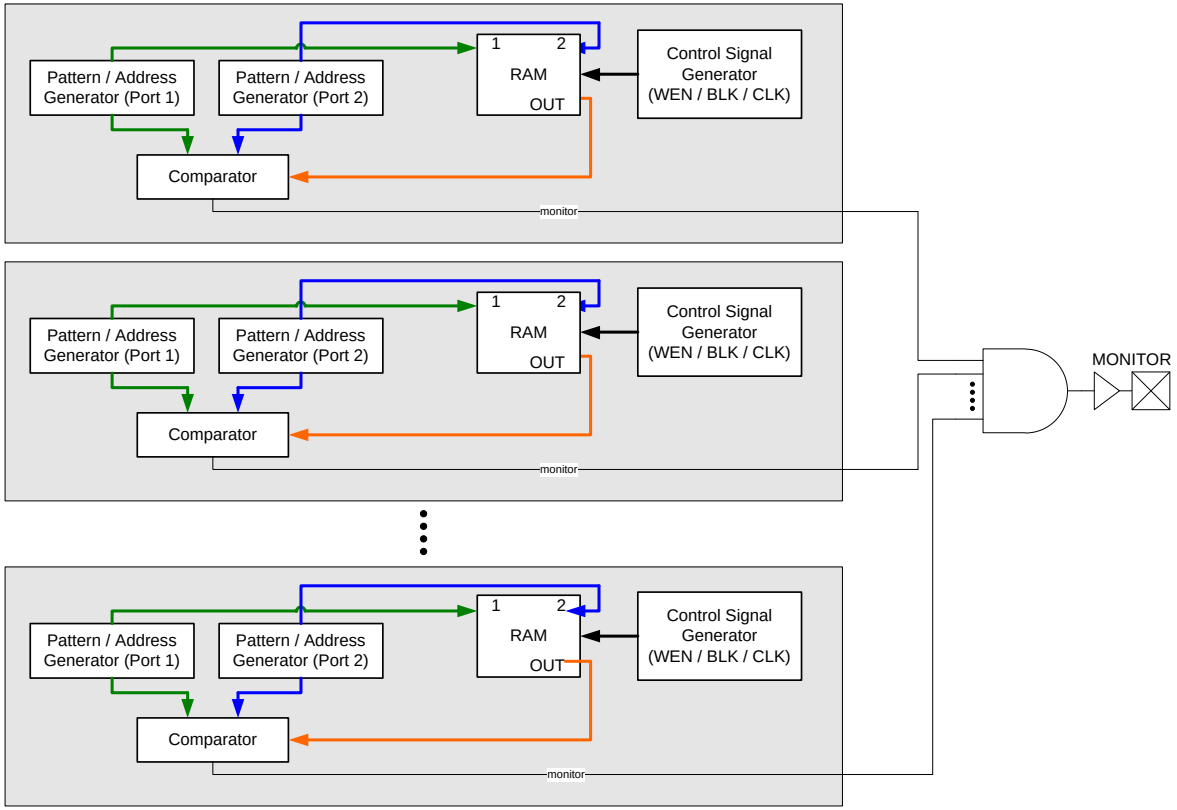


- Combo Block
  - Combinatorial macros available in the RTG4 library are exercised and compared to reference during burn-in
- Register & Latch Block
  - Sequential macros available in the RTG4 library are exercised and compared to reference during burn-in.
- UPROM
  - Checkerboard pattern is stored into the UPROM to maximize output toggle rate; LFSR generated addresses for read access
  - Output read out of UPROM is compared to reference during burn-in

RTG4 Burn-In Design Overview (2 of 5)

Dynamic BI

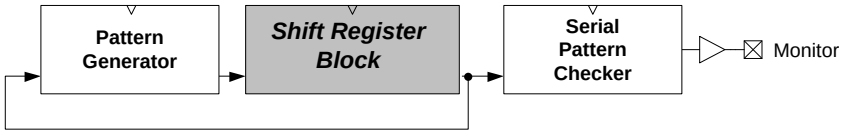
- Embedded SRAM blocks
  - Full R/W toggle coverage on all 209 fabric LSRAM and 210 uRAM blocks
  - Dual Port / Two Port configurations ; Maximum width configurations (x18)
  - Built-in BIST to monitor functionality during Burn-In



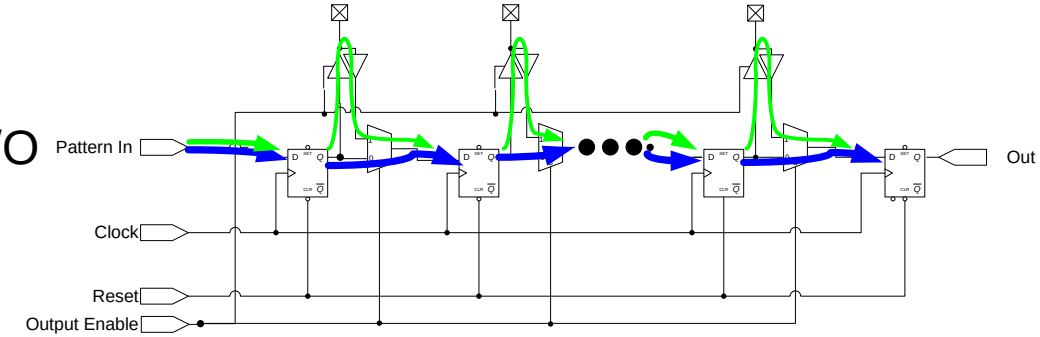
RTG4 Burn-In Design Overview (3 of 5)

Dynamic BI

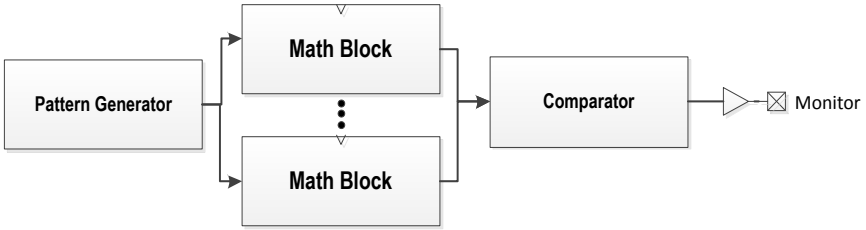
- Shift Register Block
  - Scalable block to maximize core utilization
  - Controlled SSR



- IO Block
  - Scalable block for maximizing I/O utilization
  - Controlled SSO



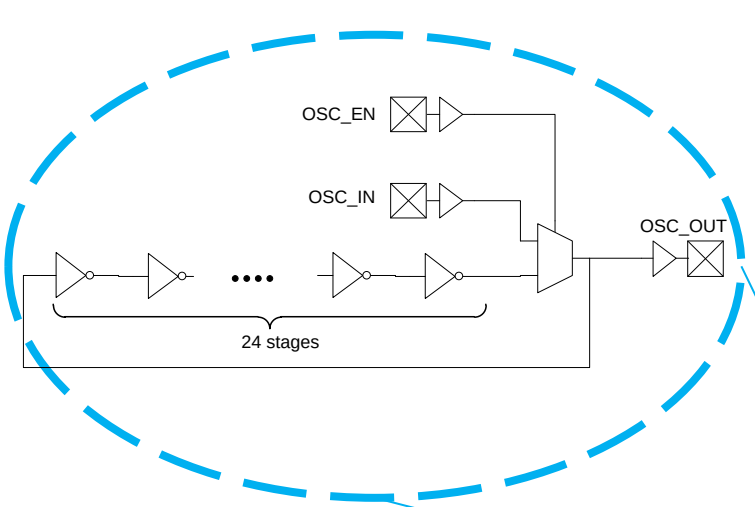
- Math Block
  - Full toggle coverage on all 462 fabric Mathblocks
  - Maximum width configuration

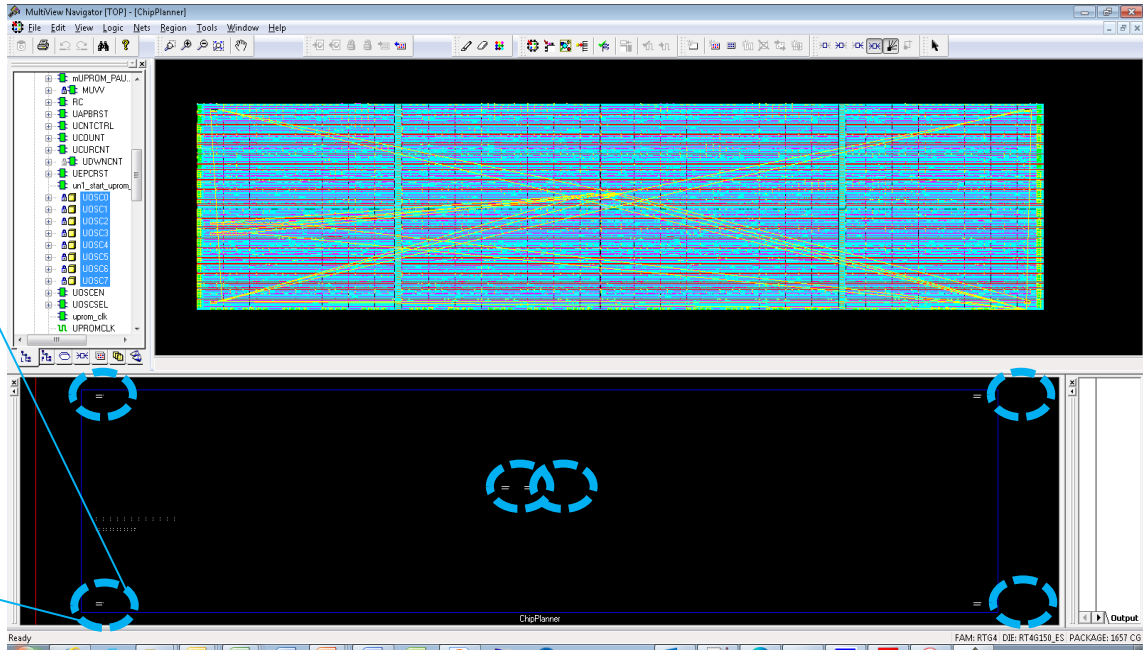


RTG4 Burn-In Design Overview (4 of 5)

Dynamic BI

- Oscillator Block (Delay Lines)
  - Free running ring oscillator circuits to monitor silicon performance pre & post Burn-In
  - Utilizes FPGA resources (Combinatorial, routing tracks and Flash cells)
  - Identical paths placed across the chip (6 locations) to capture on-chip variation
  - Both Intra and Inter Cluster routing resources exercised

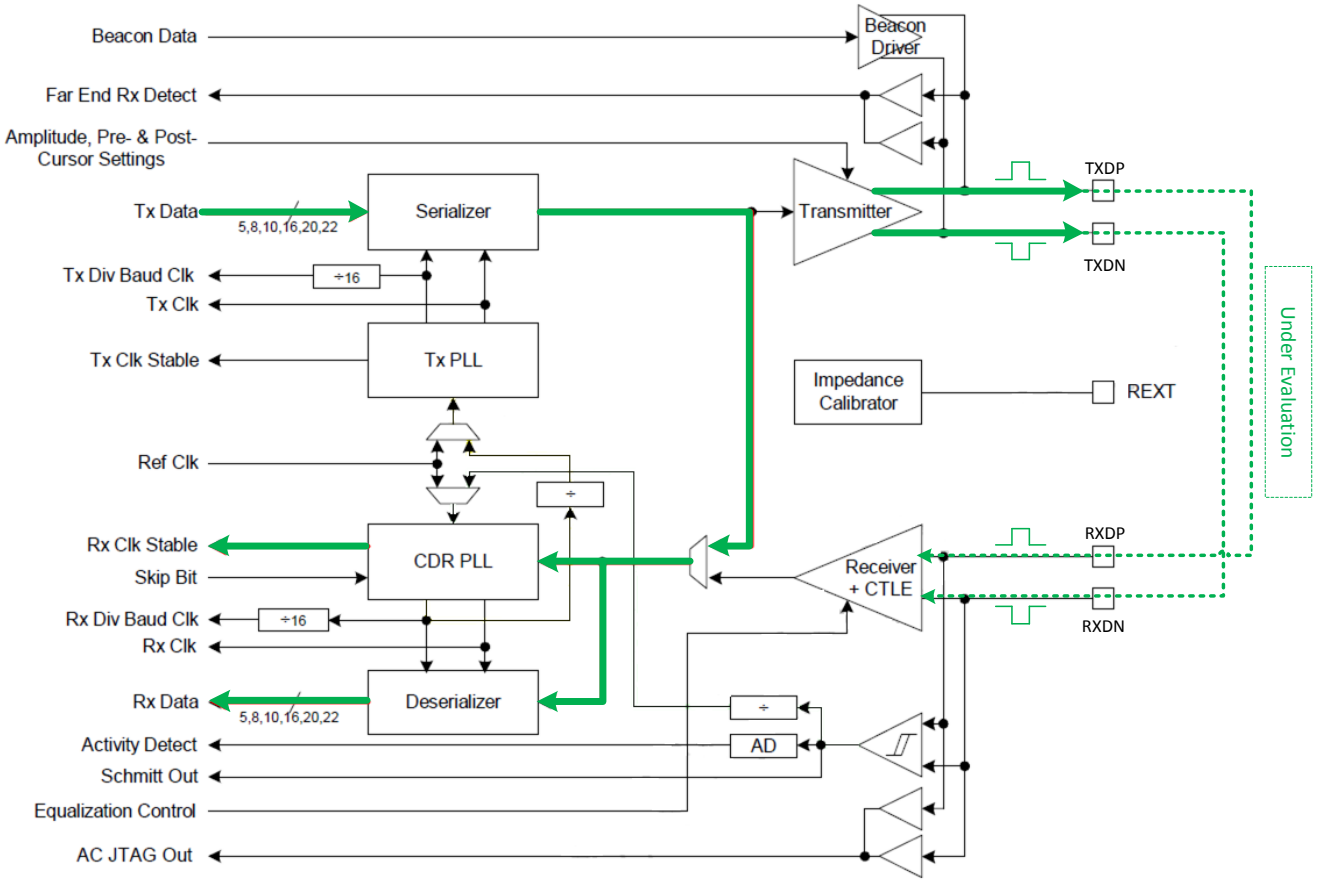




RTG4 Burn-In Design Overview (5 of 5)

Dynamic BI

- SERDES Block
  - 100% SERDES blocks utilized (24 lanes)
  - Provisions for internal loopback mode in EPCS mode



Preliminary Qualification Results

- Reliability infrastructure bring-up started
  - Reliability tests bring-up performed on samples from validation lots
  - Look-ahead enables checking silicon health
  - Pipe-cleans hardware, design and flows

- Preliminary result summary
  - HTOL
    - 1 board/6 units; Ta/Tj = 125C/146C; 168/500/1000hrs;
    - Power and performance remain stable; No failures observed
  - ESD
    - JEDEC (JS-001) HBM : 3/3 passed 2kV ESD level
  - Latch-up
    - JEDEC (JESD78) LU : 3/3 passed level 1
  - NVM
    - Non Volatile Cycling Endurance (NVCE; JESD22-A117) : 8/8 passed 400 cycles
    - High Temperature Retention (HTR, JESD22-A117) : 5/5 passed 500hrs @ Tj=250C

RTG4 Reliability and Qualification Summary

- Qualification plans defined to comply with MIL-PRF-38535K/MIL-STD-883B
- Initial reliability assessment on samples silicon shows great silicon health
- QML listing plans defined
  - Technology insertion ongoing with DLA, NASA-JPL & Aerospace
  - Qualification : Action plan defined; Review and ratification in progress
- Timeline
  - 883 class B qualification completion : Fist Half 2016
  - QML class Q classification : Target End 2016 / Early 2017
  - QML class V classification : Target late 2017

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